THEORY OF OPERATION FOR GINA 2001 RF MODULE

RECEIVE PROCESSING:

Referring to the block diagram in figure 1, From the antenna, the received input is applied to FL5, a three-pole dielectric bandpass filter, which is used to provide image rejection for the receiver. The IF frequency is 280MHz, and low-side injection is used, thereby placing the received image 560MHz below the tuned channel. FL1 also provides protection for the RF front-end from out of band interfering signals.

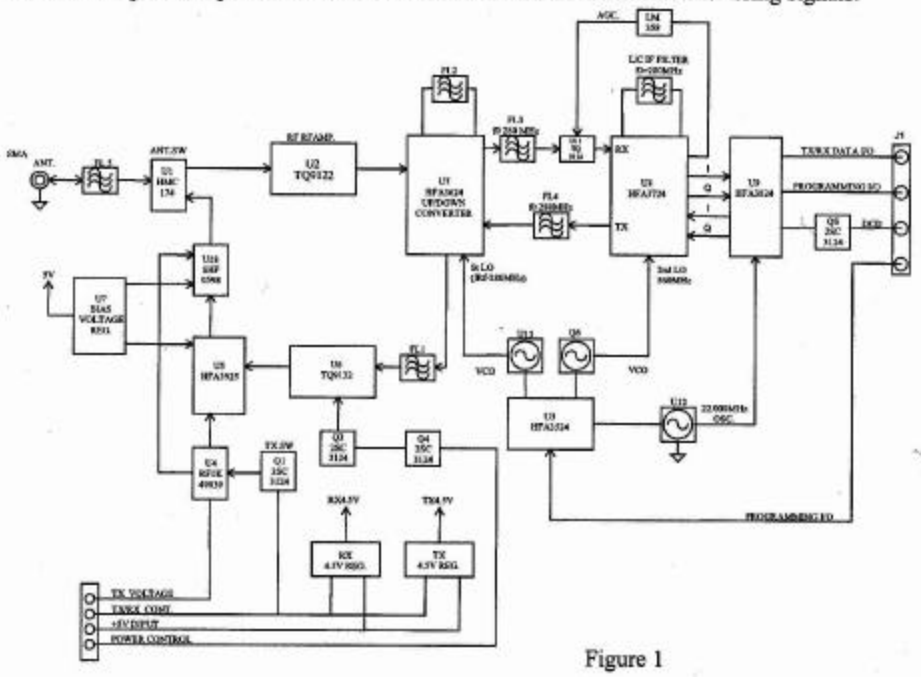

Figure 1

The T/R switch is integrated in the HMC174. Following the T/R switch, the TQ9122 Low Noise Amplifier (LNA) is used to set the receiver noise figure.

Next, the signal enters the HFA3624 RF/IF Converter LNA section, which aids in setting receiver NF. FL2 is used to suppress image noise generated in both the TQ9122 LNA and the HFA3624 LNA, and is a two-pole bandpass filter. Only modest attenuation at the image frequency is required. The insertion loss or NF is offset by the preceding gain stages. All sections of the HFA3624 RF/IF Converter operate from a regulated 5V supply.

Down conversion from the 2.4GHz – 2.5GHz band is performed in the HFA3624 RF/IF Converter mixer section. As previously mentioned, the IF center frequency is 280MHz and low-side local oscillator (LO) injection is used. A discrete LC matching network is used at the mixer output to differentially combine the IF outputs, as well as impedance match to a 50 environment. A capacitor is used as part of the narrow-band matching network. A direct impedance match to the IF filter, FL3 could be implemented if desired. The 50 environment was chosen to allow ease in measurement of portions of the radio with external test equipment.

The IF receive filter, FL3 is a SAW bandpass filter. The center frequency is 280MHz, the 3db bandwidth is 17MHz, and the differential group delay is less than 100ns. Insertion loss is typically 6dB, making it ideal for single-conversion systems. The impedance of the SAW is 270 , and a series 5pFcapacitor is used

to match the filter input to 50 . The SAW output is matched directly to the IF input of the TQ9114 (this device is IF AGC amplifier).

In the receive mode, the HFA3724 Quadrature IF Modulator/Demodulator provides two limiting amplifiers, a quadrature baseband demodulator, and two baseband low pass filters. All sections of the HFA3724 operate from a regulated 5V supply. The first limiting amplifier establishes the NF of the IF strip at approximately 7dB. A discrete one pole LC differential filter, it is placed between the two limiters to restrict the noise bandwidth of the first limiter. As both limiters exhibit a broadband response, with over 400MHz bandwidth, a noise bandwidth reduction filter is appropriate to ensure that the second limiter is fully limiting on the front-end noise within the signal bandwidth, as opposed to the broadband noise generated by the first limiter. This filter has a center frequency of 280MHz, and a 3dB bandwidth of 50MHz. It consists of a fixed 10nH inductor and a fixed 20pF capacitor, as described in the HFA3724 data sheet.

At the output of the limiters, a 200mVp.p differential signal level is maintained under all input conditions. This limited signal is then mixed in quadrature to baseband in the HFA3724 Quadrature IF Modulator/Demodulator. The LO needed for the quadrature mixing is applied at twice the IF frequency, or 560MHz. A divide by two circuits then provides an accurate quadrature LO for the mixers. The baseband outputs of the quadrature mixers are AC coupled off-chip to the integrated fifth order Butterworth filters. The output levels of the low pass filters are nominally 500mVp.p single-ended, and are interred to be AC coupled to the HFA3824A Baseband Processor. The AC coupling time constant is approximately 25 times longer than the symbol period, and is implemented with 0.01 F series capacitors. These coupling capacitors must be taken into account, however, when estimating the time it takes to power up or awaken from sleep mode.

At the input to the HFA3824A Baseband Processor, the quadrature signals are analog to digital converted in wideband 3 bit converters. The sample rate is 22 MSPS, which results in two samples per chip. A 22MHz crystal oscillator is used to provide the main clock for the HFA3824A. The signals are spread spectrum with no DC term, so it is feasible to AC couple the signals to the ADCs and avoid DC bias offsets. The signal at this point has been limited to a constant IF amplitude and then passed through two separate mixer and low pass filter paths. The component variations in these two paths can introduce offsets in amplitude and phase and can also use up some of the headroom in the ADCs. The maximum amplitude variation is 2dB and the maximum phase balance variation is 4 degrees. Since the signal is limited, the IF signals will have low peak to average ratios even with noise as an input. The I and Q signals will have sinusoidal properties with PSK modulation imposed. It is their combined vector magnitude that is limited, not their individual amplitudes. To optimize the demodulator's performance, the ADCs are operated at the point where they are at full scale on either I or Q one third of the time. To maintain this operating point in the face of component variations, there is an optional active adjustment of the ADC reference voltage by feedback. This avoids the necessity of allowing extra headroom for the variation. The adjustment circuit is very slow and averages the energy from the two channels over both packet and noise conditions.

The HFA3824A Baseband Processor correlates the PN spreading to remove it and to uncover the differential BPSK or QPSK data. The processor initially uses differential detection to identify and lock onto the signal. It then makes measurements of the carrier and symbol-timing phase and frequency and uses these to initialize tracking loops for fast acquisition. Once demodulating and tracking, the processor uses coherent demodulation for best performance. Since this radio uses a spread spectrum signal with 10.4dB of processing gain (10 log 11). The signal to noise ratio (SNR) in the chip rate bandwidth is approximately 0dB when the demodulator is at the desired bit error rate in BPSK. The radio operates with about 2.5dB of implementation loss relative to theoretical performance and achieves a sensitivity of -93dBm in the QPSK mode of operation.

The HFA3824A Baseband Processor provides differential decoding and descrambling of the data to prepare it for the controller unit.

TRANSMIT PROCESSING

The HFA3824A Baseband Processor scrambles the packet and differentially encodes it before applying the spread spectrum modulation. The data can be either DBPSK or DQPSK modulated at 1 MSPS and is a

baseband quadrature signal with I and Q components. The BPSK spreading is an 11 chip Barker sequence that is clocked at 11MHz and is modulated with the I and Q data components. These are then output to the HFA3724 as CMOS logic signals. Following the RTS/CTS/MPDU is an acknowledge (ACK) packet by the receiving side of the link.

Transmit quadrature single-bit digital inputs are applied to the HFA3724 Quadrature IF Modulator/Demodulator from the HFA3824A Baseband Processor. These inputs are attenuated by 1/7 and DC coupled to the fifth order Butterworth low pass filters, which are used to provide shaping of the phase shift keyed (PSK) signal. The required transmit spectral mask, at the antenna, is –30dBc at the first side-lobe relative to the main-lobe. An unfiltered PSK waveform would have the first side-lobe suppressed only –13dBc. The fifth-order filters are tuned to an approximate 7.7MHz cutoff, once the PSK waveform is filtered at baseband, all remaining transmit elements are operated at a 6dB back-off from compression, except for the HFA3925 RFPA, which is operated at less back-off.

The low pass filters provide initial shaping of the PSK waveform. Final shaping is provided by a transmit IF filter, FL4 a SAW bandpass filter. The low pass filter outputs are off-chip AC coupled to the quadrature up-converter in the HFA3724. As in the receive mode, the baseband AC coupling time constant is approximately 25 times longer than the symbol period, and is implemented with 0.01 F series capacitors. The same twice IF frequency LO used previously is also used in this up-conversion. The IF output of the HFA3724 is reactively matched to FL5, with a 250 resistive load presented to the HFA3724. A shunt 47uH inductor, in parallel with a 316 resistor, is used to provide this match, negate the effects of board and component capacitance, and provide a DC return to Vcc to prevent saturation in the IF output stage of the HFA3724.

Up conversion to the 2.4GHz – 2.5GHz band is performed in the HFA3624 RF/IF Converter transmit mixer. The mixer output is filtered with FL1, Three-pole band-pass filter. This filter suppresses the LO feed through from the mixer, and selects the upper sideband. The transmit buffer is the TQ9132, easing the requirement for HFA3925 RFPA gain.

FL1, three pole dialectic bandpass filter, is used to further suppress both the transmit LO leakage and the undesired sideband.

The HFA3925 RFPA amplifies the transmit signal to a level of approximately +20 dBm. This represents a back off from 1dB compression of approximately 4.5dB. Transmit side-lobe performance is approximately –32dBc to –35dBc with this level of back off.

To supply the needed negative gate bias to the HFA3925 RFPA, a ICL7660SIBA[7] charge pump is used. A second potentiometer is used to adjust the drain current on the third stage of the HFA3925 to a quiescent operating current of 90mA, as measured through a one ohm sense resistor. A base-emitter junction is used as part of the gate bias network to provide temperature compensation, and all three gates are driven from one source to reduce the impact of process variation on pinch-of voltage. The nominal quiescent drain bias currents are 20mA for stage one, 50mA for stage two, and 90mA for stage three.

Final amplifier is SHF-0589. This device will have gain about 8~10dB. A second logic-level PMOS switch, RF1K49093, is used to control the drain supply voltage to the HFA3925 RFPA and SHF-0589 final power amp.

SYNTHESIZER SECTION

The dual frequency synthesizer section uses the HFA3524[9] Synthesizer and two voltage controller oscillators to provide a tunable 2132MHz – 2204MHz first LO, and a fixed 560MHz second LO. Both feedback loops use a 1MHz reference frequency that is derived from a second 22MHz Fox F4106 crystal oscillator. Two separate crystal oscillators were used for the HSP3824 and HFA3524 to maintain a high quality, low spurious reference for the synthesizer. Sharing a common 22MHz oscillator is possible if care is taken to isolate the HFA3824A from the HFA3524. Both feedback loops are fourth order (four poles in the transfer function) and were designed to have loop bandwidths of 10kHz, and phase margins of 50 degrees. The feedback loop analysis is included for both loops in Appendix E. Measured phase noise

performance and calculated RMS phase jitter is included in Appendix F. All components in the synthesizer section operate from a regulated 3.5V supply.

The tunable 2132MHz to 2204MHz first LO oscillator. To ensure operation at low tuning voltages, a start-up circuit was added to force the tuning voltage from the HFA3524 Synthesizer RF charge pump to a high state for a short period (~1ms) following HFA3524 programming.

The fixed 560MHz second LO oscillator is discrete design, using a transistor and a varactor. The output level of the second LO to the HFA3724 Quadrature IF Modulator/Demodulator is attenuated to approximately –6dBm and a three pole low pass filter is included to preserve the duty cycle of the output. High even order components in the second LO can result in offsets from a 50% duty cycle, and will degrade the quadrature phase accuracy of the HFA3724 LO input to convert the second LO voltage into a current, as recommended in the HFA3724 data sheet. As the HFA3524 Synthesizer auxiliary IF input covers the 560MHz range, the internal divide-by-two LO buffer output of the HFA3724 is disabled, as recommended in the HFA3724 data sheet.