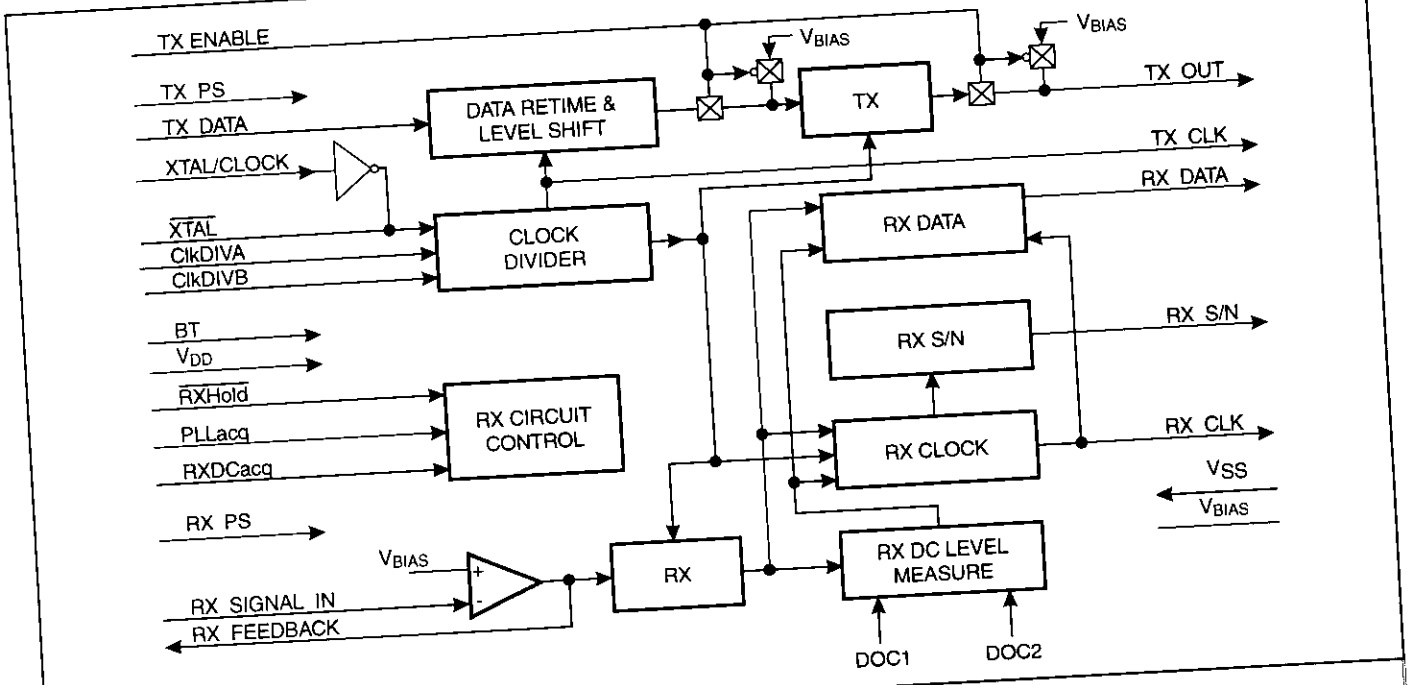
MX•COM, INC. MiXed Signal ICs

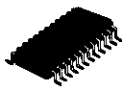
DATA BULLETIN

MX589 High Speed GMSK Modem

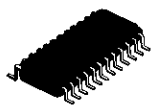
- Data Rates from 4kbps to 64kbps
- Full or Half Duplex Gaussian Minimum Shift Keying (GMSK) Operation
- Selectable BT: (0.3 or 0.5)
- Low Power:
  3.0V, 32kbps, 1.5mA typ.
  5.0V, 64kbps, 4.0mA typ.
- Low Cost
- Point of Sale Terminals
- Low Power Wireless Data Link for PCs, Laptops, and Printers
- Data for GPS/Differential GPS
- Portable Wireless Data Applications:
  Cellular Digital Packet Data (CDPD)
  Mobitex™ Mobile Data System
- Low Current Non-DSP Solution



AVAILABLE PACKAGES



MX589TN
24-pin TSSOP



MX589DW
24-pin SOIC

MX589P/J
24-pin PDIP

The MX589 is a single-chip synchronous modem designed for wireless data applications. Employing Gaussian Minimum Shift Keying (GMSK) baseband modulation, the MX589 features a wide range of available data rates: 4kbps to 64kbps. Data rates and choice of BT (0.3 or 0.5) are pin-programmable to provide for different system requirements. The Tx and Rx digital data interfaces are bit serial, synchronized to Tx and Rx data clocks generated by the modem. Separate Tx and Rx Powersave inputs allow full or half-duplex operation. Rx input levels can be set by a suitable AC and DC level adjusting circuit built with external components around an on-chip Rx Input Amplifier. Acquisition, lock and hold of Rx data signals are made easier and faster by the use of Rx Control Inputs to clamp, detect and/or hold input data levels and can be set by the µProcessor as required. The Rx S/N output provides an indication of the quality of the received signal.

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Doc. # 20480103.00

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1. Block Diagram

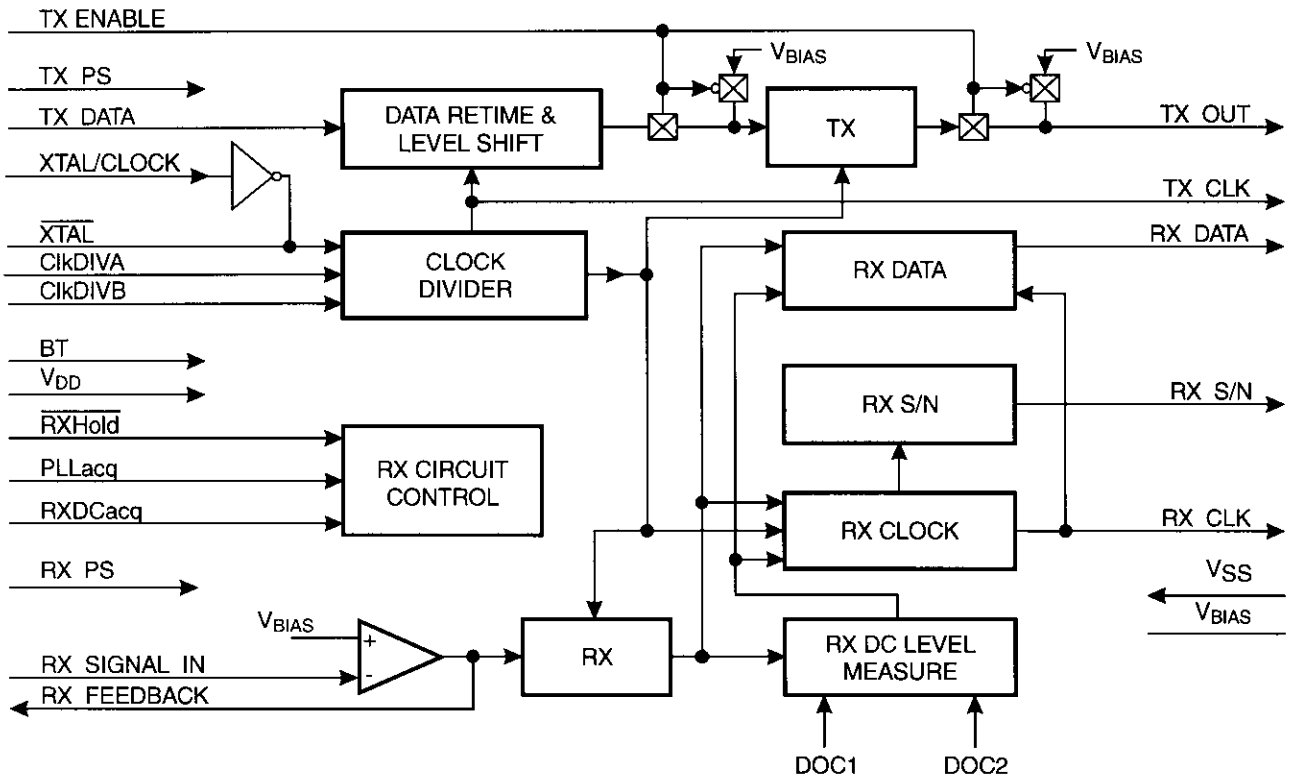

Figure 1: Device Block Diagram

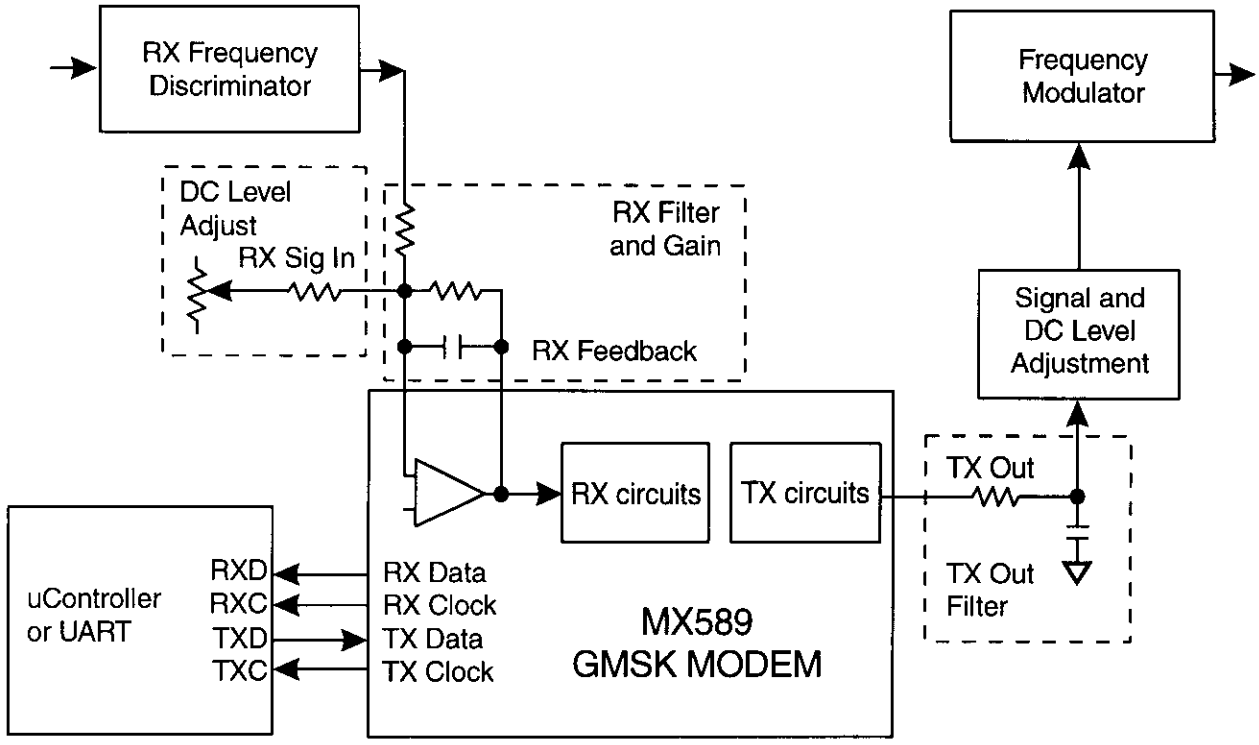

Figure 2: System Block Diagram

2. Signal List

Pin No.	Name	Type	Description
1	$\overline{XTAL}$		The output of the on-chip clock oscillator.
2	Xtal/Clock		The input to the on-chip Xtal oscillator. A Xtal, or externally derived clock (f_{XTAL}) pulse input should be connected here. If an externally generated clock is to be used, it should be connected to this pin and the $\overline{XTAL}$ pin left unconnected
3	ClkDivA		Logic level inputs control the internal clock divider and therefore the transmit and receive data rate. See Table 1
4	ClkDivB		Logic level inputs control the internal clock divider and therefore the transmit and receive data rate. See Table 1
5	$\overline{Rx\ HOLD}$		A logic 0 applied to this input will freeze the Clock Extraction and Level Measurement circuits unless they are in Acquire mode.
6	RxDCacq		A logic 1 applied to this input will set the RX Level Measurement circuitry to the Acquire mode.
7	PLLacq		A logic 1 applied to this input will set the Rx Clock Extraction circuitry to Acquire mode (see Table 2).
8	Rx PSAVE		A logic 1 applied to this input will powersave all receive circuits except for Rx CLK output (which will continue at the set bit-rate) and cause the Rx Data and Rx S/N outputs to go to a logic 0.
9	V_{BIAS}		The internal circuitry bias line, held at $V_{DD}/2$, this pin must be bypassed to V_{SS} by a capacitor mounted close to the pin.
10	Rx FB		Output of the Rx Input Amplifier.
11	Rx Signal In		Input to Rx Input Amplifier.
12	V_{SS}		Negative supply. Signal ground.
13	Doc1		Connections to the Rx Level Measurement Circuitry. A capacitor should be connected from each pin to V_{SS}. See Figure 3.
14	Doc2		Connections to the Rx Level Measurement Circuitry. A capacitor should be connected from each pin to V_{SS}. See Figure 3.
15	BT		A logic level to select the modem BT (the ratio of the Tx Filter's -3dB frequency to the Bit-Rate). A logic 1 = BT of 0.5, a logic 0 = BT of 0.3.
16	Tx Out		Tx signal output from the MX589 GMSK Modem.
17	Tx Enable		A logic 1 applied to this input enables the transmit data path through the Tx Filter to the Tx Out pin. A logic 0 will place the Tx Out pin at V_{BIAS} via a high impedance.
18	Tx PSAVE		A logic 1 applied to this input will powersave all transmit circuits except for the Tx Clock.
19	Tx Data		The logic level input for the data to be transmitted. This data should be synchronous with Tx CLK.
20	Rx Data		A logic level output carrying the received data, synchronous with Rx CLK.
21	Rx CLK		A logic level clock output at the received data bit-rate.
22	Tx CLK		A logic level clock output at the transmit-data rate.
23	Rx S/N		A logic level output which may be used as an indication of the quality of the received signal.
24	V_{DD}		Positive supply. A single 5.0V power supply is required. Levels and voltages within this modem are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor mounted close to the pin.

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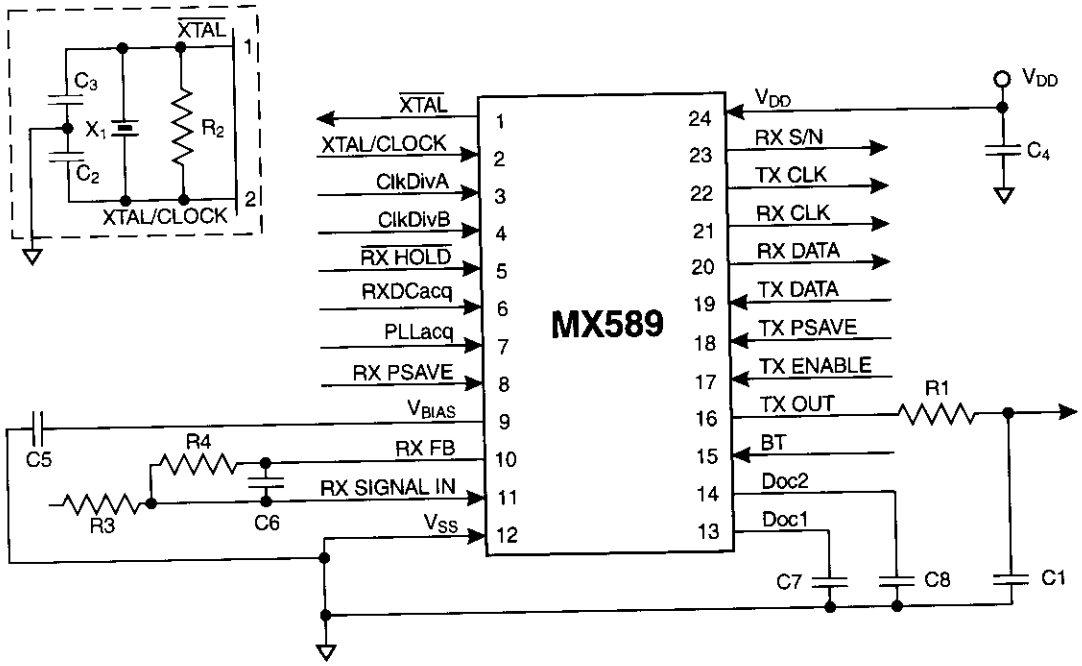
3. External Components



R1	Note 1	±5%
R2	1.0MΩ	±10%
R3	Note 2	±10%
R4	100kΩ	±10%
C1	Note 1	±10%
C2	Note 3	
C3	Note 3	

C4	0.1µF	±20%
C5	1.0µF	±20%
C6	22.0pF	±20%
C7	Note 4	
C8	Note 4	
X1	Note 5	

Figure 3: Recommended External Components

External Components Notes:

1. The RC network formed by R1 and C1 is required between the Tx Out pin and the input to the modulator. This network, which can form part of any DC level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering. The ground connection to the capacitor C1 should be positioned to give maximum attenuation of high-frequency noise into the modulator.

   The component values should be chosen so that the product of the resistance and the capacitance is:

   BT of 0.3 = 0.34/bit rate (bps) BT of 0.5 = 0.22/bit rate (bps)

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Data Rate bps	BT = 0.3		BT = 0.5	
	R1	C1	R1	C1
4000	120kΩ	680pF	120kΩ	470pF
4800	100kΩ	680pF	100kΩ	470pF
8000	91kΩ	470pF	120kΩ	220pF
9600	91kΩ	390pF	47kΩ	470pF
16000	47kΩ	470pF	91kΩ	150pF
19200	100kΩ	180pF	91kΩ	120pF
32000	47kΩ	220pF	47kΩ	150pF
38400 *	47kΩ	180pF	47kΩ	120pF
64000 *	56kΩ	100pF	51kΩ	68pF
* $V_{DD} \geq 4.5V$				

Note: In all cases the value of R1 should not be less than 20.0 kΩ, and the calculated value of C1 includes calculated parasitic capacitance.

2. R3, R4 and C6 form the gain components for the Rx Input signal. R3 should be chosen as required by the signal input level.
3. The values chosen for C2 and C3 (including stray capacitance), should be suitable for the applied V_{DD} and the frequency of X1.

   As a guide : C2 = C3 = 33pF at 1.0MHz falling to 18pF at the maximum frequency.

   At 3.0 volts, C2 = C3 = 33pF falling to 18pF at 5.0MHz. The equivalent series resistance of X1 should be less that 2.0kΩ falling to 150Ω at the maximum frequency. Stray capacitance on the Xtal/Clock circuit pins must be minimized.
4. C7 and C8 should both be .015µF for a data rate of 8kbps, and inversely proportional to the data rate for other data rates, e.g. .030µF at 4kbps, .0018µF at 64kbps.
5. The MX589 can operate correctly with Xtal/Clock frequencies between 1.0MHz and 8.2MHz (V_{DD} = 5.0V) and 1.0MHz to 5.0MHz (V_{DD} = 3.0V) see Table 1 for examples. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer. Operation of this device without a Xtal or Clock input may cause device damage.

4. General Description

4.1 Clock Oscillator Divider

The Tx and (nominal) Rx data rates are determined by division of the frequency present at the $\overline{\text{Xtal}}$ pin, which may be generated by the on-chip Xtal oscillator or derived from an external source. Any Xtal/clock frequency in the range 1.0MHz to 5.0MHz for V_{DD} = 3.0V, or 1.0 MHz to 8.2MHz for V_{DD} = 5.0V may be used, depending on the desired data rate.

The division ratio is controlled by the logic level inputs on ClkDivA and ClkDivB pins, as shown in Table 1, together with an indication of how various standard data rates may be derived from common µP Xtal frequencies.

$$\text{Data Rate} = \frac{\text{Xtal/Clock Frequency}}{\text{Division Ratio (Clk Div A/B)}}$$

Inputs		Division Ratio Xtal Freq. Data Rate	Xtal/Clock Frequency (MHz)				
			8.192	4.9152	4.096	2.4576	2.048
					(12.288/3)	(12.288/5)	(6.144/3)
ClkDiv A	ClkDiv B		Data Rate (bps)				
0	0	128	64000*	38400*	32000	19200	16000
0	1	256	32000	19200	16000	9600	8000
1	0	512	16000	9600	8000	4800	4000
1	1	1024	8000	4800	4000		

* V_{DD} > = 4.5V

Table 1: Clock/Data Rates

Note: The device operation is not guaranteed above 64kbps or below 4kbps at the relevant supply voltage.

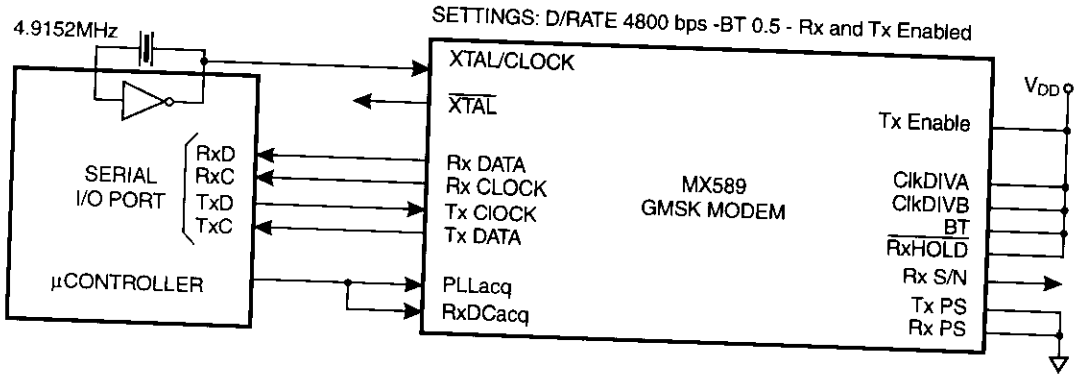

Figure 4: Minimum µController System Connections

4.2 Receive

4.2.1 Rx Signal Path Description

The function of the Rx circuitry is to:

1. Set the incoming signal to a usable level.
2. Clean the signal by filtering.
3. Provide DC level thresholds for clock and data extraction.
4. Provide clock timing information for data extraction and external circuits.
5. Provide Rx data in a binary form.
6. Assess signal quality and provide Signal-to-Noise information.

The output of the radio receiver's Frequency Discriminator should be fed to the MX589's Rx Filter by a suitable gain and DC level adjusting circuit. This circuit can be built with external components around the on-chip Rx Input Amplifier. The gain should be set so that the signal level at the Rx Feedback pin is nominally 1V peak to peak (for V_{DD} = 5.0V) centered around V_{BIAS} when receiving a continuous 1111000011110000.. data pattern.

Positive going signal excursions at Rx Feedback pin will produce a logic 0 at the Rx Data Output. Negative going excursions will produce a logic 1.

The received signal is fed through the lowpass Rx Filter, which has a -3dB corner frequency of 0.56 times the data bit-rate, before being applied to the Level Measure and Clock and Data extraction blocks.

The Level Measuring block consists of two voltage detectors, one of which measures the amplitude of the positive parts of the received signal. The other measures the amplitude of the negative portions. (Positive refers to signal levels higher than $V_{DD}/2$, and negative to levels lower than $V_{DD}/2$.) External capacitors are used by these detectors, via the Doc1 &

Doc2 pins, to form voltage hold or integrator circuits. These two levels are then used to establish the optimum DC level decision-thresholds for the Clock and Data extraction, depending upon the Rx signal amplitude and any DC offset.

4.2.2 Rx Circuit Control Modes

The operating characteristics of the Rx Level Measurement and Clock Extraction circuits are controlled, as shown in Table 2, by logic level inputs applied to the PLLacq, $\overline{\text{Rx HOLD}}$ and RxDCacq pins to suit a particular application, or to cope with changing reception conditions.

With reference to Figure 5, the Rx Mode Control diagram:

In general, a data transmission will begin with a preamble, for example, 1100110011001100, to allow the receive modem to establish timing and level-lock as quickly as possible. After the Rx carrier has been detected, and during the time that the preamble is expected, the RxDCacq and PLLacq Inputs should be switched from a logic 0 to a logic 1 so that the Level Measuring and Clock Extraction modes are operated and sequenced as shown.

The $\overline{\text{Rx HOLD}}$ input should normally be held at a logic 1 while data is being received, but may be driven to a logic 0 to freeze the Level Measuring Clock Extraction circuits during a fade. If the fade lasts for less than 200 bit periods, normal operation can be resumed by returning the $\overline{\text{Rx HOLD}}$ input to a logic 1 at the end of the fade. For longer fades , it may be better to reset the Level Measuring circuits by placing the RxDCacq to a logic 1 for 10 to 20 bit periods.

$\overline{\text{Rx HOLD}}$ has no effect on the level Measuring circuits while RxDCacq is at a logic 1, and has no effect on the PLL while PLLacq is at a logic 1.

A logic 0 on $\overline{\text{Rx HOLD}}$ does not disable the Rx Clock output, and the Rx Data Extraction and S/N Detector circuits will continue to operate.

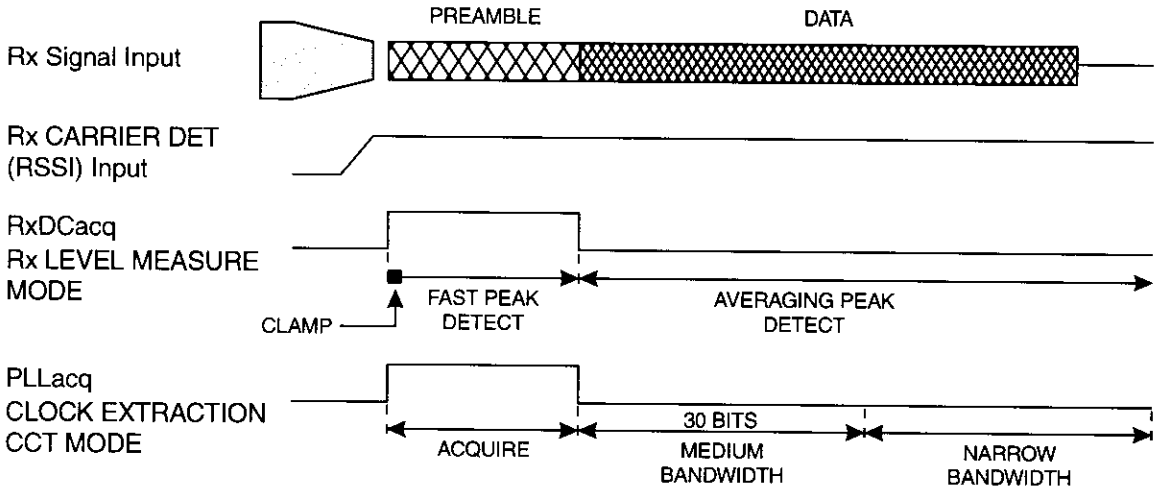

Figure 5: Rx Mode Control Diagram

PLLacq	$\overline{\text{Rx HOLD}}$	PLL Action	
1	1	Acquire	Sets the PLL bandwidth wide enough to allow a lock to the received signal in less than 8 zero crossings. This mode will operate as long as PLLacq is a logic 1
1 to 0	1	Medium Bandwidth	The correction applied to the extracted clock is limited to a maximum of ± 1/16th bit-period for every two received zero crossings. The PLL operates in this mode for a period of about 30 bits immediately following a 1 to 0 transition of PLLacq input, provided that the $\overline{\text{Rx HOLD}}$ Input is a logic 1.
0	1	Narrow Bandwidth	The correction applied to the extracted clock is limited to a maximum of ± 1/64th bit-period for every two received zero crossings. The PLL operates in this mode whenever the $\overline{\text{Rx HOLD}}$ Input is a logic 1 and PLLacq has been a logic 0 for at least 30 bit periods (after Medium Bandwidth operation for instance)
0	0	Hold	The PLL feedback loop is broken, allowing the Rx Clock to freewheel during signal fade periods.
RxDCacq	**$\overline{\text{Rx HOLD}}$**	**Rx Level Measure Action**	
0 to 1	X	Clamp	Operates for one bit-time after a 0 to 1 transition of the RxDCacq input. The external capacitors are rapidly charged towards a voltage mid way between the received signal input level and V_{BIAS} with the charge time-constant being of the order of 0.5 bit-time.
1	X	Fast Peak Detect	The voltage detectors act as peak detectors, one capacitor is used to capture the positive -going signal peaks of the Rx Filter output signal and the other capturing the negative-going peaks. The detectors operate in this mode whenever the RxDCacq input is at a logic 1 except for the initial 1-bit Clamp Mode time.
0	1	Averaging Peak Detect	Provides a slower but more accurate measurement of the signal peak amplitudes.
0	0	Hold	The capacitor charging circuits are disabled so that the outputs of the voltage detectors remain substantially at the last readings (discharging very slowly [time-constant approx. 2,000 bits] towards V_{BIAS})

X = Don't care

Table 2: PLL and Rx Level Measurement Operational Modes

4.2.3 Rx Clock Extraction

Synchronized by a PLL circuit to zero-crossings of the incoming data, the Rx Clock Extraction circuitry controls the Rx Clock output. The Rx Clock is also used internally by the Data Extraction circuitry. The PLL parameters can be varied by the Rx Circuit Control inputs PLLacq and Rx HOLD to operated in one of four PLL modes as described in Table 2

4.2.4 Rx Data Extraction

The Rx Data Extraction circuit decides whether each received bit is a 1 or 0 by sampling the received signal, after filtering, and comparing the sample values to an adaptive threshold derived from the Level Measuring circuit. This threshold is adapted from bit to bit to compensate for intersymbol interference caused by the bandlimiting of the overall transmission path and the Gaussian premodulation filter. The extracted data is output from the Rx Data pin, and should be sampled externally on the rising edge of the Rx CLK.

4.2.5 Rx S/N Detection

The Rx S/N Detector system classifies the incoming zero-crossings as GOOD or BAD depending upon the time when each crossing actually occurs with respect to its expected time as determined by the Clock Extraction PLL. This information is then processed to provide a logic level output at the Rx S/N pin. A high level indicates a series of GOOD crossings; a low level indicates a BAD crossing.

By averaging this output it is possible to derive a measure of the Signal-to-Noise-Ratio and therefore the Bit-Error-Rate of the received signal.

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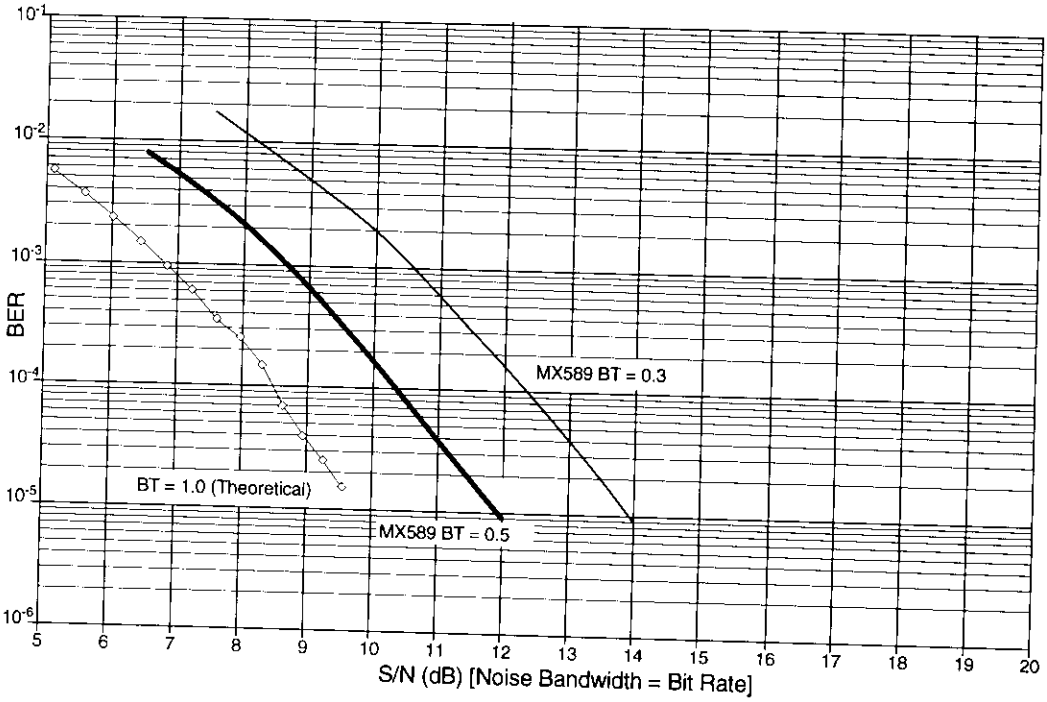

Figure 6: Typical Bit-Error-Rate Performance

4.2.6 Rx Signal Quality

The effect of input Rx signal quality on the Rx S/N output is shown in Figure 7.

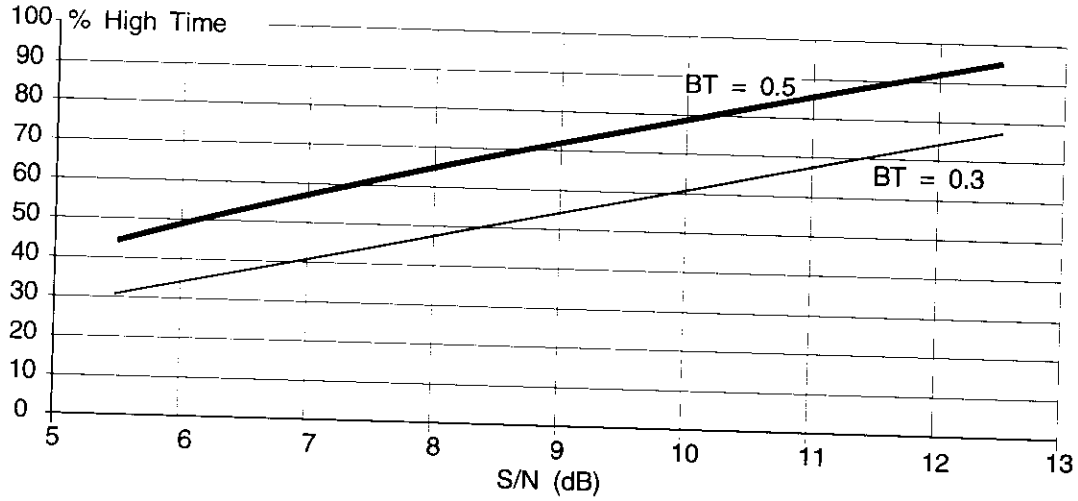

Figure 7: Typical Rx S/N Output High time (%) vs Input S/N

4.3 Transmit

4.3.1 Tx Signal Path Description

The binary data applied to the Tx Data input is retimed within the chip on each rising edge of the Tx Clock and then converted to a 1-volt peak-to-peak binary signal centered about V_{BIAS} (for V_{DD} = 5.0V)

If the Tx Enable input is high, then this internal binary signal will be connected to the input of the lowpass Tx Filter, and the output of the filter connected to the Tx Out pin.

Tx Enable	Tx Filter Input	Tx Out Pin
1	$V_{DD}/5$ V_{P-P} Data	Filtered Data
0	V_{BIAS}	V_{BIAS} via 500kΩ

A low input to the Tx Enable will connect the input of the Tx Filter to V_{BIAS}, and disconnect the Tx Out pin from the filter, connecting it instead to V_{BIAS} through a high resistance (nominally 500kΩ).

The Tx Filter has a lowpass frequency response, which is approximately gaussian in shape as shown in Figure 9, to minimize amplitude and phase distortion of the binary signal while providing sufficient attenuation of the high frequency-components which would otherwise cause interference into adjacent radio channels. The actual filter bandwidth to be used in any particular application will be determined by the overall system requirements. The attenuation-vs-frequency response of the transmit filtering provided by the MX589 have been designed to meet the specifications for most GMSK modem systems, having a -3dB bandwidth switchable between 0.3 and 0.5 times the data bit-rate (BT).

Note: An external RC network is required between the Tx Out pin and the input to the Frequency Modulator (see Figure 2 and Figure 3). This network, which can form part of any DC level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering. The ground connection to capacitor C1 should be positioned to give maximum attenuation of high-frequency noise into the modulator.

The signal at Tx Out is centered around V_{BIAS}, going positive for logic 1 (high) level inputs to the Tx Data input and negative for logic 0 (low) inputs.

When the transmit circuits are put into a powersave mode (by a logic 1 to the Tx PS pin) the output voltage of the Tx Filter will go to V_{SS}. When power is subsequently restored to the Tx Filter, its output will take several bit-times to settle. The Tx Enable input can be used to prevent these abnormal voltages from appearing at the Tx Out pin.

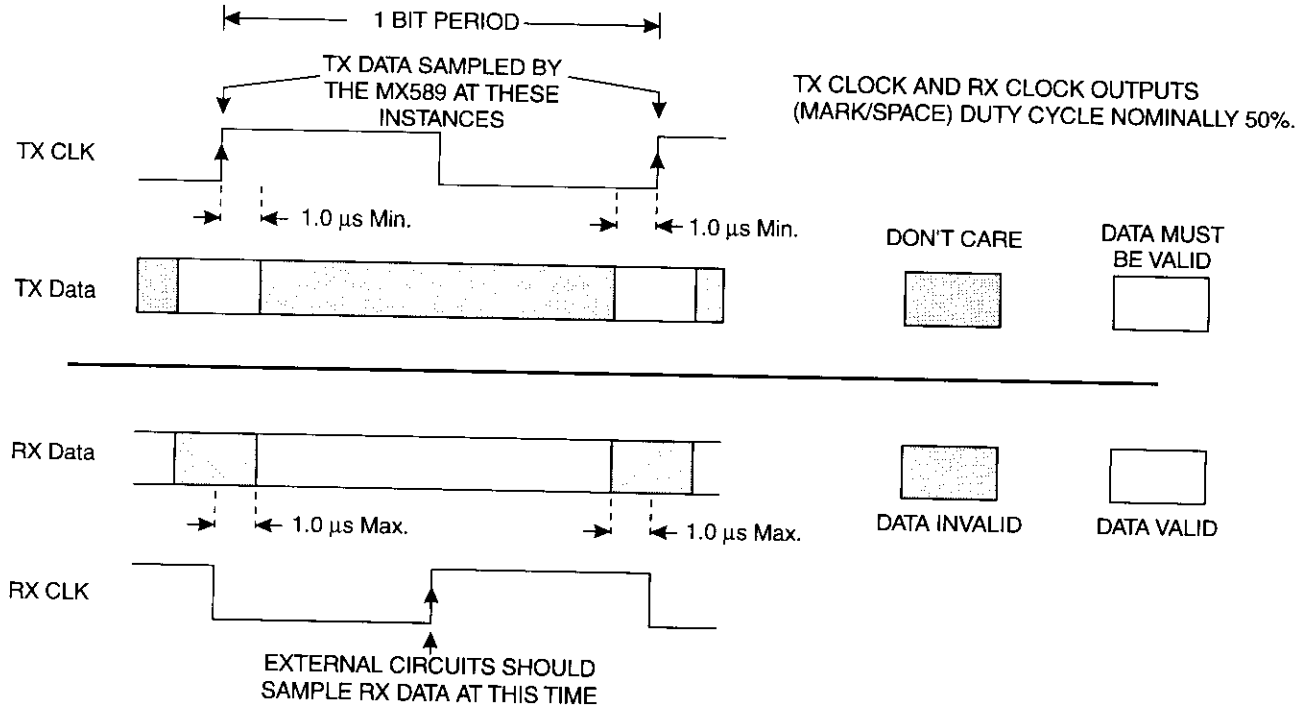

Figure 8: Rx and Tx Clock Data Timings

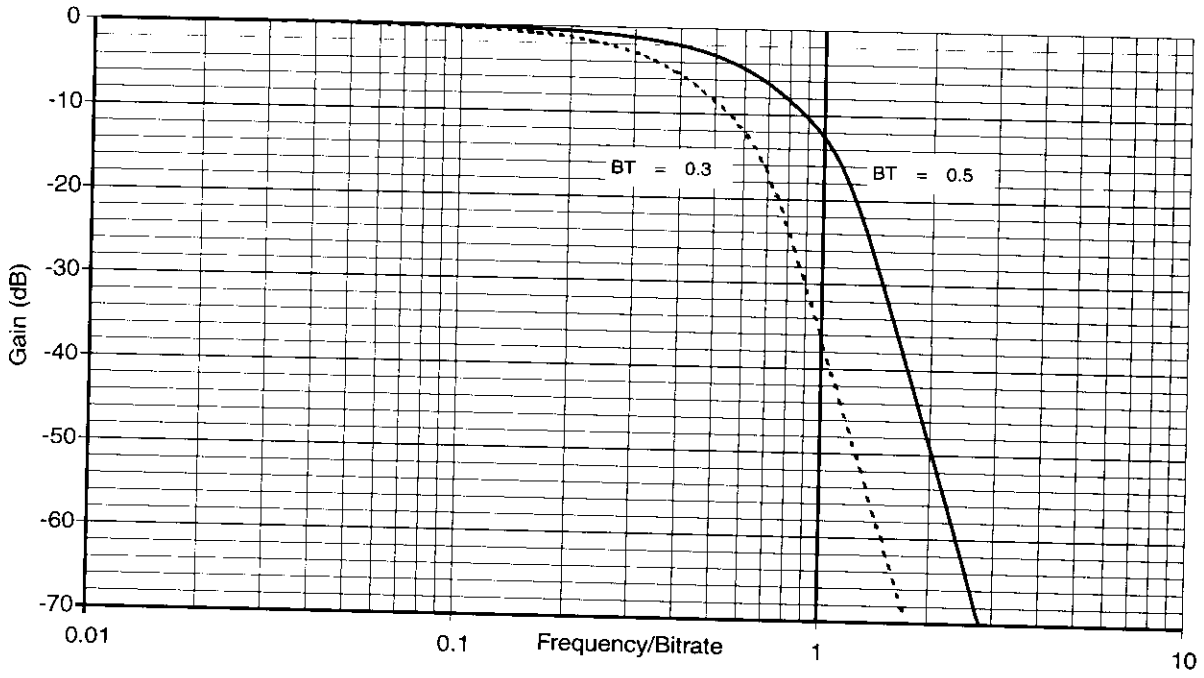

Figure 9: Tx Filter Response

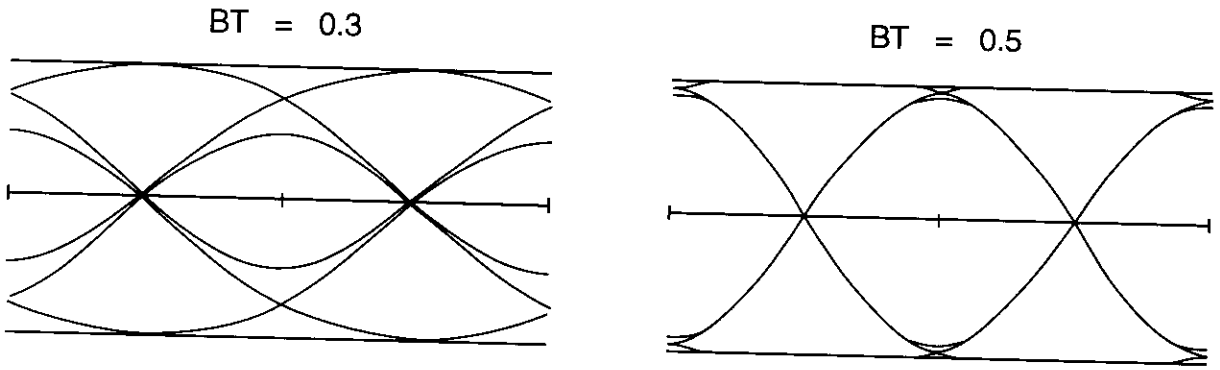

Figure 10: Typical Transmit Eye Patterns

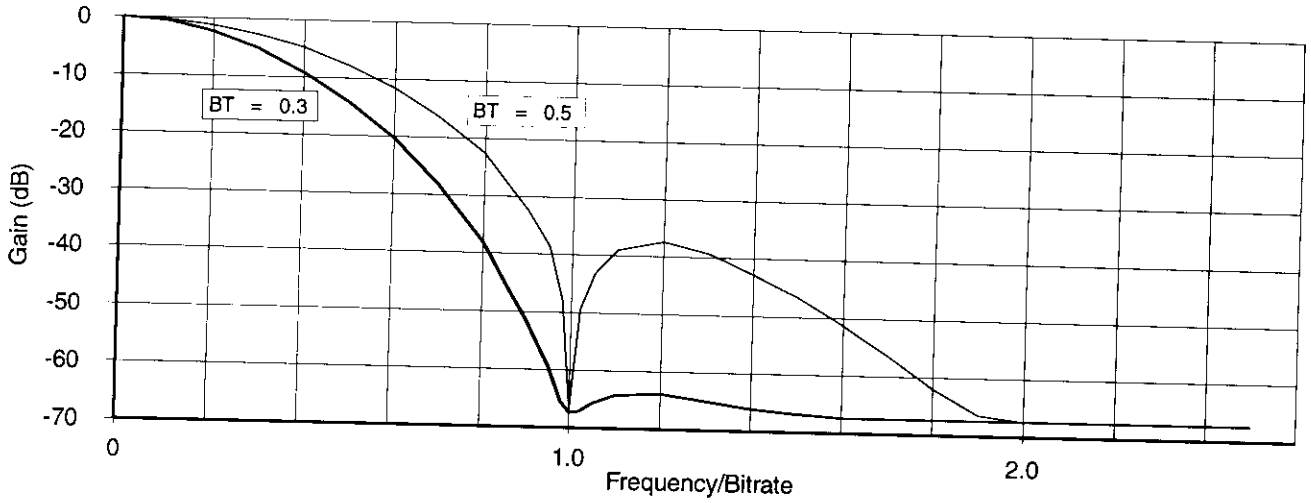

Figure 11: Tx Output spectrum (Random Data)

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4.4 Data Formats

The receive section of the MX589 works best with data which has a reasonably random structure --the data should contain approximately the same number of ones as zeroes with no long sequences (>100 bits) of consecutive ones or zeroes. Also, long sequences (>100 bits) of 10101010 ... patterns should be avoided.

For this reason, it is recommended that data is made random in some manner before transmission, for example by exclusive-ORing it with the output of a binary pseudo-random pattern generator.

Where data is transmitted in bursts, each burst should be preceded by a preamble designed to allow the receive modem to establish timing and level lock as quickly as possible. This preamble for BT = 0.3 should be at least 16 bits long, and should preferably consist of alternating pairs of ones and zeroes i.e. 110011001100 .....; the eye of pattern 10101010 .... has the most gradual slope and will yield poor peak levels for the Rx circuits. For BT = 0.5 the eye pattern of 10101010... has reduced intersymbol interference and may be used as the preamble (DC Acq pin should be held high during preamble). See Fig. 6.

4.5 Acquisition and Hold Modes

The RxDCacq and PLLacq inputs must be pulsed High for about 16 bits at the start of reception to ensure that the DC measurement and timing extraction circuits lock-on to the received signal correctly. Once lock has been achieved, then the above inputs should be taken Low again.

In most applications, there will be a DC step in the output voltage from the receiver FM discriminator due to carrier frequency offsets as channels are changed or when the remote transmitter is turned on.

The MX589 can tolerate DC offsets in the received signal of at least ±0.5V with respect to V_{BIAS}, (measured at the Rx Feedback pin). However, to ensure that the DC offset compensation circuit operates correctly and with minimum delay, the Low to High transition of the RxDCacq and PLLacq inputs should occur after the mean input voltage to the MX589 has settled to within about 0.1V of its final value.

Note: This can place restrictions on the value of any series signal coupling capacitor.

As well as using the Rx Hold input to freeze the Level Measuring and Clock Extraction circuits during a signal fade, it may also be used in systems which use a continuously transmitting control channel to freeze the Rx circuitry during transmission of a data packet, allowing reception to resume afterwards without losing bit synchronization. To achieve this, the MX589 Xtal clock needs to be accurate enough that the derived RxClock output does not drift by more than about 0.1 bit time from the actual received data-rate during the time that the RxHold input is Low.

The RxDCacq input, however, may need to be pulsed high for 2 bit durations to re-establish the level measurements if the RxHold input is low for more that a few hundred bit-times (exact number depends on system crystal tolerances).

The voltages on the Doc1 and Doc2 pins reflect the average peak positive and negative excursions of the (filtered) receive signal, and could therefore be used to derive a measure of the data signal amplitude.

Note: These pins are driven from very high-impedance circuits, so that the DC load presented by any external circuitry should exceed 10MΩ to V_{BIAS}.

5. Application

5.1 Radio Channel Requirements

To achieve legal adjacent channel performance at high bit-rates, a radio with an accurate carrier frequency and an accurate modulation index is required. For optimum channel utilization, (e.g. low BER and high data-rates) attention must be paid to the phase and frequency response of both the IF and baseband circuitry.

5.1.1 Bitrate, BT and Bandwidth

The maximum data rate that can be transmitted over a radio channel depends on the following:

Channel spacing

Allowable adjacent channel interference

Tx filter bandwidth

Peak carrier deviation (Modulation Index)

Tx and Rx carrier frequency accuracies

Modulator and Demodulator linearity

Rx IF filter frequency and phase characteristics

Use of error correction techniques

Acceptable error-rate

As a guide to MOBITEX operation, a raw data-rate of 8kbps at 12.5kHz channel spacing may be achievable -depending on local regulatory requirements- using a ±2kHz maximum deviation, a BT of 0.3, and no more than 1.5kHz discrepancy between Tx & Rx carrier frequencies. Forward error correction (FEC) could then be used with interleaving to reduce the effect of burst errors.

Reducing the data-rate to 4.8kbps would allow the BT to be increased to 0.5, improving the error-rate performance.

5.1.2 FM Modulator, Demodulator and IF

For optimum performance, the eye pattern of the received signal (when receiving random data) applied to the MX589 should be as close as possible to the Transmit eye pattern examples shown in Figure 11.

Of particular importance are general symmetry, cleanliness of the zero-crossings, and for a BT of 0.3, the relative amplitude of the inner eye opening.

To achieve this, attention must be paid to -

Linearity and frequency/phase response of the Tx frequency modulator. Unless the transmit data is especially encoded to remove low frequency components, the modulator frequency response should extend down to a few hertz. This is because two-point modulation is necessary for synthesized radios.

Bandwidth & phase response of the Rx IF filters.

Accuracy of the Tx and Rx carrier frequencies -any difference will shift the received signal towards one of the skirts of the IF filter response.

Ideally, the Rx demodulator should be DC coupled to the MX589 Rx Signal In pin (with a DC bias added to center the signal at the Rx Feedback pin around $V_{DD}/2$ [V_{BIAS}]). However AC coupling can be used provided that:

The 3 dB cut-off frequency is 20Hz or below (i.e. a 0.1µF capacitor in series with 100kΩ).

The data does not contain long sequences of consecutive ones or zeroes.

Sufficient time is allowed after a step change at the discriminator output (resulting from channel changing or the appearance of an RF carrier) for the voltage into the MX589 to settle before the RxDCacq line is strobed.

5.1.3 Two Point Modulation

When designing the MX589 into a radio that uses a frequency synthesizer, a two-point modulation technique is recommended. This is both to prevent the radio's PLL circuitry from counteracting the modulation process, and to provide a clean flat modulation response down to DC

Figure 12 shows a suggested basic configuration to provide a two-point modulation drive from the MX589 Tx Output using MX•COM's MX019 Digitally Controlled Quad Amplifier Array. The MX019 elements provide individual set-up, calibration and dynamic control of modulation levels. Level setting control of the amplifiers/attenuators of the MX019 is via an 8-bit data word.

With reference to Figure 12:

The buffer amplifier is required to prevent loading of the MX589 external RC circuit.

Stage B, with R1/R2, provides suitable signal and DC levels for the VCO varactor; C1 is RF decoupling. The drive level should be adjusted (digitally) to provide the desired deviation.

Stage C, with R3/R4, provides the Reference Oscillator drive (application dependent). This parameter is set by adjusting for minimum AC signal on the PLL control voltage with a low-frequency modulating signal (inside the PLL bandwidth) applied.

Stage D could be used with the components shown if a negative reference drive is required.

Stage A provides buffering and overall level control.

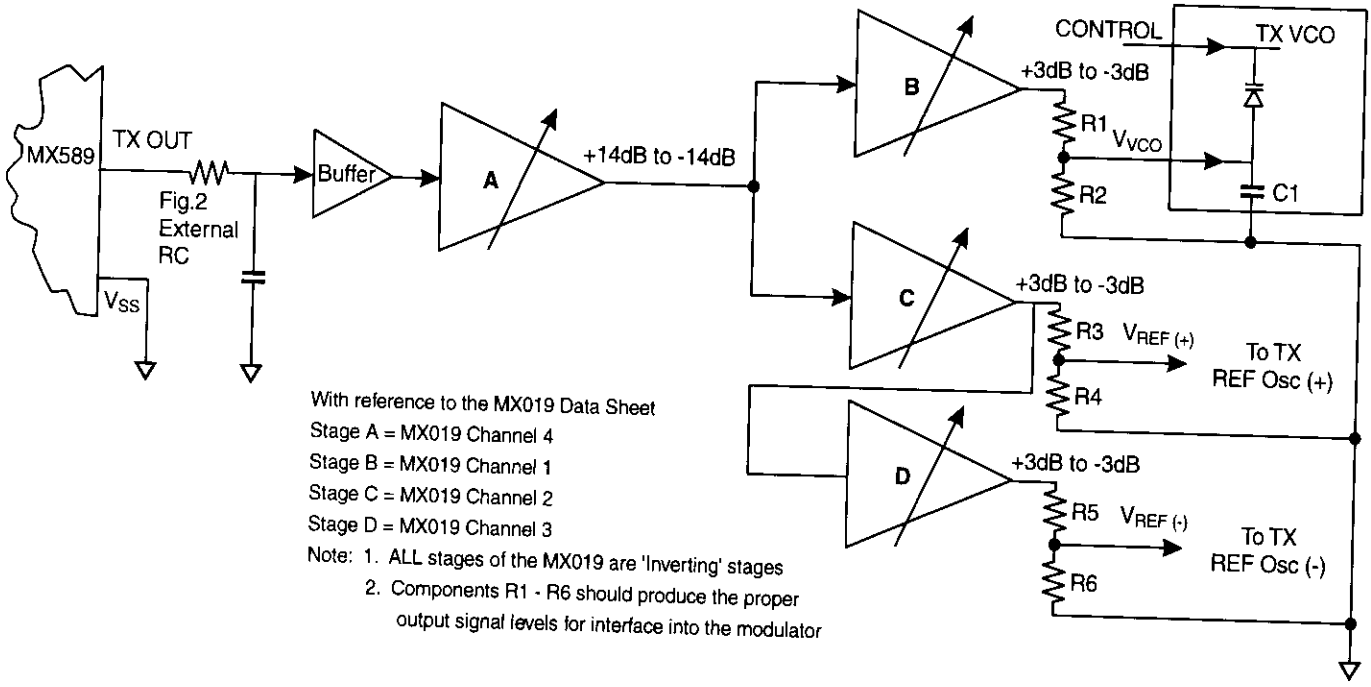

Figure 12: An Example of Two-Point Modulation Drive with Individual Adjustment Using the MX019

5.2 AC Coupling of Tx and Rx Signals

In practical applications, it will usually be possible to arrange for any AC coupling between the MX589 Tx Output and the frequency modulator to cut-off at a very low frequency such as 5.0Hz, but Ac coupling between the receive discriminator and the input of the MX589 may need to have a shorter time-constant to avoid problems from voltage steps at the output of the discriminator when changing channels or when the distant transmitter turns on.

For these reasons, as well as to maintain reasonable BER, the optimum -3dB cut-off frequencies are around 5.0Hz in the Tx path and 20.Hz in the Rx path.

Figure 13 shows the typical static Bit-Error-Rate performance of the MX589 operating under nominal conditions for various degrees of AC coupling at the Rx input and the Tx Output:

Data Rate = 8kbps V_{DD} = 5.0V T_{AMB} = 25°C Tx BT = 0.3

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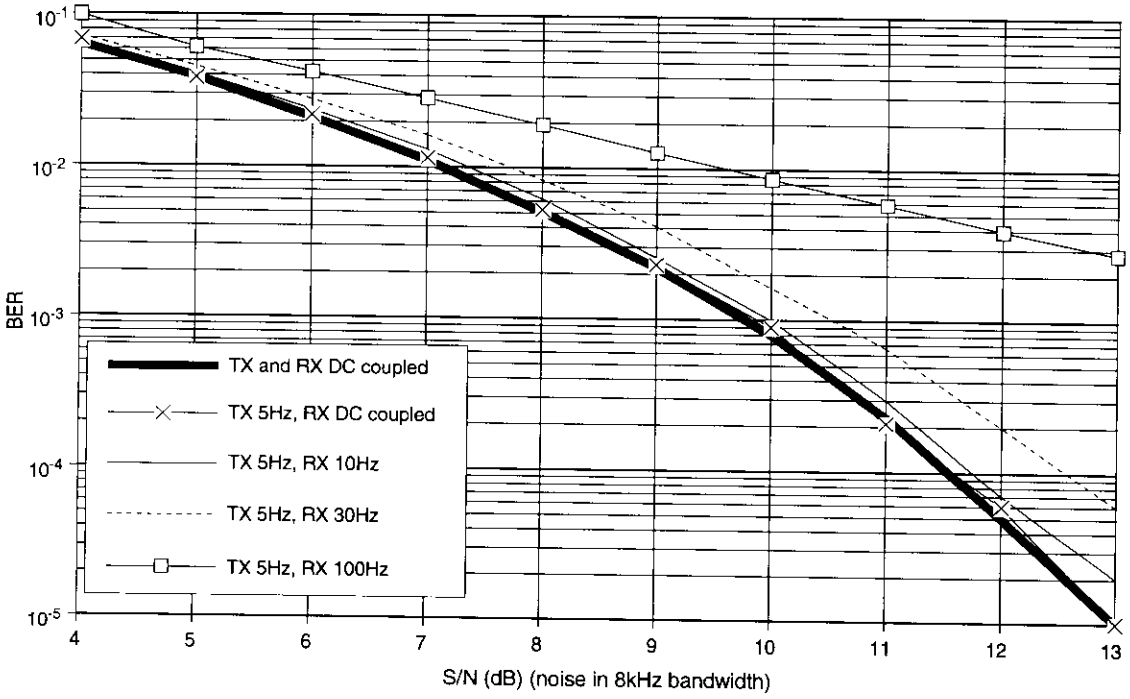

Figure 13: Effect of AC Coupling on Typical Bit-Error Rate

6. Performance Specification

6.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pins	-20	20	mA
DW / PDIP Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	85	°C
Operating Temperature	-40	85	°C
TN Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		550	mW
Derating above 25°C		9	mW/°C above 25°C
Storage Temperature	-55	85	°C
Operating Temperature	-40	85	°C

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Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Temperature		-40	85	°C
Rx and Tx Data Rate				
$V_{DD} \geq 3.0V$		4	32	kbps
$V_{DD} \geq 4.5V$		4	64	kbps
Xtal/Clock Frequency				
$V_{DD} \geq 3.0V$		1.0	5.0	MHz
$V_{DD} \geq 4.5V$		1.0	10.3	MHz
High Pulse Width	1	40		ns
Low Pulse Width	1	40		ns

Operating Limits Notes:

1. Timing for an external clock input to the Xtal/Clock pin.

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Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 5.0V @ T_{AMB} = 25°C

Xtal Frequency = 4.096mhz Data Rate = 8kbps Noise Bandwidth = Bit Rate

			Notes	Min.	Typ.	Max	Units
Static Values							
Supply Current	Tx PS	Rx PS	1				
I_{DD} (V_{DD} = 3.0V)							
	1	1			0.5		mA
	0	1			1.0		mA
	1	0			1.0		mA
	0	0			1.5		mA
I_{DD}							
	1	1			1.0		mA
	0	1			2.0		mA
	1	0			3.0		mA
	0	0			4.0		mA
Input Logic Level							
Logic 1 Input Level				3.5			V
Logic 0 Input Level						1.5	V
Logic Input Current			2	-5.0		5.0	µA
Logic 1 Output Level (I_{OH} = -120µA)				4.6			V
Logic 0 Output Level (I_{OL} = -120µA)						0.4	V
Transmit Parameters							
Tx OUT, Output Impedance			3		1.0		kΩ
Tx OUT, Level			4,10	0.8	1.0	1.2	V_{P-P}
Tx Data Delay							
BT = 0.3			5		2.0	2.5	bit-periods
BT = 0.5			5		1.5	2.0	bit-periods
Tx PS to Output-Stable time			6		4.0		
Receive Parameters							
Rx Amplifier-							
Input Impedance				1.0			MΩ
Output Impedance			7		10.0		kΩ
Voltage Gain					50.0		dB
Rx Filter Signal Input Level			8, 10	0.7	1.0	1.3	V_{P-P}
Rx Time Delay			9			3.0	bit-periods
On-Chip Xtal Oscillator							
R_{IN}				10.0			MΩ
R_{OUT}			11		50.0		kΩ
Voltage Gain			11		25.0		dB

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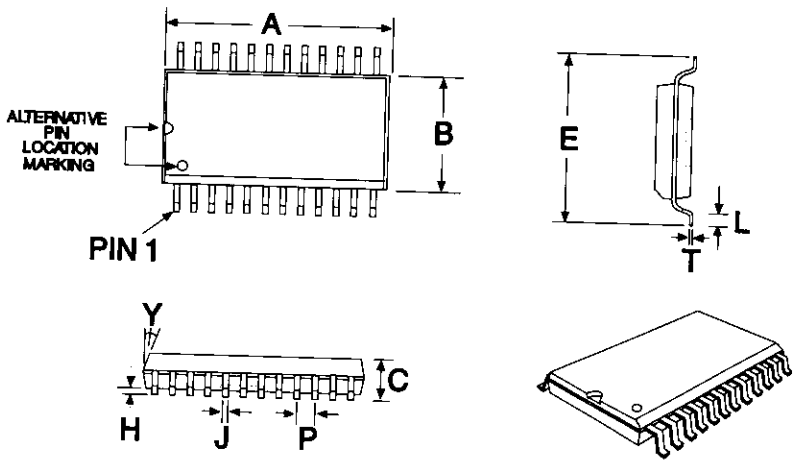
Operating Characteristics Notes:

1. Not including current drawn from the MX589 pins by external circuitry. See Absolute Maximum Ratings.
2. For V_{IN} in the range V_{SS} to V_{DD}.
3 For a load of 10kW or greater. Tx PS input at logic 0; Tx Enable = 1.
4. Data pattern of 1111000011110000 ..
5. Measured between the rising edge of Tx Clock and the center of the corresponding bit at Tx Out.
6. Time between the falling edge of Tx PS and the Tx Out voltage stabilizing to normal output levels.
7. For a load of 10kW or greater. Rx PS input at logic 0.
8. For optimum performance, Measured at the Rx Feedback pin for a 1111000011110000 ... pattern.
9. Measured between the center of bit at Rx Signal In and corresponding rising edge of the Rx Clock.
10 Levels are proportional to applied V_{DD}.
11. Small signal measurement at 1.0kHz with no load on Xtal output.

6.2 Packaging

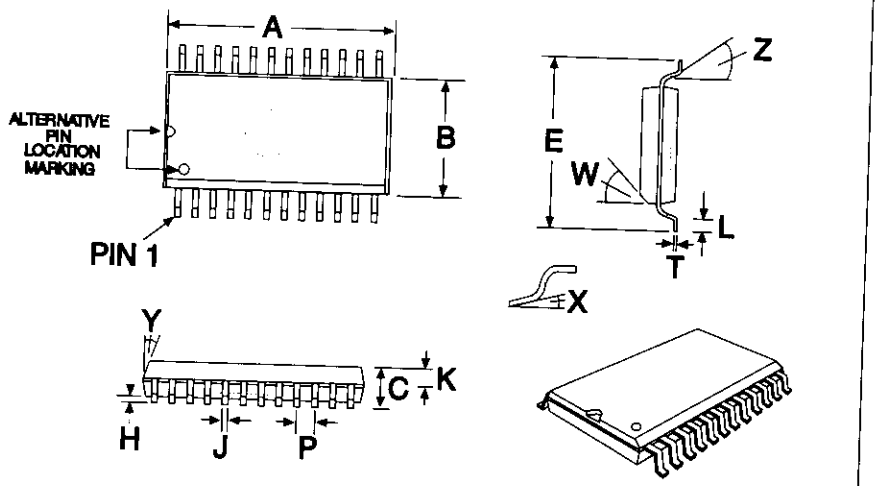


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.303 (7.70)		0.311 (7.90)
B	0.169 (4.30)		0.177 (4.50)
C	----------		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.0256 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
Y	0°		8°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 14: 24-pin TSSOP Mechanical Outline: *Order as part no. MX589TN*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 15: 24-pin SOIC Mechanical Outline: *Order as part no. MX589DW*

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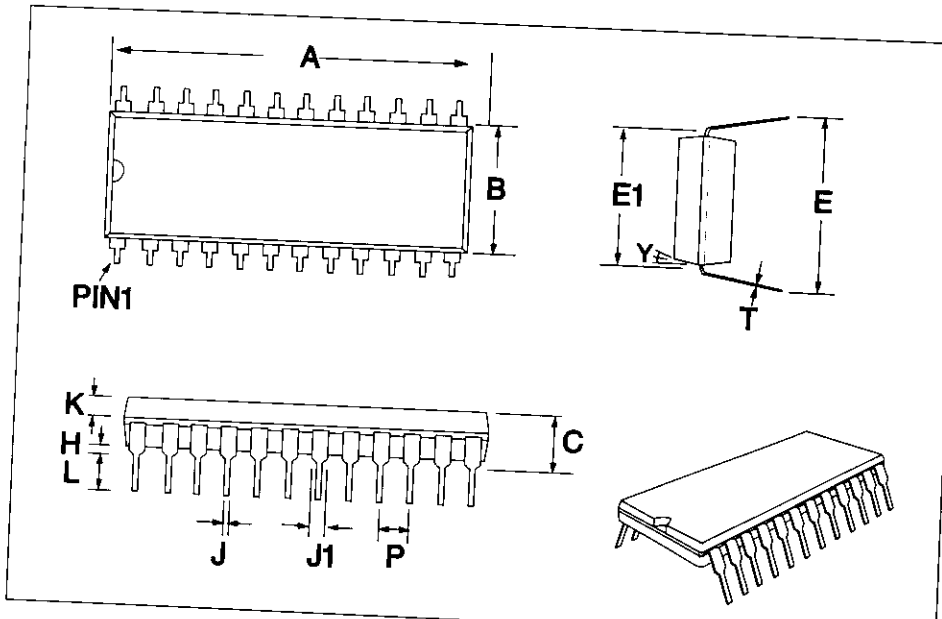

Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 16: 24-pin PDIP Mechanical Outline: ***Order as part no. MX589P***

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MC68HC16Z1

Technical Supplement

25.17 MHz Electrical Characteristics

Devices in the M68HC16 Modular Microcontroller Family are built up from a selection of standard functional modules. Published electrical characteristics for MC68HC16Z1 devices are based on a16.78 MHz system clock. New products that operate at clock frequencies of 25.17 MHz are now available. This supplement consists of a new electrical characteristics appendix (Appendix A) that supplements those published in the *MC68HC16Z1 User's Manual* (MC68HC16Z1UM/AD).

The supplement contains the following updated specifications:

Table A–1 Maximum Ratings

Num	Rating	Symbol	Value	Unit
1	Supply Voltage[1, 2, 3]	V_{DD}	– 0.3 to + 6.5	V
2	Input Voltage [1, 2, 3, 4, 5,7]	V_{IN}	– 0.3 to + 6.5	V
3	Instantaneous Maximum Current Single Pin Limit (all pins)[1, 3, 5, 6]	I_D	25	mA
4	Operating Maximum Current Digital Input Disruptive Current[3, 5, 6, 7, 8] $V_{NEGCLMAP} \cong -0.3$ V $V_{POSCLAMP} \cong V_{DD} + 0.3$	I_{ID}	– 500 to 500	µA
5	Operating Temperature Range "C" Suffix "V" Suffix "M" Suffix	T_A	TL to TH – 40 to 85 – 40 to 105 – 40 to 125	°C
6	Storage Temperature Range	T_{stg}	– 55 to 150	°C

NOTES:

1. Permanent damage can occur if maximum ratings are exceeded. Exposure to voltages or currents in excess of recommended values affects device reliability. Device modules may not operate normally while being exposed to electrical extremes.
2. Although sections of the device contain circuitry to protect against damage from high static voltages or electrical fields, take normal precautions to avoid exposure to voltages higher than maximum-rated voltages.
3. This parameter is periodically sampled rather than 100% tested.
4. All pins except TSC.
5. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
6. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current.
7. All functional non-supply pins are internally clamped to V_{SS}. All functional pins except EXTAL and XFC are internally clamped to V_{DD}.
8. Total input current for all digital input-only and all digital input/output pins must not exceed 10 mA. Exceeding this limit can cause disruption of normal operation.

Table A–2 Typical Ratings

Num	Rating	Symbol	Value	Unit
1	Supply Voltage	V_{DD}	5.0	V
2	Operating Temperature	T_A	25	°C
3	V_{DD} Supply Current RUN LPSTOP, VCO off LPSTOP, External clock, max f_{sys}	I_{DD}	 113 125 3.75	 mA µA mA
4	Clock Synthesizer Operating Voltage	V_{DDSYN}	5.0	V
5	V_{DDSYN} Supply Current VCO on, maximum f_{sys} External Clock, maximum f_{sys} LPSTOP, VCO off V_{DD} powered down	I_{DDSYN}	 1.0 5.0 100 50	 mA mA µA µA
6	RAM Standby Voltage	V_{SB}	3.0	V
7	RAM Standby Current Normal RAM operation Standby operation	ISB	 7.0 40	 µA µA
8	Power Dissipation	P_D	570	mW

Table A–3 Thermal Characteristics

Num	Characteristic	Symbol	Value	Unit
1	Thermal Resistance[1] Plastic 132-Pin Surface Mount Plastic 144-Pin Surface Mount	Θ_{JA}	 38 49	°C/W

NOTES:

1. The average chip-junction temperature (TJ) in C can be obtained from (1):

$$T_J = T_A + (P_D \cdot \Theta_{JA})$$

where:

T_A= Ambient Temperature, °C

Θ_{JA}= Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$, Watts — Chip Internal Power

$P_{I/O}$= Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is (2):

$$P_D = K + (T_J + 273°C)$$

Solving equations (1) and (2) for K gives (3):

$$K = P_D + (T_A + 273°C) + \Theta_{JA} \times P_{D^2}$$

Where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring PD (at equilibrium) for a known TA. Using this value of K, the values of PD and TJ can be obtained by solving equations (1) and (2) iteratively for any value of TA.

Table A–4 Clock Control Timing

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, Stable External Reference)[1]

Num	Characteristic	Symbol	Minimum	Maximum	Unit
1	PLL Reference Frequency Range	f_{ref}	25	50	kHz
2	System Frequency[2] On-Chip PLL System Frequency External Clock Operation	f_{sys}	dc 0.131 dc	25.17 25.17 25.17	MHz
3	PLL Lock Time[3,5,6,7]	t_{lpll}	—	20	ms
4	VCO Frequency[4]	f_{VCO}	—	2 (f_{sys} max)	MHz
5	Limp Mode Clock Frequency SYNCR X bit = 0 SYNCR X bit = 1	f_{limp}	— —	f_{sys} max /2 f_{sys} max	MHz
6	CLKOUT Jitter[5,6,7,8] Short term (5 µs interval) Long term (500 µs interval)	J_{clk}	–1.0 –0.5	1.0 0.5	%

NOTES:

1. Tested with a 32.768 kHz reference.
2. All internal registers retain data at 0 Hz.
3. Assumes that stable V_{DDSYN} is applied, and that the crystal oscillator is stable. Lock time is measured from the time V_{DD} and V_{DDSYN} are valid until $\overline{RESET}$ is released. This specification also applies to the period required for PLL lock after changing the W and Y frequency control bits in the synthesizer control register (SYNCR) while the PLL is running, and to the period required for the clock to lock after LPSTOP.
4. Internal VCO frequency (f_{VCO}) is determined by SYNCR W and Y bit values.
   The SYNCR X bit controls a divide-by-two circuit that is not in the synthesizer feedback loop.
   When X = 0, the divider is enabled, and $f_{sys} = f_{VCO} \div 4$.
   When X = 1, the divider is disabled, and $f_{sys} = f_{VCO} \div 2$.
   X must equal one when operating at maximum specified f_{sys}.
5. This parameter is periodically sampled rather than 100% tested.
6. Assumes that a low-leakage external filter network is used to condition clock synthesizer input voltage. Total external resistance from the XFC pin due to external leakage must be greater than 15 M Ω to guarantee this specification. Filter network geometry can vary depending upon operating environment.
7. Proper layout procedures must be followed to achieve specifications.
8. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SS} and variation in crystal oscillator frequency increase the J_{clk} percentage for a given interval. When jitter is a critical constraint on control system operation, this parameter should be measured during functional testing of the final system.

Table A–5 DC Characteristics

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Num	Characteristic	Symbol	Min	Max	Unit
1	Input High Voltage	V_{IH}	0.7 (V_{DD})	V_{DD} + 0.3	V
2	Input Low Voltage	V_{IL}	V_{SS} – 0.3	0.2 (V_{DD})	V
3	Input Hysteresis[1, 2]	V_{HYS}	0.5	—	V
4	Input Leakage Current[3,16] V_{in} = V_{DD} or V_{SS}	I_{in}	– 2.5	2.5	µA
5	High Impedance (Off-State) Leakage Current[4,16] V_{in} = V_{DD} or V_{SS}	I_{OZ}	– 2.5	2.5	µA
6	CMOS Output High Voltage[5,6,16] I_{OH} = –10.0 µA	V_{OH}	V_{DD} – 0.2	—	V
7	CMOS Output Low Voltage[6,16] I_{OL} = 10.0 µA	V_{OL}	—	0.2	V
8	Output High Voltage[5,6,16] I_{OH} = –0.8 mA	V_{OH}	V_{DD} –0.8	—	V
9	Output Low Voltage[7,16] I_{OL} = 1.6 mA I_{OL} = 5.3 mA I_{OL} = 12 mA	V_{OL}	— — —	0.4 0.4 0.4	V
10	Three State Control Input High Voltage	V_{IHTSC}	1.6 (V_{DD})	9.1	V
11	Data Bus Mode Select Pull-up Current[8,9] V_{in} = V_{IL} V_{in} = V_{IH}	I_{MSP}	— –15	–120 —	µA
12	V_{DD} Supply Current[10,11, 12] Run LPSTOP, crystal reference, VCO Off (STSIM = 0) LPSTOP, external clock input frequency = maximum f_{sys}	I_{DD}	— — —	140 350 5	mA µA µA
13	Clock Synthesizer Operating Voltage	V_{DDSYN}	4.75	5.25	V
14	V_{DDSYN} Supply Current[6,12] Crystal reference, VCO on, maximum f_{sys} External clock input, maximum f_{sys} Crystal reference, LPSTOP, VCO off (STSIM = 0) Crystal reference, V_{DD} powered down	I_{DDSYN}	— — — —	2 7 150 100	mA mA µA µA
15	RAM Standby Voltage[13] Specified V_{DD} applied V_{DD} = V_{SS}	V_{SB}	0.0 3.0	5.25 5.25	V
16	RAM Standby Current[10] Normal RAM operation[14] $V_{DD} > V_{SB} – 0.5$ V Transient condition $V_{SB} – 0.5$ V ≥ V_{DD} ≥ V_{SS} + 0.5 V Standby operation[13] $V_{DD} < V_{SS}$ + 0.5 V	I_{SB}	— — —	10 3 50	µA mA µA
17	Power Dissipation[15, 16]	P_D	—	766	mW
18	Input Capacitance[2, 16] All input-only pins except ADC pins All input/output pins	C_{in}	— —	10 20	pF

Table A–5 DC Characteristics (Continued)

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Num	Characteristic	Symbol	Min	Max	Unit
19	Load Capacitance[16]				
	Group 1 I/O Pins, CLKOUT, FREEZE/QUOT, IPIPE0	C_L	—	90	pF
	Group 2 I/O Pins and $\overline{CSBOOT}$, $\overline{BG}/\overline{CS}$		—	100	
	Group 3 I/O Pins		—	130	
	Group 4 I/O Pins		—	200	

NOTES:

1. Applies to:
   Port ADA[7:0] — AN[7:0]
   Port E[7:4] — SIZ[1:0], $\overline{AS}$, $\overline{DS}$
   Port F[7:0] — IRQ[7:1], MODCLK
   Port GP[7:0] — IC4/OC5/OC1, IC[3:1], OC[4:1]/OC1
   Port QS[7:0] — TXD, PCS[3:1], PCS0/$\overline{SS}$, SCK, MOSI, MISO
   $\overline{BKPT}$/DSCLK, DSI/IPIPE1, PAI, PCLK, $\overline{RESET}$, RXD, TSC
   EXTAL (when PLL enabled)
2. This parameter is periodically sampled rather than 100% tested.
3. Applies to all input-only pins except ADC pins.
4. Applies to all input/output and output pins
5. Does not apply to $\overline{HALT}$ and $\overline{RESET}$ because they are open drain pins. Does not apply to Port QS[7:0] (TXD, PCS[3:1], PCS0/$\overline{SS}$, SCK, MOSI, MISO) in wired-OR mode.
6. Applies to Group 1, 2, 4 input/output and all output pins
7. Applies to Group 1, 2, 3, 4 input/output pins, $\overline{BG}/\overline{CS}$, CLKOUT, $\overline{CSBOOT}$, FREEZE/QUOT, and IPIPE0
8. Applies to DATA[15:0]
9. Use of an active pulldown device is recommended.
10. Total operating current is the sum of the appropriate I_{DD}, I_{DDSYN}, and I_{SB} values, plus I_{DDA}. I_{DD} values include supply currents for device modules powered by V_{DDE} and V_{DDI} pins.
11. Current measured at maximum system clock frequency, all modules active.
12. Tested with a 32.768 kHz crystal reference.
13. The SRAM module will not switch into standby mode as long as V_{SB} does not exceed V_{DD} by more than 0.5 volts. The SRAM array cannot be accessed while the module is in standby mode.
14. When V_{SB} is more than 0.3 V greater than V_{DD}, current flows between the V_{STBY} and V_{DD} pins, which causes standby current to increase toward the maximum transient condition specification. System noise on the V_{DD} and V_{STBY} pin can contribute to this condition.
15. Power dissipation measured at specified system clock frequency, all modules active. Power dissipation can be calculated using the expression:

$$P_D = \text{Maximum } V_{DD} (I_{DD} + I_{DDSYN} + I_{SB}) + \text{Maximum } V_{DDA} (I_{DDA})$$

    I_{DD} includes supply currents for all device modules powered by V_{DDE} and V_{DDI} pins.
16. Input-Only Pins: EXTAL, TSC, BKPT/DSCLK, PAI, PCLK, RXD
    Output-Only Pins: $\overline{CSBOOT}$, $\overline{BG}/\overline{CS1}$, CLKOUT, FREEZE/QUOT, DS0/IPIPE0, PWMA, PWMB
    Input/Output Pins:
    Group 1: Port GP[7:0] — IC4/OC5/OC1, IC[3:1], OC[4:1]/OC1
    DATA[15:0], DSI/IPIPE1
    Group 2: Port C[6:0] — ADDR[22:19]/$\overline{CS}$[9:6], FC[2:0]/$\overline{CS}$[5:3]
    Port E[7:0] — SIZ[1:0], $\overline{AS}$, $\overline{DS}$, $\overline{AVEC}$, $\overline{DSACK}$[1:0]
    Port F[7:0] — $\overline{IRQ}$[7:1], MODCLK
    Port QS[7:3] — TXD, PCS[3:1], PCS0/$\overline{SS}$, ADDR23/$\overline{CS10}$/ECLK
    ADDR[18:0], R/$\overline{W}$, $\overline{BERR}$, $\overline{BR}/\overline{CS0}$, $\overline{BGACK}/\overline{CS2}$
    Group 3: $\overline{HALT}$, $\overline{RESET}$
    Group 4: MISO, MOSI, SCK

Table A–6 AC Timing

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)[1]

Num	Characteristic	Symbol	Min	Max	Unit
F1	Frequency of Operation[2]	f	4 (f_{ref})	25.166	MHz
1	Clock Period	t_{cyc}	39.7	—	ns
1A	ECLK Period	t_{Ecyc}	318	—	ns
1B	External Clock Input Period[3]	t_{Xcyc}	39.7	—	ns
2, 3	Clock Pulse Width	t_{CW}	15	—	ns
2A, 3A	ECLK Pulse Width	t_{ECW}	155	—	ns
2B, 3B	External Clock Input High/Low Time[3]	t_{XCHL}	19.8	—	ns
4, 5	CLKOUT Rise and Fall Time	t_{Crf}	—	5	ns
4A, 5A	Rise and Fall Time (All Outputs except CLKOUT)	t_{rf}	—	8	ns
4B, 5B	External Clock Input Rise and Fall Time[4]	t_{XCrf}	—	4	ns
6	Clock High to ADDR, FC, SIZE Valid	t_{CHAV}	0	19	ns
7	Clock High to ADDR, Data, FC, SIZE, High Impedance	t_{CHAZx}	0	39	ns
8	Clock High to ADDR, FC, SIZE, Invalid	t_{CHAZn}	0	—	ns
9	Clock Low to $\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Asserted	t_{CLSA}	2	19	ns
9A	$\overline{AS}$ to $\overline{DS}$ or $\overline{CS}$ Asserted (Read)[5]	t_{STSA}	–10	15	ns
11	ADDR, FC, SIZE Valid to $\overline{AS}$, $\overline{CS}$, (and $\overline{DS}$ Read) Asserted	t_{AVSA}	8	—	ns
12	Clock Low to $\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Negated	t_{CLSN}	2	19	ns
13	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Negated to ADDR, FC SIZE Invalid (Address Hold)	t_{SNAI}	8	—	ns
14	$\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ Read) Width Asserted	t_{SWA}	65	—	ns
14A	$\overline{DS}$, $\overline{CS}$ Width Asserted (Write)	t_{SWAW}	25	—	ns
14B	$\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ Read) Width Asserted (Fast Cycle)	t_{SWDW}	22	—	ns
15	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Width Negated[6]	t_{SN}	22	—	ns
16	Clock High to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ High Impedance	t_{CHSZ}	—	39	ns
17	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Negated to R/$\overline{W}$ High	t_{SNRN}	10	—	ns
18	Clock High to R/$\overline{W}$ High	t_{CHRH}	0	19	ns
20	Clock High to R/$\overline{W}$ Low	t_{CHRL}	0	19	ns
21	R/$\overline{W}$ High to $\overline{AS}$, $\overline{CS}$ Asserted	t_{RAAA}	10	—	ns
22	R/$\overline{W}$ Low to $\overline{DS}$, $\overline{CS}$ Asserted (Write)	t_{RASA}	40	—	ns
23	Clock High to Data Out Valid	t_{CHDO}	—	19	ns
24	Data Out Valid to Negating Edge of $\overline{AS}$, $\overline{CS}$ (Fast Write Cycle)	t_{DVASN}	7	—	ns
25	$\overline{DS}$, $\overline{CS}$ Negated to Data Out Invalid (Data Out Hold)	t_{SNDOI}	5	—	ns
26	Data Out Valid to $\overline{DS}$, $\overline{CS}$ Asserted (Write)	t_{DVSA}	8	—	ns

Table A–6 AC Timing (Continued)

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)[1]

Num	Characteristic	Symbol	Min	Max	Unit
27	Data In Valid to Clock Low (Data Setup)	t_{DICL}	5	—	ns
27A	Late $\overline{BERR}$, $\overline{HALT}$ Asserted to Clock Low (Setup Time)	t_{BELCL}	10	—	ns
28	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{DSACK[1:0]}$, $\overline{BERR}$, $\overline{HALT}$, $\overline{AVEC}$ Negated	t_{SNDN}	0	50	ns
29	$\overline{DS}$, $\overline{CS}$ Negated to Data In Invalid (Data In Hold)[7]	t_{SNDI}	0	—	ns
29A	$\overline{DS}$, $\overline{CS}$ Negated to Data In High Impedance[7, 8]	t_{SHDI}	—	45	ns
30	CLKOUT Low to Data In Invalid (Fast Cycle Hold)[7]	t_{CLDI}	8	—	ns
30A	CLKOUT Low to Data In High Impedance[7]	t_{CLDH}	—	60	ns
31	$\overline{DSACK[1:0]}$ Asserted to Data In Valid[9]	t_{DADI}	—	35	ns
33	Clock Low to $\overline{BG}$ Asserted/Negated	t_{CLBAN}	—	19	ns
35	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted[10]	t_{BRAGA}	1	—	t_{cyc}
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	t_{GAGN}	1	2	t_{cyc}
39	$\overline{BG}$ Width Negated	t_{GH}	2	—	t_{cyc}
39A	$\overline{BG}$ Width Asserted	t_{GA}	1	—	t_{cyc}
46	R/$\overline{W}$ Width Asserted (Write or Read)	t_{RWA}	90	—	ns
46A	R/$\overline{W}$ Width Asserted (Fast Write or Read Cycle)	t_{RWAS}	55	—	ns
47A	Asynchronous Input Setup Time $\overline{BR}$, $\overline{BGACK}$, $\overline{DSACK[1:0]}$, $\overline{BERR}$, $\overline{AVEC}$, $\overline{HALT}$	t_{AIST}	5	—	ns
47B	Asynchronous Input Hold Time	t_{AIHT}	10	—	ns
48	$\overline{DSACK[1:0]}$ Asserted to $\overline{BERR}$, $\overline{HALT}$ Asserted[11]	t_{DABA}	—	27	ns
53	Data Out Hold from Clock High	t_{DOCH}	0	—	ns
54	Clock High to Data Out High Impedance	t_{CHDH}	—	23	ns
55	R/W Asserted to Data Bus Impedance Change	t_{RADC}	25	—	ns
70	Clock Low to Data Bus Driven (Show Cycle)	t_{SCLDD}	0	19	ns
71	Data Setup Time to Clock Low (Show Cycle)	t_{SCLDS}	8	—	ns
72	Data Hold from Clock Low (Show Cycle)	t_{SCLDH}	8	—	ns
73	$\overline{BKPT}$ Input Setup Time	t_{BKST}	10	—	ns
74	$\overline{BKPT}$ Input Hold Time	t_{BKHT}	10	—	ns
75	Mode Select Setup Time (DATA[15:0], $\overline{MODCLK}$, $\overline{BKPT}$)	t_{MSS}	20	—	t_{cyc}
76	Mode Select Hold Time (DATA[15:0], $\overline{MODCLK}$, $\overline{BKPT}$)	t_{MSH}	0	—	ns
77	$\overline{RESET}$ Assertion Time[12]	t_{RSTA}	4	—	t_{cyc}
78	$\overline{RESET}$ Rise Time[13,14]	t_{RSTR}	—	10	t_{cyc}

Table A–6 AC Timing (Continued)

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)[1]

Num	Characteristic	Symbol	Min	Max	Unit
100	CLKOUT High to Phase 1 Asserted[15]	t_{CHP1A}	3	34	ns
101	CLKOUT High to Phase 2 Asserted[15]	t_{CHP2A}	3	34	ns
102	Phase 1 Valid to $\overline{AS}$ or $\overline{DS}$ Asserted[15]	t_{P1VSA}	9	—	ns
103	Phase 2 Valid to $\overline{AS}$ or $\overline{DS}$ Asserted[15]	t_{P2VSN}	9	—	ns
104	$\overline{AS}$ or $\overline{DS}$ Valid to Phase 1 Negated[15]	t_{SAP1N}	9	—	ns
105	$\overline{AS}$ or $\overline{DS}$ Negated to Phase 2 Negated[15]	t_{SNP2N}	9	—	ns

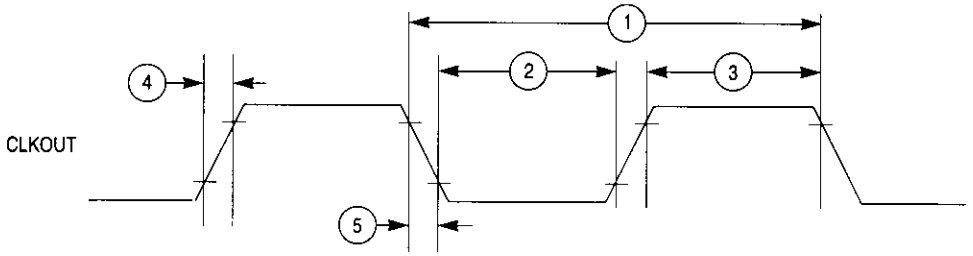
NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
2. Minimum system clock frequency is four times the crystal frequency, subject to specified limits.
3. When an external clock is used, minimum high and low times are based on a 50% duty cycle. The minimum allowable t_{Xcyc} period is reduced when the duty cycle of the external clock varies. The relationship between external clock input duty cycle and minimum t_{Xcyc} is expressed:

   Minimum t_{Xcyc} period = minimum t_{XCHL} / (50% – external clock input duty cycle tolerance).
4. Parameters for an external clock signal applied while the internal PLL is disabled (MODCLK pin held low during reset). Does not pertain to an external VCO reference applied while the PLL is enabled (MODCLK pin held high during reset). When the PLL is enabled, the clock synthesizer detects successive transitions of the reference signal. If transitions occur within the correct clock period, rise/fall times and duty cycle are not critical.
5. Specification 9A is the worst-case skew between $\overline{AS}$ and $\overline{DS}$ or $\overline{CS}$. The amount of skew depends on the relative loading of these signals. When loads are kept within specified limits, skew will not cause $\overline{AS}$ and $\overline{DS}$ to fall outside the limits shown in specification 9.
6. If multiple chip selects are used, $\overline{CS}$ width negated (specification 15) applies to the time from the negation of a heavily loaded chip select to the assertion of a lightly loaded chip select. The $\overline{CS}$ width negated specification between multiple chip selects does not apply to chip selects being used for synchronous ECLK cycles.
7. Hold times are specified with respect to $\overline{DS}$ or $\overline{CS}$ on asynchronous reads and with respect to CLKOUT on fast cycle reads. The user is free to use either hold time.
8. Maximum value is equal to (t_{cyc} / 2) + 25 ns.
9. If the asynchronous setup time (specification 47A) requirements are satisfied, the $\overline{DSACK[1:0]}$ low to data setup time (specification 31) and $\overline{DSACK[1:0]}$ low to $\overline{BERR}$ low setup time (specification 48) can be ignored. The data must only satisfy the data-in to clock low setup time (specification 27) for the following clock cycle. $\overline{BERR}$ must satisfy only the late $\overline{BERR}$ low to clock low setup time (specification 27A) for the following clock cycle.
10. To ensure coherency during every operand transfer, $\overline{BG}$ is not asserted in response to $\overline{BR}$ until after all cycles of the current operand transfer are complete.
11. In the absence of $\overline{DSACK[1:0]}$, $\overline{BERR}$ is an asynchronous input using the asynchronous setup time (specification 47A).
12. After external $\overline{RESET}$ negation is detected, a short transition period (approximately 2 t_{cyc}) elapses, then the SIM drives $\overline{RESET}$ low for 512 tcyc.
13. External assertion of the $\overline{RESET}$ input can overlap internally-generated resets. To insure that an external reset is recognized in all cases, $\overline{RESET}$ must be asserted for at least 590 CLKOUT cycles.
14. External logic must pull $\overline{RESET}$ high during this period in order for normal MCU operation to begin.
15. Eight pipeline states are multiplexed into IPIPE[1:0]. The multiplexed signals have two phases.
16. Address access time = (2.5 + WS) t_{cyc} – t_{CHAV} – t_{DICL}

    Chip select access time = (2 + WS) t_{cyc} – t_{CLSA} – t_{DICL}

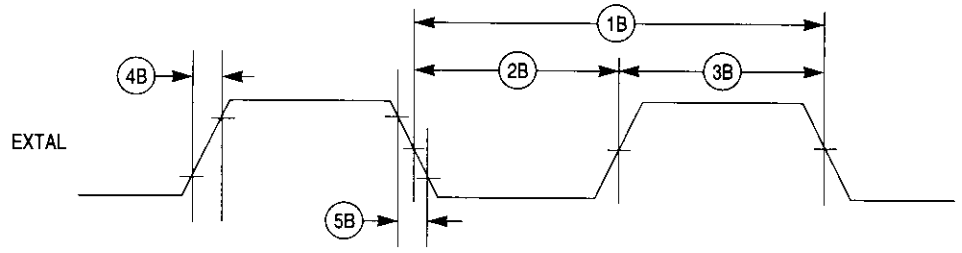
    Where: WS = number of wait states. When fast termination is used (2 clock bus) WS = –1.



NOTE: TIMING SHOWN WITH RESPECT TO 20% AND 70% V_{DD}

16 CLKOUT TIM

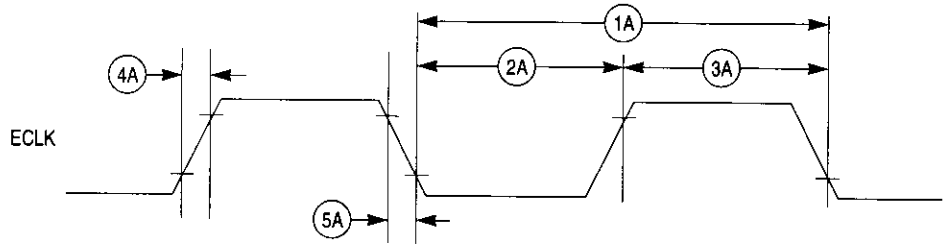
Figure A–1 CLKOUT Output Timing Diagram



NOTE: TIMING SHOWN WITH RESPECT TO 20% AND 70% V_{DD}
PULSE WIDTH SHOWN WITH RESPECT TO 50% V_{DD}

16 EXT CLK INPUT TIM

Figure A–2 External Clock Input Timing Diagram



NOTE: TIMING SHOWN WITH RESPECT TO 20% AND 70% V_{DD}

16 ECLK OUTPUT TIM

Figure A–3 ECLK Output Timing Diagram

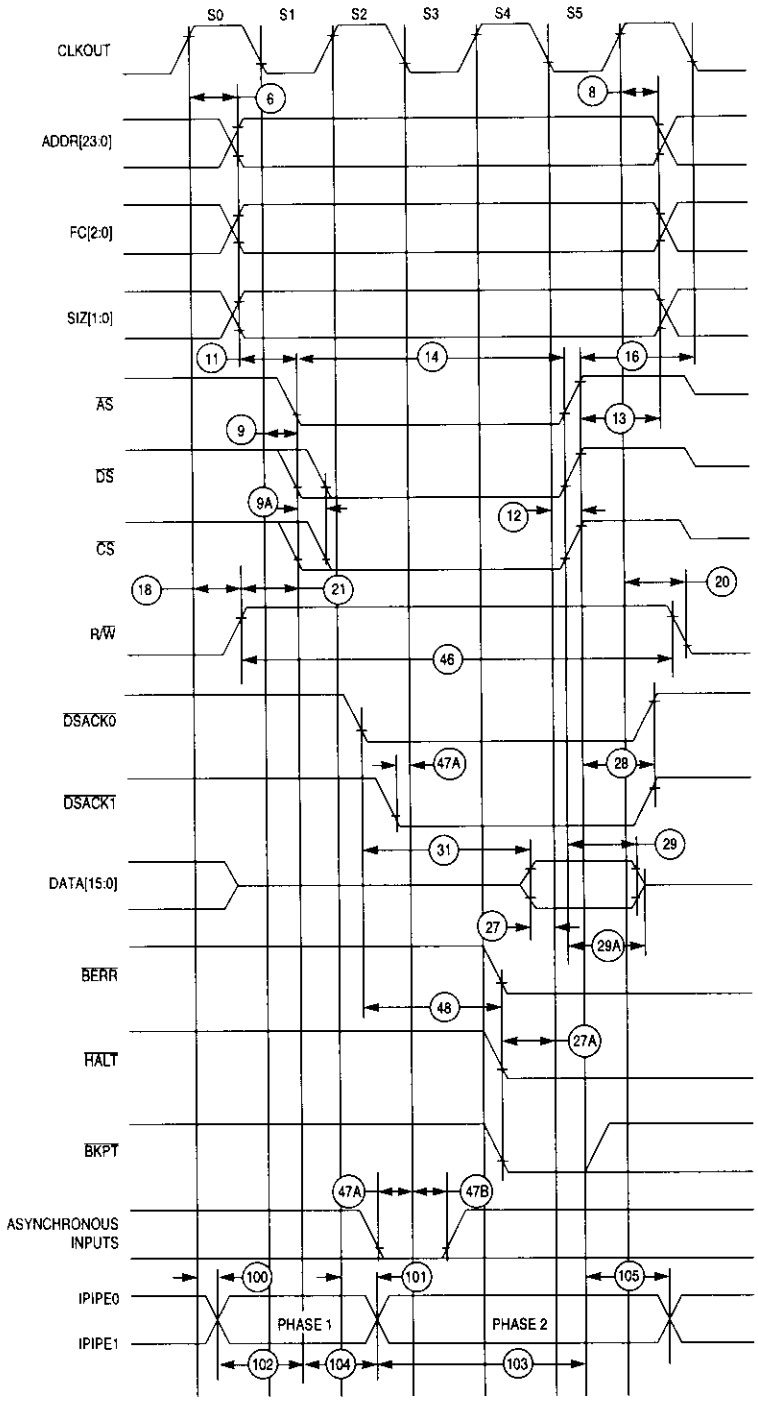
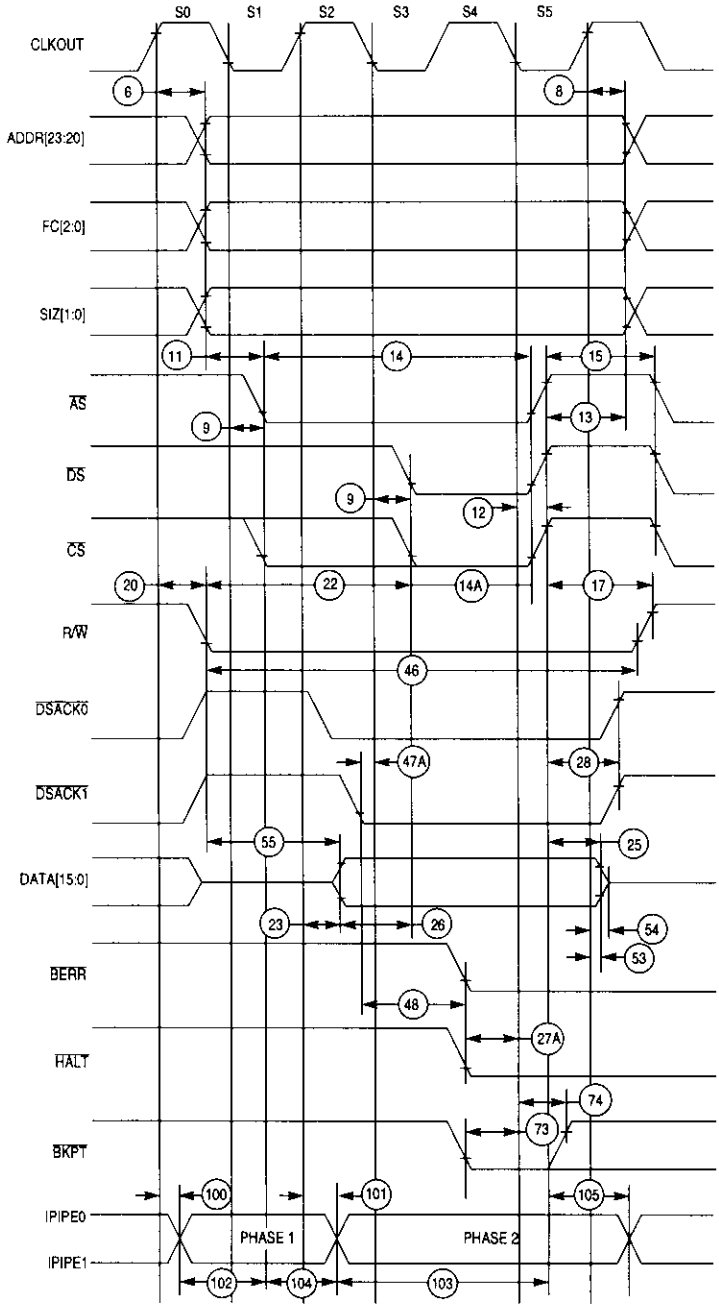


Figure A–4 Read Cycle Timing Diagram



16 WR CYC TIM

Figure A–5 Write Cycle Timing Diagram

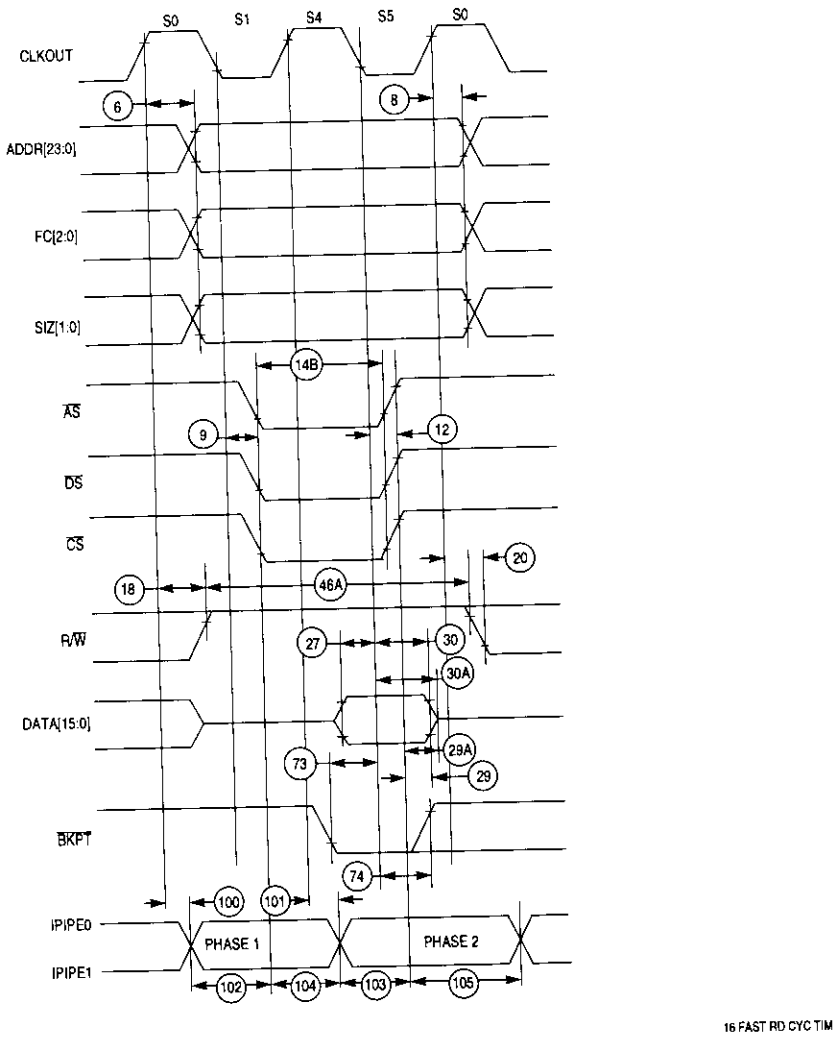


Figure A–6 Fast Termination Read Cycle Timing Diagram

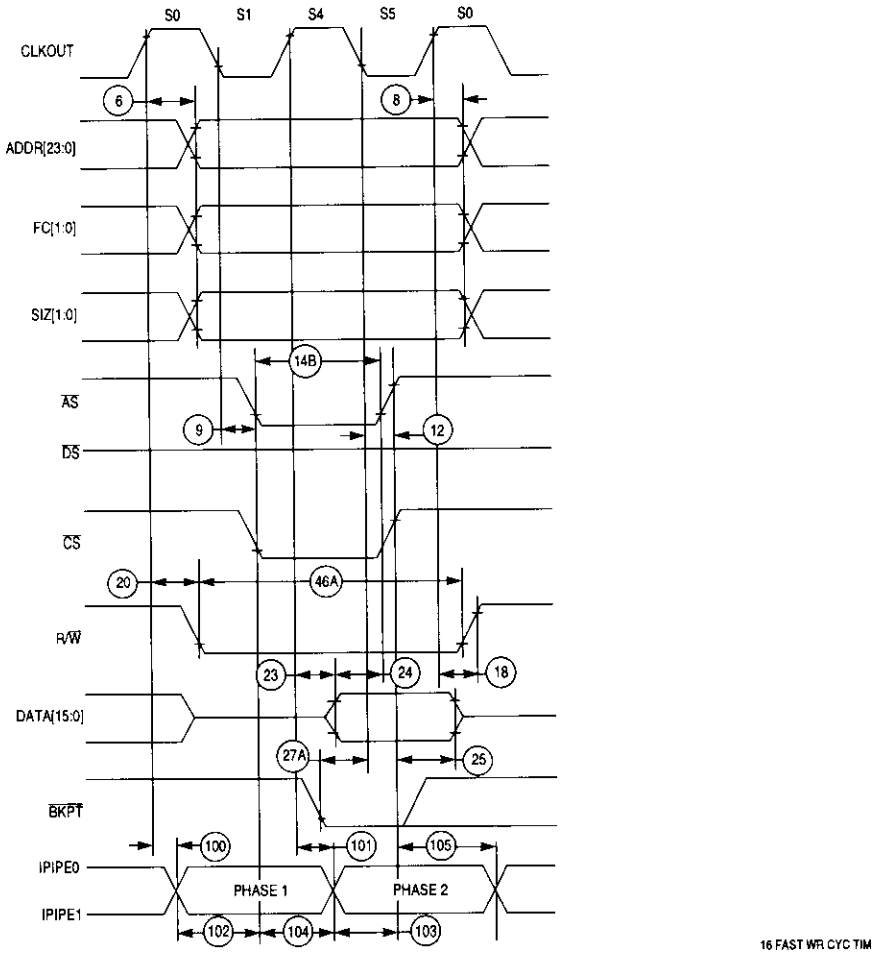


Figure A–7 Fast Termination Write Cycle Timing Diagram

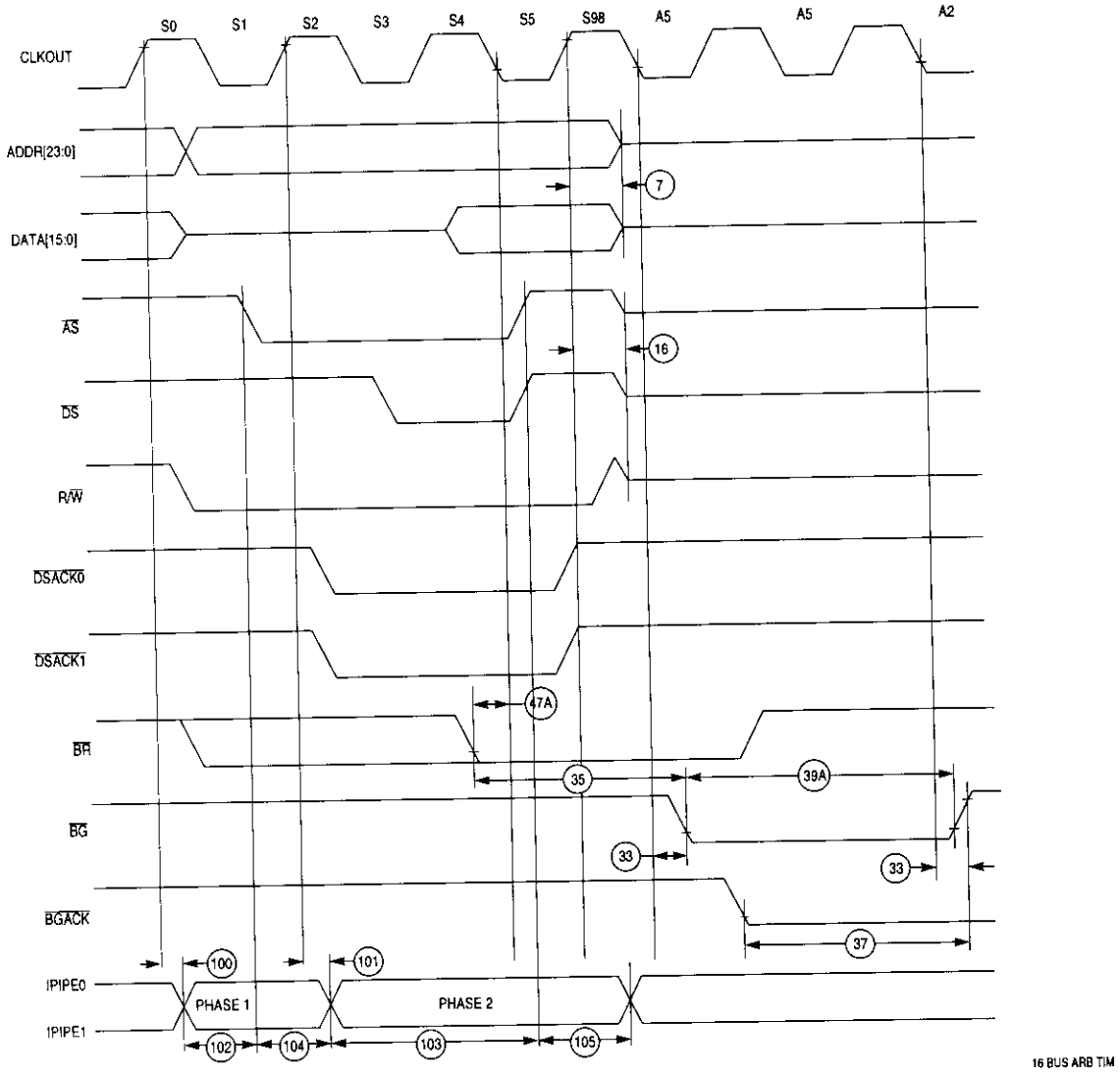
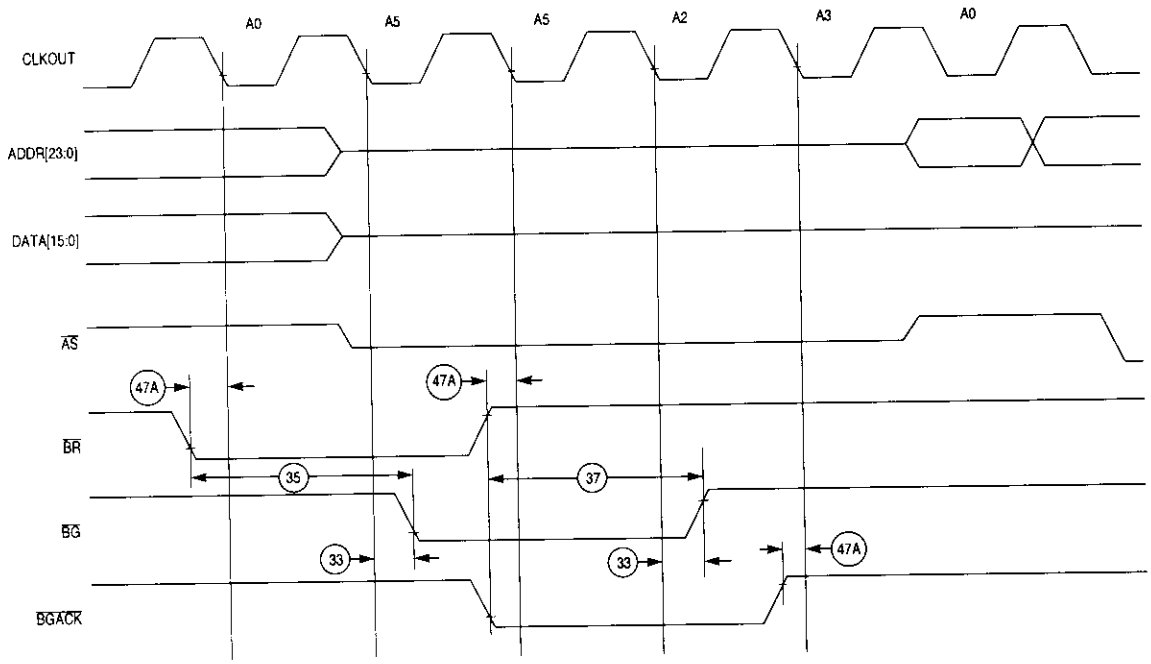
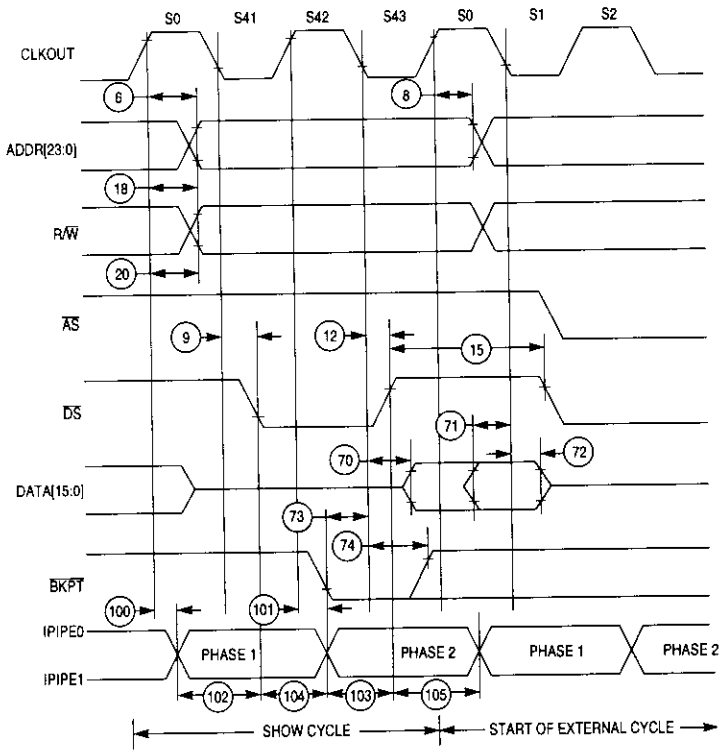


Figure A–8 Bus Arbitration Timing Diagram — Active Bus Case



16 BUS ARB TIM IDLE

Figure A–9 Bus Arbitration Timing Diagram — Idle Bus Case



NOTE:
Show cycles can stretch during clock phase S42 when bus accesses take longer than two cycles due to IMB module wait-state insertion.

16 SHW CYC TIM

Figure A–10 Show Cycle Timing Diagram

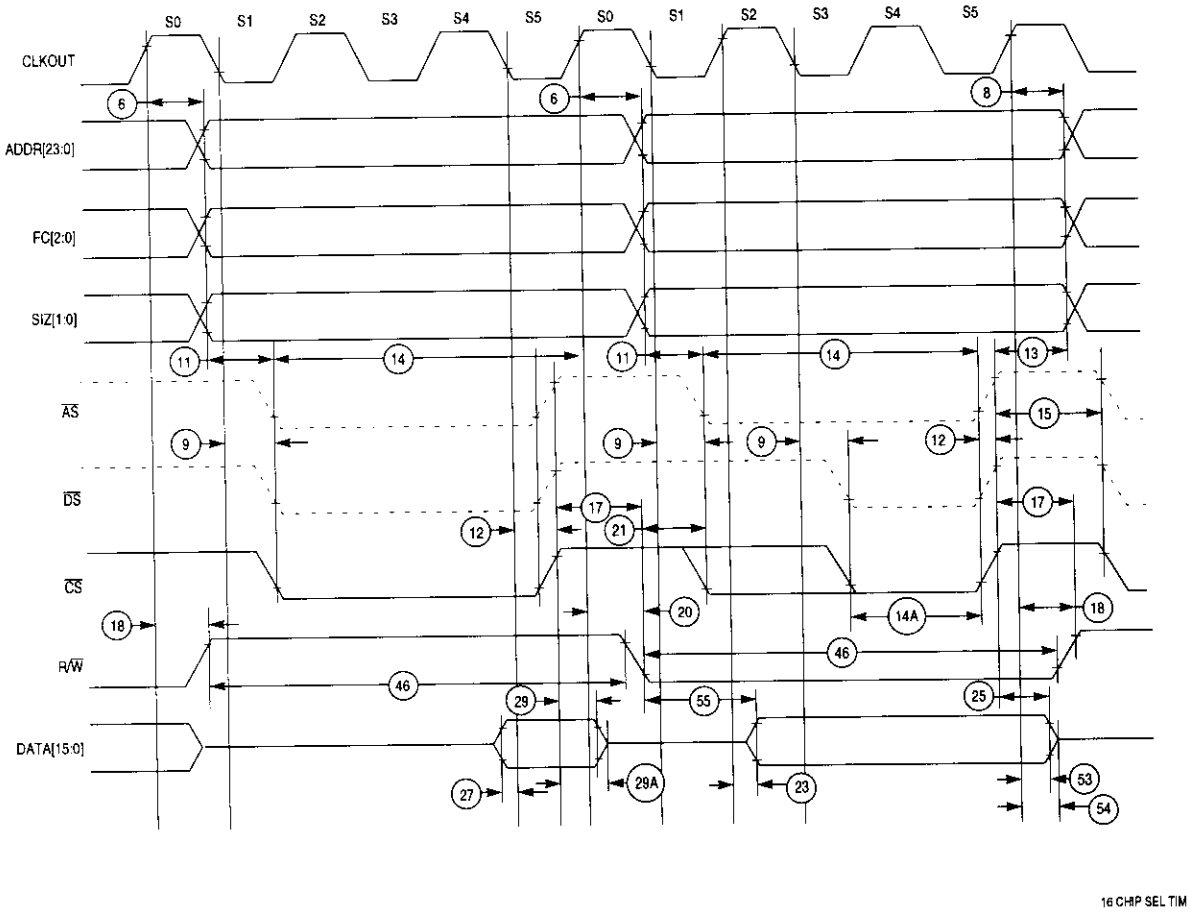


Figure A–11 Chip-Select Timing Diagram

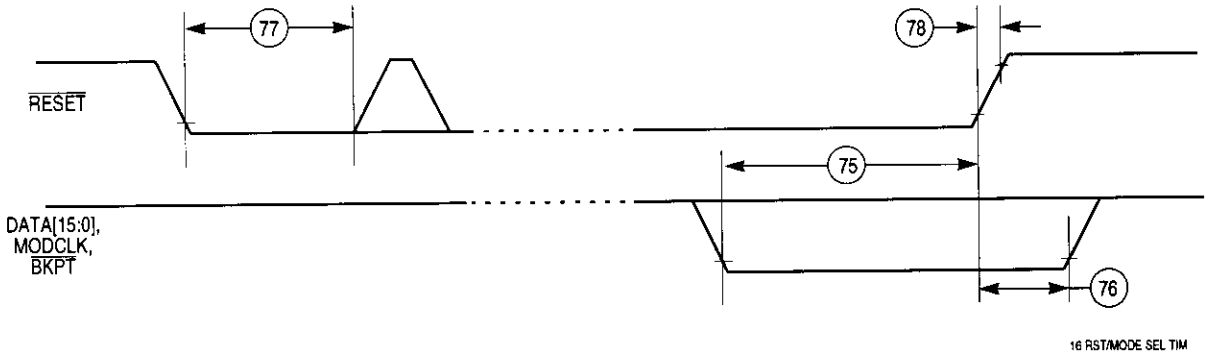


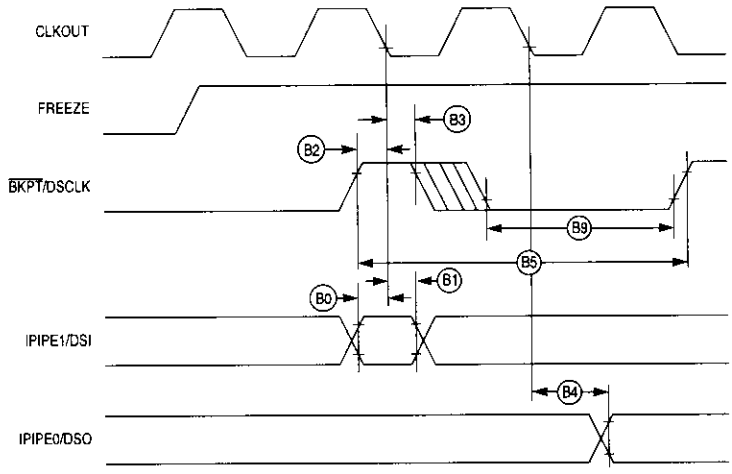
Figure A–12 Reset and Mode Select Timing Diagram

Table A–7 Background Debugging Mode Timing

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)[1]

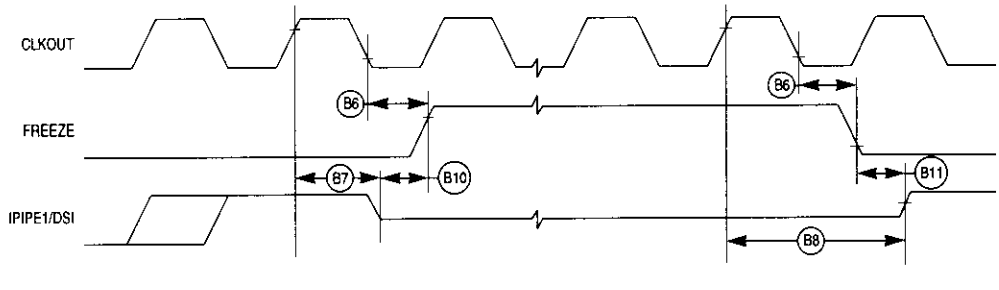
Num	Characteristic	Symbol	Min	Max	Unit
B0	DSI Input Setup Time	t_{DSISU}	10	—	ns
B1	DSI Input Hold Time	t_{DSIH}	5	—	ns
B2	DSCLK Setup Time	t_{DSCSU}	10	—	ns
B3	DSCLK Hold Time	t_{DSCH}	5	—	ns
B4	DSO Delay Time	t_{DSOD}	—	20	ns
B5	DSCLK Cycle Time	t_{DSCCYC}	2	—	t_{cyc}
B6	CLKOUT High to FREEZE Asserted/Negated	t_{FRZAN}	—	20	ns
B7	CLKOUT High to IPIPE1 High Impedance	t_{IPZ}	—	20	ns
B8	CLKOUT High to IPIPE1 Valid	t_{IP}	—	20	ns
B9	DSCLK Low Time	t_{DSCLO}	1	—	t_{cyc}
B10	IPIPE1 High Impedance to FREEZE Asserted	t_{IPFA}	TBD	—	t_{cyc}
B11	FREEZE Negated to IPIPE[0:1] Active	t_{FRIP}	TBD	—	t_{cyc}

NOTES:
1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.



16 BDM SER COM TIM

Figure A–13 BDM Serial Communication Timing Diagram



16 BDM FRZ TIM

Figure A–14 BDM Freeze Assertion Timing Diagram

Table A–8 ECLK Bus Timing

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)[1]

Num	Characteristic	Symbol	Min	Max	Unit
E1	ECLK Low to Address Valid[2]	t_{EAD}	—	40	ns
E2	ECLK Low to Address Hold	t_{EAH}	10	—	ns
E3	ECLK Low to $\overline{CS}$ Valid ($\overline{CS}$ Delay)	t_{ECSD}	—	100	ns
E4	ECLK Low to $\overline{CS}$ Hold	t_{ECSH}	10	—	ns
E5	$\overline{CS}$ Negated Width	t_{ECSN}	20	—	ns
E6	Read Data Setup Time	t_{EDSR}	25	—	ns
E7	Read Data Hold Time	t_{EDHR}	5	—	ns
E8	ECLK Low to Data High Impedance	t_{EDHZ}	—	40	ns
E9	$\overline{CS}$ Negated to Data Hold (Read)	t_{ECDH}	0	—	ns
E10	$\overline{CS}$ Negated to Data High Impedance	t_{ECDZ}	—	1	t_{cyc}
E11	ECLK Low to Data Valid (Write)	t_{EDDW}	—	2	t_{cyc}
E12	ECLK Low to Data Hold (Write)	t_{EDHW}	5	—	ns
E13	Address Access Time (Read)[3]	t_{EACC}	255	—	ns
E14	Chip-Select Access Time (Read)[4]	t_{EACS}	195	—	ns
E15	Address Setup Time	t_{EAS}	—	1/2	t_{cyc}

NOTES:
1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
2. When previous bus cycle is not an ECLK cycle, the address may be valid before ECLK goes low.
3. Address access time = $t_{Ecyc} - t_{EAD} - t_{EDSR}$.
4. Chip select access time = $t_{Ecyc} - t_{ECSD} - t_{EDSR}$.

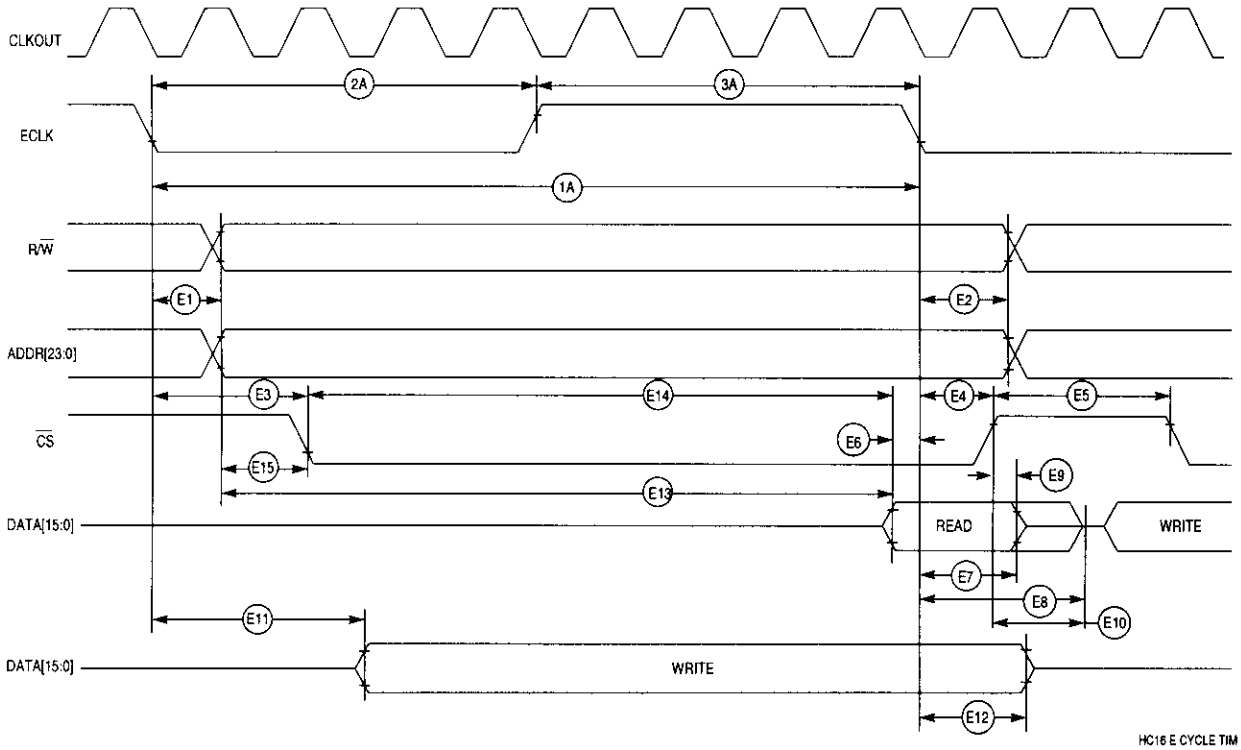


Figure A–15 ECLK Timing Diagram

Table A–9 QSPI Timing

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, 200 pF load on all QSPI pins)[1]

Num	Function	Symbol	Min	Max	Unit
1	Operating Frequency Master Slave	f_{op}	 DC DC	 1/4 1/4	 System Clock Frequency System Clock Frequency
2	Cycle Time Master Slave	t_{qcyc}	 4 4	 510 —	 t_{cyc} t_{cyc}
3	Enable Lead Time Master Slave	t_{lead}	 2 2	 128 —	 t_{cyc} t_{cyc}
4	Enable Lag Time Master Slave	t_{lag}	 — 2	 1/2 —	 SCK t_{cyc}
5	Clock (SCK) High or Low Time Master Slave[2]	t_{sw}	 2 t_{cyc} – 30 2 t_{cyc} – n	 255 t_{cyc} —	 ns ns
6	Sequential Transfer Delay Master Slave (Does Not Require Deselect)	t_{td}	 17 13	 8192 —	 t_{cyc} t_{cyc}
7	Data Setup Time (Inputs) Master Slave	t_{su}	 20 20	 — —	 ns ns
8	Data Hold Time (Inputs) Master Slave	t_{hi}	 0 20	 — —	 ns ns
9	Slave Access Time	t_a	—	1	t_{cyc}
10	Slave MISO Disable Time	t_{dis}	—	2	t_{cyc}
11	Data Valid (after SCK Edge) Master Slave	t_v	 — —	 50 50	 ns ns
12	Data Hold Time (Outputs) Master Slave	t_{ho}	 0 0	 — —	 ns ns
13	Rise Time Input Output	 t_{ri} t_{ro}	 — —	 2 30	 µs ns
14	Fall Time Input Output	 t_{fi} t_{fo}	 — —	 2 30	 µs ns

NOTES:
1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
2. For high time, n = External SCK rise time; for low time, n = External SCK fall time.

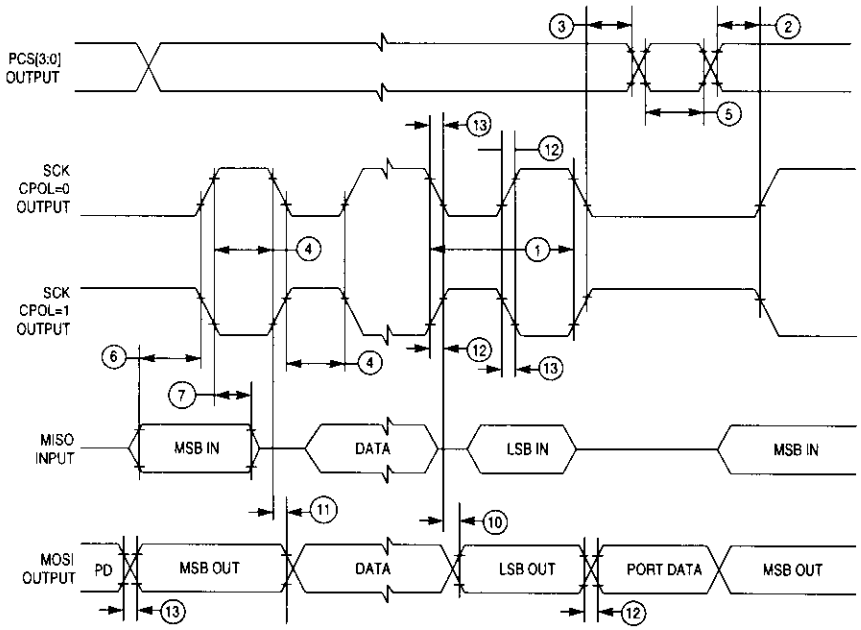


Figure A–16 QSPI Timing — Master, CPHA = 0

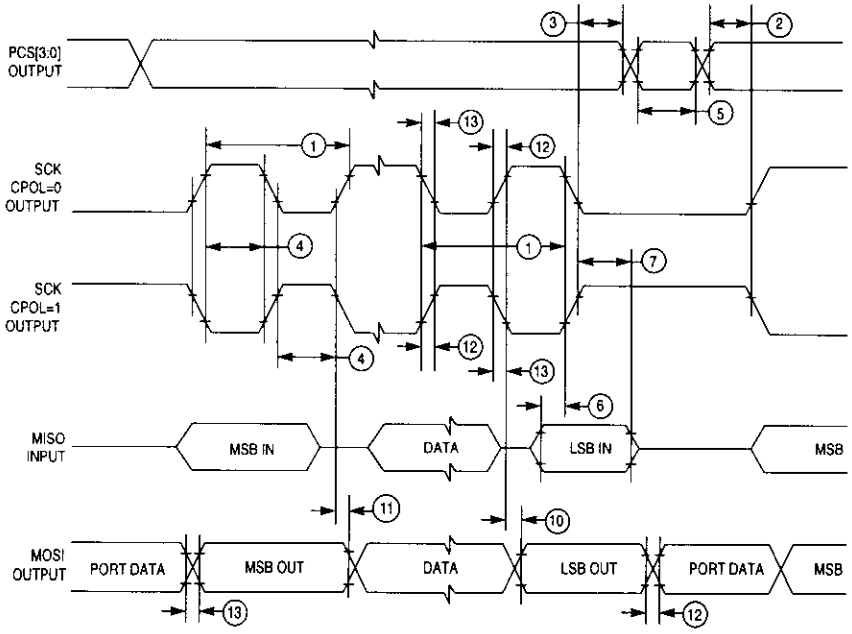
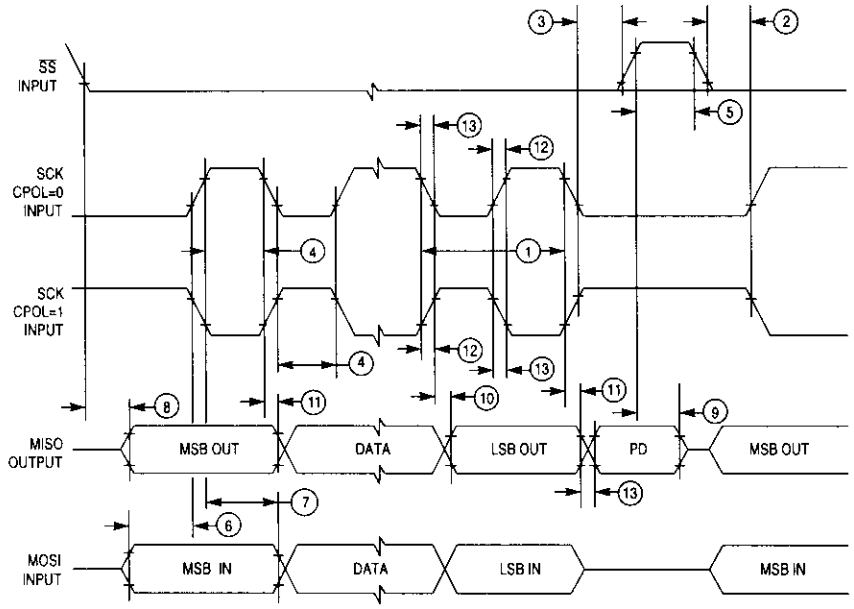
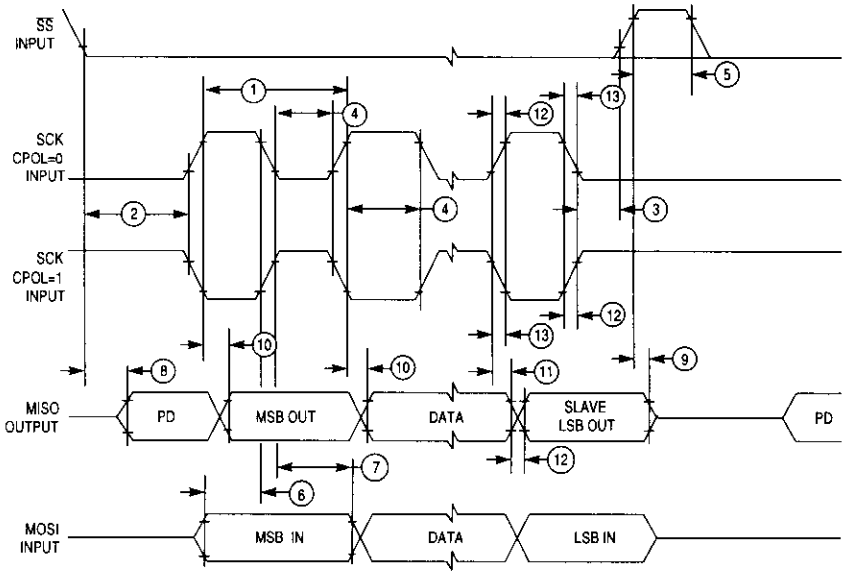


Figure A–17 QSPI Timing — Master, CPHA = 1



16 QSPI SLV CPHA0

Figure A–18 QSPI Timing — Slave, CPHA = 0



16 QSPI SLV CPHA1

Figure A–19 QSPI Timing — Slave, CPHA = 1

Table A–10 ADC Maximum Ratings

Num	Parameter	Symbol	Min	Max	Unit
1	Analog Supply	V_{DDA}	–0.3	6.5	V
2	Internal Digital Supply, with reference to V_{SSI}	V_{DDI}	–0.3	6.5	V
3	Reference Supply, with reference to V_{SSI}	V_{RH}, V_{RL}	–0.3	6.5	V
4	V_{SS} Differential Voltage	$V_{SSI} - V_{SSA}$	–0.1	0.1	V
5	V_{DD} Differential Voltage	$V_{DDI} - V_{DDA}$	–6.5	6.5	V
6	V_{REF} Differential Voltage	$V_{RH} - V_{RL}$	–6.5	6.5	V
7	V_{RH} to V_{DDA} Differential Voltage	$V_{RH} - V_{DDA}$	–6.5	6.5	V
8	V_{RL} to V_{SSA} Differential Voltage	$V_{RL} - V_{SSA}$	–6.5	6.5	V
9	Disruptive Input Current[1,2,3,4,5,6,7] $V_{NEGCLAMP} \cong -0.3$ V $V_{POSCLAMP} \cong 8$ V	I_{NA}	–500	500	µA
10	Positive Overvoltage Current Coupling Ratio[1,5,6,8]	K_P	2000	—	—
11	Negative Overvoltage Current Coupling Ratio[1,5,6,8]	K_N	500	—	—
12	Maximum Input Current [3,4,6] $V_{NEGCLAMP} \cong -0.3$ V $V_{POSCLAMP} \cong 8$ V	I_{MA}	–25	25	mA

NOTES:

1. Below disruptive current conditions, a stressed channel will store the maximum conversion value for analog inputs greater than V_{RH} and the minimum conversion value for inputs less than V_{RL}. This assumes that $V_{RH} \leq V_{DDA}$ and $V_{RL} \geq V_{SSA}$ due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions
2. Input signals with large slew rates or high frequency noise components cannot be converted accurately. These signals also interfere with conversion of other channels.
3. Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.
4. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using positive and negative clamp values, then use the larger of the calculated values.
5. This parameter is periodically sampled rather than 100% tested.
6. Applies to single pin only.
7. The values of external system components can change the maximum input current value, and affect operation. A voltage drop may occur across the external source impedances of the adjacent pins, impacting conversions on these adjacent pins. The actual maximum may need to be determined by testing the complete design.
8. Current coupling is the ratio of the current induced from overvoltage (positive or negative, through an external series coupling resistor), divided by the current induced on adjacent pins. A voltage drop may occur across the external source impedances of the adjacent pins, impacting conversions on these adjacent pins

Table A–11 ADC DC Electrical Characteristics (Operating)

(V_{SS} = 0 Vdc, ADCLK = 2.1 MHz, $T_A = T_L$ to T_H)

Num	Parameter	Symbol	Min	Max	Unit
1	Analog Supply[1]	V_{DDA}	4.5	5.5	V
2	Internal Digital Supply[1]	V_{DDI}	4.5	5.5	V
3	V_{SS} Differential Voltage	$V_{SSI} - V_{SSA}$	– 1.0	1.0	mV
4	V_{DD} Differential Voltage	$V_{DDI} - V_{DDA}$	– 1.0	1.0	V
5	Reference Voltage Low[2, 3]	V_{RL}	V_{SSA}	V_{DDA} / 2	V
6	Reference Voltage High[2, 3]	V_{RH}	V_{DDA} / 2	V_{DDA}	V
7	V_{REF} Differential Voltage[3]	$V_{RH} - V_{RL}$	4.5	5.5	V
8	Input Voltage[2]	V_{INDC}	V_{SSA}	V_{DDA}	V
9	Input High, Port ADA	V_{IH}	0.7 (V_{DDA})	V_{DDA} + 0.3	V
10	Input Low, Port ADA	V_{IL}	V_{SSA} – 0.3	0.2 (V_{DDA})	V
11	Analog Supply Current Normal Operation[4] Low-power stop	I_{DDA}	 — —	 1.0 200	 mA µA
12	Reference Supply Current	I_{REF}	—	250	µA
13	Input Current, Off Channel[5]	I_{OFF}	—	150	nA
14	Total Input Capacitance, Not Sampling	C_{INN}	—	10	pF
15	Total Input Capacitance, Sampling	C_{INS}	—	15	pF

NOTES:
1. Refers to operation over full temperature and frequency range.
2. To obtain full-scale, full-range results, $V_{SSA} \le V_{RL} \le V_{INDC} \le V_{RH} \le V_{DDA}$.
3. Accuracy tested and guaranteed at $V_{RH} - V_{RL}$ = 5.0 V ± 5%.
4. Current measured at maximum system clock frequency with ADC active.
5. Maximum leakage occurs at maximum operating temperature. Current decreases by approximately one-half for each 10°C decrease from maximum temperature.

Table A–12 ADC AC Characteristics (Operating)

(V_{DD} and V_{DDA} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, T_A within operating temperature range)

Num	Parameter	Symbol	Min	Max	Unit
1	ADC Clock Frequency	f_{adclk}	0.5	2.1	MHz
2	8-bit Conversion Time[1] F_{ADCLK} = 1.0 MHz F_{ADCLK} = 2.1 MHz	t_{conv}	 15.2 7.6	—	µs
3	10-bit Conversion Time[1] F_{ADCLK} = 1.0 MHz F_{ADCLK} = 2.1 MHz	t_{conv}	 17.1 8.6	—	µs
4	Stop Recovery Time	t_{sr}	—	10	µs

NOTES:
1. Conversion accuracy varies with f_{adclK} rate. Reduced conversion accuracy occurs at maximum.

Table A–13 ADC Conversion Characteristics (Operating)

(V_{DD} and V_{DDA} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H,
0.5 MHz ≤ f_{adclk} ≤ 1.0 MHz, 2 clock input sample time)

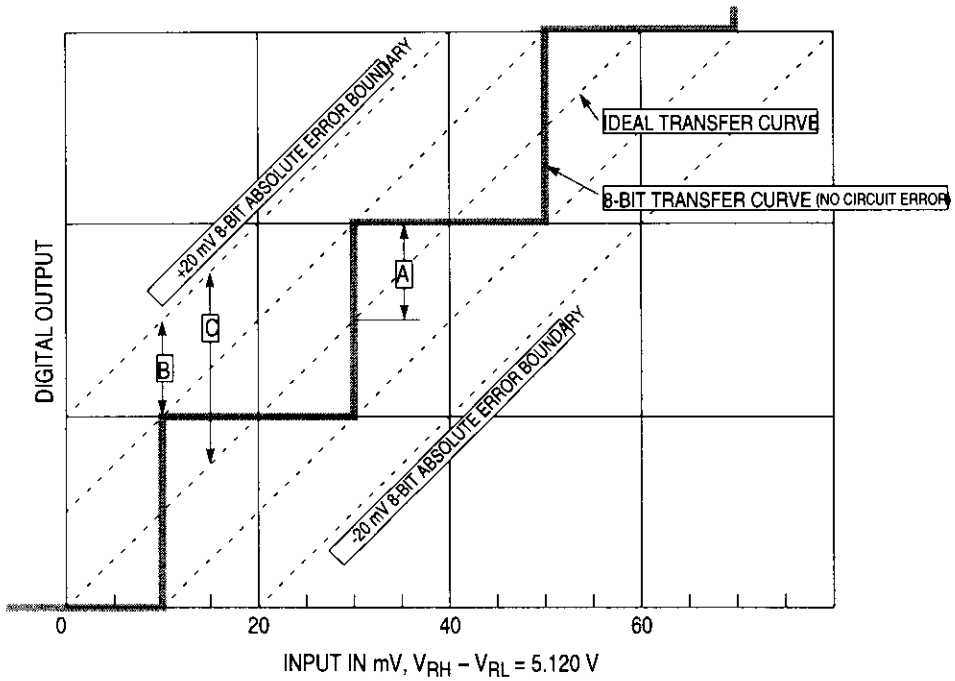
Num	Parameter	Symbol	Min	Typ	Max	Unit
1	8-bit Resolution[1]	1 Count	—	20	—	mV
2	8-bit Differential Nonlinearity	DNL	–0.5	—	0.5	Counts
3	8-bit Integral Nonlinearity	INL	–1	—	1	Counts
4	8-bit Absolute Error[2]	AE	–1	—	1	Counts
5	10-bit Resolution[1]	1 Count	—	5	—	mV
6	10-bit Differential Nonlinearity[3]	DNL	–0.5	—	0.5	Counts
7	10-bit Integral Nonlinearity[3]	INL	–2.0	—	2.0	Counts
8	10-bit Absolute Error[3, 4]	AE	–2.5	—	2.5	Counts
9	Source Impedance at Input[5]	R_S	—	20	—	kΩ

NOTES:

1. At $V_{RH} - V_{RL}$ = 5.12 V, one 10-bit count = 5 mV and one 8-bit count = 20 mV.
2. 8-bit absolute error of 1 count (20 mV) includes 1/2 count (10 mV) inherent quantization error and 1/2 count (10 mV) circuit (differential, integral, and offset) error.
3. Conversion accuracy varies with f_{adclk} rate. Reduced conversion accuracy occurs at maximum F_{ADCLK}. Assumes that minimum sample time (2 ADC Clocks) is selected.
4. 10-bit absolute error of 2.5 counts (12.5 mV) includes 1/2 count (2.5 mV) inherent quantization error and 2 counts (10 mV) circuit (differential, integral, and offset) error.
5. Maximum source impedance is application-dependent. Error resulting from pin leakage depends on junction leakage into the pin and on leakage due to charge-sharing with internal capacitance.
   Error from junction leakage is a function of external source impedance and input leakage current. In the following expression, expected error in result value due to junction leakage (V_{errj}) is expressed:

$$V_{errj} = R_S \times I_{OFF}$$

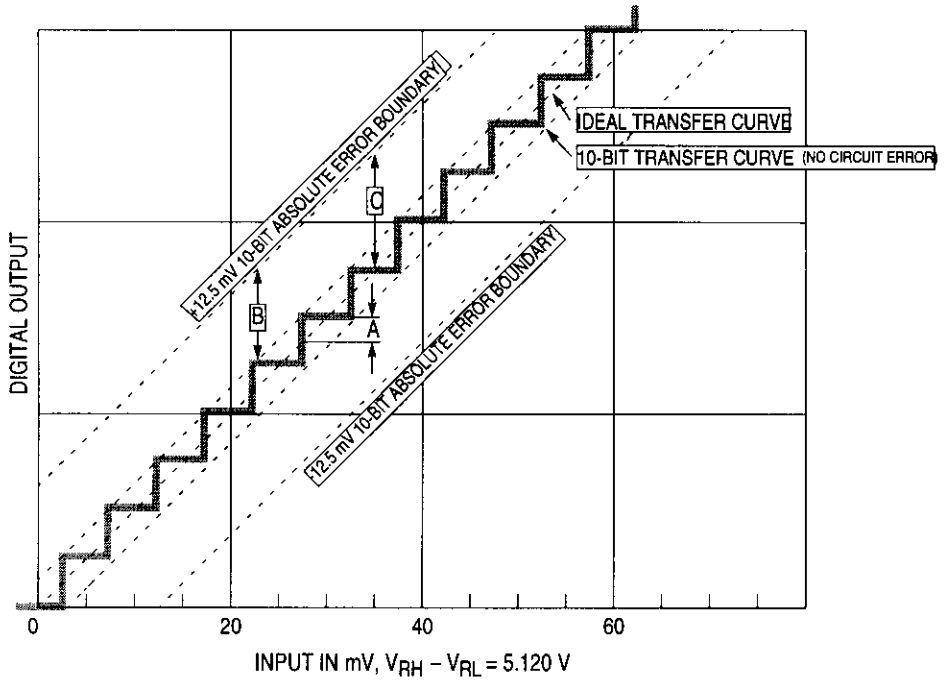
   where I_{OFF} is a function of operating temperature, as shown in table A-11.
   Charge-sharing leakage is a function of input source impedance, conversion rate, change in voltage between successive conversions, and the size of the decoupling capacitor used. Error levels are best determined empirically. In general, continuous conversion of the same channel may not be compatible with high source impedance.



A – +1/2 COUNT (10 mV) INHERENT QUANTIZATION ERROR
B – CIRCUIT-CONTRIBUTED +10 mV ERROR
C – + 20 mV ABSOLUTE ERROR (ONE 8-BIT COUNT)

ADC 8-BIT ACCURACY

Figure A–20 8-Bit ADC Conversion Accuracy



A – +.5 COUNT (2.5 mV) INHERENT QUANTIZATION ERROR
B – CIRCUIT-CONTRIBUTED +10 mV ERROR
C – +12.5 mV ABSOLUTE ERROR (2.5 10-BIT COUNTS)

ADC 10-BIT ACCURACY

Figure A–21 10-Bit ADC Conversion Accuracy

NOTES

How to reach us:
USA/EUROPE: Motorola Literature Distribution;
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MFAX: RMFAX0@email.sps.mot.com - TOUCHTONE (602) 244-6609
INTERNET: http://Design-NET.com
JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, Toshikatsu Otsuki,
6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-3521-8315
HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

Dual High Efficiency, Low Noise, Synchronous Step-Down Switching Regulators

FEATURES

- **Maintains Constant Frequency at Low Output Currents**
- Dual N-Channel MOSFET Synchronous Drive
- **Programmable Fixed Frequency (PLL Lockable)**
- **Wide V_{IN} Range: 3.5V to 36V Operation**
- Ultrahigh Efficiency
- Very Low Dropout Operation: 99% Duty Cycle
- Low Dropout, 0.5A Linear Regulator for VPP Generation or Low Noise Audio Supply
- Built-In Power-On Reset Timer
- Programmable Soft Start
- Low-Battery Detector
- Remote Output Voltage Sense
- Foldback Current Limiting (Optional)
- Pin Selectable Output Voltage
- Logic-Controlled Micropower Shutdown: $I_Q < 30\mu A$
- Output Voltages from 1.19V to 9V
- Available in 28- and 36-Lead SSOP Packages

APPLICATIONS

- Notebook and Palmtop Computers, PDAs
- Portable Instruments
- Battery-Operated Devices
- DC Power Distribution Systems

DESCRIPTION

The LTC®1438/LTC1439 are dual, synchronous step-down switching regulator controllers which drive external N-channel power MOSFETs in a phase-lockable fixed frequency architecture. The Adaptive Power™ output stage selectively drives two N-channel MOSFETs at frequencies up to 400kHz while reducing switching losses to maintain high efficiencies at low output currents.

An auxiliary 0.5A linear regulator using an external PNP pass device provides a low noise, low dropout voltage source. A secondary winding feedback control pin (SFB1) guarantees regulation regardless of load on the main output by forcing continuous operation.

An additional comparator is available for use as a low battery detector. A power-on reset timer (POR) is included which generates a signal delayed by $65536/f_{CLK}$ (typ 300ms) after the output is within 5% of the regulated output voltage. Internal resistive dividers provide pin selectable output voltages with remote sense capability on one of the two outputs.

The operating current levels are user-programmable via external current sense resistors. Wide input supply range allows operation from 3.5V to 30V (36V maximum).

TYPICAL APPLICATION

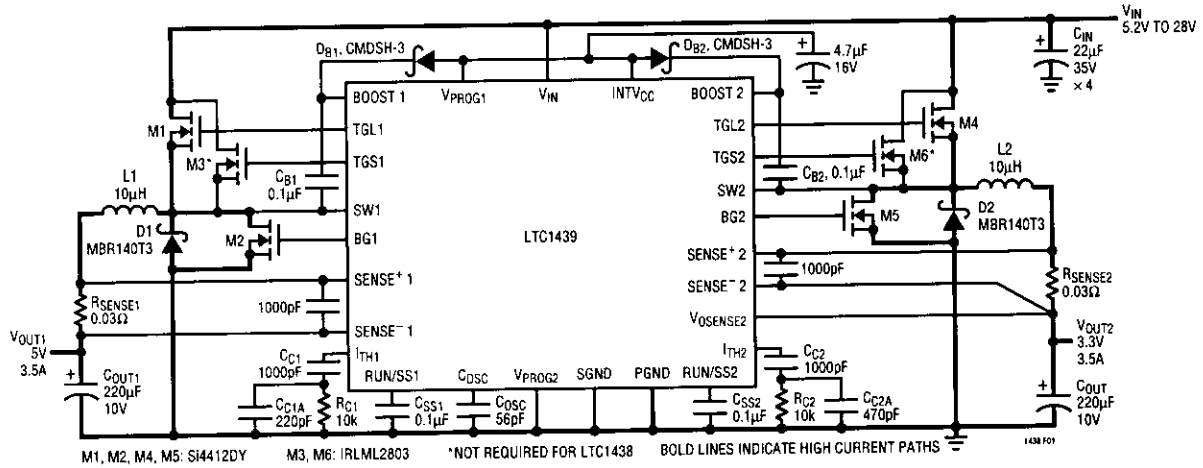
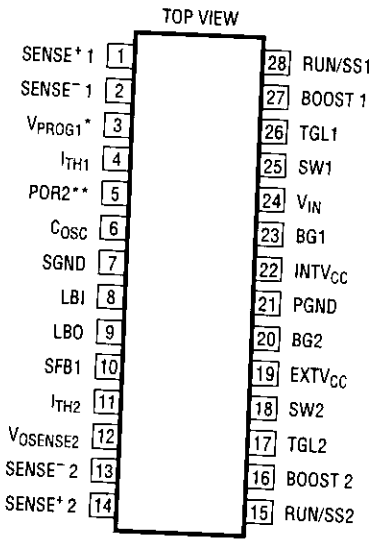


Figure 1. High Efficiency Dual 5V/3V Step-Down Converter

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (V_{IN}) ..... 36V to –0.3V
Topside Driver Voltage (BOOST 1, 2) ..... 42V to –0.3V
Switch Voltage (SW1, 2) ..... V_{IN} + 5V to –5V
$EXTV_{CC}$ Voltage ..... 10V to –0.3V
POR2, LBO Voltages ..... 12V to –0.3V
AUXFB Voltage ..... 20V to –0.3V
AUXDR Voltage ..... 28V to –0.3V
$SENSE^+$ 1, $SENSE^+$ 2, $SENSE^-$ 1, $SENSE^-$ 2,
$V_{OSENSE2}$ Voltages ..... $INTV_{CC}$ + 0.3V to –0.3V
V_{PROG1}, V_{PROG2} Voltages ..... $INTV_{CC}$ to –0.3V
PLL LPF, I_{TH1}, I_{TH2} Voltages ..... 2.7V to –0.3V
AUXON, PLLIN, SFB1,
RUN/SS1, RUN/SS2, LBI Voltages ..... 10V to –0.3V
Peak Output Current < 10µs (TGL1, 2, BG1, 2) 2A
Peak Output Current < 10µs (TGS1, 2) 250mA
$INTV_{CC}$ Output Current 50mA
Operating Ambient Temperature Range
Commercial ..... 0°C to 70°C
Industrial ..... –40°C to 85°C
Junction Temperature (Note 1) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



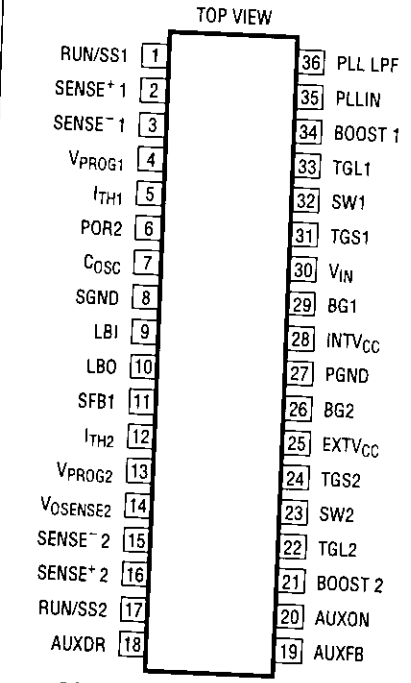
G PACKAGE
28-LEAD PLASTIC SSOP

*$V_{OSENSE1}$ ON LTC1438-ADJ
**NC ON THE LTC1438XCG

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER

LTC1438CG
LTC1438CG-ADJ
LTC1438IG
LTC1438IG-ADJ
LTC1438XCG



G PACKAGE
36-LEAD PLASTIC SSOP

GW PACKAGE
36-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W (G)
T_{JMAX} = 125°C, θ_{JA} = 85°C/W (GW)

ORDER PART NUMBER

LTC1439CG
LTC1439IG
LTC1439CGW
LTC1439IGW

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 15V, $V_{RUN/SS1,2}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loops							
I_{IN} $V_{OSENSE1,2}$	Feedback Current	V_{PROG1}, V_{PROG2} Pins Open (Note 2)			10	50	nA
$V_{OUT1,2}$	Regulated Output Voltage	(Note 2)					
	1.19V (Adjustable) Selected	V_{PROG1}, V_{PROG2} Pins Open	●	1.178	1.19	1.202	V
	3.3V Selected	V_{PROG1}, V_{PROG2} = 0V	●	3.220	3.30	3.380	V
	5V Selected	V_{PROG1}, V_{PROG2} = INT V_{CC}	●	4.900	5.00	5.100	V
$V_{LINEREG1,2}$	Reference Voltage Line Regulation	V_{IN} = 3.6V to 20V (Note 2), $V_{PROG1,2}$ Pins Open			0.002	0.01	%/V
$V_{LOADREG1,2}$	Output Voltage Load Regulation	$I_{TH1,2}$ Sinking 5µA (Note 2)	●		0.5	0.8	%
		$I_{TH1,2}$ Sourcing 5µA	●		−0.5	−0.8	%
V_{SFB1}	Secondary Feedback Threshold	V_{SFB1} Ramping Negative	●	1.16	1.19	1.22	V
I_{SFB1}	Secondary Feedback Current	V_{SFB1} = 1.5V			−1	−2	µA
V_{OVL}	Output Overvoltage Lockout	$V_{PROG1,2}$, SENSE⁻1 and $V_{OSENSE1,2}$ Pins Open		1.24	1.28	1.32	V
$I_{PROG1,2}$	$V_{PROG1,2}$ Input Current	0.5V > $V_{PROG1,2}$			−3	−6	µA
		INTV_{CC} − 0.5V < $V_{PROG1,2}$ < INTV_{CC}			3	6	µA
I_Q	Input DC Supply Current	EXTV_{CC} = 5V (Note 3)					
	Normal Mode	3.6V < V_{IN} < 30V, V_{AUXON} = 0V			320		µA
	Shutdown	$V_{RUN/SS1,2}$ = 0V, 3.6V < V_{IN} < 15V			16	30	µA
$V_{RUN/SS1,2}$	Run Pin Threshold		●	0.8	1.3	2	V
$I_{RUN/SS1,2}$	Soft Start Current Source	$V_{RUN/SS1,2}$ = 0V		1.5	3	4.5	µA
$\Delta V_{SENSE(MAX)}$	Maximum Current Sense Threshold	$V_{OSENSE1,2}$ = 0V, 5V $V_{PROG1,2}$ = Pins Open		130	150	180	mV
TGL1, 2 t_r, t_f	TGL1, TGL2 Transition Time						
	Rise Time	C_{LOAD} = 3000pF			50	150	ns
	Fall Time	C_{LOAD} = 3000pF			50	150	ns
TGS1, 2 t_r, t_f	TGS1, TGS2 Transition Time						
	Rise Time	C_{LOAD} = 500pF			100	150	ns
	Fall Time	C_{LOAD} = 500pF			50	150	ns
BG1, 2 t_r, t_f	BG1, BG2 Transition Time						
	Rise Time	C_{LOAD} = 3000pF			50	150	ns
	Fall Time	C_{LOAD} = 3000pF			50	150	ns
Internal V_{CC} Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{IN} < 30V, V_{EXTVCC} = 4V	●	4.8	5.0	5.2	V
$V_{LDO\ INT}$	INTV_{CC} Load Regulation	I_{INTVCC} = 20mA, V_{EXTVCC} = 4V			−0.2	−1	%
$V_{LDO\ EXT}$	EXTV_{CC} Voltage Drop	I_{INTVCC} = 20mA, V_{EXTVCC} = 5V			170	300	mV
V_{EXTVCC}	EXTV_{CC} Switchover Voltage	I_{INTVCC} = 20mA, EXTV_{CC} Ramping Positive	●	4.5	4.7		V
Oscillator and Phase-Locked Loop							
f_{OSC}	Oscillator Frequency	C_{OSC} = 100pF, LTC1439: PLL LPF = 0V (Note 4)		112	125	138	kHz
	VCO High	LTC1439, V_{PLLLPF} = 2.4V		200	240		kHz
R_{PLLIN}	PLLIN Input Resistance				50		kΩ
I_{PLLLPF}	Phase Detector Output Current	LTC1439					
	Sinking Capability	f_{PLLIN} < f_{OSC}		10	15	20	µA
	Sourcing Capability	f_{PLLIN} > f_{OSC}		10	15	20	µA
Power-On Reset							
$V_{SATPOR2}$	POR2 Saturation Voltage	I_{POR2} = 1.6mA, $V_{OSENSE2}$ = 1V, V_{PROG2} Pin Open			0.6	1	V
I_{LPOR2}	POR2 Leakage	V_{POR2} = 12V, $V_{OSENSE2}$ = 1.2V, V_{PROG2} Pin Open			0.2	1	µA
V_{THPOR2}	POR2 Trip Voltage	V_{PROG2} Pin Open % of V_{REF}					
		$V_{OSENSE2}$ Ramping Negative		−11	−7.5	−4	%
t_{DPOR2}	POR2 Delay	V_{PROG2} Pin Open			65536		Cycles

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 15V, $V_{RUN/SS1,2}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Low-Battery Comparator							
V_{SATLBO}	LBO Saturation Voltage	I_{LBO} = 1.6mA, V_{LBI} = 1.1V			0.6	1	V
I_{LLBO}	LBO Leakage	V_{LBO} = 12V, V_{LBI} = 1.4V	●		0.01	1	µA
V_{THLB1}	LBI Trip Voltage	High to Low Transition on LBO	●	1.16	1.19	1.22	V
I_{INLB1}	LBI Input Current	V_{LBI} = 1.19V	●		1	50	nA
V_{HYSLBO}	LBO Hysteresis				20		mV
Auxiliary Regulator/Comparator							
I_{AUXDR}	AUXDR Current	V_{EXTVCC} = 0V		10	15		mA
	Max Current Sinking Capability	V_{AUXDR} = 4V, V_{AUXFB} = 1.0V, V_{AUXON} = 5V			1	5	µA
	Control Current	V_{AUXDR} = 5V, V_{AUXFB} = 1.5V, V_{AUXON} = 5V			0.01	1	µA
	Leakage when OFF	V_{AUXDR} = 24V, V_{AUXFB} = 1.5V, V_{AUXON} = 0V			0.01	1	µA
$I_{INAUXFB}$	AUXFB Input Current	V_{AUXFB} = 1.19V, V_{AUXON} = 5V			0.01	1	µA
$I_{INAUXON}$	AUXON Input Current	V_{AUXON} = 5V		1.0	1.19	1.4	V
$V_{THAUXON}$	AUXON Trip Voltage	V_{AUXDR} = 4V, V_{AUXFB} = 1V			0.4	0.8	V
$V_{SATAUXDR}$	AUXDR Saturation Voltage	I_{AUXDR} = 1.6mA, V_{AUXFB} = 1V, V_{AUXON} = 5V		11.5	12.0	12.5	V
V_{AUXFB}	AUXFB Voltage	V_{AUXON} = 5V, 11V < V_{AUXDR} < 24V (Note 5)	●	1.14	1.19	1.24	V
		V_{AUXON} = 5V, 3V < V_{AUXDR} < 7V	●	7.5	8.5	9.5	V
$V_{THAUXDR}$	AUXFB Divider Disconnect Voltage	V_{AUXON} = 5V (Note 5); Ramping Negative					

The ● denotes specifications which apply over the full operating temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LTC1438CG, LTC1439CG: $T_J = T_A + (P_D)(95°C/W)$

LTC1439CGW: $T_J = T_A + (P_D)(85°C/W)$

Note 2: The LTC1438 and LTC1439 are tested in a feedback loop which servos $V_{OSENSE1,2}$ to the balance point for the error amplifier ($V_{ITH1,2}$ = 1.19V).

Note 3: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

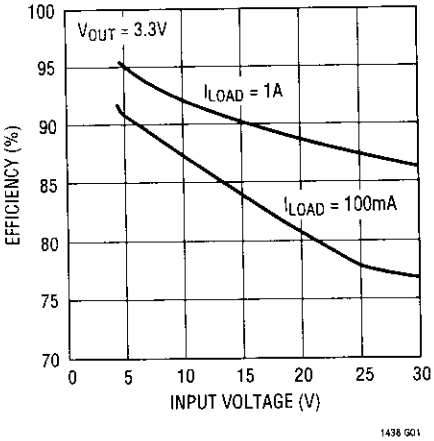
Note 4: Oscillator frequency is tested by measuring the C_{OSC} charge and discharge current (I_{OSC}) and applying the formula:

$$f_{OSC}\,(kHz) = 8.4(10^8)[C_{OSC}\,(pF) + 11]^{-1}\,(1/I_{CHG} + 1/I_{DISC})^{-1}$$

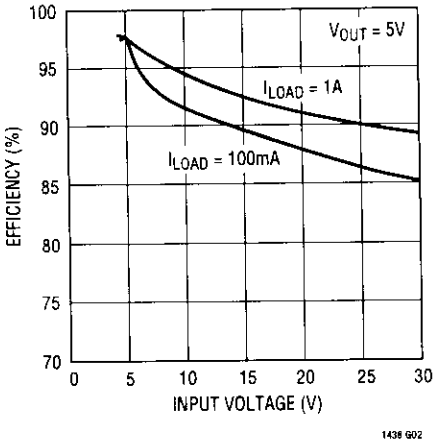
Note 5: The auxiliary regulator is tested in a feedback loop which servos V_{AUXFB} to the balance point for the error amplifier. For applications with V_{AUXDR} > 9.5V, V_{AUXFB} uses an internal resistive divider. See Applications Information section.

TYPICAL PERFORMANCE CHARACTERISTICS

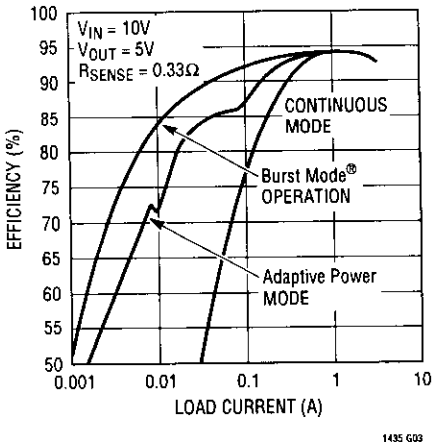
Efficiency vs Input Voltage
V_{OUT} = 3.3V



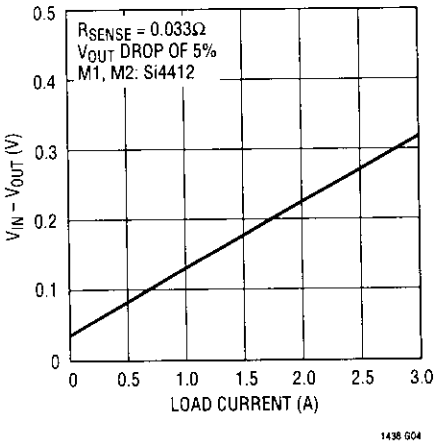
Efficiency vs Input Voltage
V_{OUT} = 5V



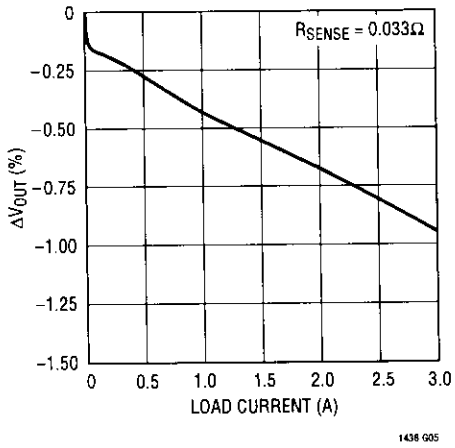
Efficiency vs Load Current



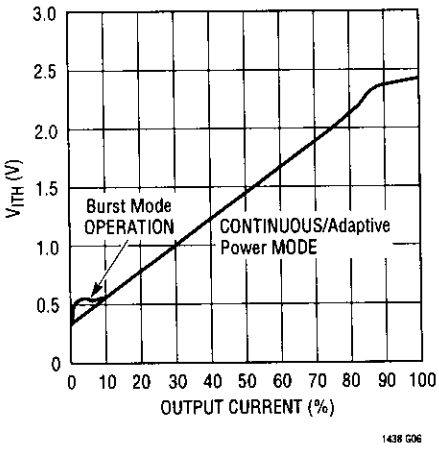
V_{IN} – V_{OUT} Dropout Voltage vs Load Current



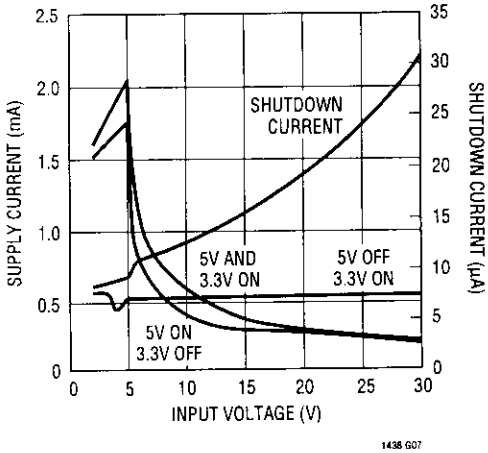
Load Regulation



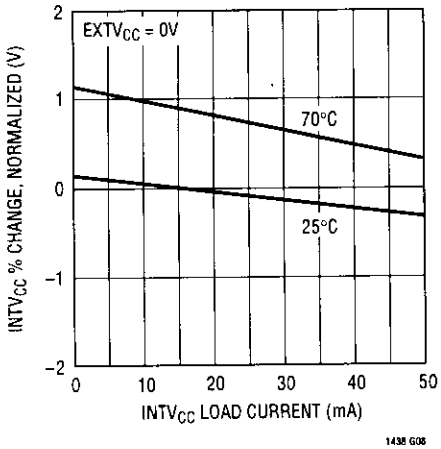
V_{ITH} Pin Voltage vs Output Current



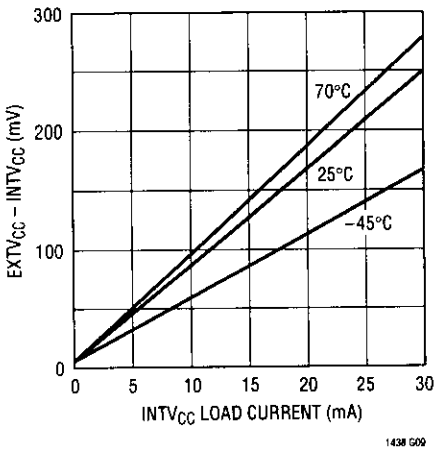
Input Supply Current vs Input Voltage



$INTV_{CC}$ Regulation vs $INTV_{CC}$ Load Current



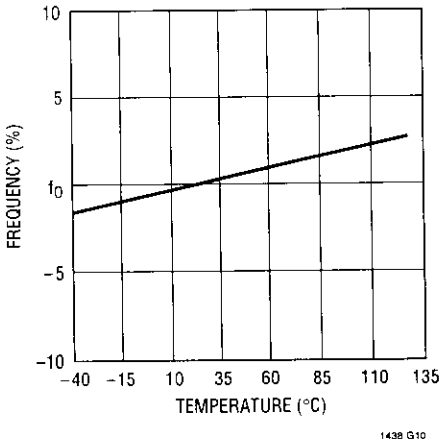
$EXTV_{CC}$ Switch Drop vs $INTV_{CC}$ Load Current



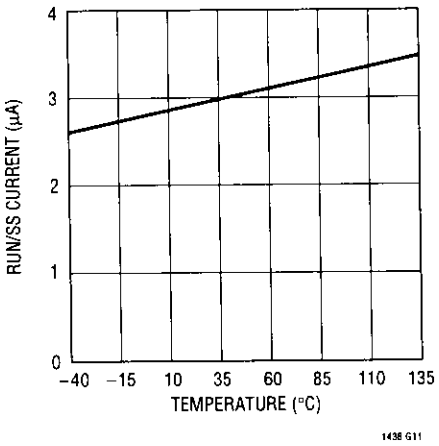
Burst Mode is a trademark of Linear Technology Corporation.

TYPICAL PERFORMANCE CHARACTERISTICS

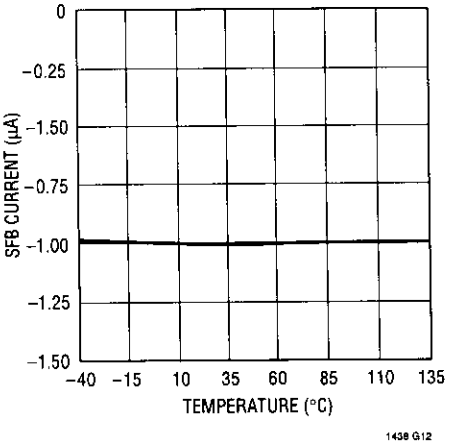
Normalized Oscillator Frequency vs Temperature



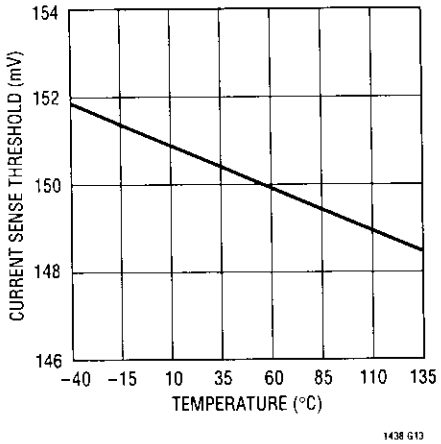
RUN/SS Pin Current vs Temperature



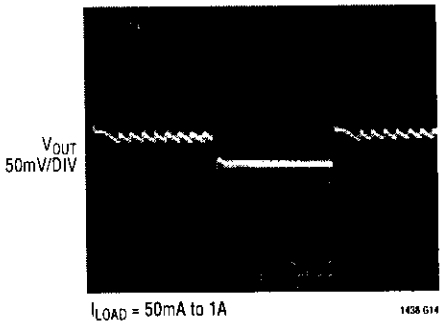
SFB1 Pin Current vs Temperature



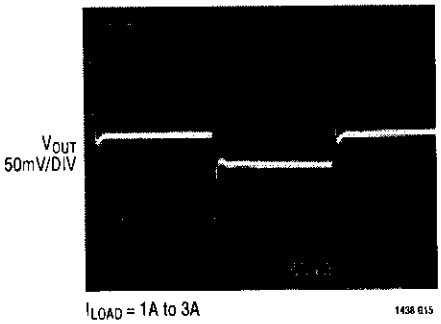
Maximum Current Sense Threshold Voltage vs Temperature



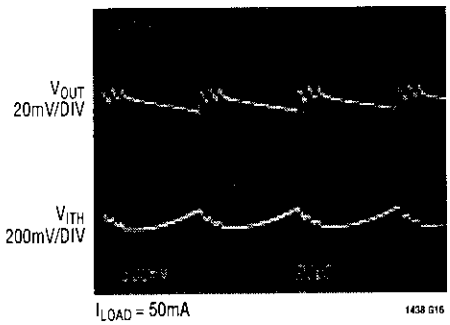
Transient Response



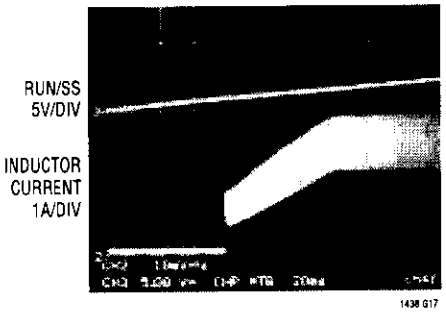
Transient Response



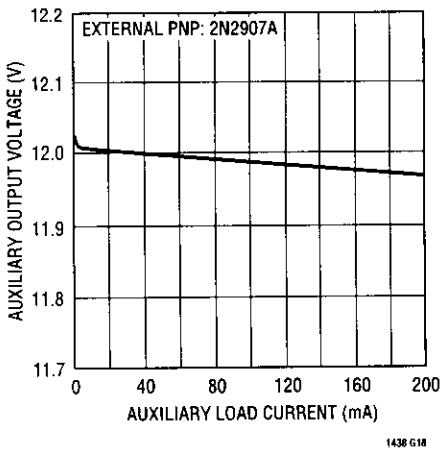
Burst Mode Operation



Soft Start: Load Current vs Time

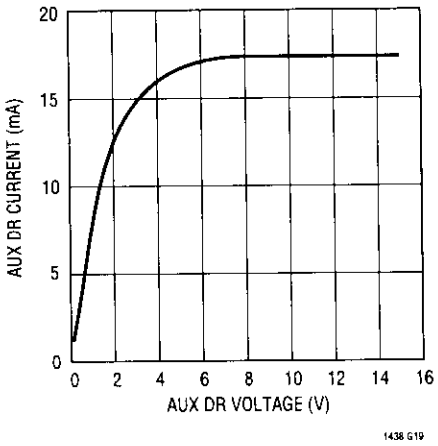


Auxiliary Regulator Load Regulation

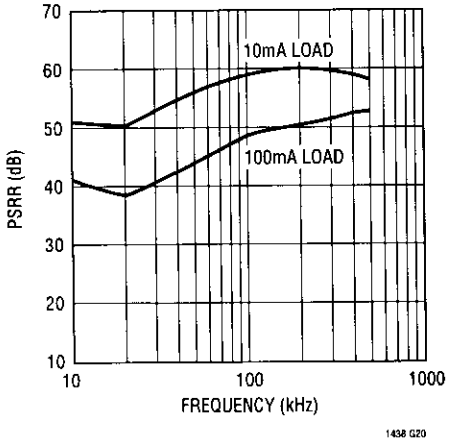


TYPICAL PERFORMANCE CHARACTERISTICS

Auxiliary Regulator Sink Current Available



Auxiliary Regulator PSRR



PIN FUNCTIONS

V_{IN}: Main Supply Pin. Must be closely decoupled to the IC's signal ground pin.

$INTV_{CC}$: Output of the Internal 5V Regulator and the $EXTV_{CC}$ Switch. The driver and control circuits are powered from this voltage. Must be closely decoupled to power ground with a minimum of 2.2µF tantalum or electrolytic capacitor. The $INTV_{CC}$ regulator turns off when both RUN/SS1 and RUN/SS2 are low. Refer to the LTC1538/LTC1539 for 5V keep-alive applications.

$EXTV_{CC}$: External Power Input to an Internal Switch. This switch closes and supplies $INTV_{CC}$, bypassing the internal low dropout regulator whenever $EXTV_{CC}$ is higher than 4.7V. Connect this pin to V_{OUT} of the controller with the higher output voltage. Do not exceed 10V on this pin. See $EXTV_{CC}$ connection in Applications Information section.

BOOST 1, BOOST 2: Supplies to the Topside Floating Drivers. The bootstrap capacitors are returned to these pins. Voltage swing at these pins is from $INTV_{CC}$ to $V_{IN} + INTV_{CC}$.

SW1, SW2: Switch Node Connections to Inductors. Voltage swing at these pins is from a Schottky diode (external) voltage drop below ground to V_{IN}.

SGND: Small-Signal Ground. Common to both controllers, must be routed separately from high current grounds to the (–) terminals of the C_{OUT} capacitors.

PGND: Driver Power Ground. Connects to sources of bottom N-channel MOSFETs and the (–) terminals of C_{IN}.

$SENSE^-$ 1, $SENSE^-$ 2: Connects to the (–) input for the current comparators. Except for the LTC1438-ADJ, $SENSE^-$ 1 is internally connected to the first controller's V_{OUT} sensing point. The first controller can only be used as a 3.3V or 5.0V regulator controlled by the V_{PROG1} pin with the LTC1438, LTC1438X and LTC1439. The LTC1438-ADJ Controller 1 implements a remote sensing adjustable regulator. The second controller can be set to a 3.3V, 5.0V or an adjustable regulator controlled by the V_{PROG2} pin (see Table 1).

Table 1. Output Voltage Table

	LTC1438-ADJ	LTC1438/LTC1438X	LTC1439
Controller 1	Adjustable Only	5V or 3.3V Only	
	Secondary Feedback Loop		
Controller 2	Adjustable Only Remote Sensing POR2 Output	Adjustable Only Remote Sensing POR2 Output	5V/3.3V/Adjustable Remote Sensing POR2 Output

PIN FUNCTIONS

SENSE⁺ 1, SENSE⁺ 2: The (+) Input to Each Current Comparator. Built-in offsets between SENSE⁻ 1 and SENSE⁺ 1 pins in conjunction with R_{SENSE1} set the current trip threshold (same for second controller).

$V_{OSENSE1,2}$: Receives the remotely sensed feedback voltage either from the output directly or from an external resistive divider across the output. The V_{PROG2} pin determines which point $V_{OSENSE2}$ must connect to. The $V_{OSENSE1}$ pin, only available on the LTC1438-ADJ, requires an external resistive divider to set the output voltage.

V_{PROG1}, V_{PROG2}: Programs Internal Voltage Attenuators for Output Voltage Sensing. The voltage sensing for thefirst controller is internally connected to SENSE⁻ 1 while the $V_{OSENSE2}$ pin allows for remote sensing for the second controller. For V_{PROG1}, $V_{PROG2} < V_{INTVCC}/3$, the divider is set for an output voltage of 3.3V. With V_{PROG1}, $V_{PROG2} > V_{INTVCC}/1.5$ the divider is set for an output voltage of 5V. Leaving V_{PROG2} open (DC) allows the output voltage of the second controller to be set by an external resistive divider connected to $V_{OSENSE2}$.

C_{OSC}: External capacitor C_{OSC} from this pin to ground sets the operating frequency.

I_{TH1}, I_{TH2}: Error Amplifier Compensation Point. Each associated current comparator threshold increases with this control voltage.

RUN/SS1, RUN/SS2: Combination of Soft Start and Run Control Inputs. A capacitor to ground at each of these pins sets the ramp time to full current output. The time is approximately 0.5s/µF. Forcing either of these pins below 1.3V causes the IC to shut down the circuitry required for that particular controller. Forcing both of these pins below 1.3V causes the device to shut down completely. For applications which require 5V keep-alive, refer to the LTC1538-AUX/LTC1539.

TGL1, TGL2: High Current Gate Drives for Main Top N-Channel MOSFET. These are the outputs of floating drivers with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltage SW1 and SW2.

TGS1, TGS2: Gate Drives for Small Top N-Channel MOSFET. These are the outputs of floating drivers with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltage SW. Leaving TGS1 or TGS2 open invokes Burst Mode operation for that controller.

BG1, BG2: High Current Gate Drive Outputs for Bottom N-Channel MOSFETs. Voltage swing at these pins is from ground to $INTV_{CC}$.

SFB1: Secondary Winding Feedback Input. This input acts only on the first controller and is normally connected to a feedback resistive divider from the secondary winding. Pulling this pin below 1.19V will force continuous synchronous operation for the first controller. This pin should be tied to: ground to force continuous operation; $INTV_{CC}$ in applications that don't use a secondary winding; and a resistive divider from the output in applications using a secondary winding.

POR2: This output is a drain of an N-channel pull-down. This pin sinks current when the output voltage of the second controller drops 7.5% below its regulated voltage and releases 65536 oscillator cycles after the output voltage of the second controller rises to within –5% value of its regulated value. The POR2 output is asserted when RUN/SS1 and RUN/SS2 are both low, independant of the V_{OUT2}. This pin is not functional on the LTC1438X.

LBO: This output is a drain of an N-channel pull-down. This pin will sink current when the LBI pin goes below 1.19V.

LBI: The (+) input of a comparator which can be used as a low-battery voltage detector. The (–) input is connected to the 1.19V internal reference.

PLLIN: External Synchronizing Input to Phase Detector. This pin is internally terminated to SGND with 50kΩ. Tie this pin to SGND in applications which do not use the phase-locked loop.

PLL LPF: Output of Phase Detector and Control Input o Oscillator. Normally a series RC lowpass filter network i connected from this pin to ground. Tie this pin to SGND i applications which do not use the phase-locked loop. Ca be driven by a 0V to 2.4V logic signal for a frequenc shifting option.

AUXFB: Feedback Input to the Auxiliary Regulator/Cor parator. When used as a linear regulator, this input c either be connected to an external resistive divider directly to the collector of the external PNP pass device

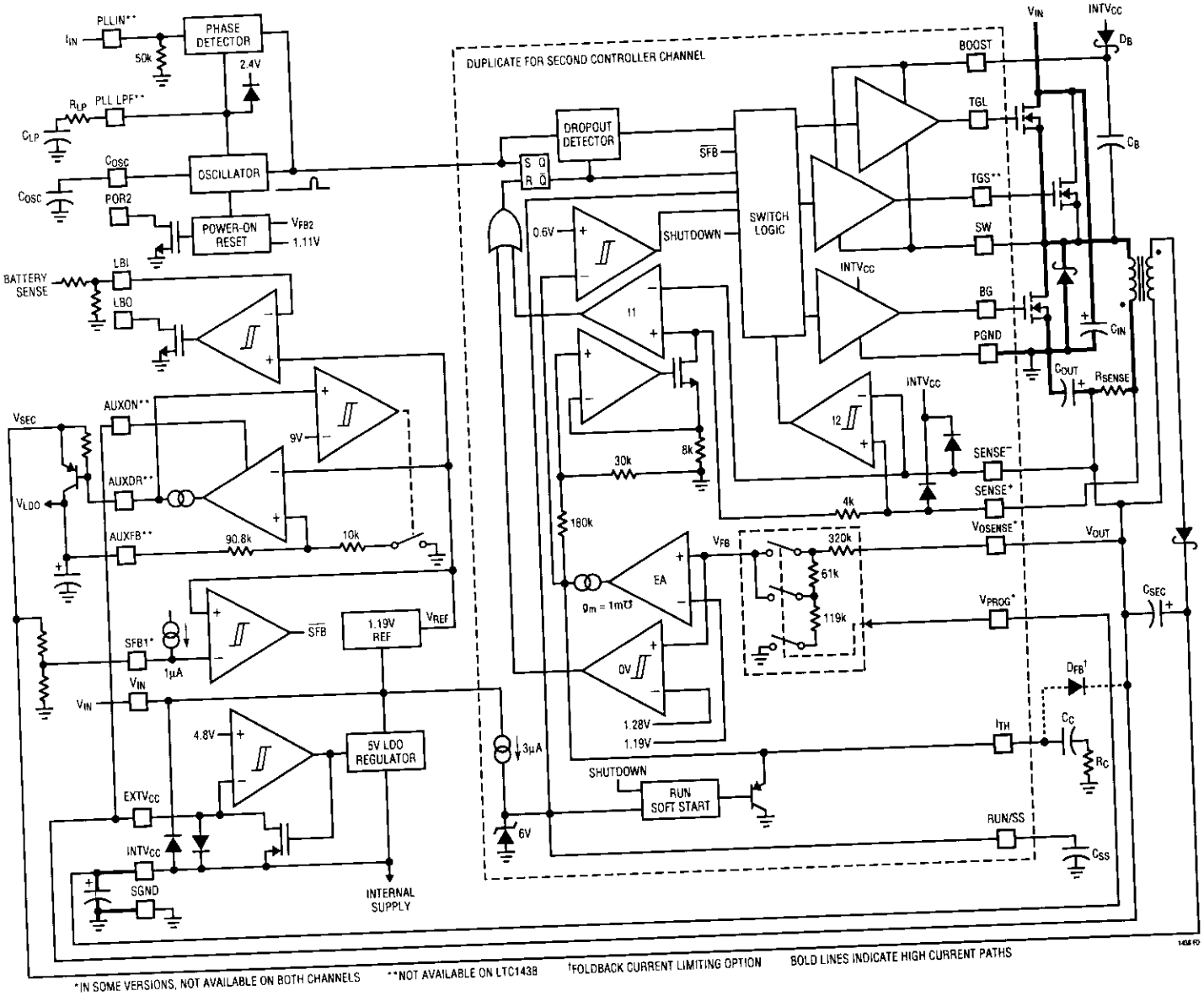
PIN FUNCTIONS

12V operation. When used as a comparator, this is the noninverting input of a comparator whose inverting input is tied to the internal 1.19V reference. See Auxiliary Regulator Application section.

AUXON: Pulling this pin high turns on the auxiliary regulator/comparator. The threshold is 1.19V. This is a convenient linear power supply logic-controlled on/off input.

AUXDR: Open Drain Output of the Auxiliary Regulator/Comparator. The base of an external PNP device is connected to this pin when used as a linear regulator. An external pull-up resistor is required for use as a comparator. A voltage >9.5V on AUXDR causes the internal 12V resistive divider to be connected in series with the AUXFB pin.

FUNCTIONAL DIAGRAM



*IN SOME VERSIONS, NOT AVAILABLE ON BOTH CHANNELS **NOT AVAILABLE ON LTC1438 †FOLDBACK CURRENT LIMITING OPTION BOLD LINES INDICATE HIGH CURRENT PATHS

OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC1438/LTC1439 use a constant frequency, current mode step-down architecture. During normal operation, the top MOSFET is turned on each cycle when the oscillator sets the RS latch and turned off when the main current comparator I1 resets the RS latch. The peak inductor current at which I1 resets the RS latch is controlled by the voltage on the I_{TH1} (I_{TH2}) pin, which is the output of each error amplifier (EA). The V_{PROG1} pin, described in the Pin Functions, allows the EA to receive a selectively attenuated output feedback voltage V_{FB1} from the SENSE$^-$1 pin while V_{PROG2} and $V_{OSENSE2}$ allow EA to receive an output feedback voltage V_{FB2} from either internal or external resistive dividers on the second controller. When the load current increases, it causes a slight decrease in V_{FB} relative to the 1.19V reference, which in turn causes the I_{TH1} (I_{TH2}) voltage to increase until the average inductor current matches the new load current. After the large top MOSFET has turned off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by current comparator I2, or the beginning of the next cycle.

The top MOSFET drivers are biased from floating boot strap capacitor C_B, which normally is recharged during each Off cycle. When V_{IN} decreases to a voltage close to V_{OUT}, however, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector counts the number of oscillator cycles that the top MOSFET remains on and periodically forces a brief off period to allow C_B to recharge.

The main control loop is shut down by pulling the RUN/SS1 (RUN/SS2) pin low. Releasing RUN/SS1 (RUN/SS2) allows an internal 3µA current source to charge soft start capacitor C_{SS}. When C_{SS} reaches 1.3V, the main control loop is enabled with the I_{TH1} (I_{TH2}) voltage clamped at approximately 30% of its maximum value. As C_{SS} continues to charge, I_{TH1} (I_{TH2}) is gradually released allowing normal operation to resume. When both RUN/SS1 and RUN/SS2 are low, all LTC1438/LTC1439 functions are shut down. Refer to the LTC1538-AUX/LTC1539 data sheet for 5V keep-alive applications.

Comparator OV guards against transient overshoots > 7.5% by turning off the top MOSFET and keeping it off until the fault is removed.

Low Current Operation

Adaptive Power mode allows the LTC1439 to automatically change between two output stages sized for different load currents. The TGL1 (TGL2) and BG1 (BG2) pins drive large synchronous N-channel MOSFETs for operation at high currents, while the TGS1 (TGS2) pin drives a much smaller N-channel MOSFET used in conjunction with a Schottky diode for operation at low currents. This allows the loop to continue to operate at normal operating frequency as the load current decreases without incurring the large MOSFET gate charge losses. If the TGS1 (TGS2) pin is left open, the loop defaults to Burst Mode operation in which the large MOSFETs operate intermittently based on load demand.

Adaptive Power mode provides constant frequency operation down to approximately 1% of rated load current. This results in an order of magnitude reduction of load current before Burst Mode operation commences. Without the small MOSFET (i.e., no Adaptive Power mode) the transition to Burst Mode operation is approximately 10% of rated load current.

The transition to low current operation begins when comparator I2 detects current reversal and turns off the bottom MOSFET. If the voltage across R_{SENSE} does not exceed the hysteresis of I2 (approximately 20mV) for one full cycle, then on following cycles the top drive is routed to the small MOSFET at the TGS1 (TGS2) pin and the BG1 (BG2) pin is disabled. This continues until an inductor current peak exceeds 20mV/R_{SENSE} or the I_{TH1} (I_{TH2}) voltage exceeds 0.6V, either of which causes drive to be returned to the TGL1 (TGL2) pin on the next cycle.

Two conditions can force continuous synchronous operation, even when the load current would otherwise dictate low current operation. One is when the common mode voltage of the SENSE$^+$ 1 (SENSE$^+$ 2) and SENSE$^-$ 1 (SENSE$^-$ 2) pins are below 1.4V, and the other is when the SFB1 pin is below 1.19V. The latter condition is used to assist in secondary winding regulation, as described in the Applications Information section.

OPERATION (Refer to Functional Diagram)

Frequency Synchronization

A Phase-Locked Loop (PLL) is available on the LTC1439 to allow the oscillator to be synchronized to an external source connected to the PLLIN pin. The output of the phase detector at the PLL LPF pin is also the control input of the oscillator, which operates over a 0V to 2.4V range corresponding to –30% to 30% in frequency. When locked, the PLL aligns the turn-on of the top MOSFET to the rising edge of the synchronizing signal. When PLLIN is left open, PLL LPF goes low, forcing the oscillator to minimum frequency.

Power-On Reset

The POR2 pin is an open drain output which pulls low when the main regulator output voltage of the second controller is out of regulation. When the output voltage rises to within 7.5% of regulation, a timer is started which releases POR2 after 2^{16} (65536) oscillator cycles. This function is not available on the LTC1438X.

Auxiliary Linear Regulator

The auxiliary linear regulator in the LTC1439 controls an external PNP transistor for operation up to 500mA. A precise internal AUXFB resistive divider is invoked when the AUXDR pin is above 9.5V to allow regulated 12V VPP supplies to be easily implemented. When AUXDR is below 8.5V an external feedback divider may be used to set other output voltages. Taking the AUXON pin low shuts down the auxiliary regulator providing a convenient logic-controlled power supply.

The AUX block can be used as a comparator having its inverting input tied to the internal 1.19V reference. The AUXDR pin is used as the output and requires an external pull-up to a supply of less than 8.5V in order to inhibit the invoking of the internal resistive divider.

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most of the other LTC1438/LTC1439 circuitry is derived from the $INTV_{CC}$ pin. The bottom MOSFET driver supply is also connected to $INTV_{CC}$. When the $EXTV_{CC}$ pin is left open, an internal 5V low dropout regulator supplies $INTV_{CC}$ power. If $EXTV_{CC}$ is taken above 4.8V, the 5V regulator is turned off and an internal switch is turned on to connect $EXTV_{CC}$ to $INTV_{CC}$. This allows the $INTV_{CC}$ power to be derived from a high efficiency external source such as the output of the regulator itself or a secondary winding, as described in the Applications Information section.

APPLICATIONS INFORMATION

The basic LTC1439 application circuit is shown in Figure 1. External component selection is driven by the load requirement and begins with the selection of R_{SENSE}. Once R_{SENSE} is known, C_{OSC} and L can be chosen. Next, the power MOSFETs and D1 are selected. Finally, C_{IN} and C_{OUT} are selected. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 28V (limited by the external MOSFETs).

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The LTC1438/LTC1439 current comparator has a maximum threshold of 150mV/R_{SENSE} and an input common mode range of SGND to $INTV_{CC}$. The current comparator threshold sets the peak of the inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current, ΔI_L.

Allowing some margin for variations in the LTC1438/LTC1439 and external component values yield:

$$R_{SENSE} = \frac{100mV}{I_{MAX}}$$

The LTC1438/LTC1439 work well with values of R_{SENSE} from 0.005Ω to 0.2Ω.

C_{OSC} Selection for Operating Frequency

The LTC1438/LTC1439 use a constant frequency architecture with the frequency determined by an external oscillator capacitor on C_{OSC}. Each time the topside MOSFET turns on, the voltage on C_{OSC} is reset to ground. During the on-time, C_{OSC} is charged by a fixed current plus an additional current which is proportional to the output voltage of the phase detector (V_{PLLLPF})(LTC1439 only). When the voltage on the capacitor reaches 1.19V, C_{OSC} is reset to ground. The process then repeats.

The value of C_{OSC} is calculated from the desired operating frequency. Assuming the phase-locked loop has no external oscillator input (V_{PLLLPF} = 0V):

$$C_{OSC}(pF) = \left[\frac{1.37(10^4)}{\text{Frequency (kHz)}}\right] - 11$$

A graph for selecting C_{OSC} vs frequency is given in Figure 2. As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The maximum recommended switching frequency is 400kHz. When using Figure 2 for synchronizable applications, choose C_{OSC} corresponding to a frequency approximately 30% below your center frequency. (See Phase-Locked Loop and Frequency Sychronization).

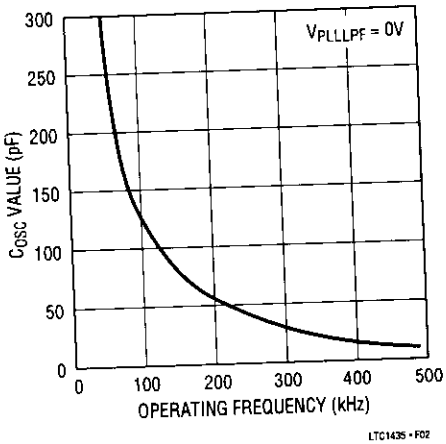


Figure 2. Timing Capacitor Value

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition to this basic trade off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance or frequency and increases with higher V_{IN} or V_{OUT}:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

APPLICATIONS INFORMATION

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4(I_{MAX})$. Remember, the maximum ΔI_L occurs at the maximum input voltage.

The inductor value also has an effect on low current operation. The transition to low current operation begins when the inductor current reaches zero while the bottom MOSFET is on. Lower inductor values (higher ΔI_L) will cause this to occur at higher load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation (TGS1, 2 pins open), lower inductance values will cause the burst frequency to decrease.

The Figure 3 graph gives a range of recommended inductor values vs operating frequency and V_{OUT}.

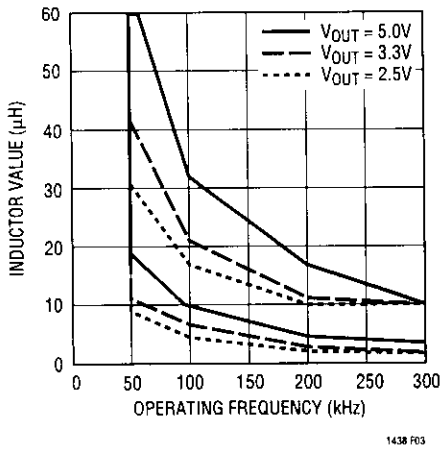


Figure 3. Recommended Inductor Values

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mμ® cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. **Do not allow the core to saturate!**

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, designs for surface mount are available which do not increase the height significantly.

Power MOSFET and D1 Selection

Three external power MOSFETs must be selected for each controller with the LTC1439: a pair of N-channel MOSFETs for the top (main) switch and an N-channel MOSFET for the bottom (synchronous) switch. Only one top MOSFET is required for each LTC1438 controller.

To take advantage of the Adaptive Power output stage, two topside MOSFETs must be selected. A large [low $R_{SD(ON)}$] MOSFET and a small [higher $R_{DS(ON)}$] MOSFET are required. The large MOSFET is used as the main switch and works in conjunction with the synchronous switch. The smaller MOSFET is only enabled under low load current conditions. The benefit of this is to boost low to midcurrent efficiencies while continuing to operate at constant frequency. Also, by using the small MOSFET the circuit will keep switching at a constant frequency down to lower currents and delay skipping cycles.

The $R_{DS(ON)}$ recommended for the small MOSFET is around 0.5Ω. Be careful not to use a MOSFET with an $R_{DS(ON)}$ that is too low; remember, we want to conserve gate charge. (A higher $R_{DS(ON)}$ MOSFET has a smaller gate capacitance and thus requires less current to charge its gate). For all LTC1438 and cost sensitive LTC1439 applications, the small MOSFET is not required. The circuit then begins Burst Mode operation as the load current drops.

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The peak-to-peak drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5V during start-up (see $EXTV_{CC}$ Pin Connection). Consequently, logic level threshold MOSFETs must be used in most LTC1438/LTC1439 applications. The only exception is applications in which $EXTV_{CC}$ is powered from an external supply greater than 8V (must be less than 10V), in which standard threshold MOSFETs ($V_{GS(TH)} < 4V$) may be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the "ON" resistance $R_{SD(ON)}$, reverse transfer capacitance C_{RSS}, input voltage and maximum output current. When the LTC1438/LTC1439 are operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{(V_{IN} - V_{OUT})}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} + k(V_{IN})^{1.85}(I_{MAX})(C_{RSS})(f)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and k is a constant inversely related to the gate drive current.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For $V_{IN} < 20V$ the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$ the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{RSS} actual provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage or during a short circuit when the duty cycle in this switch is nearly 100%. Refer to the Foldback Current Limiting section for further applications information.

The term $(1 + \delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs. C_{RSS} is usually specified in the MOSFET characteristics. The constant k = 2.5 can be used to estimate the contributions of the two terms in the main switch dissipation equation.

The Schottky diode D1 shown in Figure 1 serves two purposes. During continuous synchronous operation, D1 conducts during the dead-time between the conduction of the two large power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on and storing charge during the dead-time, which could cost as much as 1% in efficiency. During low current operation, D1 operates in conjunction with the small top MOSFET to provide an efficient low current output stage. A 1A Schottky is generally a good compromise for both regions of operation due to the relatively small average current.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top N-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx I_{MAX}\frac{[V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question.

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The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement is satisified the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{4fC_{OUT}} \right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. With $\Delta I_L = 0.4 I_{OUT(MAX)}$ the output ripple will be less than 100mV at max V_{IN} assuming:

C_{OUT} Required ESR < $2R_{SENSE}$

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest (ESR size) product of any aluminum electrolytic at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo OS-CON, Nichicon PL series and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

$INTV_{CC}$ Regulator

An internal P-channel low dropout regulator produces 5V at the $INTV_{CC}$ pin from the V_{IN} supply pin. $INTV_{CC}$ powers the drivers and internal circuitry within the LTC1438/LTC1439. The $INTV_{CC}$ pin regulator can supply 40mA and must be bypassed to ground with a minimum of 2.2µF tantalum or low ESR electrolytic capacitor. Good bypassing is necessary to supply the high transient currents required by the MOSFET gate drivers.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC1438/LTC1439 to be exceeded. The IC supply current is dominated by the gate charge supply current when not using an output derived $EXTV_{CC}$ source. The gate charge is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 1 of the Electrical Characteristics. For example, the LTC1439 is limited to less than 21mA from a 30V supply:

$T_J = 70°C + (21mA)(30V)(85°C/W) = 124°C$

To prevent maximum junction temperature from being exceeded, the input supply current must be checked while operating in continuous mode at maximum V_{IN}.

$EXTV_{CC}$ Connection

The LTC1438/LTC1439 contain an internal P-channel MOSFET switch connected between the $EXTV_{CC}$ and $INTV_{CC}$ pins. When the voltage applied to $EXTV_{CC}$ rises above 4.8V, the internal regulator is turned off and an internal switch closes, connecting the $EXTV_{CC}$ pin to the $INTV_{CC}$ pin thereby supplying internal power to the IC. The switch remains closed as long as the voltage applied to $EXTV_{CC}$ remains above 4.5V. This allows the MOSFET driver and control power to be derived from the output during normal operation (4.8V < V_{OUT} < 9V) and from the internal regulator when the output is out of regulation (start-up, short circuit). Do not apply greater than 10V to the $EXTV_{CC}$ pin and ensure that $EXTV_{CC} \leq V_{IN}$.

Significant efficiency gains can be realized by powering $INTV_{CC}$ from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of Duty Cycle/Efficiency. For 5V regulators this supply means connecting the $EXTV_{CC}$ pin directly to V_{OUT}. However, for 3.3V and other lower voltage regulators, additional circuitry is required to derive $INTV_{CC}$ power from the output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ left open (or grounded). This will cause $INTV_{CC}$ to be powered from the internal 5V regulator resulting

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in an efficiency penalty of up to 10% at high input voltages.

2. $EXTV_{CC}$ connected directly to V_{OUT}. This is the normal connection for a 5V regulator and provides the highest efficiency.

3. $EXTV_{CC}$ connected to an output-derived boost network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage which has been boosted to greater than 4.8V. This can be done with either the inductive boost winding as shown in Figure 4a or the capacitive charge pump shown in Figure 4b. The charge pump has the advantage of simple magnetics.

4. $EXTV_{CC}$ connected to an external supply. If an external supply is available in the 5V to 10V range ($EXTV_{CC} \leq V_{IN}$) it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements. When driving standard threshold MOSFETs, the external supply must be always present during operation to prevent MOSFET failure due to insufficient gate drive.

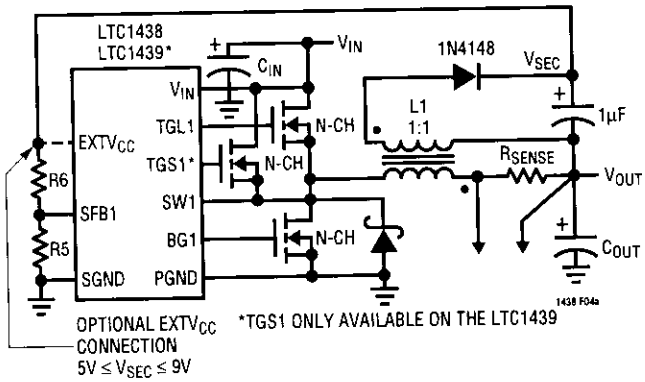

Figure 4a. Secondary Output Loop and $EXTV_{CC}$ Connection

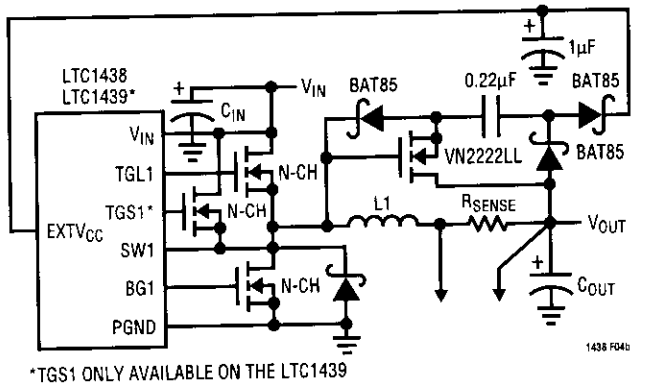

Figure 4b. Capacitive Charge Pump for $EXTV_{CC}$

Topside MOSFET Driver Supply (C_B, D_B)

External bootstrap capacitors C_B connected to the BOOST 1 and BOOST 2 pins supply the gate drive voltages for the topside MOSFETs. Capacitor C_B in the Functional Diagram is charged through diode D_B from $INTV_{CC}$ when the SW1(SW2) pin is low. When one of the topside MOSFETs is to be turned on, the driver places the C_B voltage across the gate source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage SW1(SW2) rises to V_{IN} and the BOOST 1(BOOST 2) pin follows. With the topside MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{INTVCC}$. The value of the boost capacitor C_B needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown on D_B must be greater than $V_{IN(MAX)}$.

Output Voltage Programming

The LTC1438/LTC1439 have pin selectable output voltage programming. Controller 1 on the LTC1438-ADJ is a dedicated adjustable controller. The output voltage is selected by the V_{PROG1} (V_{PROG2}) pin as follows on all of the other parts:

$V_{PROG1,2} = 0V$	$V_{OUT1,2} = 3.3V$
$V_{PROG1,2} = INTV_{CC}$	$V_{OUT1,2} = 5V$
$V_{PROG2} =$ Open (DC)	$V_{OUT2} =$ Adjustable

Except for the LTC1438-ADJ, the top of an internal resistive divider is connected to $SENSE^-1$ pin in Controller 1. For fixed output voltage applications the $SENSE^-1$ pin is connected to the output voltage as shown in Figure 5a. When using an external resistive divider for an adjustable regulator, the V_{PROG2} pin is left open (V_{PROG1} is internally left open on the LTC1438-ADJ) and the $V_{OSENSE2}$ pin is connected to the feedback resistors as shown in Figure 5b. The adjustable controller will force the externally attenuated output voltage to 1.19V.

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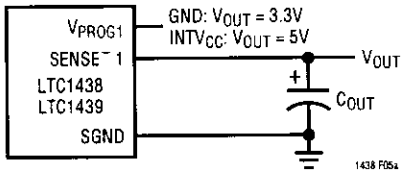

Figure 5a. LTC1438/LTC1439 Fixed Output Applications

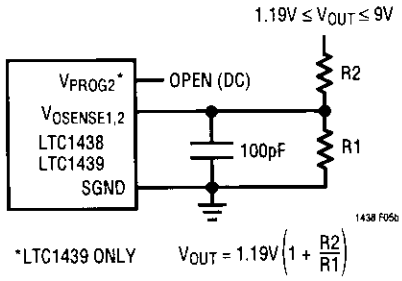

Figure 5b. LTC1438/LTC1439 Adjustable Applications

Power-On Reset Function (POR)

The power-on reset function (not available on the LTC1438X) monitors the output voltage of the second controller and turns on an open drain device when it is below its properly regulated voltage. An external pull-up resistor is required on the POR2 pin.

When power is first applied or when coming out of shutdown, the POR2 output is held at ground. When the output voltage rises above a level which is 5% below the final regulated output value, an internal counter starts. After this counter counts 2^{16} (65536) clock cycles, the POR2 pull-down device turns off.

The POR2 output will go low whenever the output voltage of the second controller drops below 7.5% of its regulated value for longer than approximately 30µs, signaling an out-of-regulation condition. In shutdown, when RUN/SS1 and RUN/SS2 are both below 1.3V, the POR2 output is pulled low even if the regulator's output is held up by an external source. The POR2 output is active during shutdown if V_{IN} is powered.

Run/Soft Start Function

The RUN/SS1 and RUN/SS2 pins each serve two functions. Each pin provides the soft start function and a means to shut down each controller. Soft start reduces surge currents from V_{IN} by providing a gradual ramp-up of the internal current limit. *Power supply sequencing* can also be accomplished using this pin.

An internal 3µA current source charges up an external capacitor C_{SS}. When the voltage on RUN/SS1 (RUN/SS2) reaches 1.3V the particular controller is permitted to start operating. As the voltage on the pin continues to ramp from 1.3V to 2.4V, the internal current limit is also ramped at a proportional linear rate. The current limit begins at approximately 50mV/R_{SENSE} (at $V_{RUN/SS}$ = 1.3V) and ends at 150mV/R_{SENSE} ($V_{RUN/SS} \geq$ 2.7V). The output current thus ramps up slowly, reducing the starting surge current required from the input power supply. If RUN/SS has been pulled all the way to ground there is a delay before starting of approximately 500ms/µF, followed by a similar time to reach full current on that controller.

By pulling both RUN/SS controller pins below 1.3V, the LTC1438/LTC1439 are put into low current shutdown (I_Q < 25µA). These pins can be driven directly from logic as shown in Figure 6. Diode D1 in Figure 6 reduces the start delay but allows C_{SS} to ramp up slowly providing the soft start function; this diode and C_{SS} can be deleted if soft start is not needed. Each RUN/SS pin has an internal 6V Zener clamp (See Functional Diagram).

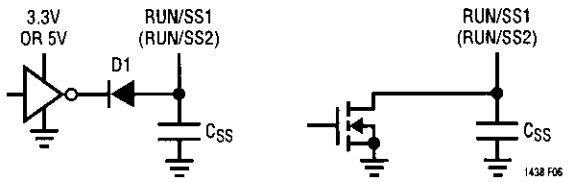

Figure 6. RUN/SS Pin Interfacing

Foldback Current Limiting

As described in Power MOSFET and D1 Selection, the worst-case dissipation for either MOSFET occurs with a short-circuited output, when the synchronous MOSFET conducts the current limit value almost continuously. In most applications this will not cause excessive heating, even for extended fault intervals. However, when heat sinking is at a premium or higher $R_{DS(ON)}$ MOSFETs are being used, foldback current limiting should be added to reduce the current in proportion to the severity of the fault.

Foldback current limiting is implemented by adding diode D_{FB} between the output and the I_{TH} pin as shown in the

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Functional Diagram. In a hard short (V_{OUT} = 0V) the current will be reduced to approximately 25% of the maximum output current. This technique may be used for all applications with regulated output voltages of 1.8V or greater.

Phase-Locked Loop and Frequency Synchronization

The LTC1439 has an internal voltage-controlled oscillator and phase detector comprising a phase-locked loop. This allows the top MOSFET turn-on to be locked to the rising edge of an external source. The frequency range of the voltage-controlled oscillator is ±30% around the center frequency f_O.

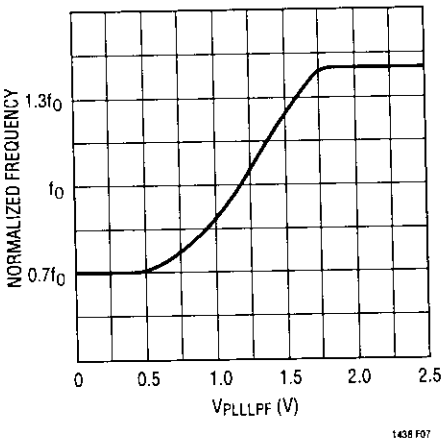

Figure 7. Operating Frequency vs V_{PLLLPF}

The value of C_{OSC} is calculated from the desired operating frequency (f_O). Assuming the phase-locked loop is *locked* (V_{PLLLPF} = 1.19V):

$$C_{OSC}(pF) = \left[\frac{2.1(10^4)}{\text{Frequency (kHz)}}\right] - 11$$

Stating the frequency as a function of V_{PLLLPF} and C_{OSC}:

$$\text{Frequency}(kHz) = \frac{8.4(10^8)}{\left[C_{OSC}(pF)+11\right]\left[\frac{1}{17\mu A + 18\mu A\left(\frac{V_{PLLLPF}}{2.4V}\right)} + 2000\right]}$$

The phase detector used is an edge sensitive digital type which provides zero degrees phase shift between the external and internal oscillators. This type of phase detector will not lock up on input frequencies close to the harmonics of the VCO center frequency. The PLL hold-in range, Δf_H, is equal to the capture range, Δf_C:

$$\Delta f_H = \Delta f_C = \pm 0.3\ f_O.$$

The output of the phase detector is a complementary pair of current sources charging or discharging the external filter network on the PLL LPF pin. A simplified block diagram is shown in Figure 8.

If the external frequency f_{PLLIN} is greater than the oscillator frequency f_{OSC}, current is sourced continuously, pulling up the PLL LPF pin. When the external frequency is less than f_{OSC}, current is sunk continuously, pulling down the PLL LPF pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. Thus the voltage on the PLL LPF pin is adjusted until the phase and frequency of the external and internal oscillators are identical. At this stable operating point the phase comparator output is open and the filter capacitor

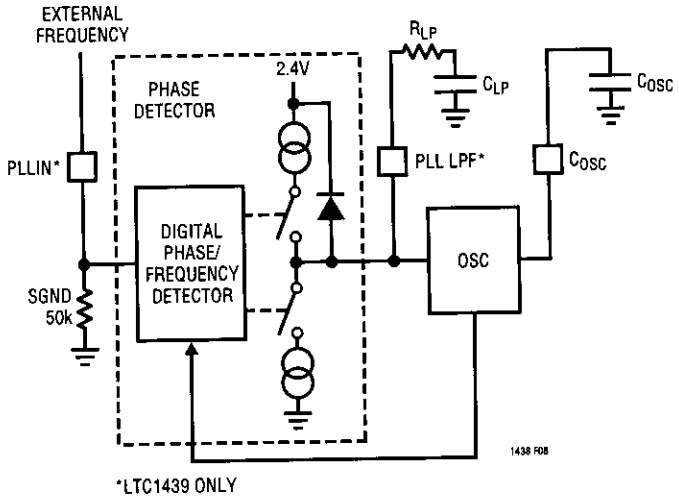

Figure 8. Phase-Locked Loop Block Diagram

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C_{LP} holds the voltage. The LTC1439 PLLIN pin must be driven from a low impedance such as a logic gate located close to the pin. Any external attenuator used needs to be referenced to SGND.

The loop filter components C_{LP}, R_{LP} smooth out the current pulses from the phase detector and provide a stable input to the voltage-controlled oscillator. The filter components C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically, R_{LP}=10k and C_{LP} is 0.01µF to 0.1µF. The low side of the filter needs to be connected to SGND.

The PLL LPF pin can be driven with external logic to obtain a 1:1.9 frequency shift. The circuit shown in Figure 9 will provide a frequency shift from f_0 to $1.9f_0$ as the voltage on V_{PLLLPF} increases from 0V to 2.4V. Do not exceed 2.4V on V_{PLLLPF}.

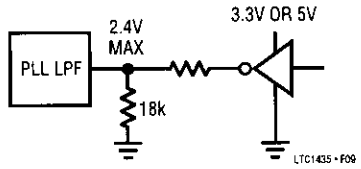

Figure 9. Directly Driving PLL LPF Pin

Low-Battery Comparator

The LTC1438/LTC1439 have an on-chip low-battery comparator which can be used to sense a low-battery condition when implemented as shown in Figure 10. The resistor divider R3/R4 sets the comparator trip point as follows:

$$V_{LBITRIP} = 1.19V\left(1+\frac{R4}{R3}\right)$$

The divided down voltage at the negative (–) input to the comparator is compared to an internal 1.19V reference. A 20mV hysteresis is built in to assure rapid switching. The output is an open drain MOSFET and requires a pull-up resistor. This comparator is *not* active when both the RUN/SS1 and RUN/SS2 pins are low. Refer to the LTC1538/LTC1539 for a comparator which is active during shutdown. The low side of the resistive divider needs to be connected to SGND.

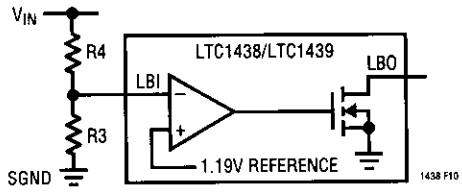

Figure 10. Low-Battery Comparator

SFB1 Pin Operation

When the SFB1 pin drops below its ground referenced 1.19V threshold, continuous mode operation is forced. In continuous mode, the large N-channel main and synchronous switches are used regardless of the load on the main output.

In addition to providing a logic input to force continuous synchronous operation, the SFB1 pin provides a means to regulate a flyback winding output. The use of a synchronous switch removes the requirement that power must be drawn from the inductor primary in order to extract power from the auxiliary winding. With the loop in continuous mode, the auxiliary output may be loaded without regard to the primary output load. The SFB1 pin provides a way to force continuous synchronous operation as needed by the flyback winding.

The secondary output voltage is set by the turns ratio of the transformer in conjunction with a pair of external resistors returned to the SFB1 pin as shown in Figure 4a. The secondary regulated voltage V_{SEC} in Figure 4a is given by:

$$V_{SEC} \approx (N+1)V_{OUT} > 1.19V\left(1+\frac{R6}{R5}\right)$$

where N is the turns ratio of the transformer, and V_{OUT} is the main output voltage sensed by Sense$^-$1.

Auxiliary Regulator/Comparator

The auxiliary regulator/comparator can be used as a comparator or low dropout regulator (by adding an external PNP pass device).

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When the voltage present at the AUXON pin is greater than 1.19V the regulator/comparator is on. The amplifier is stable when operating as a low dropout regulator. This same amplifier can be used as a comparator whose inverting input is tied to the 1.19V reference.

The AUXDR pin is internally connected to an open drain MOSFET which can sink up to 10mA. The voltage on AUXDR determines whether or not an internal 12V resistive divider is connected to AUXFB as described below. A pull-up resistor is required on AUXDR and the voltage must not exceed 28V.

With the addition of an external PNP pass device, a linear regulator capable of supplying up to 0.5A is created. As shown in Figure 11a, the base of the external PNP connects to the AUXDR pin together with a pull-up resistor. The output voltage V_{OAUX} at the collector of the external PNP is sensed by the AUXFB pin.

The input voltage to the auxiliary regulator can be taken from a secondary winding on the primary inductor as shown in Figure 11a. In this application, the SFB1 pin regulates the input voltage to the PNP regulator (see SFB1 Pin Operation) and should be set to approximately 1V to 2V above the required output voltage of the auxiliary regulator. A Zener clamp diode may be required to keep the secondary winding resultant output voltage under the 28V AUXDR pin specification when the primary is heavily loaded and the secondary is not.

The AUXFB pin is the feedback point of the regulator. An internal resistor divider is available to provide a 12V output by simply connecting AUXFB directly to the collector of the external PNP. The internal resistive divider is switched in when the voltage at AUXFB goes above 9.5V with 1V built-in hysteresis. For other output voltages, an external resistive divider is fed back to AUXFB as shown in Figure 11b. The output voltage V_{OAUX} is set as follows:

$$V_{OAUX} = 1.19V\left(1+\frac{R8}{R7}\right) < 8V \quad AUXDR < 8.5V$$

$$V_{OAUX} = 12V \quad AUXDR \geq 12V$$

When used as a voltage comparator as shown in Figure 11c, the auxiliary block has a noninverting characteristic. When AUXFB drops below 1.19V, the AUXDR pin will be pulled low. A minimum current of 5µA is required to pull up the AUXDR pin to 5V when used as a comparator output in order to counteract a 1.5µA internal pull-down current source.

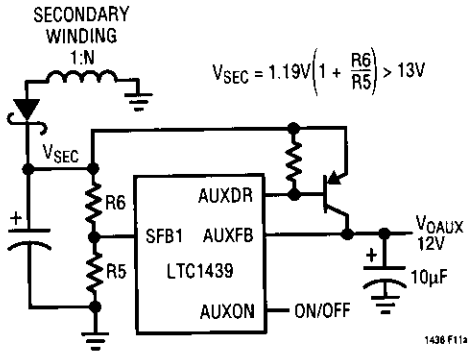

Figure 11a. 12V Output Auxiliary Regulator Using Internal Feedback Resistors

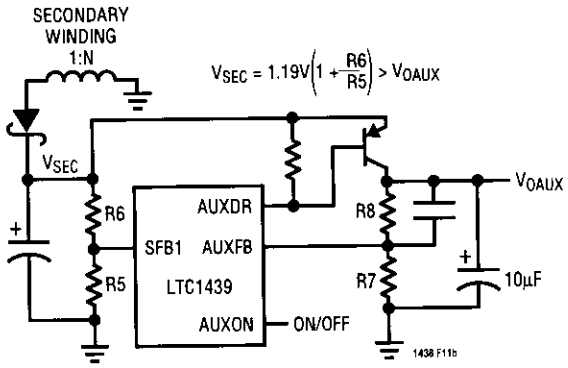

Figure 11b. 5V Output Auxiliary Regulator Using External Feedback Resistors

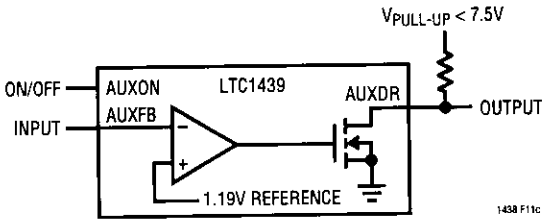

Figure 11c. Auxiliary Comparator Configuration

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Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

$$\text{Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1438/LTC1439 circuits. LTC1438/LTC1439 V_{IN} current, $INTV_{CC}$ current, I^2R losses and topside MOSFET transition losses.

1. The V_{IN} current is the DC supply current given in the Electrical Characteristics which excludes MOSFET driver and control currents. V_{IN} current typically results in a small ($\ll 1\%$) loss which increases with V_{IN}.

2. $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ which is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs. It is for this reason that the large topside and synchronous MOSFETs are turned off during low current operation in favor of the small topside MOSFET and external Schottky diode, allowing efficient, constant-frequency operation at low output currents.

   By powering $EXTV_{CC}$ from an output-derived source, the additional V_{IN} current resulting from the driver and control currents will be scaled by a factor of Duty Cycle/Efficiency. For example, in a 20V to 5V application, 10mA of $INTV_{CC}$ current results in approximately 3mA of V_{IN} current. This reduces the midcurrent loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

3. I^2R losses are predicted from the DC resistances of the MOSFET, inductor and current sense R. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the topside main MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)} = 0.05\Omega$, $R_L = 0.15\Omega$ and $R_{SENSE} = 0.05\Omega$, then the total resistance is 0.25Ω. This results in losses ranging from 3% to 10% as the output current increases from 0.5A to 2A. I^2R losses cause the efficiency to roll off at high output currents.

4. Transition losses apply only to the topside MOSFET(s) and only when operating at high input voltages (typically 20V or greater). Transition losses can be estimated from:

   $$\text{Transition Loss} \approx 2.5(V_{IN})^{1.85}(I_{MAX})(C_{RSS})(f)$$

   Other losses including C_{IN} and C_{OUT} ESR dissipative losses, Schottky conduction losses during dead-time, and inductor core losses, generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $(\Delta I_{LOAD})(ESR)$ where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal which forces the regulator loop to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing which would indicate a stability problem. The I_{TH} external components shown in Figure 1 will prove adequate compensation for most applications.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load

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switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately (25)(C_{LOAD}). Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Automotive Considerations: Plugging into the Cigarette Lighter

As battery-powered devices go mobile, there is a natural interest in plugging into the cigarette lighter in order to conserve or even recharge battery packs during operation. But before you connect, be advised: you are plugging into the supply from hell. The main battery line in an automobile is the source of a number of nasty potential transients, including load dump, reverse battery and double battery.

Load dump is the result of a loose battery cable. When the cable breaks connection, the field collapse in the alternator can cause a positive spike as high as 60V which takes several hundred milliseconds to decay. Reverse battery is just what it says, while double battery is a consequence of tow-truck operators finding that a 24V jump start cranks cold engines faster than 12V.

The network shown in Figure 12 is the most straightforward approach to protect a DC/DC converter from the ravages of an automotive battery line. The series diode prevents current from flowing during reverse battery, while the transient suppressor clamps the input voltage during load dump. Note that the transient suppressor should not conduct during double battery operation, but must still clamp the input voltage below breakdown of the converter. Although the LT1438/LT1439 has a maximum input voltage of 36V, most applications will be limited to 30V by the MOSFET BV_{DSS}.

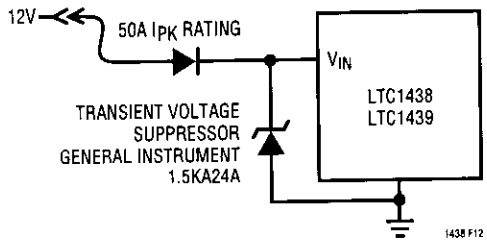

Figure 12. Automotive Application Protection

Design Example

As a design example, assume V_{IN} = 12V(nominal), V_{IN} = 22V(max), V_{OUT} = 3.3V, I_{MAX} = 3A and f = 250kHz, R_{SENSE} and C_{OSC} can immediately be calculated:

$R_{SENSE} = 100mV/3A = 0.033\Omega$

$C_{OSC} = [1.37(10^4)/250] - 11 \approx 43pF$

Refering to Figure 3, a 10µH inductor falls within the recommended range. To check the actual value of the ripple current the following equation is used :

$$\Delta I_L = \frac{V_{OUT}}{(f)(L)}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

The highest value of the ripple current occurs at the maximum input voltage:

$$\Delta I_L = \frac{3.3V}{250kHz(10\mu H)}\left(1-\frac{3.3V}{22V}\right) = 1.12A$$

The power dissipation on the topside MOSFET can be easily estimated. Using a Siliconix Si4412DY for example; $R_{DS(ON)}$ = 0.042Ω, C_{RSS} = 100pF. At maximum input voltage with T(estimated) = 50°C:

$$P_{MAIN} = \frac{3.3V}{22V}(3)^2[1+(0.005)(50°C-25°C)](0.042\Omega) + 2.5(22V)^{1.85}(3A)(100pF)(250kHz) = 122mW$$

The most stringent requirement for the synchronous N-channel MOSFET is with V_{OUT} = 0V (i.e. short circuit). During a continuous short circuit, the worst-case dissipation rises to:

$$P_{SYNC} = [I_{SC(AVG)}]^2(1+\delta)R_{DS(ON)}$$

With the 0.033Ω sense resistor $I_{SC(AVG)}$ = 4A will result, increasing the Si4412DY dissipation to 950mW at a die temperature of 105°C.

C_{IN} will require an RMS current rating of at least 1.5A at temperature and C_{OUT} will require an ESR of 0.03Ω for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

$$V_{ORIPPLE} = R_{ESR}(\Delta I_L) = 0.03\Omega(1.12A) = 34mV_{P-P}$$

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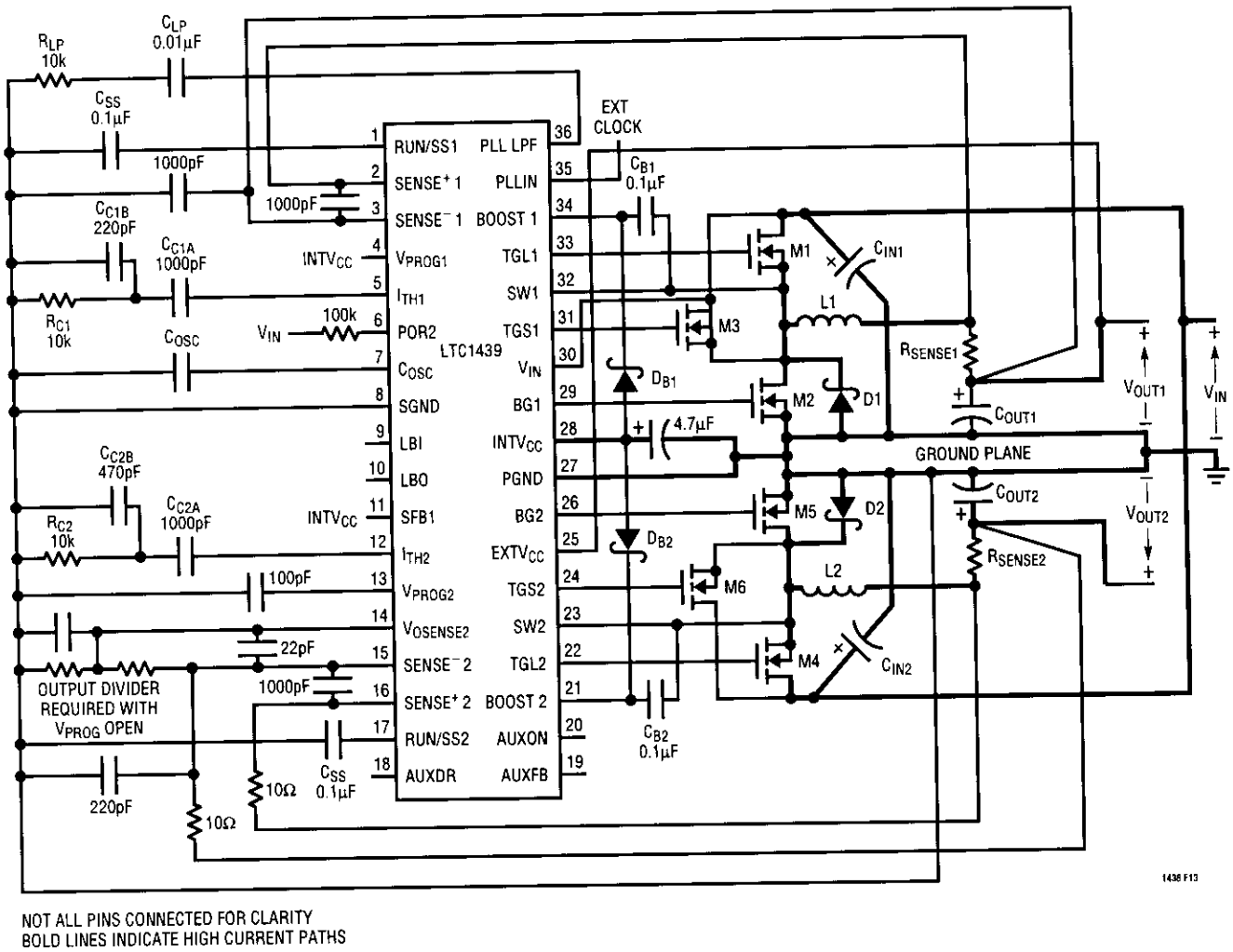

NOT ALL PINS CONNECTED FOR CLARITY
BOLD LINES INDICATE HIGH CURRENT PATHS

Figure 13. LTC1439 Physical Layout Diagram

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1438/LTC1439. These items are also illustrated graphically in the layout diagram of Figure 13. Check the following in your layout:

1. Are the high current power ground current paths using or running through any part of signal ground? The LTC1438/LTC1438X/LTC1439 ICs have their sensitive pins on one side of the package. These pins include the signal ground for the reference, the oscillator input, the voltage and current sensing for both controllers and the low-battery/comparator input. The signal ground area used on this side of the IC must return to the bottom plates of all of the output capacitors. The high current power loops formed by the input capacitors and the ground returns to the sources of the bottom N-channel MOSFETs, anodes of the Schottky diodes and (–) plates of C_{IN}, should be as short as possible and tied through a low resistance path to the bottom plates of the output capacitors for the ground return.
2. Do the LTC1438/LTC1439 SENSE$^-$1 and $V_{OSENSE2}$ pins connect to the (+) plates of C_{OUT}? In adjustable applications, the resistive divider R1/R2 must be connected between the (+) plate of C_{OUT} and signal ground and the HF decoupling capacitor should be as close as possible to the LTC1438/LTC1439.

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3. Are the SENSE$^-$ and SENSE$^+$ leads routed together with minimum PC trace spacing? The filter capacitors between SENSE$^+$1 (SENSE$^+$2) and SENSE$^-$1 (SENSE$^-$2) should be as close as possible to the LTC1438/LTC1439.
4. Do the (+) plates of C_{IN} connect to the drains of the topside MOSFETs as closely as possible? This capacitor provides the AC current to the MOSFETs.
5. Is the $INTV_{CC}$ decoupling capacitor connected closely between $INTV_{CC}$ and the power ground pin? This capacitor carries the MOSFET driver peak currents.
6. Keep the switching nodes, SW1 (SW2), away from sensitive small-signal nodes. Ideally the switch nodes should be placed at the furthest point from the LTC1438/LTC1439.
7. Use a low impedance source such as a logic gate to drive the PLLIN pin and keep the lead as short as possible.

PC Board Layout Suggestions

Switching power supply printed circuit layouts are certainly among the most difficult analog circuits to design. The following suggestions will help to get a reasonably close solution on the first try.

The output circuits, including the external switching MOSFETs, inductor, secondary windings, sense resistor, input capacitors and output capacitors all have very large voltage and/or current levels associated with them. These components and the radiated fields (electrostatic and/or electromagnetic) **must** be kept away from the very sensitive control circuitry and loop compensation components required for a current mode switching regulator.

The electrostatic or capacitive coupling problems can be reduced by increasing the distance from the radiator, typically a very large or very fast moving voltage signal. The signal points that cause problems generally include: the "switch" node, any secondary flyback winding voltage and any nodes which also move with these nodes. The switch, MOSFET gate and boost nodes move between V_{IN} and PGND each cycle with less than a 100ns transition time. The secondary flyback winding output has an AC signal component of $-V_{IN}$ times the turns ratio of the transformer, and also has a similar <100ns transition time. The feedback control input signals need to have less than a few millivolts of noise in order for the regulator to perform properly. A rough calculation shows that 80dB of isolation at 2MHz is required from the switch node for low noise switcher operation. The situation is worse by a factor of the turns ratio for the secondary flyback winding. Keep these switch node related PC traces small and away from the "quiet" side of the IC (not just above and below each other on the opposite side of the board).

The electromagnetic or current loop induced feedback problems can be minimized by keeping the high AC current (transmitter) paths **and** the feedback circuit (receiver) path small and/or short. Maxwell's equations are at work here, trying to disrupt our clean flow of current and voltage information from the output back to the controller input. It is crucial to understand and minimize the susceptibility of the control input stage as well as the more obvious reduction of radiation from the high current output stage(s). An inductive transmitter depends upon the frequency, current amplitude and the size of the current loop to determine the radiation characteristic of the generated field. The current levels are set in the output stage once the input voltage, output voltage and inductor value(s) have been selected. The frequency is set by the output stage transition times. The only parameter over which we have some control is the size of the antenna we create on the PC board, i.e., the loop. A loop is formed with the input capacitance, the top MOSFET, the Schottky diode and the path from the Schottky diode's ground connection and the input capacitor's ground connection. A second path is formed when a secondary winding is used comprising the secondary output capacitor, the secondary winding and the rectifier diode or switching MOSFET (in the case of a synchronous approach). These "loops" should be kept as small and tightly packed as possible in order to minimize their "far field" radiation effects. The radiated field produced is picked up by the current comparator input filter circuit(s), as well as by the voltage feedback circuit(s). The current comparator's filter capacitor placed across the sense pins attenuates the radiated current signal. It is important to place this capacitor immediately adjacent to the IC sense pins. The voltage sensing input(s) minimizes the inductive pickup component by using an input capacitance filter to SGND. The capacitors in both case serve to integrate the induced

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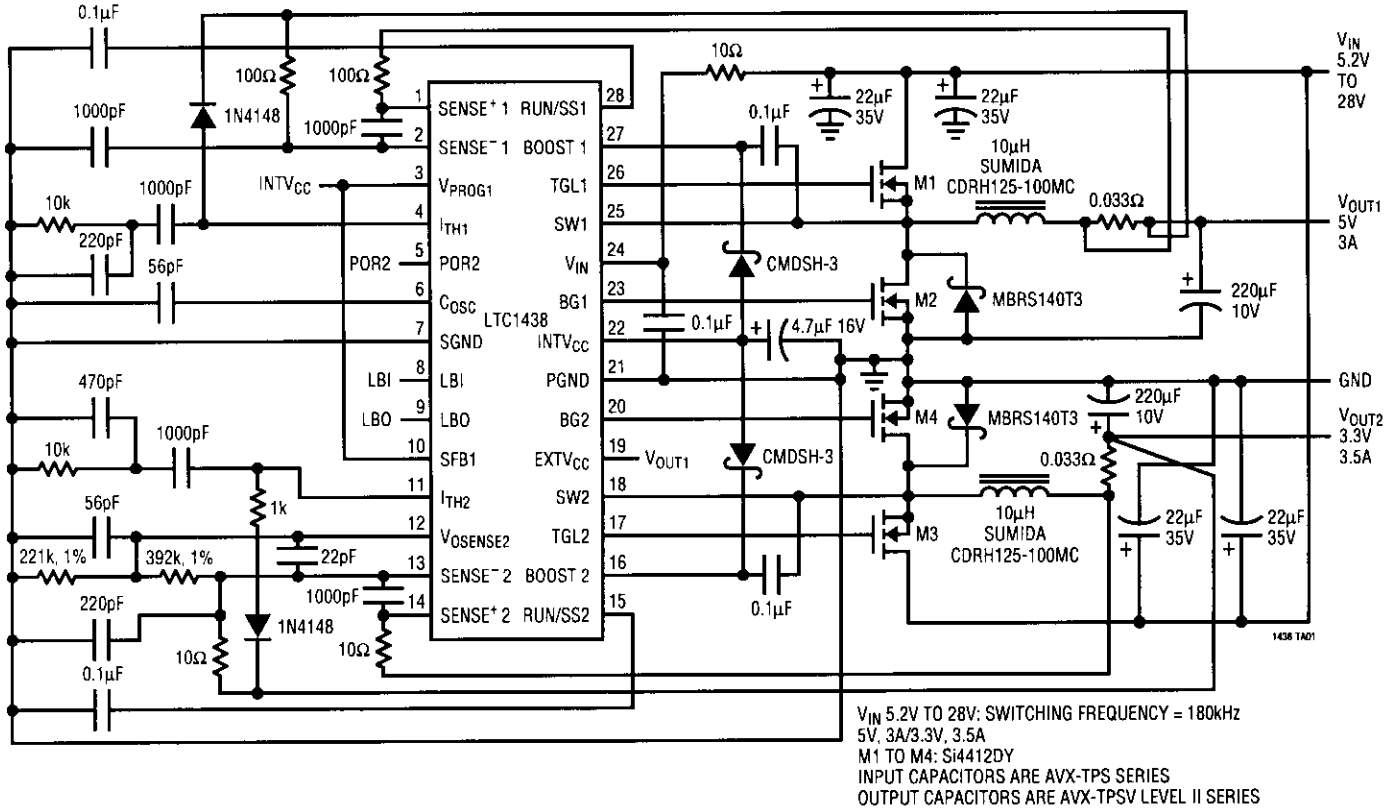
current, reducing the susceptibility to both the "loop" radiated magnetic fields and the transformer or inductor leakage fields.

The capacitor on $INTV_{CC}$ acts as a reservoir to supply the high transient currents to the bottom gates *and* to recharge the boost capacitor. This capacitor should be a 4.7µF tantalum capacitor placed as close as possible to the $INTV_{CC}$ and PGND pins of the IC. Peak current driving the MOSFET gates exceeds 1A. The PGND pin of the IC, connected to this capacitor, should connect directly to the lower plates of the output capacitors to minimize the AC ripple on the $INTV_{CC}$ IC power supply.

The previous instructions will yield a PC layout which has three separate ground regions returning separately to the bottom plates of the output capacitors: a signal ground, a MOSFET gate/$INTV_{CC}$ ground and the ground from the input capacitors, Schottky diode and synchronous MOSFET. In practice, this may produce a long power ground path from the input and output capacitors. A long, low resistance path between the input and output capacitor power grounds will not upset the operation of the switching controllers as long as the signal and power grounds from the IC pins does not "tap in" along this path.

TYPICAL APPLICATIONS

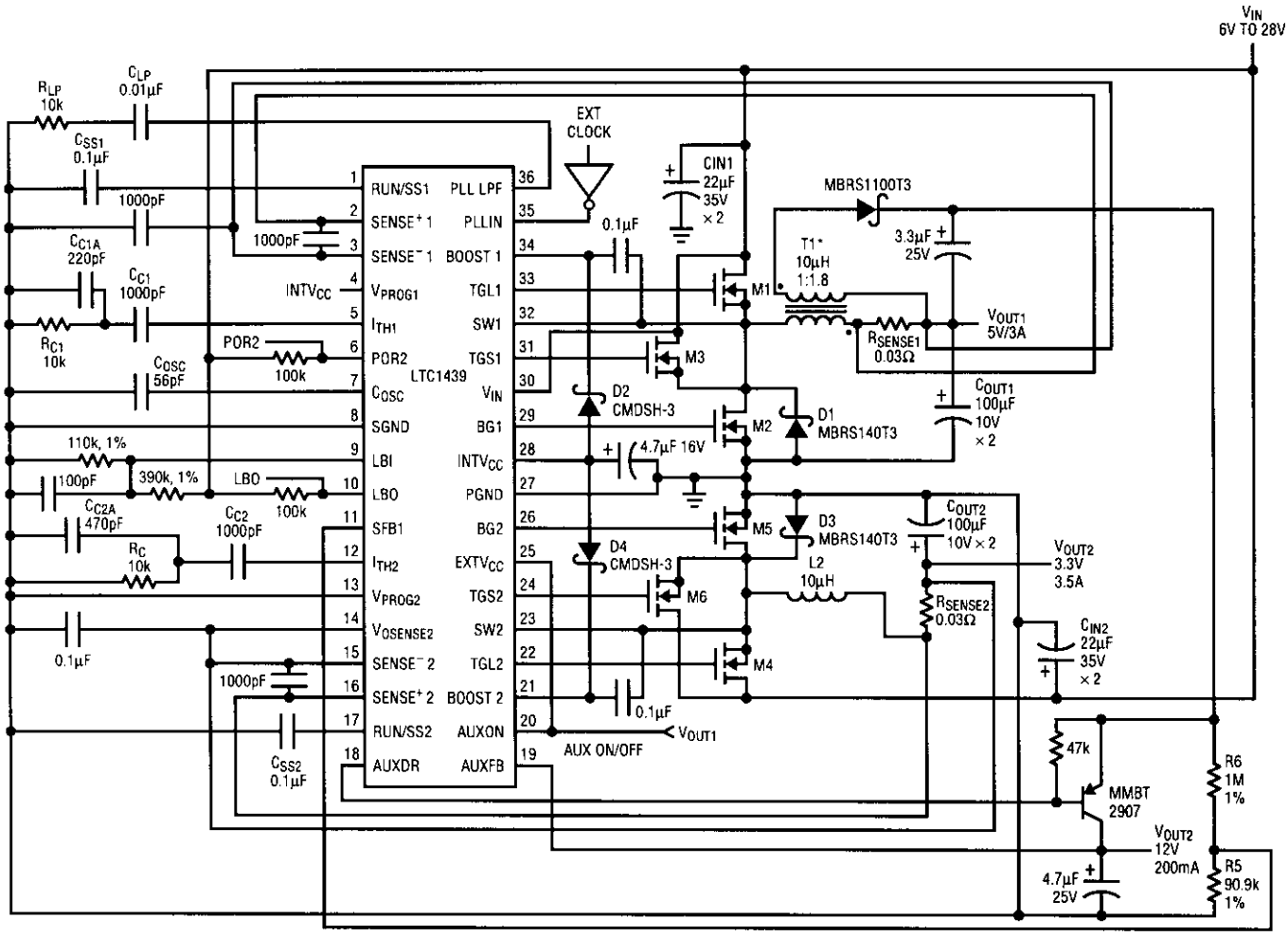
LTC1438 5V/3A, 3.3V/3.5A Regulator



V_{IN} 5.2V TO 28V: SWITCHING FREQUENCY = 180kHz
5V, 3A/3.3V, 3.5A
M1 TO M4: Si4412DY
INPUT CAPACITORS ARE AVX-TPS SERIES
OUTPUT CAPACITORS ARE AVX-TPSV LEVEL II SERIES

TYPICAL APPLICATIONS

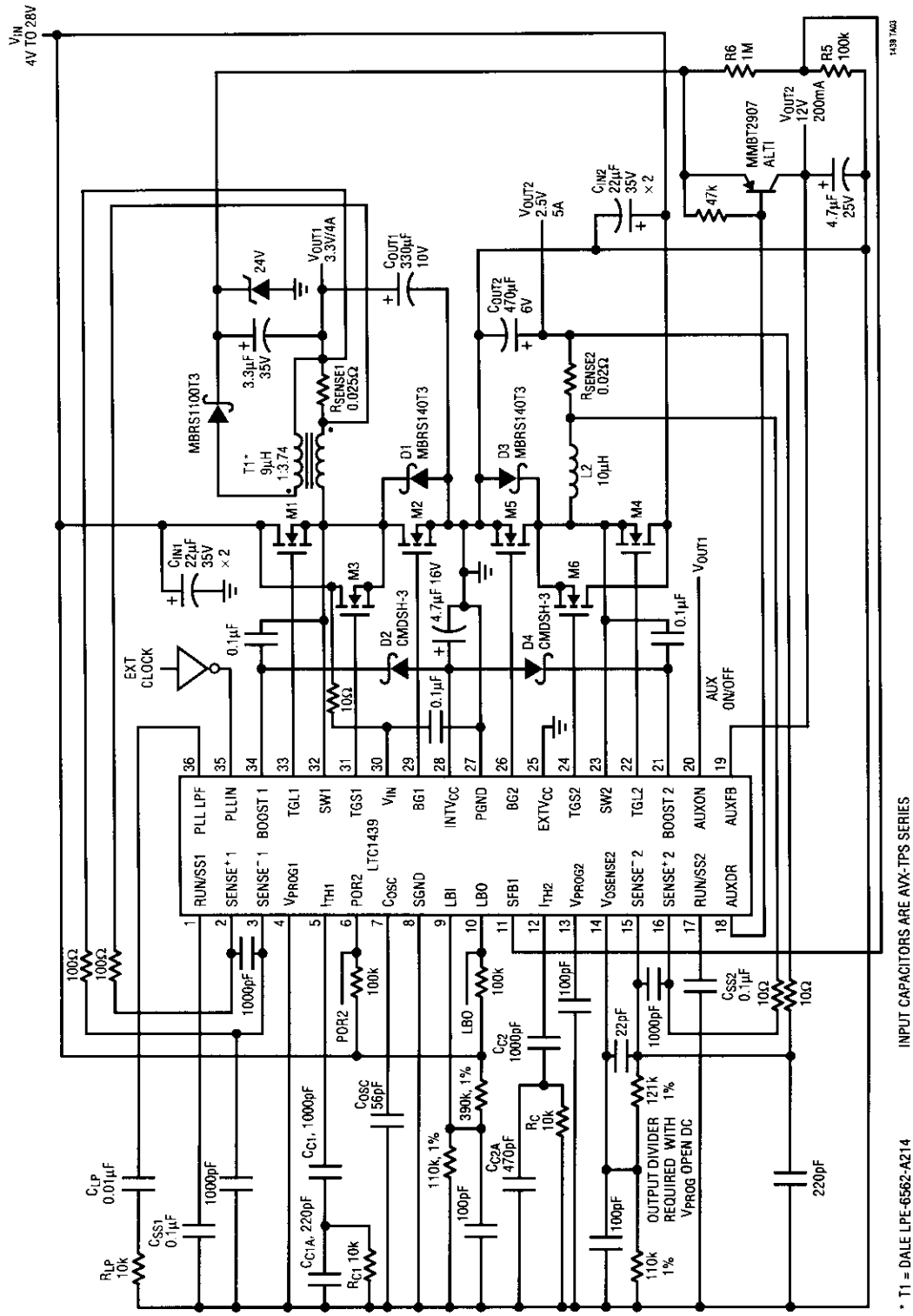
LTC1439 High Efficiency Low Noise 5V/3A, 3.3V/3.5A and 12V/200mA Regulator



* T1 = DALE LPE-6562-A262 GAPPED E-CORE
BH ELECTRONICS 501-0657 GAPPED TOROID
M1, M2, M4, M5 = IRF7403
M3, M6 = IRLML2803
L2 = SUMIDA CDRH125-100MC
ALL INPUT OUTPUT CAPACITORS ARE AVX-TPS SERIES

TYPICAL APPLICATIONS

LTC1439 High Efficiency 3.3V/2.5V Regulator with Low Noise 12V Linear Regulator

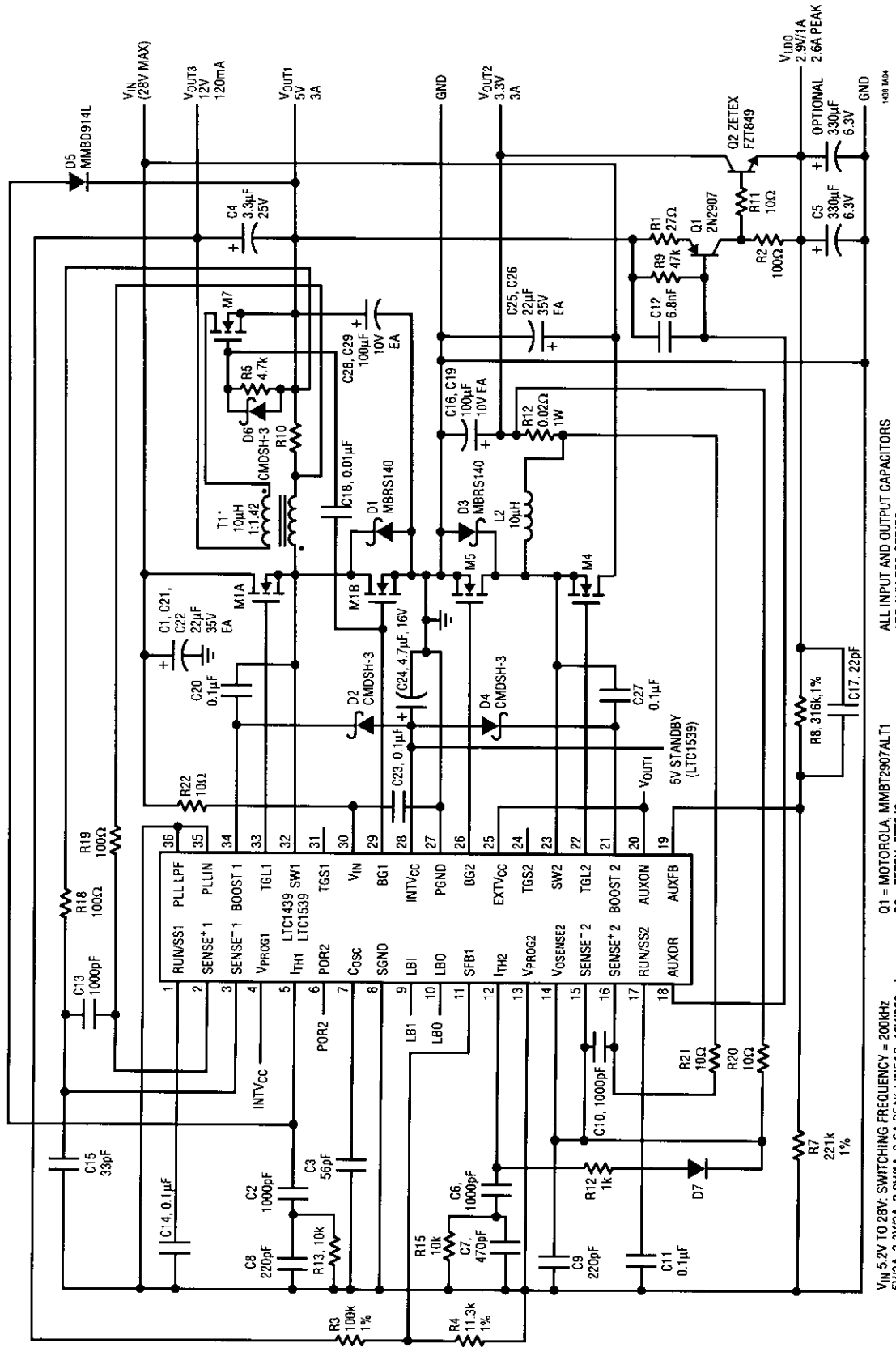


* T1 = DALE LPE-6562-A214
M1, M2, M4, M5 = Si9410DY
M3, M6 = IRLML2803
L2 = SUMIDA CDRH125-100MC

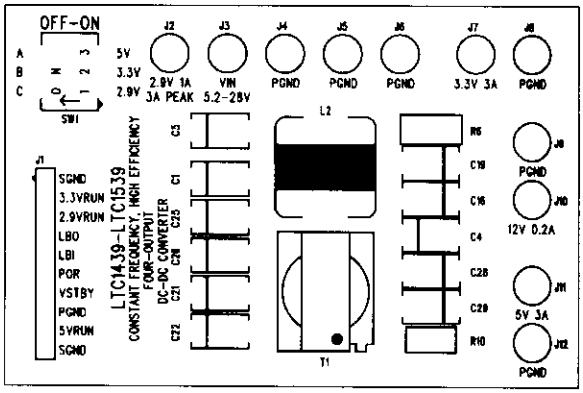
INPUT CAPACITORS ARE AVX-TPS SERIES
OUTPUT CAPACITORS ARE AVX-TPSV LEVEL II SERIES

TYPICAL APPLICATIONS

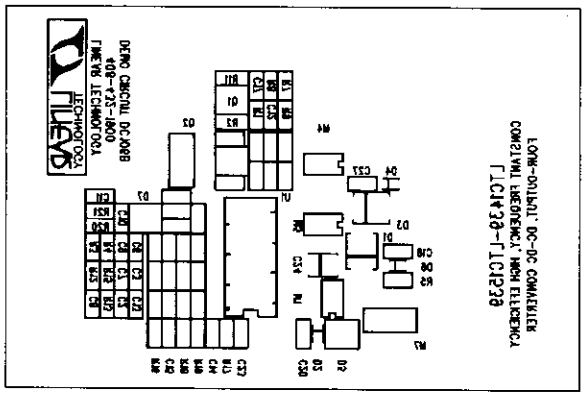
LTC1439/LTC1539 4-Output High Efficiency Low Noise 5V/3A, 3.3V/3A, 2.9V/2.6A, 12V/200mA Notebook Computer Power Supply
(See PCB LAYOUT AND FILM for Layout of Schematic)



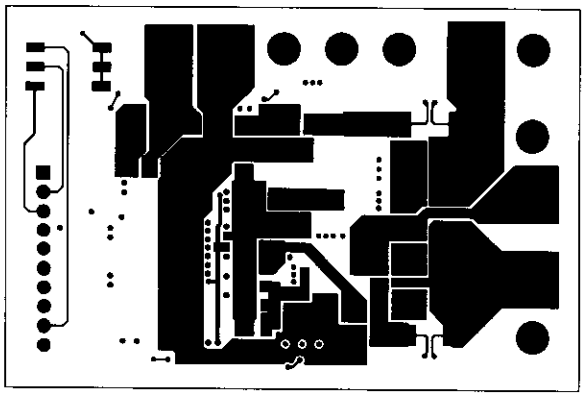
PCB LAYOUT AND FILM (Gerber files for this circuit board are available. Call LTC Marketing.)



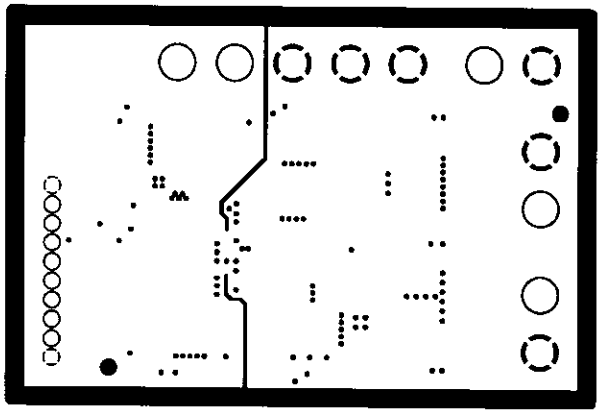
Silkscreen Top



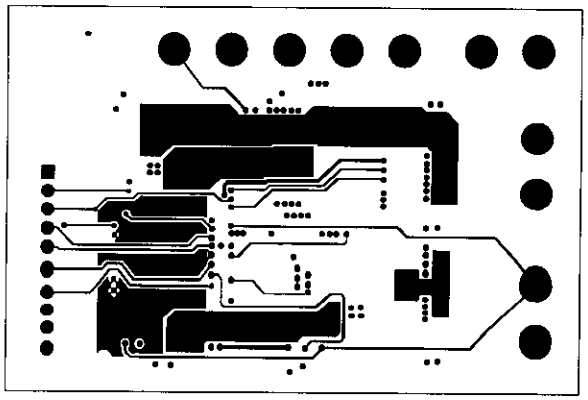
Silkscreen Bottom



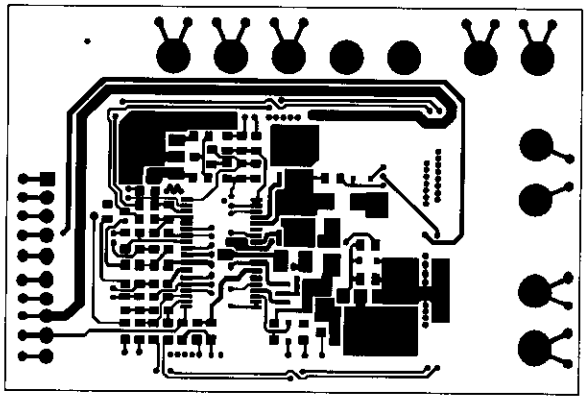
Copper Layer 1



Copper Layer 2 Ground Plane



Copper Layer 3

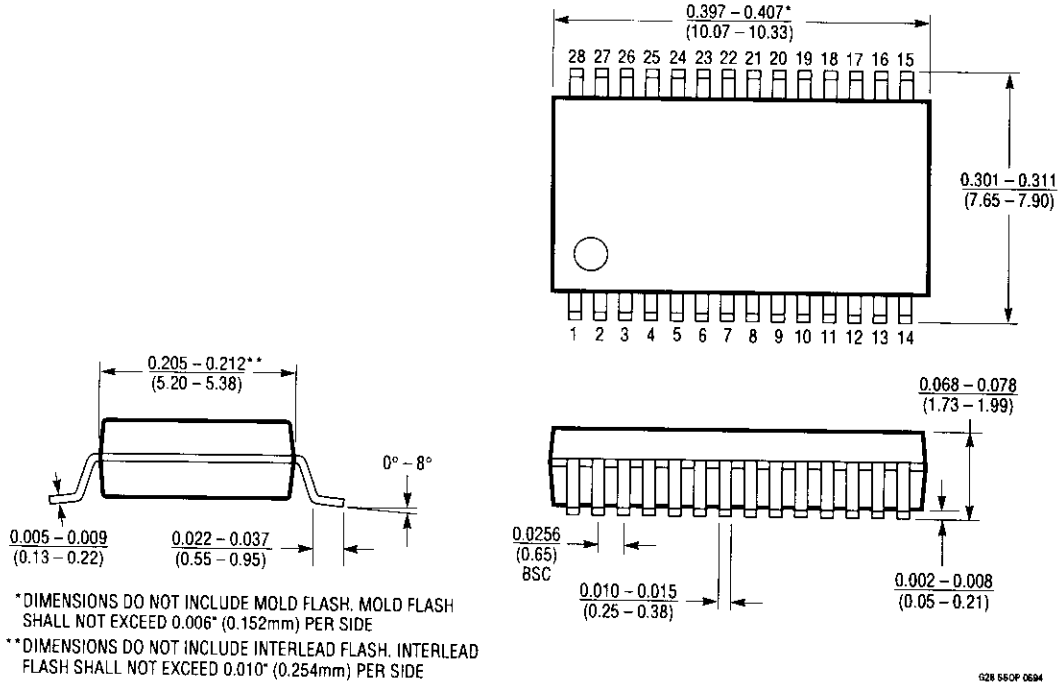


Copper Layer 4

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

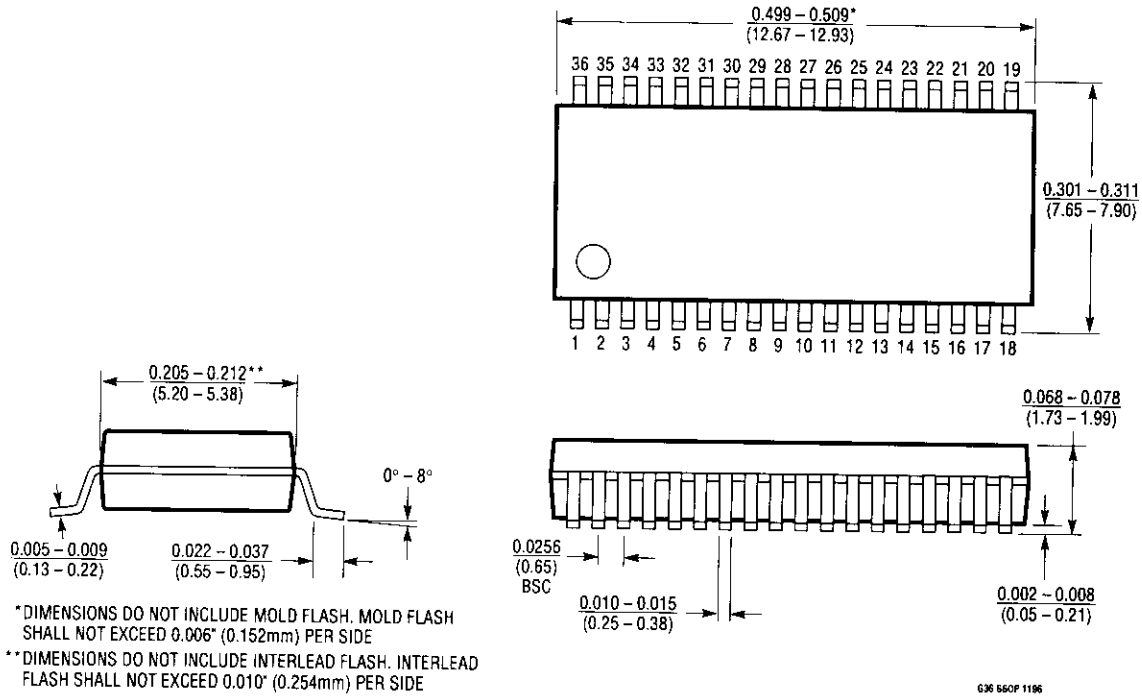
G Package
28-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

G Package
36-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



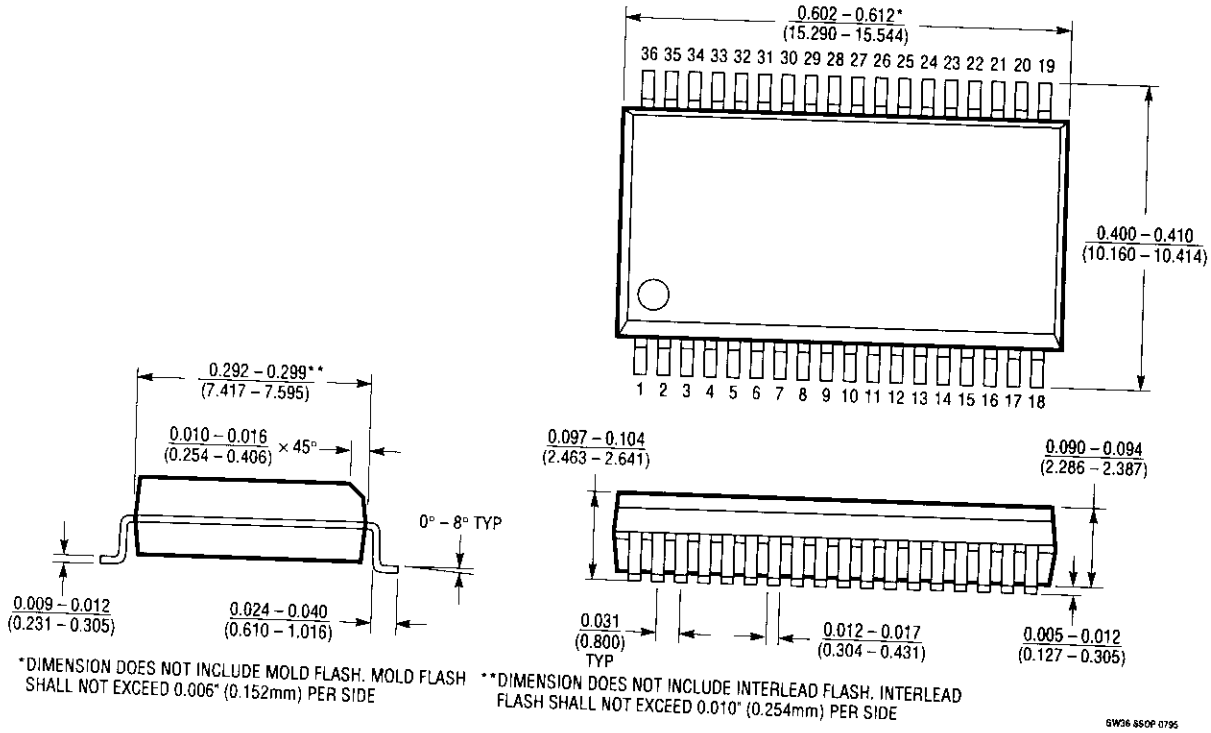
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

GW Package
36-Lead Plastic SSOP (Wide 0.300)
(LTC DWG # 05-08-1642)



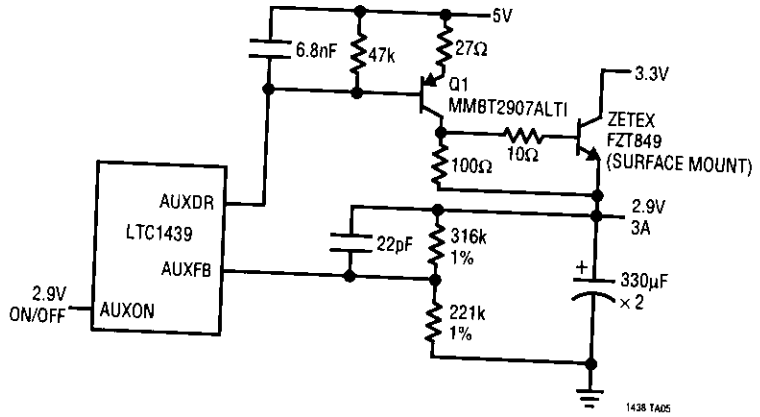
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GW36 SSOP 0795

TYPICAL APPLICATION

3.3V to 2.9V at 3A Low Noise Linear Regulator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1142/LTC1142HV	Dual High Efficiency Synchronous Step-Down Switching Regulators	Dual Synchronous, $V_{IN} \leq 20V$
LTC1148/LTC1148HV	High Efficiency Step-Down Switching Regulator Controllers	Synchronous, $V_{IN} \leq 20V$
LTC1159	High Efficiency Step-Down Switching Regulator Controller	Synchronous, $V_{IN} \leq 40V$, For Logic Threshold FETs
LT®1375/LT1376	1.5A, 500kHz Step-Down Switching Regulators	High Frequency, Small Inductor, High Efficiency Switchers, 1.5A Switch
LTC1430	High Power Step-Down Switching Regulator Controller	High Efficiency 5V to 3.3V Conversion at Up to 15A
LTC1435	Single High Efficiency Low Noise Switching Regulator Controller	16-Pin Narrow SO and SSOP Packages
LTC1436/LTC1436-PLL/ LTC1437	High Efficiency Low Noise Synchronous Step-Down Switching Regulator Controllers	Full-Featured Single Controller
LT1510	Constant-Voltage/Constant-Current Battery Charger	1.3A, Li-Ion, NiCd, NiMH, Pb-Acid Charger
LTC1538-AUX	Dual, Synchronous Controller with AUX Regulator	5V Standby in Shutdown
LTC1539	Dual High Efficiency, Low Noise, Synchronous Step-Down Switching Regulator Controller	5V Standby in Shutdown

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
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MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX919B 4-Level FSK Modem Data Pump

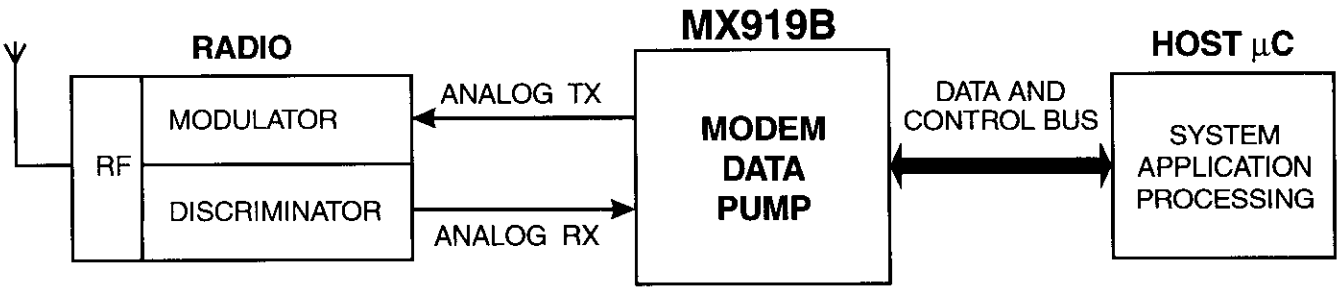
PRELIMINARY INFORMATION

Features

- **4-Level Root Raised Cosine FSK Modulation**
- **Half Duplex, 4800 to 19.2kbps**
- **Increase Channel Bit Rate/Hz**
- **Full Data Packet Framing**
- **Impulse and NRZ Signal Modes**
- **Enhanced Performance in Noisy Conditions**
- **Error Detection and Error Correction**
- **Low Power 3.3V/5.0V Operation**

Applications

- **Wireless Data Terminals**
- **Two Way Paging Systems**
- **Digital Radio Systems**
- **Wide Area Wireless Data Broadcasts**
- **Point to Point Wireless Data Links**



The MX919B is a low voltage CMOS device containing all of the baseband signal processing and Medium Access Control (MAC) protocol functions required for a high performance 4-level FSK Wireless Packet Data Modem. It interfaces with the modem host µC and the radio modulation/demodulation circuits to deliver reliable two-way transfer of the application data over a wireless link.

The MX919B assembles application data received from the host µC, adds forward error correction (FEC) and error detection (CRC) information, and interleaves the result for burst-error protection. After automatically adding symbol and frame sync codewords, the data packet is converted into filtered 4-level analog signals for modulating the radio transmitter.

In receive mode, the MX919B performs the reverse function using the analog signals from the receiver discriminator. After error correction and removal of the packet overhead, the recovered application data is supplied to the host µC. CRC detected residual uncorrected data errors will be flagged. A readout of the SNR value during receipt of a packet is also provided.

The MX919B uses data block sizes and FEC/CRC suitable for applications where high speed transfer of data over narrow-band wireless links is required. The device is programmable to operate at standard bit rates from a wide range of Xtal/clock frequencies.

The MX919B may be used with a 3.0V to 5.0V power supply and is available in the following package styles: 24-pin SSOP (MX919BDS), 24-pin SOIC (MX919BDW), 24-pin PLCC (MX919BLH), and 24-pin PDIP (MX919BP).

www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20480170.001

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Figures

Figure **Page**

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1 Block Diagram

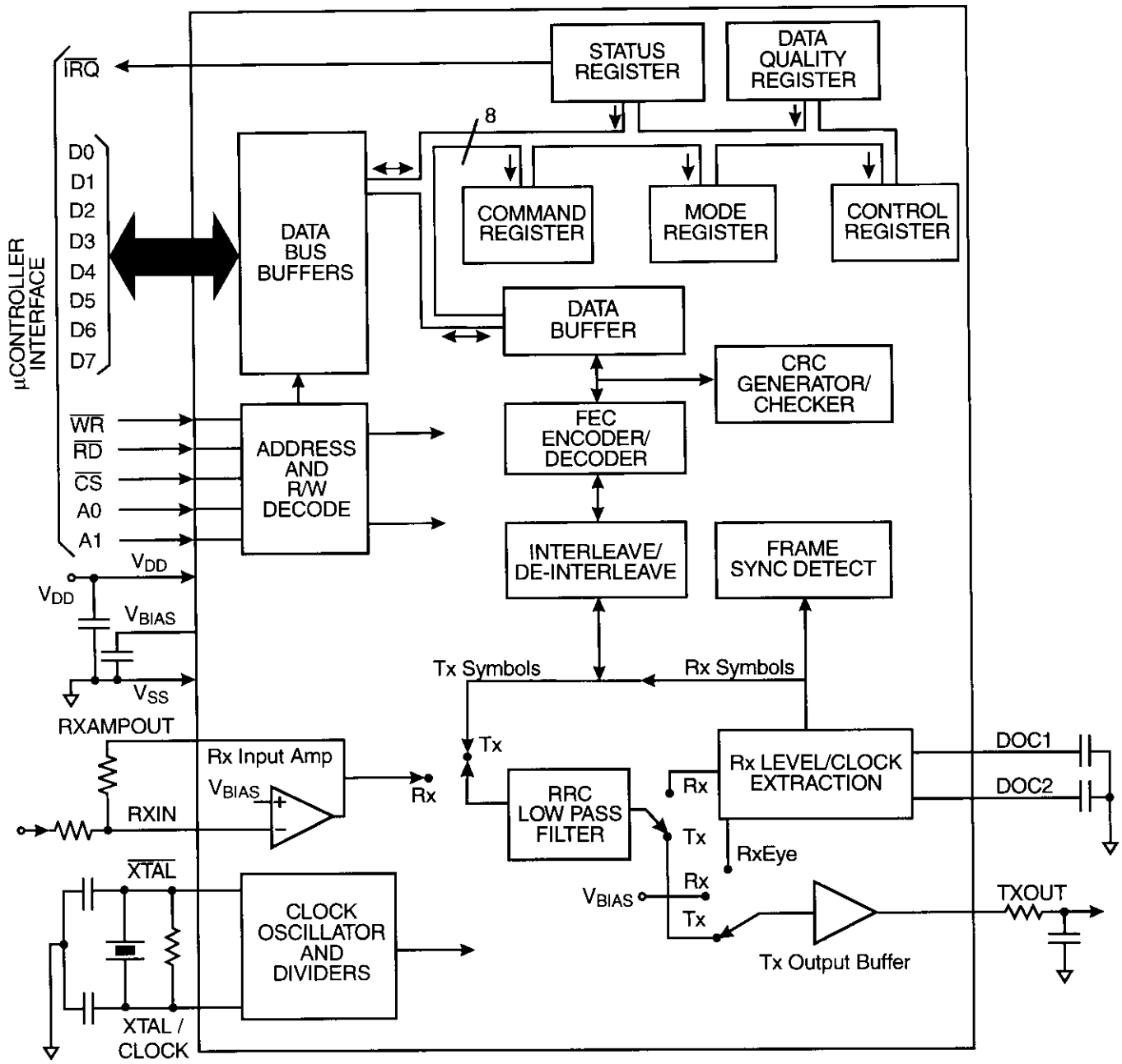

Figure 1: Block Diagram

2 Signal List

Pin No.	Signal	Type	Description
1	$\overline{IRQ}$	output	A 'wire-ORable' output for connection to the host µC's Interrupt Request input. When active, this output has a low impedance pull down to V_{SS}. It has a high impedance when inactive.
2	D7	BUS	Pins 2-9 (D7-D0) are 8-bit, bi-directional, 3-state µC interface data lines
3	D6	BUS	
4	D5	BUS	
5	D4	BUS	
6	D3	BUS	
7	D2	BUS	
8	D1	BUS	
9	D0	BUS	
10	$\overline{RD}$	input	Read. An active low logic level input used to control the reading of data from the modem into the host µC.
11	$\overline{WR}$	input	Write. An active low logic level input used to control the writing of data into the modem from the host µC.
12	V_{SS}	power	Negative supply (ground).
13	$\overline{CS}$	input	Chip Select. An active low logic level input to the modem used to enable a data read or write operation.
14	A0	input	Logic level modem register select input
15	A1	input	Logic level modem register select input
16	$\overline{XTAL}$	output	Output of the on-chip oscillator.
17	XTAL/CLOCK	input	Input to the on-chip oscillator, for an external Xtal circuit or clock.
18	DOC 2	output	Connection to the Rx level measurement circuitry. Should be capacitive coupled to V_{SS}.
19	DOC 1	output	Connection to the Rx level measurement circuitry. Should be capacitive coupled to V_{SS}
20	TXOUT	output	Tx signal output from the modem.
21	V_{BIAS}	output	A bias line for the internal circuitry held at V_{DD} /2. This pin must be bypassed to V_{SS} by a capacitor mounted close to the device pins.
22	RXIN	input	Input to the Rx input amplifier.
23	RXAMPOUT	output	Output of the Rx input amplifier.
24	V_{DD}	power	Positive supply. Levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor mounted close to the device pins.

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3 External Components

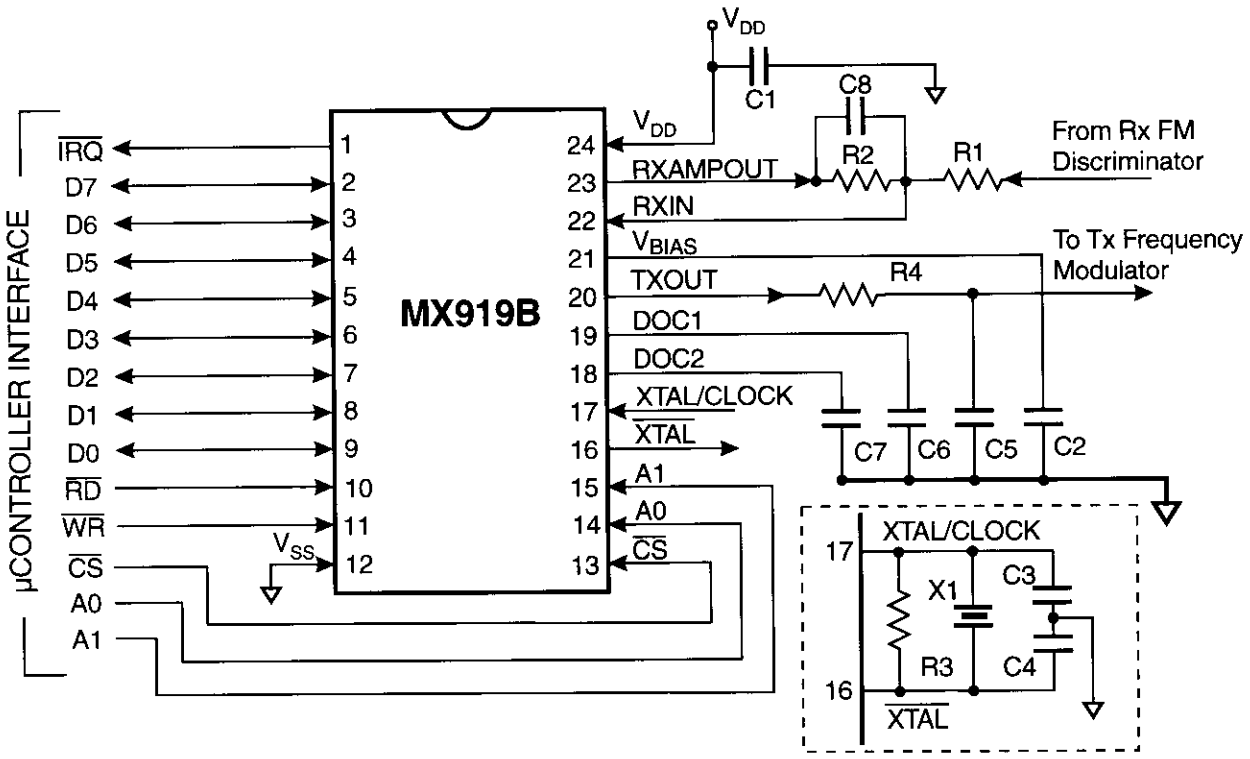

Figure 2: Recommended External Components

Component	Notes	Value	Tolerance
R1	1		±20%
R2		100kΩ	±5%
R3		1MΩ	±20%
R4		100kΩ	±5%
C1		0.1 µF	±20%
C2		0.1 µF	±20%
C3	3		±20%

Component	Notes	Value	Tolerance
C4	3		±20%
C5	4		±5%
C6	5		±20%
C7	5		±20%
C8	4		±5%
X1	2, 3		

Recommended External Component Notes:

1. See Section 4.1.10.
2. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.
3. The values used for C3 and C4 should be suitable for the frequency of the crystal X1. As a guide, values (including stray capacitance) of 33pF at 1MHz falling to 18pF at 10MHz will generally prove suitable. Crystal frequency tolerances are discussed in Section 4.5.3.4.
4. Values C5 and C8 should be equal to 750,000 / symbol rate, e.g.
5. Values C6 and C7 should be equal to 50,000 / symbol rate, e.g.

Symbol Rate	C5 and C8
2400 symbols/second	330pF
4800 symbols/second	150pF
9600 symbols/second	82pF

Symbol Rate	C6 and C7
2400 symbols/second	0.022µF
4800 symbols/second	0.01µF
9600 symbols/second	4700pF

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4 General Description

4.1 Description of Blocks

4.1.1 Data Bus Buffers

Eight bi-directional 3-state logic level buffers between the modem's internal registers and the host µC's data bus lines.

4.1.2 Address and R/W Decode

This block controls the transfer of data bytes between the µC and the modem's internal registers according to the state of the Write and Read Enable inputs ($\overline{WR}$ and $\overline{RD}$), the Chip Select input ($\overline{CS}$), and the Register Address inputs A0 and A1.

The Data Bus Buffers, Address, and R/W Decode blocks provide a byte-wide parallel µC interface, which can be memory-mapped, as shown in Figure 3.

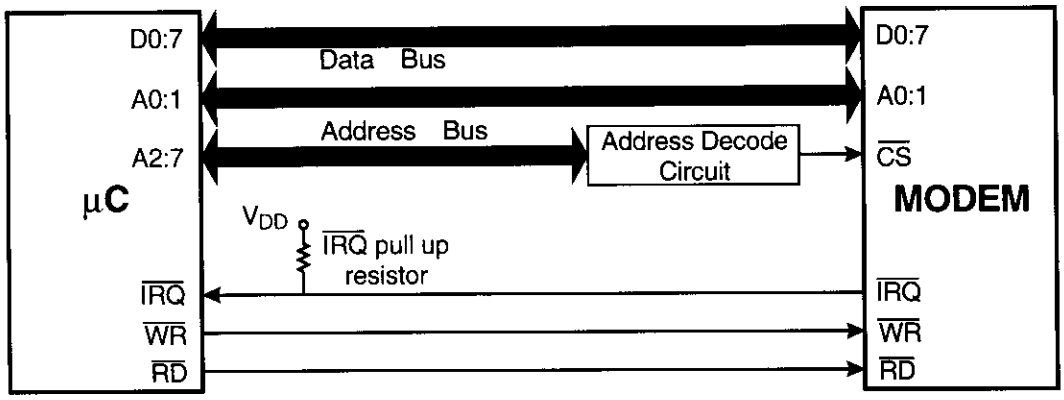

Figure 3: Typical Modem µC connections

4.1.3 Status and Data Quality Registers

Two, 8-bit registers which the µC can read, to determine the status of the modem and received data quality.

4.1.4 Command, Mode, and Control Registers

The values written by the µC to these 8-bit registers control the operation of the modem.

4.1.5 Data Buffer

A 12-byte buffer used to hold receive or transmit data to or from the µC.

4.1.6 CRC Generator/Checker

A circuit which generates (in transmit mode) or checks (in receive mode) the Cyclic Redundancy Checksum bits, which may be included in the transmitted data blocks so the receive modem can detect transmission errors.

4.1.7 FEC Generator/Checker

In transmit mode, this circuit adds Forward Error Correction bits to the transmitted data, resulting in the conversion of binary data to 4-level symbols. In receive mode, this circuit translates received 4-level symbols to binary data, using the FEC information to correct a large proportion of transmission errors.

4.1.8 Interleave/De-Interleave Buffer

This circuit interleaves data symbols within a block before transmission and de-interleaves the received data so that the FEC system is best able to handle short noise bursts or fades.

4.1.9 Frame Sync Detect

This circuit, which is only active in receive mode, is used to look for the 24-symbol Frame Synchronization pattern that is transmitted to mark the start of every frame.

4.1.10 Rx Input Amp

This amplifier allows the received signal input to the modem to be set to the optimum level by suitable selection of the external components R1 and R2. The value of R1 should be calculated to give 0.2 x V_{DD} volts$_{P-P}$ at the RXAMPOUT pin for a received '...+3 +3 -3 -3 ...' sequence.

A capacitor may be placed in series with R1 if ac coupling of the received signal is desired (see Section 5.4), otherwise the DC level of the received signal should be adjusted so that the signal at the modem's RXAMPOUT pin is centered around V_{BIAS} (V_{DD}/2).

4.1.11 RRC Low Pass Filter

This filter, which is used in both transmit and receive modes, is a linear-phase lowpass filter with a 'Root Raised Cosine' frequency response defined by:

$$H(f) = 1 \text{ for } 0 \le f < \frac{1-b}{2T}$$

$$H(f) = \sqrt{\frac{1}{2} - \frac{\sin\frac{(\pi Tf - \frac{\pi}{2})}{b}}{2}} \text{ for } \frac{1-b}{2T} \le f \le \frac{1+b}{2T}$$

$$H(f) = 0 \text{ for } f > \frac{1+b}{2T}$$

$$\text{Where } b = 0.2, \quad T = \frac{1}{\text{symbol rate}}$$

This frequency response is illustrated in Figure 5 and Figure 6.

In transmit mode, the 4-level symbols are passed through this filter to eliminate the high frequency components which would otherwise cause interference into adjacent radio channels. The input applied to the RRC Tx filter may be impulses or full-width symbols depending on the setting of the Command Register TXIMP bit. See Section 4.7

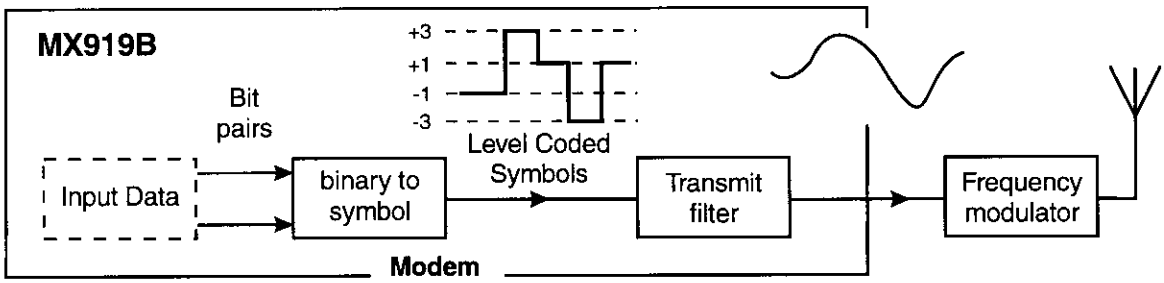

Figure 4: Translation of Binary Data to Filtered 4-Level Symbols in Tx Mode

In receive mode, the filter is used to reject HF noise and to equalize the received signal to a form suitable for extracting the 4-level symbols. The equalization characteristics are determined by the setting of the Command Register TXIMP bit.

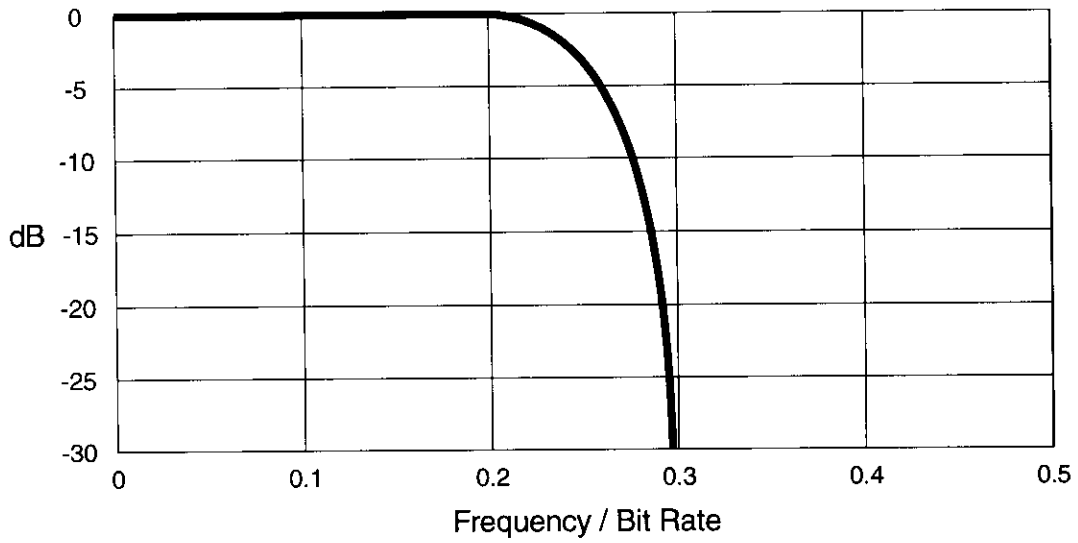

Figure 5: RRC Filter Frequency Response vs. Bit Rate (including the external RC filter R4/C5)

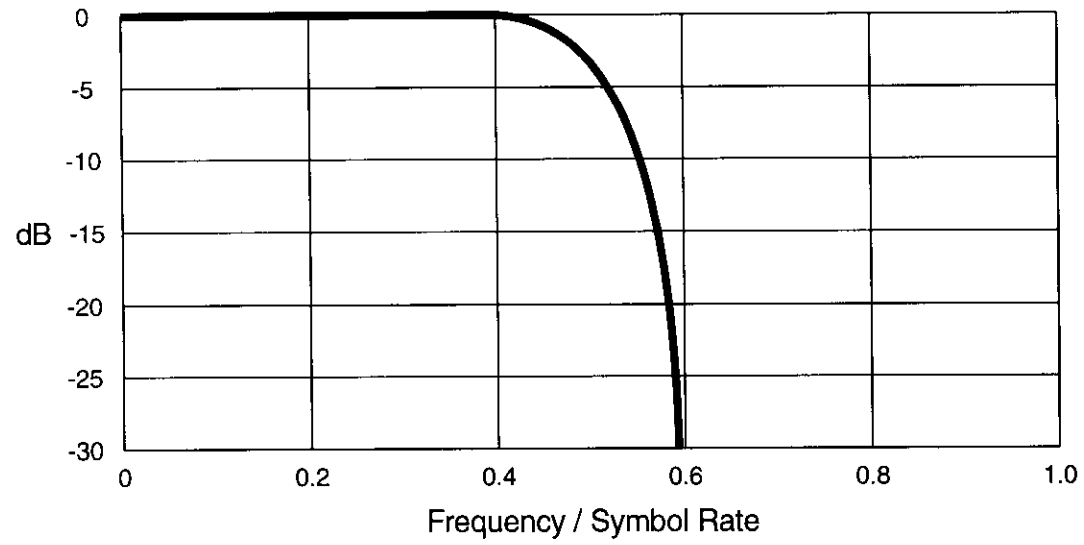

Figure 6: RRC Filter Frequency Response vs. Symbol Rate (including the external RC filter R4/C5)

4.1.12 Tx Output Buffer

This is a unity gain amplifier used in the transmit mode to buffer the output of the Tx low pass filter. In receive mode, the input of this buffer is connected to V_{BIAS}, unless the RXEYE bit of the Control Register is '1', in which case it is connected to the received signal. When changing from Rx to Tx mode, the input to this buffer will be connected to V_{BIAS} for 8 symbol times while the RRC filter settles.

Note: The RC low pass filter formed by the external components R4 and C5 between the TXOUT pin and the input to the radio's frequency modulator forms an important part of the transmit signal filtering. These components may form part of any DC level-shifting and gain adjustment circuitry. The value used for C5 should take into account stray circuit capacitance, and its ground connection should be positioned to give maximum attenuation of high frequency noise into the modulator.

The signal at the TXOUT pin is centered around V_{BIAS}. It is approximately 0.2 x V_{DD} $volts_{P-P}$ for a continuous '+3 +3 -3 -3...' pattern with TXIMP = 0. For typical Tx Eye Diagrams refer to Section 4.7, Figure 17 and Figure 18. For typical Rx Eye Diagrams refer to Section 4.5.4.4, Figure 14.

A capacitor may be placed in series with the input to the frequency modulator if AC coupling is desired. See Section 5.4.

4.1.13 Rx Level/Clock Extraction

These circuits, which operate only in receive mode, derive a symbol rate clock from the received signal and measure the received signal amplitude and DC offset. This information is then used to extract the received 4-level symbols and also to provide an input to the received Data Quality measuring circuit. The external capacitors C6 and C7 form part of the received signal level measuring circuit.

The capacitors C6 and C7 are driven from a very high impedance source so any measurement of the voltages on the DOC pins must be made via high input impedance (MOS input) voltage followers to avoid disturbance of the level measurement circuits.

Further details of the level and clock extraction functions are given in Section 5.3.

4.1.14 Clock Oscillator and Dividers

These circuits derive the transmit symbol rate (and the nominal receive symbol rate) by frequency division of a reference frequency which may be generated by the on-chip Xtal oscillator or applied from an external source.

Note: If the on-chip Xtal oscillator is to be used, then the external components X1, C3, C4, and R3 are required. If an external clock source is to be used, then it should be connected to the XTAL/CLOCK input pin, the $\overline{\text{XTAL}}$ pin should be left unconnected, and X1, C3, C4, and R3 should not be installed.

4.2 Modem - µC Interaction

In general, data is transmitted over-air in the form of messages, or 'Frames', consisting of a 'Frame Preamble' followed by one or more formatted data blocks. The Frame Preamble includes a Frame Synchronization pattern designed to allow the receiving modem to identify the start of a frame. The following data blocks are constructed from the 'raw' data using a combination of CRC (Cyclic Redundancy Checksum) generation, Forward Error Correction coding, and Interleaving. Details of the message formats handled by the modem are provided in Section 4.4, Figure 7, and Figure 8.

To reduce the processing load on the associated µC, the MX919B modem has been designed to perform as much of the computationally intensive work involved in Frame formatting and de-formatting and (when in receive mode) searching for and synchronizing onto the Frame Preamble. In normal operation, the modem will only require servicing by the µC once per received or transmitted block.

Therefore, to transmit a block, the controlling µC needs only to load the unformatted 'raw' binary data into the modem's Data Block Buffer, then instruct the modem to format and transmit that data. The modem will then calculate and add the CRC bits as required, encode the result as 4-level symbols (with Forward Error Correction coding), and interleave the symbols before transmission.

In receive mode, the modem can be instructed to assemble a block's worth of received symbols, de-interleave the symbols, translate them to binary, perform Forward Error Correction, and check the resulting CRC before placing the received binary data into the Data Block Buffer for the µC to read.

The modem can also handle the transmission and reception of unformatted data using the T4S, T24S, and R4S tasks as described in Sections 4.3 and 4.5.2. These tasks are normally used for the transmission of Symbol and Frame Synchronization sequences. These tasks may also be used for the transmission and reception of special test patterns or special data formats. In such a case, care should be taken to ensure that the transmitted TXOUT signal contains enough level and timing information for the receiving modem's level and clock extraction circuits to function correctly. See Section 5.3.

4.3 Binary to Symbol Translation

Although the over-air signal, and therefore the signals at the modem TXOUT and RXIN pins, consists of 4-level symbols, the raw data passing between the modem and the µC is in binary form. Translation between binary data and the 4-level symbols is done in one of two ways, depending on the task being performed.

1. Direct way: (simplest form) - converts between 2 binary bits and a single symbol.

SYMBOL	MSB	LSB
+3	1	1
+1	1	0
-1	0	0
-3	0	1

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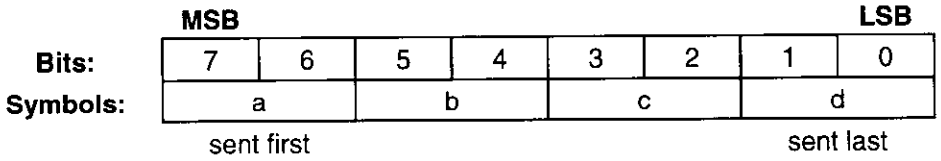
Accordingly, 1 byte = 4 symbols = 8 bits, and one byte translates to four symbols for the T4S and R4S tasks and six bytes translates to twenty-four symbols for the T24S task described in Section 4.5.2.



2. FEC way: (more complicated) - essentially translates groups of 3 binary bits to pairs of 4-level symbols using a Forward Error Correcting coding scheme for the block oriented tasks THB, TIB, TLB, RHB, and RILB described in Section 4.5.2.

4.4 Frame Structure

Figure 7 shows how an over-air message frame may be constructed from a sequence of: a Symbol Sync pattern (preamble), a Frame Sync pattern, and one or more 'Header', 'Intermediate' or 'Last' blocks.

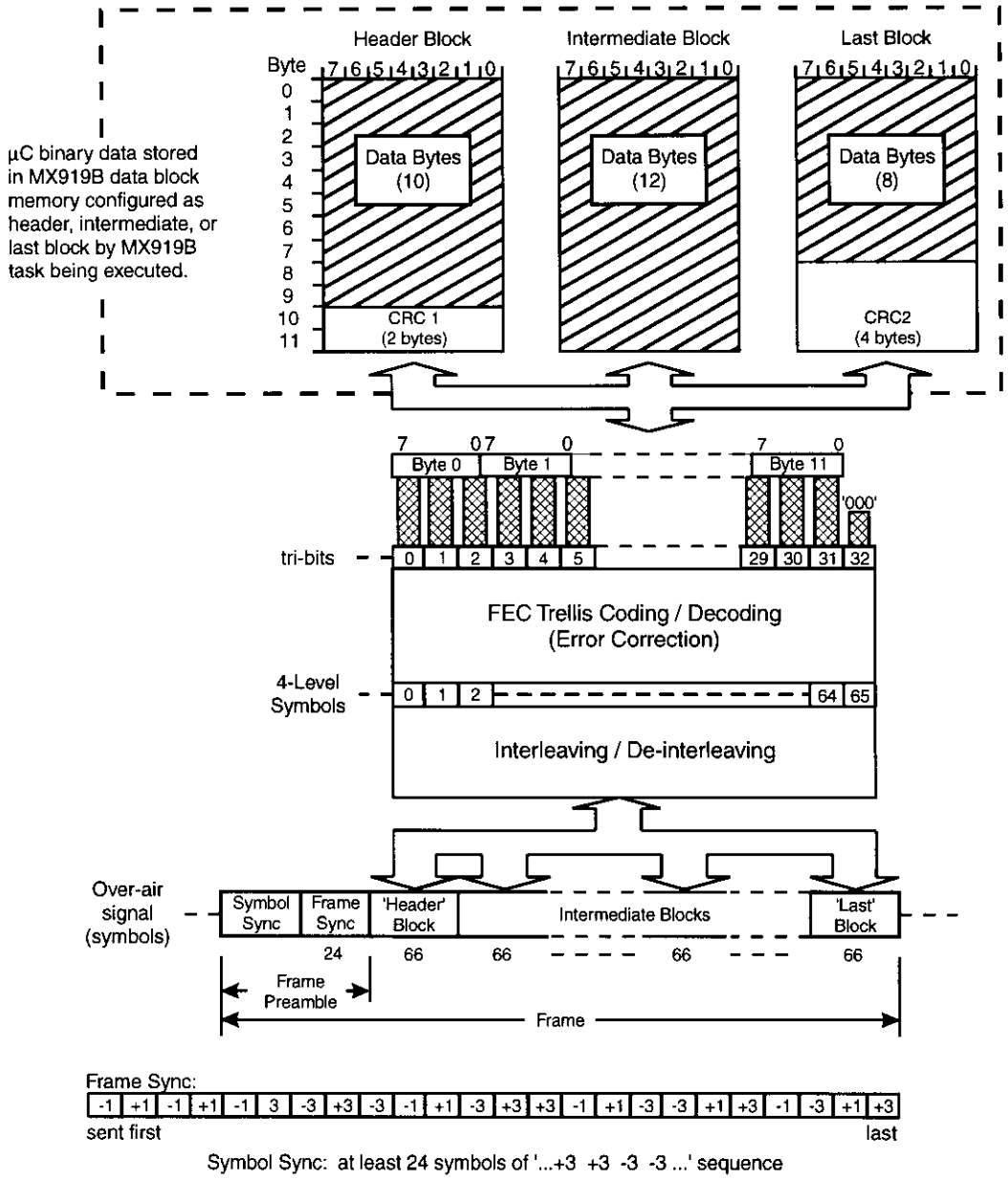


Figure 7: Over-Air Signal Format

The 'Header' block is self-contained and includes its own checksum (CRC1). It would normally carry information such as the address of the calling and called parties, the number of following blocks in the frame (if any), and miscellaneous control information. The number of following blocks (if any) is required to allow the Rx device software to expect the Last Block and interpret it as a Last Block rather than an Intermediate Block. There is no other indicator to differentiate a Last Block and an Intermediate Block.

The 'Intermediate' block(s) contain only data, the checksum for all of the data in the 'Intermediate' and 'Last' blocks (CRC2) being contained at the end of the 'Last' block.

This arrangement, while efficient in terms of data capacity, may not be optimum for poor signal-to-noise conditions, since a reception error in any one of the 'Intermediate' or 'Last' blocks would invalidate the whole frame. In such conditions, increased throughput may be obtained by using the 'Header' block format for all blocks of the frame, so blocks that are

received correctly can be identified as such, and do not need to be re-transmitted. These, and some other possible frame structures, are shown in Figure 8.

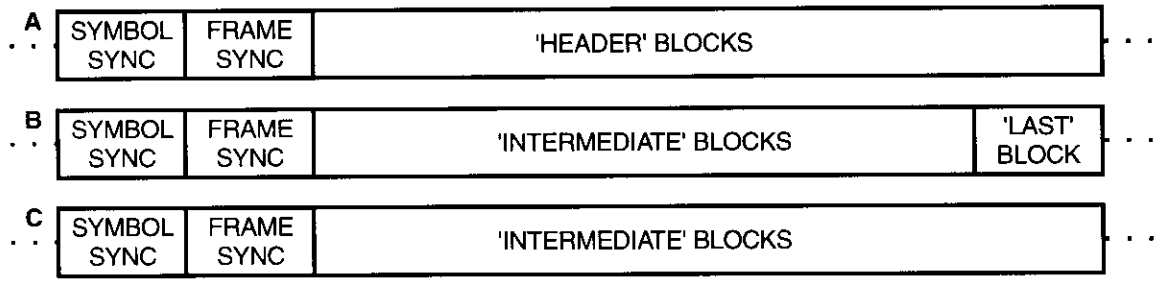


Figure 8: Alternative Frame Structures

The MX919B performs the entire block formatting and de-formatting required to convert data between µC binary form and Over-Air as shown in Figure 7.

4.5 The Programmer's View

To the programmer, the modem appears as 4 write only 8-bit registers, shadowed by 3 read only registers. The individual registers are selected by the A0 and A1 chip inputs:

A1	A0	Write to Modem	Read from Modem
0	0	Data Buffer	Data Buffer
0	1	Command Register	Status Register
1	0	Control Register	Data Quality Register
1	1	Mode Register	not used

Note: There is a minimum time allowance between accesses of the modem's registers, see Section 6.1.5.

4.5.1 Data Block Buffer

This is a 12-byte read/write buffer used to transfer data (as opposed to command, status, mode, data quality or control information) between the modem and the host µC.

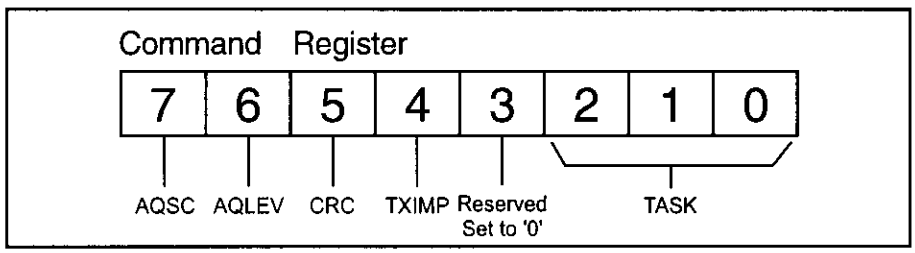
To the µC, the Data Block Buffer appears as a single 8-bit register. The modem ensures that sequential µC reads or writes to the buffer are routed to the correct locations within the buffer.

The µC should only access this buffer when the Status Register BFREE (Buffer Free) bit is '1'.

The buffer should only be written to while in Tx mode and read from while in Rx mode. Note that in receive mode, the modem will function correctly even if the received data is not read from the Data Buffer by the µC.

4.5.2 Command Register

Writing to this register tells the modem to perform a specific task as indicated by the TASK bits and modified by the AQSC, AQLEV, CRC, and TXIMP bits.



When there is no action to perform, the modem will be in an 'idle' state. If the modem is in transmit mode, the input to the Tx RRC filter will be connected to V_{BIAS}. In receive mode, the modem will continue to measure the received data quality

and extract symbols from the received signal, supplying them to the de-interleave buffer, otherwise these received symbols are ignored.

4.5.2.1 Command Register B7: AQSC - Acquire Symbol Clock

This bit has no effect in transmit mode.

In receive mode, when a byte with the AQSC bit set to '1' is written to the Command Register, and TASK is not set to RESET, it initiates an automatic sequence designed to achieve symbol timing synchronization with the received signal as quickly as possible. This involves setting the Phase Locked Loop of the received bit timing extraction circuits to its widest bandwidth, then gradually reducing the bandwidth as timing synchronization is achieved, until it reaches the 'normal' value set by the PLLBW bits of the Control Register.

Setting this bit to '0' (or changing it from '1' to '0') has no effect, however; the acquisition sequence will be re-started every time a byte written to the Command Register has the AQSC bit set to '1'.

The use of the symbol clock acquisition sequence is described in Section 5.3.

4.5.2.2 Command Register B6: AQLEV - Acquire Receive Signal Levels

This bit has no effect in transmit mode.

In receive mode, when a byte with the AQLEV bit set to '1' is written to the Command Register and TASK is not set to RESET, it initiates an automatic sequence designed to measure the amplitude and DC offset of the received signal as rapidly as possible. This sequence involves setting the measurement circuits to respond quickly at first, then gradually increasing their response time, therefore improving the measurement accuracy, until the 'normal' value set by the LEVRES bits of the Control Register is reached.

Setting this bit to '0' (or changing it from '1' to '0') has no effect, however; the acquisition sequence will be re-started every time a byte written to the Command Register has the AQLEV bit set to '1'.

The use of the level measurement acquisition sequence (AQLEV) is described in Section 5.3.

4.5.2.3 Command Register B5: CRC

This bit allows the user to select between two different initial states of the CRC1 and CRC2 checksum generators. When this bit is set to '0', the CRC generators are initialized to 'all ones' as for CCITT X25 CRC calculations. When this bit is set to '1', the CRC generators are initialized to 'all zeros'. Setting this bit to '0' provides compatibility with the MX919, a prior member of the MX919 device family. Other systems may set this bit as required. Note: This bit must be set correctly every time the Command Register is written to.

4.5.2.4 Command Register B4: TXIMP - Tx Level/Impulse Shape

This bit allows the user to choose between two transmit symbol waveform shapes as described in Section 4.7. Note: This bit must be set correctly every time the Command Register is written to.

4.5.2.5 Command Register B3 - Reserved

This bit should always be set to '0'.

4.5.2.6 Command Register B2, B1, B0: TASK

Operations such as transmitting or receiving a data block are treated by the modem as 'tasks' and are initiated when the µC writes a byte to the Command Register with the TASK bits set to anything other than the 'NULL' code.

The µC should not write a task (other than NULL or RESET) to the Command Register or write to or read from the Data Buffer when the BFREE (Buffer Free) bit of the Status Register is '0'.

Different tasks apply in receive and transmit modes.

When the modem is in transmit mode, all tasks other than NULL or RESET instruct the modem to transmit data from the Data Buffer, formatting it as required. The µC should therefore wait until the BFREE (Buffer Free) bit of the Status Register is '1', before writing the data to the Data Block Buffer, then it should write the desired task to the Command Register. If more than 1 byte needs to be written to the Data Block Buffer, byte number 0 of the block should be written first.

Once the byte containing the desired task has been written to the Command Register, the modem will:

Set the BFREE (Buffer Free) bit of the Status Register to '0'.

Take the data from the Data Block Buffer as quickly as it can - transferring it to the Interleave Buffer for eventual transmission. This operation will start immediately if the modem is 'idle' (i.e. not transmitting data from a previous task), otherwise it will be delayed until there is sufficient room in the Interleave Buffer.

Once all of the data has been transferred from the Data Block Buffer, the modem will set the BFREE and IRQ bits of the Status Register to '1', (causing the chip $\overline{IRQ}$ output to go low if the IRQEN bit of the Mode Register has been set to '1') to tell the µC that it may write new data and the next task to the modem.

This lets the µC write the next task and its associated data to the modem while the modem is still transmitting the data from its previous task.

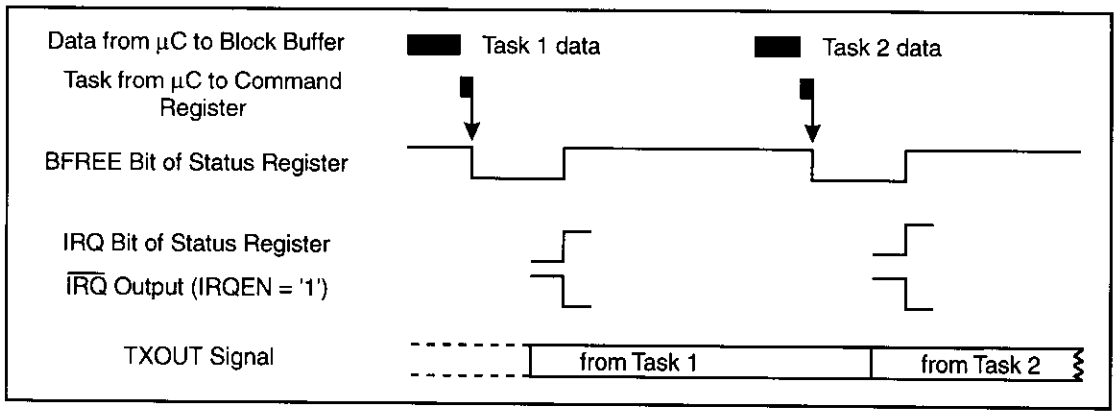


Figure 9: Transmit Task Overlapping

When the modem is in receive mode, the µC should wait until the BFREE bit of the Status Register is '1', then write the desired task to the Command Register.

Once the byte containing the desired task has been written to the Command Register, the modem will:

Set the BFREE bit of the Status Register to '0'.

Wait until enough received symbols are in the De-interleave Buffer.

Decode them as needed and transfer the resulting binary data to the Data Block Buffer

Then the modem will set the BFREE and IRQ bits of the Status Register to '1', (causing the $\overline{IRQ}$ output to go low if the IRQEN bit of the Mode Register has been set to '1') to tell the µC that it may read from the Data Block Buffer and write the next task to the modem. If more than 1 byte is contained in the buffer, byte number 0 of the data will be read out first.

In this way, the µC can read data and write a new task to the modem while the received symbols needed for this new task are being received and stored in the De-interleave Buffer.

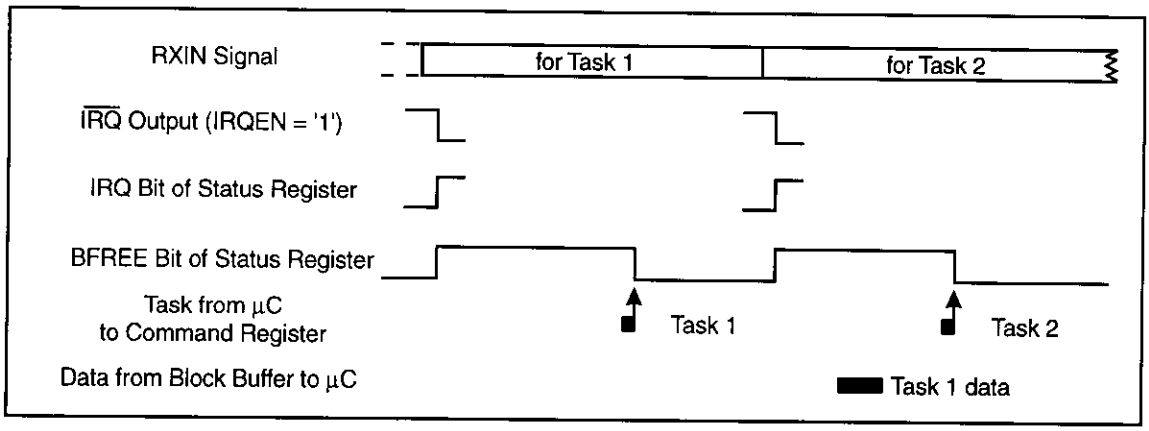


Figure 10: Receive Task Overlapping

Detailed timings for the various tasks are provide in Figure 11 and Figure 12.

MX919B Modem Tasks:

B2	B1	B0	Receive Mode		Transmit Mode	
0	0	0	NULL		NULL	
0	0	1	SFSH	Search for FS + Header	T24S	Transmit 24 symbols
0	1	0	RHB	Read Header Block	THB	Transmit Header Block
0	1	1	RILB	Read Intermediate or Last Block	TIB	Transmit Intermediate Block
1	0	0	SFS	Search for Frame Sync	TLB	Transmit Last Block
1	0	1	R4S	Read 4 symbols	T4S	Transmit 4 symbols
1	1	0	NULL		NULL	
1	1	1	RESET	Cancel any current action	RESET	Cancel any current action

4.5.2.7 NULL: No effect

This 'task' is provided so an AQSC or AQLEV command can be initiated without loading a new task.

4.5.2.8 SFSH: Search for Frame Sync plus Header Block

This task causes the modem to search the received signal for a valid 24-symbol Frame Sync sequence followed by Header Block which has a correct CRC1 checksum.

The task continues until a valid Frame Sync plus Header Block has been found.

The search consists of two stages:

First the modem will attempt to match the incoming symbols against the 24-symbol Frame Synchronization pattern to within the tolerance defined by the FSTOL bits of the Control Register.

Once a match has been found, the modem will read in the next 66 symbols as if they were a 'Header' block, decoding the symbols and checking the CRC1 checksum. If this is incorrect, the modem will resume the search, looking for a fresh Frame Sync pattern.

If the received CRC1 is correct, the 10 decoded data bytes will be placed into the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1' and the CRCERR bit cleared to '0'.

Once detecting that the BFREE bit of the Status Register has gone to '1', the µC should read the 10 bytes from the Data Block Buffer and then write the next task to the modem's Command Register.

4.5.2.9 RHB: Read Header Block

This task causes the modem to read the next 66 symbols as a 'Header' Block, decoding them, placing the resulting 10 data bytes and the 2 received CRC1 bytes into the Data Block Buffer, and setting the BFREE and IRQ bits of the Status Register to '1'. When the task is complete, it indicates that the µC may read the data from the Data Block Buffer and write the next task to the modem's Command Register.

The CRCERR bit of the Status Register will be set to '1' or '0' depending on the validity of the received CRC1 checksum bytes.

4.5.2.10 RILB: Read 'Intermediate' or 'Last' Block

This task causes the modem to read the next 66 symbols as an 'Intermediate' or 'Last' block (the µC should be able to tell from the 'Header' block how many blocks are in the frame and when to expect the 'Last' block).

In each case, it will decode the 66 symbols and place the resulting 12 bytes into the Data Block Buffer, setting the BFREE and IRQ bits of the Status Register to '1' when the task is complete.

If an 'Intermediate' block is received, then the µC should read out all 12 bytes from the Data Block Buffer and ignore the CRCERR bit of the Status Register, for a 'Last' block the µC need only read the first 8 bytes from the Data Block Buffer, and the CRCERR bit in the Status Register will reflect the validity of the received CRC2 checksum.

4.5.2.11 SFS: Search for Frame Sync

This task causes the modem to search the received signal for a 24-symbol sequence which matches the Frame Synchronization pattern to within the tolerance defined by the FSTOL bits of the Mode Register.

When a match is found the modem will set the BFREE and IRQ bits of the Status Register to '1' to indicate to the µC that it should write the next task to the Command Register.

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4.5.2.12 R4S: Read 4 Symbols

This task causes the modem to read the next 4 symbols and translate them directly (without de-interleaving or FEC) to an 8-bit byte which is placed into the Data Block Buffer. The BFREE and IRQ bits of the Status Register are then set to '1' to indicate that the µC may read the data byte from the Data Block Buffer and write the next task to the Command Register.

This task is intended for special tests and channel monitoring - perhaps preceded by a SFS task.

Note: It is possible to construct message formats, which do not rely on the block formatting of the THB, TIB, and TLB tasks. This can be accomplished by using T4S or T24S tasks to transmit and R4S to receive the user's data. One should be aware, that the receive level and timing measurement circuits need to see a reasonably 'random' distribution of all four possible symbols in the received signal to operate correctly. Accordingly, binary data may benefit from scrambling before transmission if it is not reasonably 'random' to start with.

4.5.2.13 T24S: Transmit 24 Symbols

This task, which is intended to facilitate the transmission of Symbol and Frame Sync patterns as well as special test sequences, takes 6 bytes of data from the Data Block Buffer and transmits them as 24 4-level symbols without any CRC or FEC.

Byte 0 of the Data Block Buffer is sent first, byte 5 last.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the data and command byte for the next task to the modem.

The tables below show what data needs to be written to the Data Block Buffer to transmit the MX919B Symbol and Frame Sync sequences:

'Symbol Sync' Symbols				Values written to Data Block Buffer		
					Binary	Hex
+3	+3	-3	-3	Byte 0:	11110101	F5
+3	+3	-3	-3	Byte 1:	11110101	F5
+3	+3	-3	-3	Byte 2:	11110101	F5
+3	+3	-3	-3	Byte 3:	11110101	F5
+3	+3	-3	-3	Byte 4:	11110101	F5
+3	+3	-3	-3	Byte 5:	11110101	F5

'Frame Sync' Symbols				Values written to Data Block Buffer		
					Binary	Hex
-1	+1	-1	+1	Byte 0:	00100010	22
-1	+3	-3	+3	Byte 1:	00110111	37
-3	-1	+1	-3	Byte 2:	01001001	49
+3	+3	-1	+1	Byte 3:	11110010	F2
-3	-3	+1	+3	Byte 4:	01011011	5B
-1	-3	+1	+3	Byte 5:	00011011	1B

4.5.2.14 THB: Transmit Header Block

This task takes 10 bytes of data (Address and Control) from the Data Block Buffer, calculates and appends the 2-byte CRC1 checksum, translates the result to 4-level symbols (with FEC), interleaves the symbols, and transmits the result as a formatted 'Header' Block.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

4.5.2.15 TIB: Transmit Intermediate Block

This task takes 12 bytes of data from the Data Block Buffer, updates the 4-byte CRC2 checksum for inclusion in the 'Last' block, translates the 12 data bytes to 4-level symbols (with FEC), interleaves the symbols, and transmits the result as a formatted 'Intermediate' Block.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

4.5.2.16 TLB: Transmit Last Block

This task takes 8 bytes of data from the Data Block Buffer, updates and appends the 4-byte CRC2 checksum, translates the resulting 12 bytes to 4-level symbols (with FEC), interleaves the symbols, and transmits the result as a formatted 'Last' Block.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

4.5.2.17 T4S: Transmit 4 Symbols

This command is similar to T24S but takes only one byte from the Data Block Buffer, transmitting it as four 4-level symbols.

4.5.2.18 RESET: Stop any current action

This 'task' takes effect immediately, and terminates any current action (task, AQSC or AQLEV) the modem may be performing and sets the BFREE bit of the Status Register to '1', without setting the IRQ bit. It should be used when V_{DD} is applied, to set the modem into a known state.

Note: Due to delays in the transmit filter, it will take several symbol times for any change to appear at the TXOUT pin.

4.5.2.19 Task Timing

The following table and figures describe the duration of tasks and timing sequences for Tx and Rx operation.

		Task	Time (symbol times)
t_1	Modem in idle state. Time from writing first task to application of first transmit bit to Tx RRC filter	Any	1 to 2
t_2	Time from application of first symbol of the task to the Tx RRC filter until BFREE goes to a logic '1'	T24S THB/TIB/TLB T4S	5 16 0
t_3	Time to transmit all symbols of the task	T24S THB/TIB/TLB T4S	24 66 4
t_4	Max time allowed from BFREE going to a logic '1' (high) for next task (and data) to be written to modem	T24S THB/TIB/TLB T4S	18 49 3
t_5	Time to receive all symbols of task	SFS SFSH RHB/RILB R4S	24 (minimum) 90 (minimum) 66 4
t_6	Maximum time between first symbol of task entering the de-interleave circuit and the task being written to modem	SFS SFSH RHB/RILB R4S	21 21 49 3
t_7	Maximum time from the last bit of the task entering the de interleave circuit to BFREE going to a logic '1' (high)	Any	1

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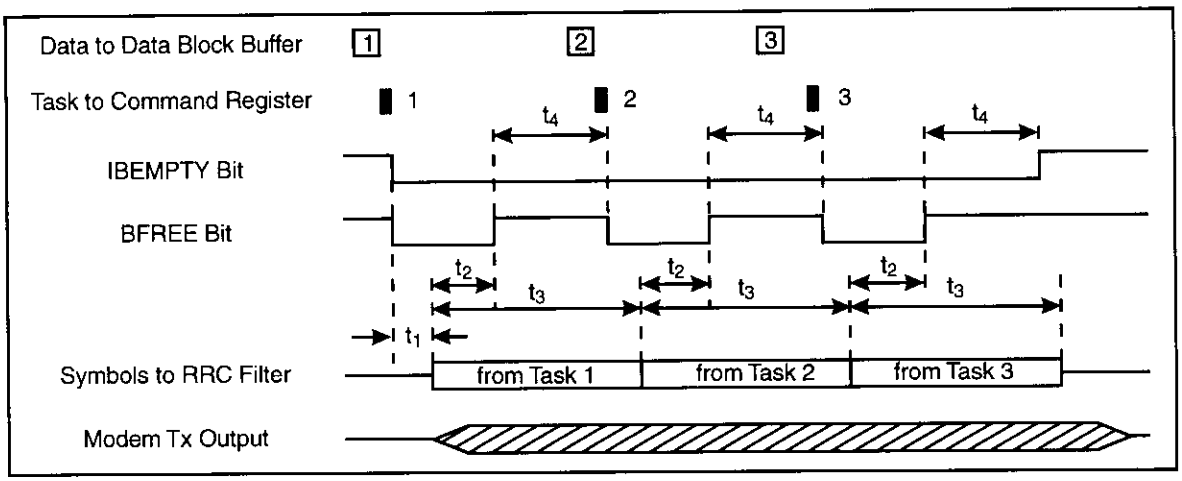


Figure 11: Transmit Task Timing Diagram

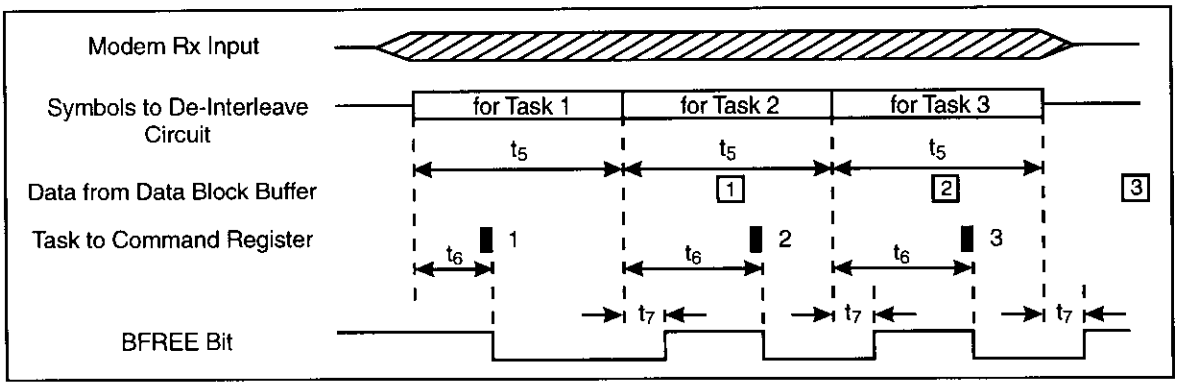


Figure 12: Receive Task Timing Diagram

4.5.2.20 RRC Filter Delay

The previous task timing figures are based on the signal at the input to the RRC filter (in transmit mode) or the input to the de-interleave buffer (in receive mode). There is an additional delay of about 8 symbol times through to the RRC filter in both transmit and receive modes, as illustrated below:

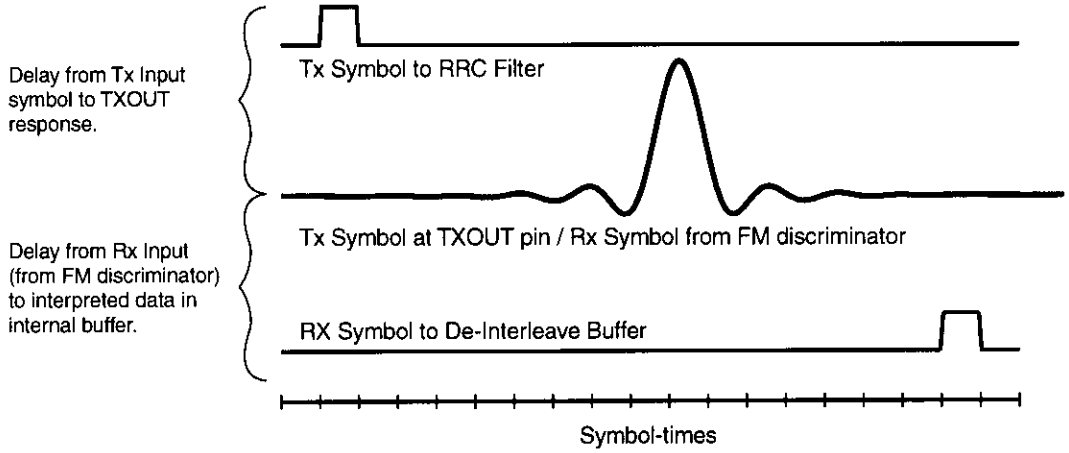
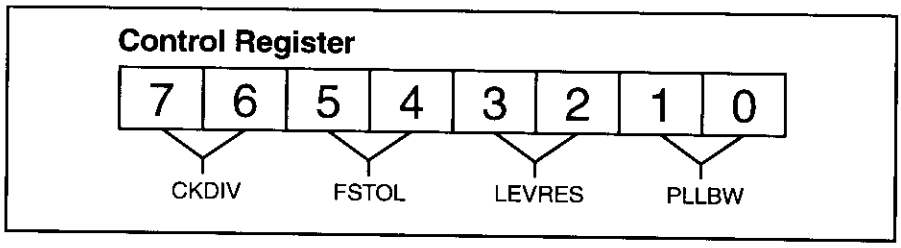


Figure 13: RRC Low Pass Filter Delay

4.5.3 Control Register

This 8-bit write-only register controls the modem's symbol rate, the response times of the receive clock extraction, signal level measurement circuits, and the Frame Sync pattern recognition tolerance to inexact matches.



4.5.3.1 Control Register B7, B6: CKDIV - Clock Division Ratio

These bits control a frequency divider driven from the clock signal present at the $\overline{XTAL}$ pin, therefore determining the nominal symbol rate. Because each symbol represents two bits, bit rates are 2x the symbol rates. The table below shows how symbol rates of 2400/4800/9600 symbols/sec (4800/9600/19200bps) may be obtained from common Xtal frequencies:

			Xtal Frequency (MHz)		
			2.4576	4.9152	9.8304
B7	B6	Division Ratio: Xtal Frequency/Symbol Rate	Symbol Rate (symbols/sec) / Bit Rate (bps)		
0	0	512	4800/9600	9600/19200	
0	1	1024	2400/4800	4800/9600	9600/19200
1	0	2048		2400/4800	4800/9600
1	1	4096			2400/4800

Note: Device operation is not guaranteed below 2400 symbols/sec (4800bps) or above 9600 symbols/sec (19200bps).

4.5.3.2 Control Register B5, B4: FSTOL - Frame Sync Tolerance to Inexact Matches

These two bits have no effect in transmit mode. In receive mode, they define the maximum number of mismatches allowed during a search for the Frame Sync pattern:

B5	B4	Mismatches allowed
0	0	0
0	1	2
1	0	4
1	1	6

Note: A single 'mismatch' is defined as the difference between two adjacent symbol levels, thus if the symbol '+1' were expected, then received symbol values of '+3' and '-1' would count as 1 mismatch, a received symbol value of '-3' would count as 2 mismatches. A setting of '4 mismatches' is recommended for normal use.

4.5.3.3 Control Register B3, B2: LEVRES - Level Measurement Modes

These two bits have no effect in transmit mode. In receive mode they set the 'normal' or 'steady state' operating mode of the Rx signal amplitude and DC offset measuring and tracking circuits. These circuits analyze the Rx signal envelope and charge the DOC1 and DOC2 capacitors to 'store' signal maximum and minimum references that are used in the data reception process. This setting is temporarily overridden during the automatic sequencing triggered by an AQLEV command when level is initially being acquired as described in Section 5.3.

B3	B2	Mode
0	0	Hold
0	1	Level Track

1	0	Lossy Peak Detect
1	1	Slow Peak Detect

In normal use the LEVRES bits should be set to '0 1' (Level Track). The other modes are intended for special purposes, for device testing, or are invoked automatically during an AQLEV sequence.

In 'Slow Peak Detect' modes, the positive and negative excursions of the received signal (after filtering) are measured by peak rectifiers driving the DOC1 and DOC2 capacitors to establish the amplitude of the signal and any DC offset with regards to V_{BIAS}. This mode provides good overall performance, particularly when acquiring level information at the start of a received message, but does not work as well with certain long sequences of repeated data byte values. It is also susceptible to large amplitude noise spikes, which can be caused by deep fades.

The 'Lossy Peak Detect' mode is similar to 'Slow Peak Detect' but the capacitor discharge time constant is much shorter so this mode is not suitable for normal data reception and is only used within part of the automatic AQLEV acquisition sequence.

In 'Level Track' mode the DOC capacitor voltages are slowly adjusted by the MX919B in such a way as to minimize the average errors seen in the received signal. This mode provides the best overall performance, being much more accurate than 'Slow Peak Detect' when receiving large amplitude noise spikes on long sequences of repeated data byte values. It does, however, depend on the measured levels and timing being approximately correct. If either of these is significantly wrong then the correction algorithm used by the 'Level Track' mode can actually drive the voltages on the DOC capacitors away from their optimum levels. For this reason, the automatic AQLEV acquisition sequence (see Section 5.3) forces the level measuring circuits into 'Slow Peak Detect' mode until a Frame Sync pattern has been found.

4.5.3.4 Control Register B1, B0: PLLBW - Phase-Locked Loop Bandwidth Modes

These two bits have no effect in transmit mode. In receive mode, they set the 'normal' or 'steady state' bandwidth of the Rx clock extraction Phase Locked Loop circuit. The PLL circuit synchronizes itself with the Rx Signal to develop a local clock signal used in the data clock recovery process. This setting will be temporarily overridden during the automatic sequencing of an AQSC command when Rx clock extraction circuits are initially being trained as described in Section 5.3.

B1	B0	PLL Mode
0	0	Hold
0	1	Narrow Bandwidth
1	0	Medium Bandwidth
1	1	Wide Bandwidth

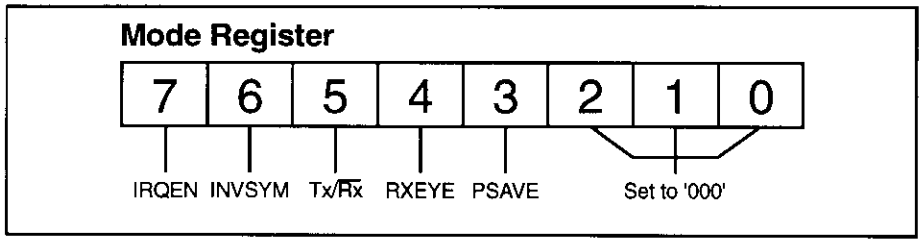
The normal setting for the PLLBW bits should be 'Medium Bandwidth' when the received symbol rate and the frequency of the receiving modem's crystal are both within ±100ppm of nominal, except at the start of a symbol clock acquisition sequence (AQSC) when 'Wide Bandwidth' should be selected as described in Section 5.3

If the received symbol rate and the crystal frequency are both within ±20ppm of nominal then selection of the 'Narrow Bandwidth' setting will provide better performance especially through fades or noise bursts which may otherwise pull the PLL away from its optimum timing. In this case however; it is recommended that the PLLBW bits only be set to 'Narrow Bandwidth' after the modem has been running in 'Medium Bandwidth' mode for about 200 symbol times to ensure accurate lock has first been achieved.

The 'Hold' setting disables the feedback loop of the PLL which continues to run at a rate determined only by the actual crystal frequency and the setting of the Control Register CKDIV bits, not the PLL's operating frequency immediately prior to the 'Hold' setting.

4.5.4 Mode Register

The contents of this 8-bit write only register control the basic operating modes of the modem:



4.5.4.1 Mode Register B7: IRQEN - $\overline{IRQ}$ Output Enable

When this bit is set to '1', the $\overline{IRQ}$ chip output pin is pulled low (V_{SS}) given the IRQ bit of the Status Register is a '1'.

4.5.4.2 Mode Register B6: INVSYM - Invert Symbols

This bit controls the polarity of the transmitted and received symbol voltages.

B6	Symbol	Signal at TXOUT	Signal at RXAMPOUT
0	'+3'	Above V_{BIAS}	Below V_{BIAS}
	'-3'	Below V_{BIAS}	Above V_{BIAS}
1	'+3'	Below V_{BIAS}	Above V_{BIAS}
	'-3'	Above V_{BIAS}	Below V_{BIAS}

Note: B6 must be normally set to the same value in Tx and Rx devices for successful operation.

4.5.4.3 Mode Register B5: TX/$\overline{RX}$ - Tx/Rx Mode

Setting this bit to '1' places the modem into the Transmit mode, clearing it to '0' puts the modem into the Receive mode.

Note: Changing between receive and transmit modes will cancel any current task.

4.5.4.4 Mode Register B4: RXEYE - Show Rx Eye

This bit should normally be set to '0'. Setting it to '1' when the modem is in receive mode configures the modem for a special test mode, in which the input of the Tx output buffer is connected to the Rx Symbol/Clock extraction circuit at a point which carries the equalized receive signal. This may be monitored with an oscilloscope (at the TXOUT pin itself), to assess the quality of the complete radio channel including the Tx and Rx modem filters, the Tx modulator and the Rx IF filters, and FM demodulator.

This mode is provided because observation of the direct discriminator output of a root raised cosine Tx filtered signal (before Rx equalization) is not very recognizable so it is generally not useful.

The resulting eye diagram (for reasonably random data) should ideally be as shown in the following Figure 14, with 4 distinct and equally spaced level crossing points.

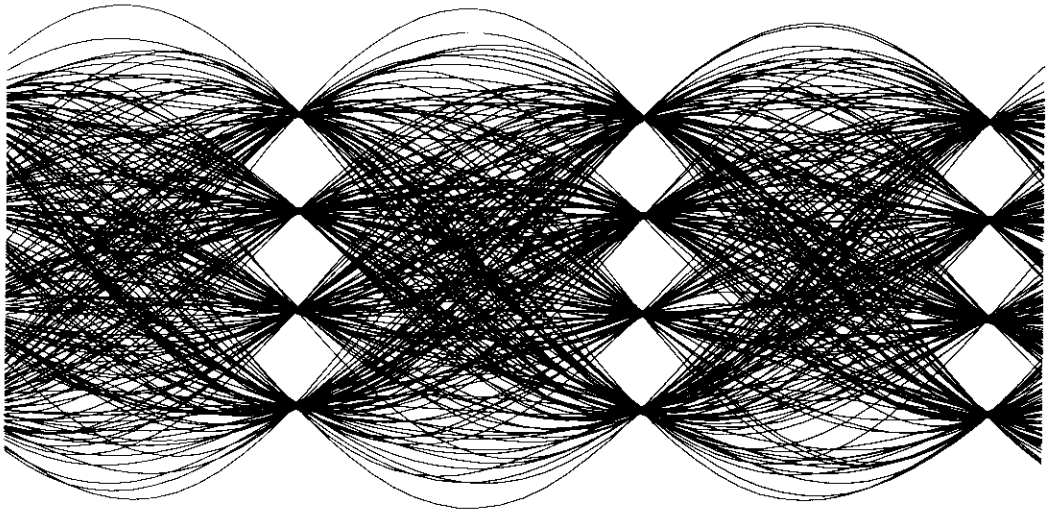


Figure 14: Ideal 'RXEYE' Signal

4.5.4.5 Mode Register B3: PSAVE - Powersave

When this bit is a '1', the modem will be in a 'powersave' mode in which the internal filters, the Rx Symbol and Clock extraction circuits, and the Tx output buffer will be disabled. The TXOUT pin will be connected to V_{BIAS} through a high value internal resistance. The Xtal clock oscillator, Rx input amplifier and the µC interface logic will continue to operate.

Setting the PSAVE bit to '0' restores power to all of the chip circuitry.

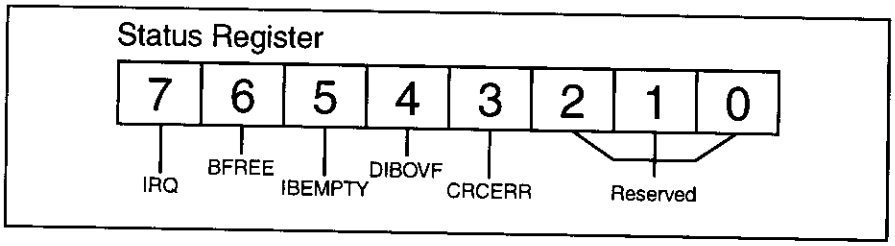
Note: The internal filters, and therefore the TXOUT pin in transmit mode, will take approximately 20 symbol-times to settle after the PSAVE bit has gone from '1' to '0'.

4.5.4.6 Mode Register B2, B1, B0

These bits should be set to '000'.

4.5.5 Status Register

This register may be read by the µC to determine the current state of the modem.



4.5.5.1 Status Register B7: IRQ - Interrupt Request

This bit is set to '1' by:

The Status Register BFREE bit going from '0' to '1', unless this is caused by a RESET task or by a change to the Mode Register TX/$\overline{RX}$ or PSAVE bits

or The Status Register IBEMPTY bit going from '0' to '1', unless this is caused by a RESET task or by changing the Mode Register TX/$\overline{RX}$ or PSAVE bits.

or The Status Register DIBOVF bit going from '0' to '1'.

The IRQ bit is cleared to '0' immediately after a read of the Status Register.

If the IRQEN bit of the Mode Register is '1', then the chip $\overline{IRQ}$ output will be pulled low (V_{SS}) when the IRQ bit is set to '1', and will go high impedance when the Status Register is read.

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4.5.5.2 Status Register B6: BFREE - Data Block Buffer Free

This bit reflects the availability of the Data Block Buffer and is cleared to '0' when a task other than NULL or RESET is written to the Command Register.

In transmit mode, the BFREE bit will be set to '1' (also setting the Status Register IRQ bit to '1') by the modem when the modem is ready for the µC to write new data to the Data Block Buffer and the next task to the Command Register.

In receive mode, the BFREE bit is set to '1' (also setting the Status Register IRQ bit to '1') by the modem when it has completed a task and any data associated with that task has been placed into the Data Block Buffer. The µC may then read that data and write the next task to the Command Register.

The BFREE bit is also set to '1' - but without setting the IRQ bit - by a RESET task or when the Mode Register TX/$\overline{RX}$ or PSAVE bits are changed.

4.5.5.3 Status Register B5: IBEMPTY - Interleave Buffer Empty

In transmit mode, this bit will be set to '1' - also setting the IRQ bit - when less than two symbols remain in the Interleave Buffer. Any transmit task written to the modem after this bit goes to '1' will be too late to avoid a gap in the transmit output signal.

The bit is also set to '1' by a RESET task or by a change of the Mode Register TX/$\overline{RX}$ or PSAVE bits, but in these cases the IRQ bit will not be set.

The bit is cleared to '0' within one symbol time after a task other than NULL or RESET is written to the Command Register.

Note: When the modem is in transmit mode and the Interleave Buffer is empty, a mid-level (halfway between '+1' and '-1') signal will be sent to the RRC filter.

In receive mode this bit will be '0'.

4.5.5.4 Status Register B4: DIBOVF - De-Interleave Buffer Overflow

In receive mode this bit will be set to '1' - also setting the IRQ bit - when a RHB, RILB or R4S task is written to the Command Register too late to allow continuous reception.

The bit is cleared to '0' immediately after reading the Status Register, by writing a RESET task to the Command Register or by changing the TX/$\overline{RX}$ or PSAVE bits of the Mode Register.

In transmit mode this bit will be '0'.

4.5.5.5 Status Register B3: CRCERR - CRC Checksum Error

In receive mode, this bit will be updated at the end of a SFSH, RHB or RILB task to reflect the result of the receive CRC check. '0' indicates that the CRC was received correctly, '1' indicates an error.

Note: This bit should be ignored when an 'Intermediate' block (which does not have an integral CRC) is received.

The bit is cleared to '0' by a RESET task or by changing the TX/$\overline{RX}$, or PSAVE bits of the Mode Register. In transmit mode this bit is '0'.

4.5.5.6 Status Register B2, B1, B0

These bits are reserved for future use.

4.5.6 Data Quality Register

In receive mode, the MX919B continually measures the 'quality' of the received signal, by comparing the actual received waveform over the previous 64 symbol times against an internally generated 'ideal' 4-level FSK baseband signal.

The result is placed into bits 3-7 of the Data Quality Register for the µC to read at any time, bits 0-2 being always set to '0'. Figure 15 shows how the value (0-255) read from the Data Quality Register varies with received signal-to-noise ratio:

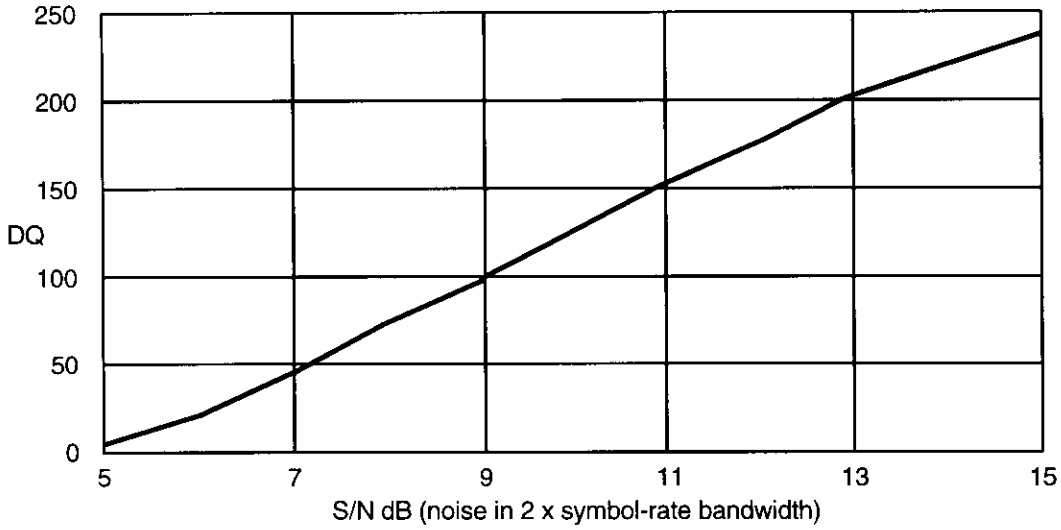

Figure 15: Typical Data Quality Reading vs S/N

The Data Quality readings are only valid when the modem has successfully acquired signal level and timing lock for at least 64 symbol times. It is invalid when an AQSC or AQLEV sequence is being performed or when the LEVRES setting is 'Lossy Peak Detect'. A low reading will be obtained if the PLLBW bits are set to 'Wide' or if the received signal waveform is distorted in any significant way.

Section 5.6 describes how monitoring the Data Quality reading can help improve the overall system performance in some applications.

4.6 CRC, FEC and Interleaving

4.6.1 Cyclic Redundancy Codes

4.6.1.1 CRC1

This is a sixteen-bit CRC check code contained in bytes 10 and 11 of the Header Block, which provides error detection coverage for the Header Block of a message. It is calculated by the modem from the first 80 bits of the Header Block (Bytes 0 to 9 inclusive) using the generator polynomial:

$$x^{16} + x^{12} + x^5 + 1$$

4.6.1.2 CRC2

This is a thirty-two-bit CRC check code contained in bytes 8 to 11 of the 'Last' Block, which provides error detection coverage for the combined Intermediate Blocks and Last Block of a message. It is calculated by the modem from all of the data and pad bytes in the Intermediate Blocks and in the first 8 bytes of the Last Block using the generator polynomial:

$$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x^1 + 1$$

Note: In receive mode the CRC2 checksum circuits are initialized on completion of any task other than NULL or RILB. In transmit mode the CRC2 checksum circuits are initialized on completion of any task other than NULL, TIB, or TLB.

Command Register bit B5 (CRC) allows the user to select between two different forms of the CRC1 and CRC2 checksums. When this bit is set to '0', the CRC generators are initialized to 'all ones' for calculations such as CCITT X25 CRC. When this bit is set to '1', the CRC generators are initialized to 'all zeros'.

4.6.1.3 Forward Error Correction

In transmit mode, the MX919B uses a Trellis Encoder to translate the 96 bits (12 bytes) of a 'Header', 'Intermediate' or 'Last' Block into a 66-symbol (132 bits) sequence which includes FEC information.

In receive mode, the MX919B decodes the received 66 symbols of a block into 96 bits of binary data using a 'Soft Decision' Viterbi algorithm to perform decoding and error correction.

4.6.1.4 Interleaving

The 66 symbols of a 'Header', 'Intermediate' or 'Last' block are interleaved by the modem before transmission to provide protection against the effects of noise bursts and short fades.

In receive mode, the MX919B de-interleaves the received symbols prior to decoding.

4.7 Transmitted Symbol Shape

Bit 4 of the Command Register (TXIMP) selects the transmit baseband signal and the receive signal equalization as follows:

If the TXIMP bit is '0', then the transmit baseband signal is generated by feeding full-symbol-time-width 4-level symbols into the RRC lowpass filter. The receive signal equalization is optimized for this type of signal. With this setting, the MX919B is compatible with the MX919A devices, another member of the MX919 device family.

If the TXIMP bit is set to '1,' impulses, rather than full-symbol-time-width symbols are fed into the RRC filter when in TX mode, and the receive signal equalization is suitably adjusted in RX mode.

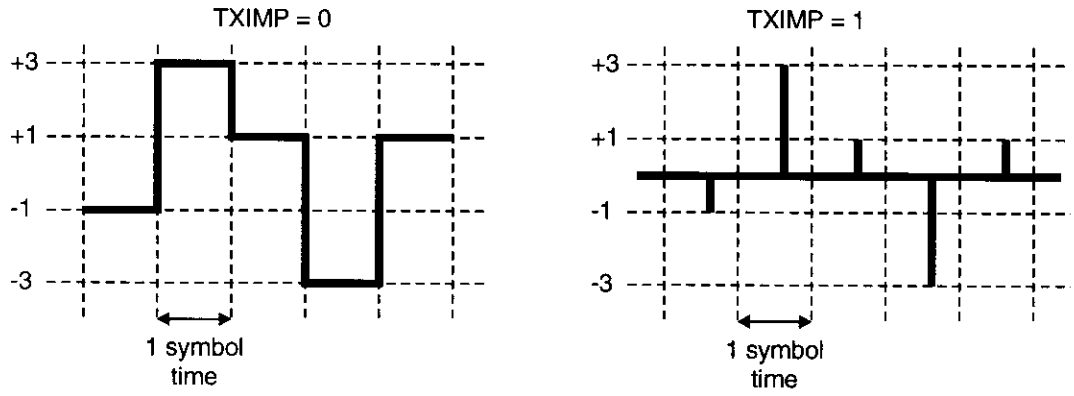

Figure 16: Input Signal to RRC Filter in Tx Mode for TXIMP = 0 and 1

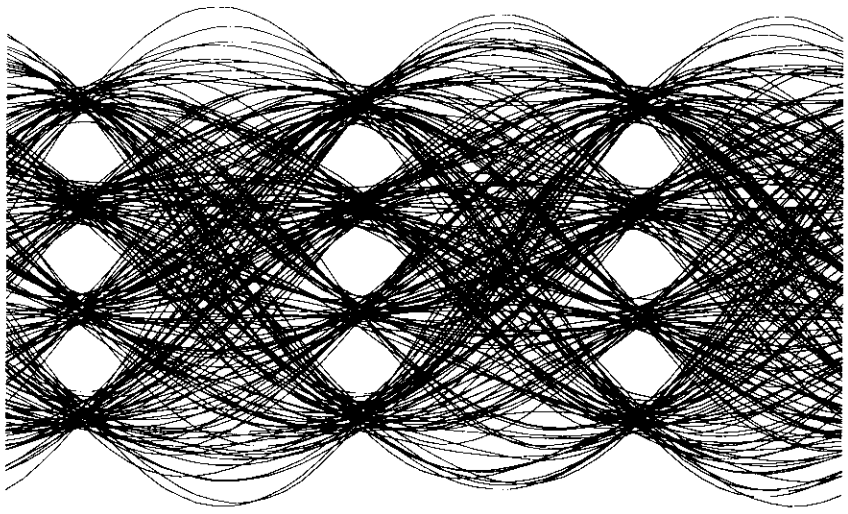

Figure 17: Tx Signal Eye TXIMP = 0

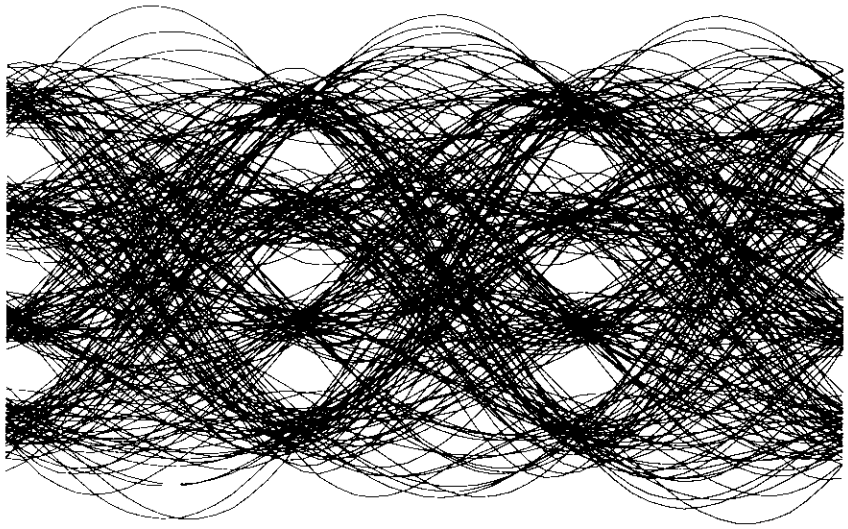

Figure 18: Tx Signal Eye TXIMP = 1

Note: Setting TXIMP to '1' affects the Tx output signal level as shown in Section 6.1.3 and the table below.

	TXIMP = 0	TXIMP = 1
Nominal Voltage difference between continuous '+3' and continuous '-3' symbol outputs.	$0.157V_{DD}$	$0.157V_{DD}$
Nominal V_{P-P} for continuous '+3 +3 -3 -3..." symbol pattern.	$0.20V_{DD}$	$0.22V_{DD}$

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5 Application

5.1 Transmit Frame Example

The operations needed to transmit a single Frame consisting of Symbol and Frame Sync sequences, and one each Header, Intermediate and Last blocks are provided below:

1. Ensure that the Control Register has been loaded with a suitable CKDIV value, that the IRQEN and TX/$\overline{RX}$ bits of the Mode Register are '1', the RXEYE and PSAVE bits are '0', and the INVSYM bit is set appropriately.
2. Read the Status Register to ensure that the BFREE bit is '1', then write 6 Symbol Sync bytes (a preamble) to the Data Block Buffer and a T24S task to the Command Register.
3. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
4. Write 6 byte Frame Sync to the Data Block Buffer and a T24S task to the Command Register.
5. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
6. Write 10 Header Block bytes to the Data Block Buffer and a THB task to the Command Register.
7. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
8. Write 12 Intermediate Block bytes to the Data Block Buffer and a TIB task to the Command Register.
9. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
10. Write 8 Last Block bytes to the Data Block Buffer and a TLB task to the Command Register.
11. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
12. Wait for another interrupt from the modem, read the Status Register; the IRQ, BFREE and IBEMPTY bits should be '1'.

Note: The final symbol of the frame will start to appear approximately 2 symbol times after the Status Register IBEMPTY bit goes to '1'; a further 16 symbol times should be allowed for the symbol to pass completely through the RRC filter.

Figure 19 and Figure 20 illustrate the host µC routines needed to send a single Frame consisting of Symbol and Frame Sync patterns, a Header block, and any number of Intermediate blocks and one Last Block. It is assumed that the Tx Interrupt Service Routine Figure 20 is called when the MX919B $\overline{IRQ}$ output line goes low.

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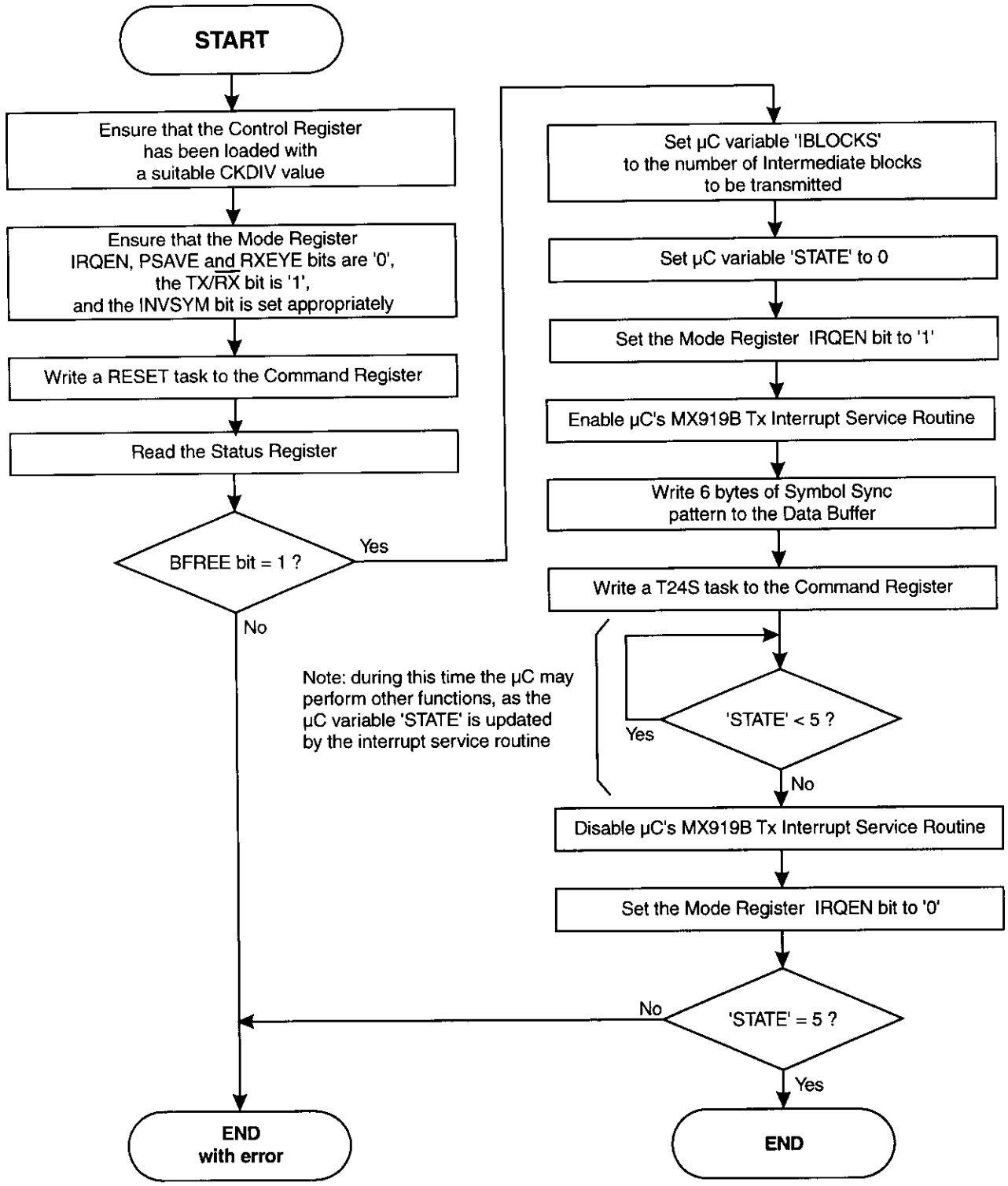

Figure 19: Transmit Frame Example Flowchart, Main Program

Notes

1. The RESET command in Figure 19 and the practice of disabling the MX919B's $\overline{IRQ}$ output when not needed are not essential but can eliminate problems during debugging and if errors occur in operation
2. The CRC and TXIMP bits should be set appropriately every time a byte is written to the Command Register.

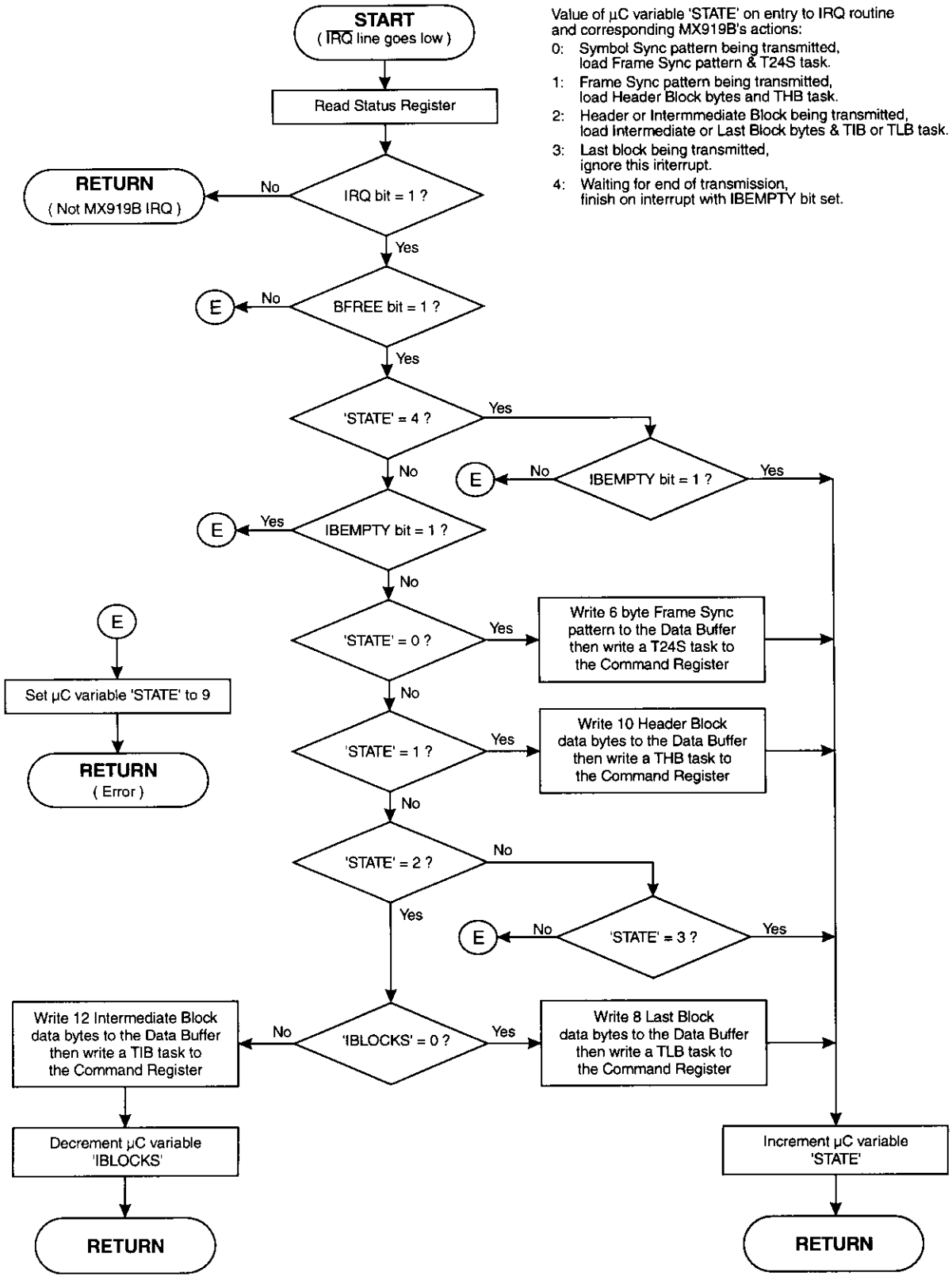

Figure 20: Tx Interrupt Service Routine

5.2 Receive Frame Example

The operations needed to receive a single Frame consisting of Symbol and Frame Sync sequences and one each Header, Intermediate and Last blocks are shown below;

1. Ensure that the Control Register has been loaded with suitable CKDIV, FSTOL, LEVRES and PLLBW values, and that the IRQEN bit of the Mode Register is '1', the TX/$\overline{RX}$ PSAVE, and RXEYE bits are '0', and the INVSYM bit is set appropriately.
2. Wait until the received carrier has been present for at least 8 symbol times (see Section 5.3).
3. Read the Status Register to ensure that the BFREE bit is '1'.
4. Write a byte containing a SFSH task and with the AQSC and AQLEV bits set to '1' to the Command Register.
5. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the CRCERR and DIBOVF bits should be '0'.
6. Check that the CRCERR bit of the Status Register is '0' and read 10 Header Block bytes from the Data Block Buffer.
7. Write a RILB task to the Command Register.
8. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the DIBOVF bit '0'.
9. Read 12 Intermediate Block bytes from the Data Block Buffer.
10. Write a RILB task to the Command Register.
11. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the DIBOVF bit '0'.
12. Check that the CRCERR bit of the Status Register is '0' and read the 8 Last Block bytes from Data Buffer.

Figure 21 and Figure 22 illustrate the host µC routines needed to receive a single Frame consisting of Symbol and Frame Sync patterns, a Header Block, any number of Intermediate blocks and one Last block. It is assumed that the Rx Interrupt Service Routine Figure 22 is called when the MX919B's $\overline{IRQ}$ output goes low.

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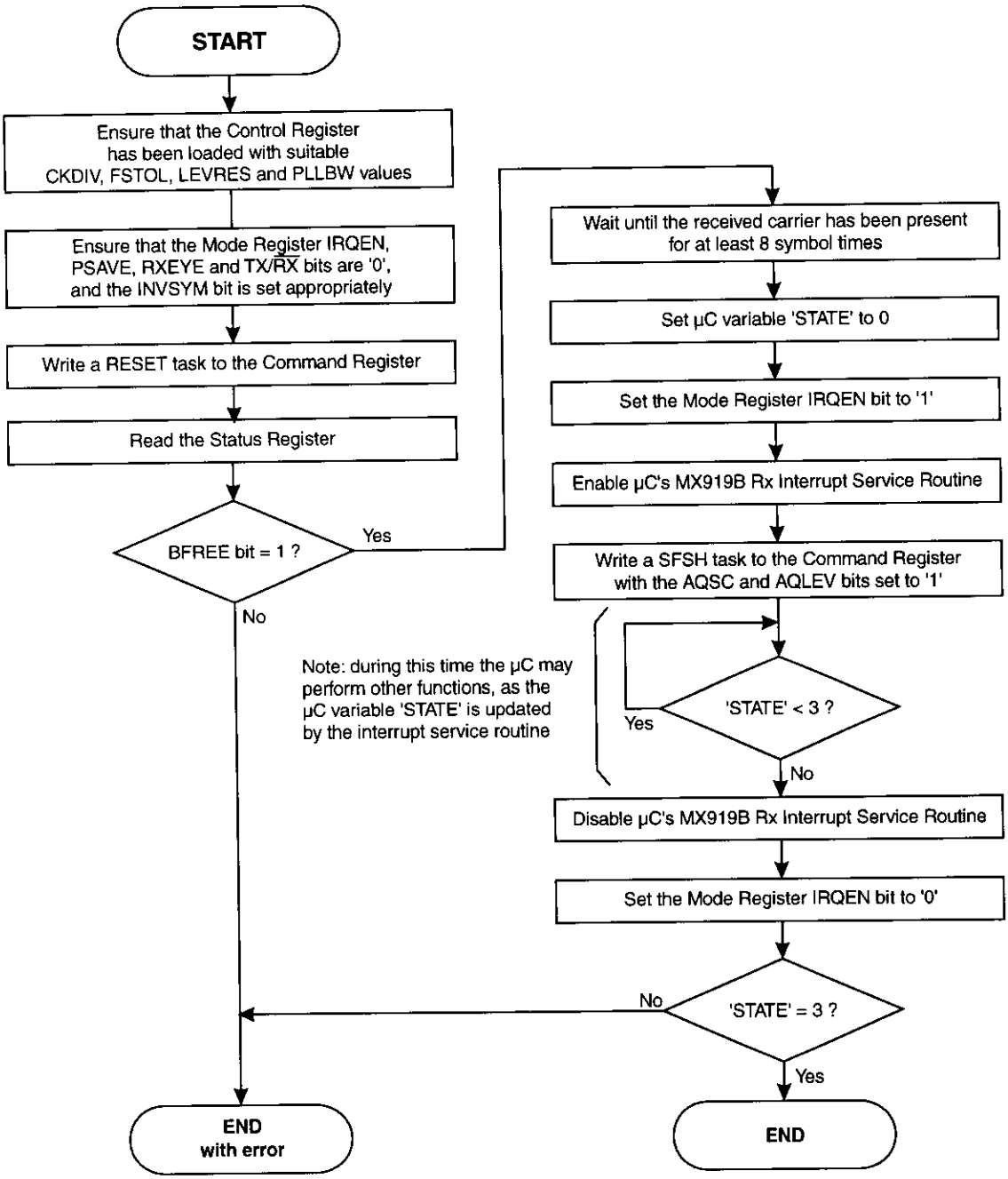

Figure 21: Receive Frame Example Flowchart, Main Program

Notes

1. The RESET command in Figure 21 and the practice of disabling the MX919B's $\overline{IRQ}$ output when not needed are not essential but can eliminate problems during debugging and if errors occur in operation.
2. The CRC and TXIMP bits should be set appropriately every time a byte is written to the Command Register.

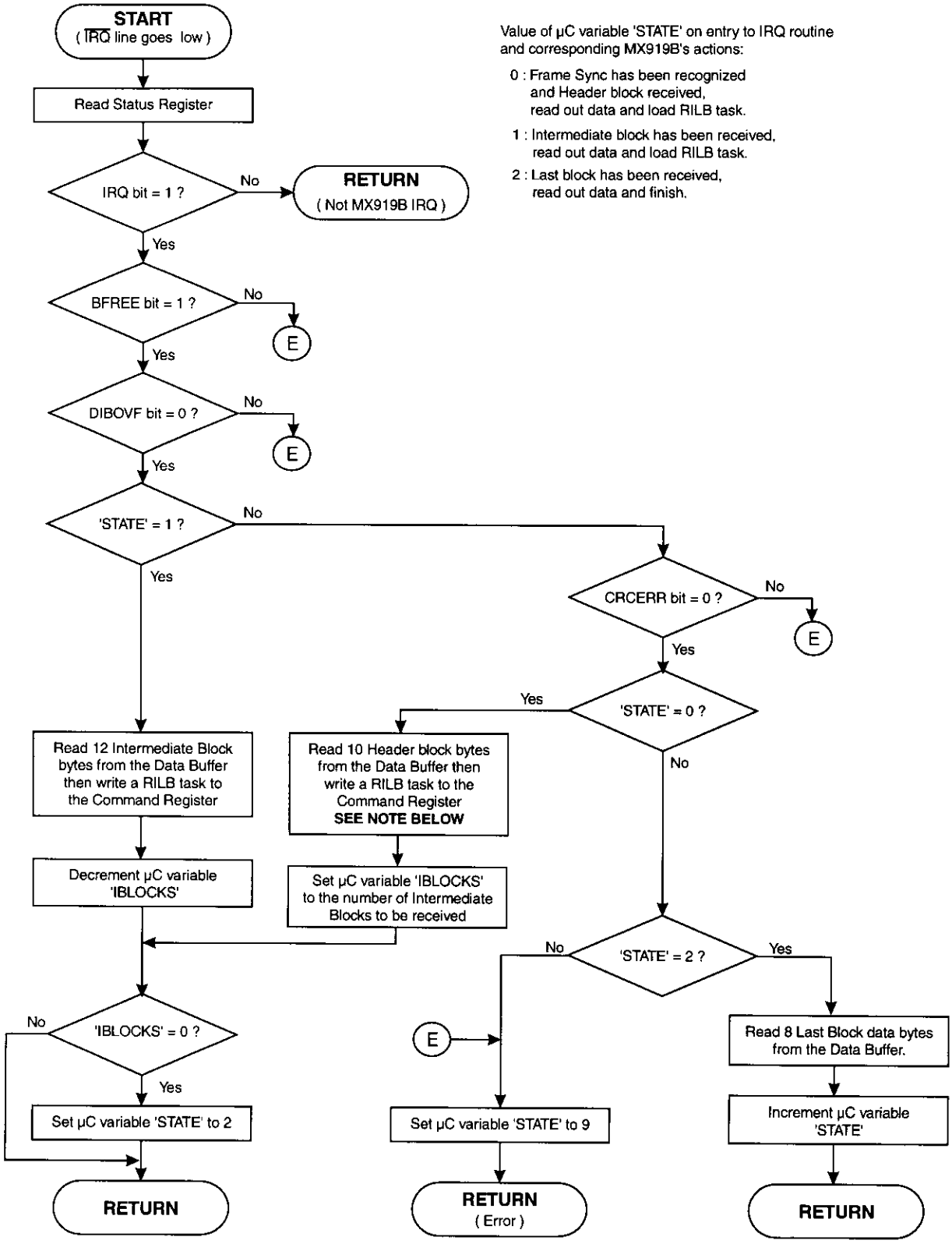

Figure 22: Rx Interrupt Service routine

Note: This routine assumes that the number of Intermediate blocks in the Frame is contained within the Header Block Data.

5.3.4 Automatic Acquisition Functions

Setting the AQSC and AQLEV bits to '1' triggers the modem's automatic Symbol Clock Extraction and Level Measurement acquisition sequences, which are designed to measure the received symbol timing, amplitude, and DC offset as quickly as possible before switching to accurate - but slower - measurement modes. These acquisition sequences act very quickly if triggered at the start of a received Symbol Sync pattern (as shown in Figure 23), but will still function correctly, although more slowly, if started any time during a normal Frame as when the receiver is switched onto a channel where the transmitter is operating continuously.

The automatic AQLEV Level Measurement acquisition sequence starts with the level measurement circuits being put into 'Clamp' Mode for one symbol time to quickly set the voltages on the DOC pins to approximately correct levels. The level measurement circuits are then automatically set to 'Lossy Peak Detect' mode for 15 symbol times, then 'Slow Peak Detect' until a received Frame Sync pattern is recognized, after which the automatic sequence ends and the level measurement circuit mode reverts to the mode set by the LEVRES bits of the Control Register (normally 'Level Track').

The peak detectors used in both 'Slow' and 'Lossy Peak Detect' modes include additional low pass filtering of the received signal which greatly reduces the effect of pattern noise on the reference voltages held on the external DOC capacitors, but means that pairs of '+3' (and '-3') symbols need to be received to establish the correct levels. Two pairs of '+3' and two pairs of '-3' symbols received after the start of an AQLEV sequence are sufficient to correctly set the levels on the DOC capacitors.

The automatic AQSC Symbol Clock acquisition sequence sets the PLL to 'Extra Wide Bandwidth' mode for 16 symbol times (this mode is not one of those which can be selected by the Control Register PLLBW bits) then changes to 'Wide' bandwidth. After 45 symbol times, the PLL mode will revert to that set by the Control Register PLLBW bits.

5.4 AC Coupling

For a practical circuit, ac coupling between the modem's transmit output to the frequency modulator and between the receiver's frequency discriminator and the receive input of the modem may be desired. There are, however, two issues which deserve consideration:

1. AC coupling of the signal degrades the Bit Error Rate performance of the modem. The following graph illustrates the typical bit error rates at 4800 symbols/sec (9600bps) without FEC for reasonably random data with differing degrees of AC coupling:

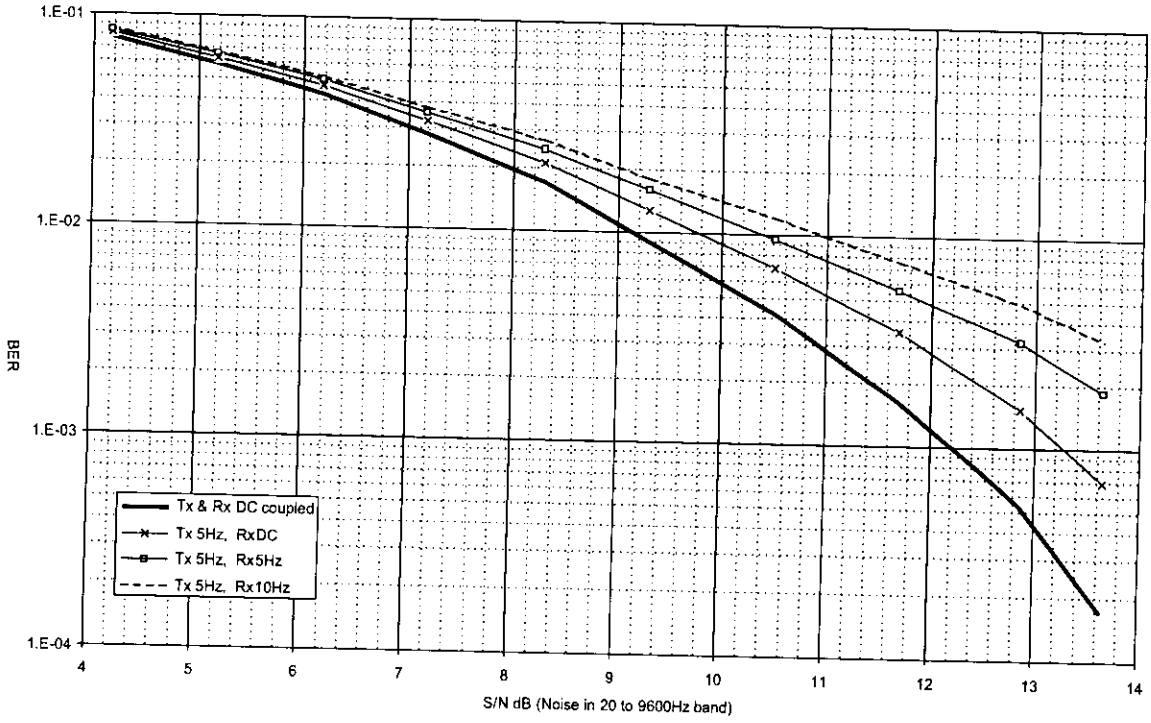

Figure 24: Effect of AC Coupling on BER (without FEC)

5.3 Clock Extraction and Level Measurement Systems

5.3.1 Supported Types of Systems

The MX919B is intended for use in systems where:

1. The Symbol Sync pattern is transmitted immediately on start-up of the transmitter, before the first Frame Sync pattern (see Figure 23).
2. A terminal may remain powered up indefinitely, transmitting concatenated Frames with or without intervening Symbol Sync patterns (each Frame having a Frame Sync pattern and symbol timing being maintained from one Frame to the next).
3. A receiving modem may be switched onto a channel before the distant transmitter has started up, or may be switched onto a channel where the transmitting station is already sending concatenated Frames

5.3.2 Clock and Level Acquisition Procedures with RF Carrier Detect

When the receiving modem is enabled or switched onto a channel, it needs to establish the received symbol levels, clock timing, and look for a Frame Sync pattern in the incoming signal. This is best done by the following procedure:

1. Ensure that the Control Register's PLLBW bits are set to 'Wide' and the LEVRES bits to 'Track'.
2. Wait until a received carrier has been present for 8 symbol times. This 8-symbol delay gives time for the received signal to propagate through the modem's RRC filter. An 'RF received 8 symbol times' qualifying function can be included in a radio's carrier detect circuitry to take this into account.
3. Write a SFS or SFSH task to the Command Register with the AQSC and the AQLEV bits set to '1'.
4. When the modem interrupts to signal that it has recognized a Frame Sync pattern (or completed the SFSH task) then change the PLLBW bits to 'Medium'.

Once the receiving modem has achieved level and symbol timing synchronization with a particular channel - as evidenced by recognition of a Frame Sync pattern - then subsequent concatenated Frames can be read by simply issuing SFS or SFSH tasks at appropriate times, keeping the ASQSC and AQLEV bits at zero, and the PLLBW and LEVRES bits at their current 'Medium' and 'Track' settings, respectively.

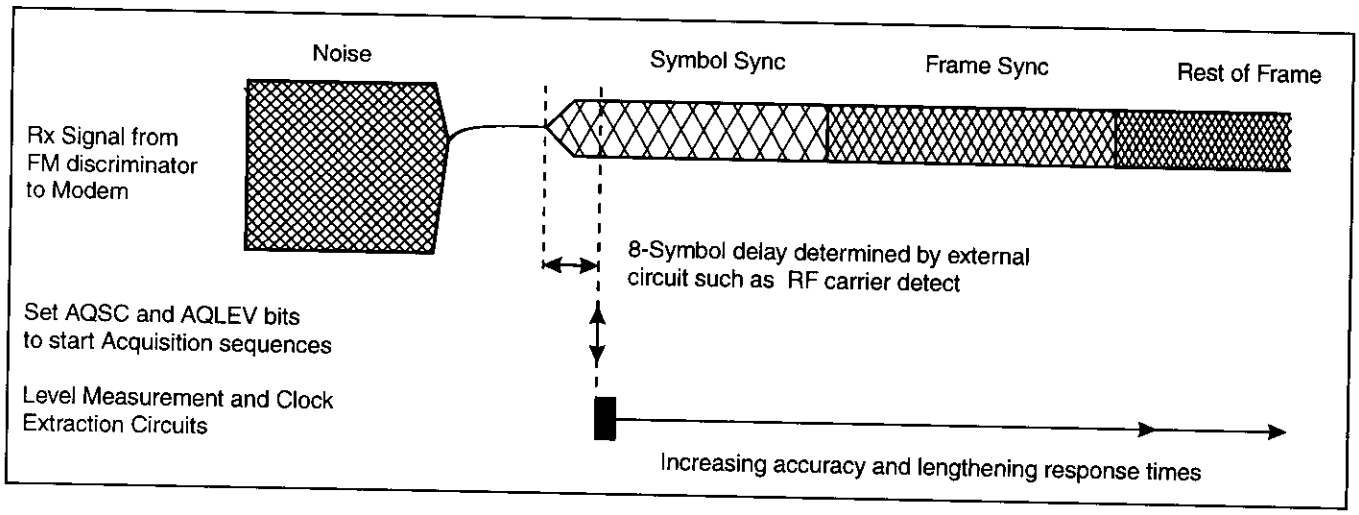

Figure 23: Acquisition Sequence Timing

5.3.3 Clock and Level Acquisition Procedure without RF Carrier Detect

It is also possible to use the modem in a system where there is an indeterminate delay between the RF transmitter turn on time and the transmission moment of the Symbol Sync pattern, or where a receive carrier detect signal is not available to the controlling µC, or where the transmitting terminal can send separate unsynchronized Frames. In these cases, each Frame should be preceded by, a Symbol Sync pattern which should be extended to about 100 symbols and the procedure provided in Section 5.3.2. used.

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2. Any ac coupling at the receive input will transform any step in the voltage at the discriminator output to a slowly decaying pulse which can confuse the modem's level measuring circuits. As illustrated in Figure 25 below, the time for this step to decay to 37% of its original value is 'RC' where:

$$RC = \frac{1}{2\pi(\text{3dB cut - off frequency of the RC network})}$$

which is 32ms, or 153 symbol times at 4800 symbols/sec (9600bps) for a 5Hz network.

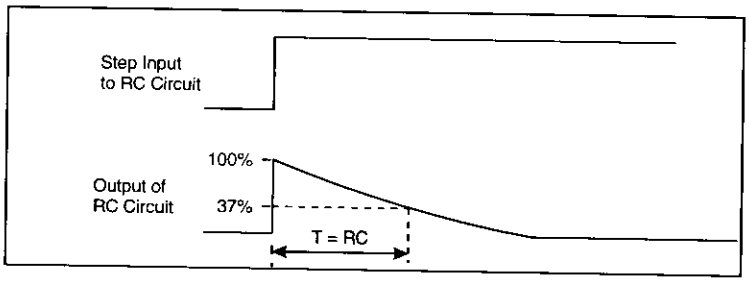

Figure 25: Decay Time - AC Coupling

In general, it is best to DC couple the receiver discriminator to the modem and ensure that any AC coupling to the transmitter's frequency modulator has a -3dB cut-off frequency of no higher than 5Hz for 4800 symbols/sec (9600bps).

5.5 Radio Performance

The maximum data rate that can be transmitted over a radio channel using these modems depends on:

- RF channel spacing.
- Allowable adjacent channel interference.
- Symbol rate.
- Peak carrier deviation (modulation index).
- Tx and Rx reference oscillator accuracy.
- Modulator and demodulator linearity.
- Receiver IF filter frequency and phase characteristics.
- Use of error correction techniques.
- Acceptable error rate.

As a guide, 4800 symbols/sec (9600bps) can be achieved (subject to local regulatory requirements) over a system with 12.5kHz channel spacing if the transmitter frequency deviation is set to ±2.5kHz peak for a repetitive ' +3 +3 -3 -3 ... ' pattern and the maximum difference between transmitter and receiver 'carrier' frequencies is less than 2400Hz.

The modulation scheme employed by these modems is designed to achieve high data throughput by exploiting as much as possible of the RF channel bandwidth. However; this does place constraints on the performance of the radio. Particular attention must be paid to:

- Linearity, frequency, and phase response of the Tx Frequency Modulator. For a 4800 symbols/sec (9600bps) system, the frequency response should be within ±2dB over the range 3Hz to 5kHz, relative to 2400Hz.
- The bandwidth and phase response of the receiver's IF filters.
- Accuracy of the Tx and Rx reference oscillators, as any difference will shift the received signal towards the skirts of the IF filter response and cause a DC offset at the discriminator output.

Viewing the equalized received signal eye diagram, using the Mode Register RXEYE function, provides a good indication of the overall RF transmitter/receiver performance.

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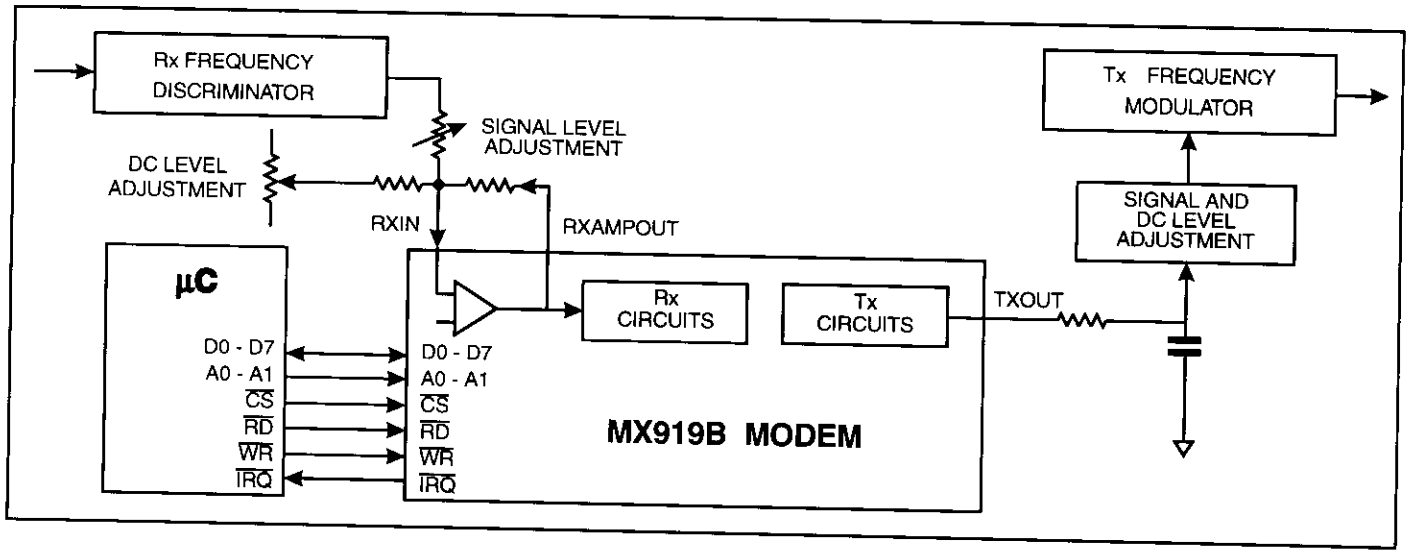

Figure 26: Typical Connections between Radio and MX919B

5.6 Received Signal Quality Monitor

In applications where the modem has to monitor a long transmission containing a number of concatenated Frames, it is recommended that the controlling software include a function which regularly checks that the modem is still receiving a good data signal and triggers a re-acquisition and possibly changes to another channel if a problem is encountered. This strategy has been shown to improve the system's overall performance in situation where fading, large noise bursts, severe co-channel interference, or loss of the received signal for long periods are likely to occur.

Such a function can be simply implemented by regularly reading the Data Quality Register, which gives a measure of the overall quality of the received signal, as well as the current effectiveness of the modem's clock extraction and level measurement systems. Experience has shown that if two consecutive DQ readings are both less than 50 then it is worth instructing the MX919B to re-acquire the received signal levels and timing once it has been established that the received carrier level is satisfactory. Re-acquisition should follow the procedure given in Section 5.3.

The intervals between Data Quality readings is not critical, but should be a minimum of 64 symbol times except for the first reading made after triggering the AQSC and AQLEV automatic acquisition sequences, which should be delayed for about 250 symbol times.

A suitable algorithm is shown in Figure 27.

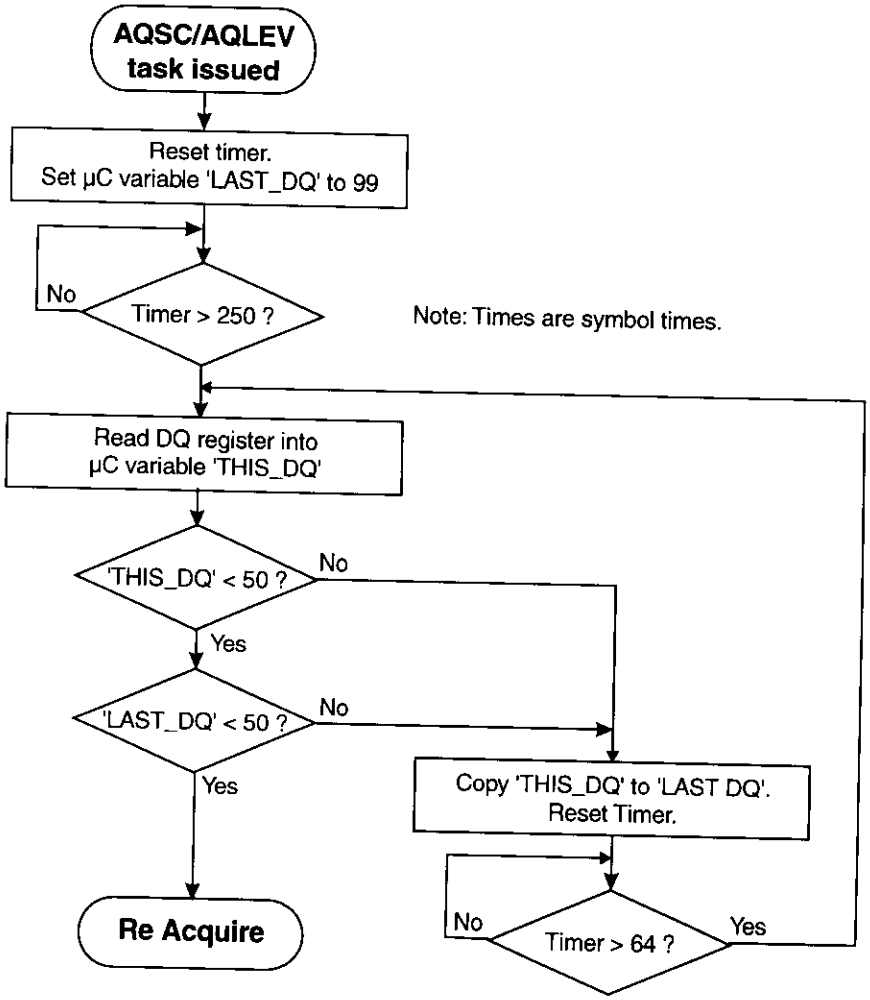

Figure 27: Received Signal Quality Monitor Flowchart

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6 Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
DW, LH, P Package	Min.	Max.	Units
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above °C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C
DS Package	Min.	Max.	Units
Total Allowable Power Dissipation at T_{AMB} = 25°C		550	mW
Derating above 25°C		9	mW/°C above °C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Symbol Rate		2400	9600	Symbols/sec
Temperature		-40	85	°C
Xtal Frequency		1.0	10.0	MHz

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6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
Xtal Frequency = 4.9152MHz, Symbol Rate = 4800 symbols/sec,
Noise Bandwidth = 0 to 9600Hz, V_{DD} = 5.0V @ T_{AMB} = 25°C

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD}	1		4.0	10.0	mA
I_{DD} (V_{DD} = 3.3V)	1		2.5	6.3	mA
I_{DD} (Powersave Mode)	1		1.5		mA
I_{DD} (Powersave Mode, V_{DD} = 3.3V)	1		0.6		mA
AC Parameters					
Tx Output					
TXOUT Impedance	2		1.0	2.5	kΩ
Signal Level					
TXIMP = 0	3	0.8	1.0	1.2	V_{P-P}
TXIMP = 1	3	0.88	1.1	1.32	V_{P-P}
Output DC Offset with respect to V_{DD} /2	4	-0.25		0.25	V
Rx Input					
RXIN Impedance (at 100Hz)			10.0		MΩ
RXIN Amp Voltage Gain (input = 1mV_{RMS} at 100Hz)			300		V/V
Input Signal Level	5	0.7	1.0	1.3	V_{P-P}
DC Offset with respect to V_{DD} /2	5	-0.5		0.5	V
XTAL/CLOCK INPUT					
'High' Pulse Width	6	40			ns
'Low' Pulse Width	6	40			ns
Input Impedance (at 100Hz)		10.0			MΩ
Inverter Gain (input = 1 mV_{RMS} at 100Hz)		20			dB
µC Interface					
Input Logic "1" Level	7, 8	70%			V_{DD}
Input Logic "0" Level	7, 8			30%	V_{DD}
Input Leakage Current (V_{IN} = 0 to V_{DD})	7, 8	-5.0		5.0	µA
Input Capacitance	7, 8		10.0		pF
Output Logic "1" Level (I_{OH} = 120µA)	8	92%			V_{DD}
Output Logic "0" Level (I_{OL} = 360µA)	8, 9			8%	V_{DD}
'Off' State Leakage Current (V_{OUT} = V_{DD})	9			10	µA

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6.1.4 Operating Characteristics Notes:

1. Not including any current drawn from the modem pins by external circuitry other than the Xtal oscillator.
2. Small signal impedance.
3. Measured after the external RC filter (R4/C5) for a "+3 +3 -3 -3...." symbol sequence, (Tx output level is proportional to V_{DD}).
4. Measured at the TXOUT pin with the modem in the Tx idle mode.
5. For optimum performance, measured at RXAMPOUT pin, for a "...+3 +3 -3 -3..." symbol sequence, TXIMP = 0 or 1, The optimum level and DC offset values are proportional to V_{DD}.
6. Timing for an external input to the XTAL/CLOCK pin.
7. $\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A0 and A1 pins.
8. D0 - D7 pins.
9. $\overline{IRQ}$ pin.

6.1.5 Timing

µC Parallel Interface Timings (ref. Figure 28)		Notes	Min.	Typ.	Max.	Units
t_{ACSL}	Address valid to $\overline{CS}$ low time		0			ns
t_{AH}	Address hold time		0			ns
t_{CSH}	$\overline{CS}$ hold time		0			ns
t_{CSHI}	$\overline{CS}$ high time	1	6			clock cycles
t_{CSRWL}	$\overline{CS}$ to $\overline{WR}$ or $\overline{RD}$ low time		0			ns
t_{DHR}	Read data hold time		0			ns
t_{DHW}	Write data hold time		0			ns
t_{DSW}	Write data setup time		90			ns
t_{RHCSL}	$\overline{RD}$ high to $\overline{CS}$ low time (write)		0			ns
t_{RACL}	Read access time from $\overline{CS}$ low	2			175	ns
t_{RARL}	Read access time from $\overline{RD}$ low	2			145	ns
t_{RL}	$\overline{RD}$ low time		200			ns
t_{RX}	$\overline{RD}$ high to D0-D7 3-state time				50	ns
t_{WHCSL}	$\overline{WR}$ high to $\overline{CS}$ low time (read)		0			ns
t_{WL}	$\overline{WR}$ low time		200			ns

Timing Notes:

1. Xtal/Clock cycles at the XTAL/CLOCK pin.
2. With 30pF max to V_{SS} on D0 - D7 pins.

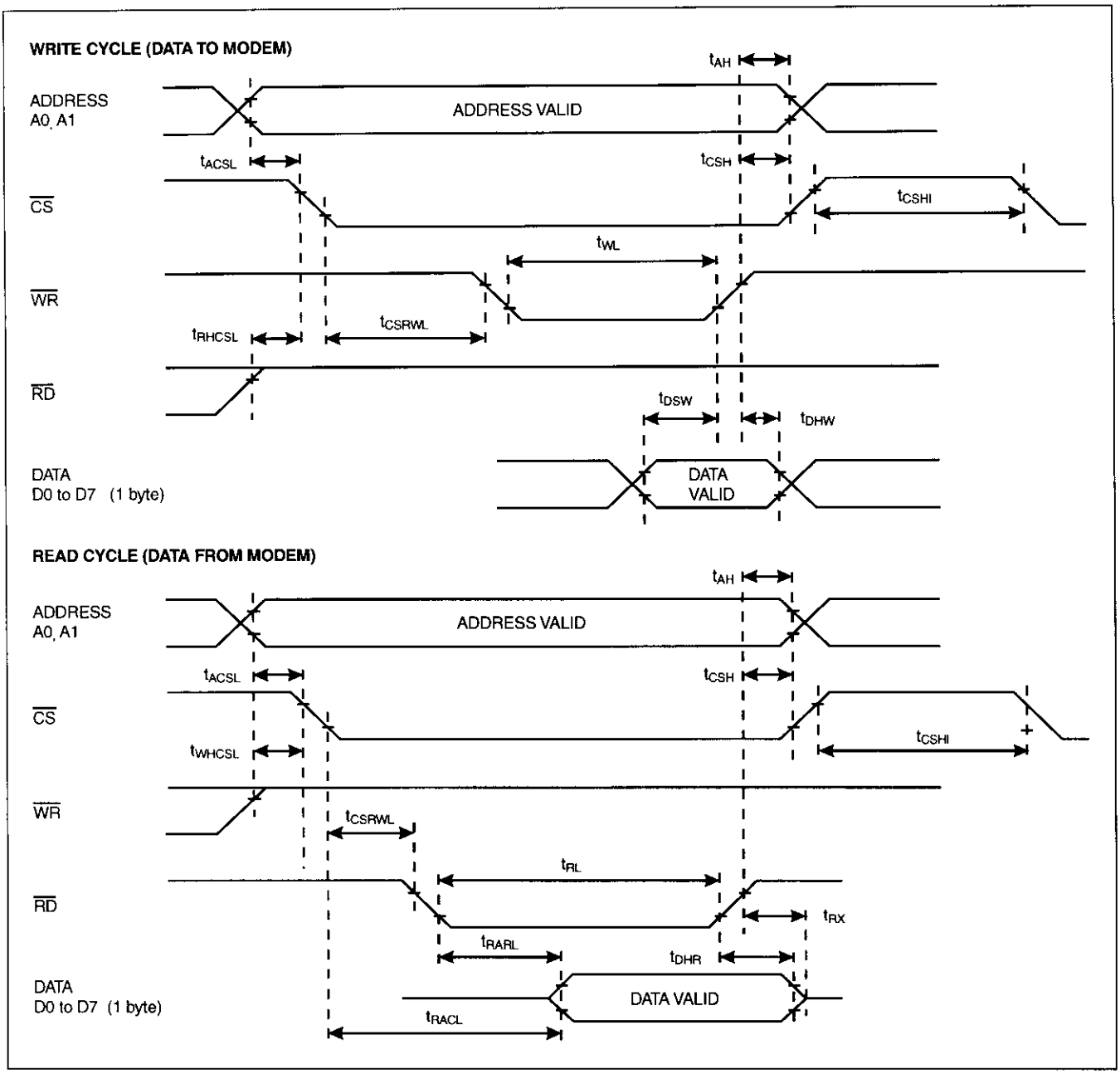
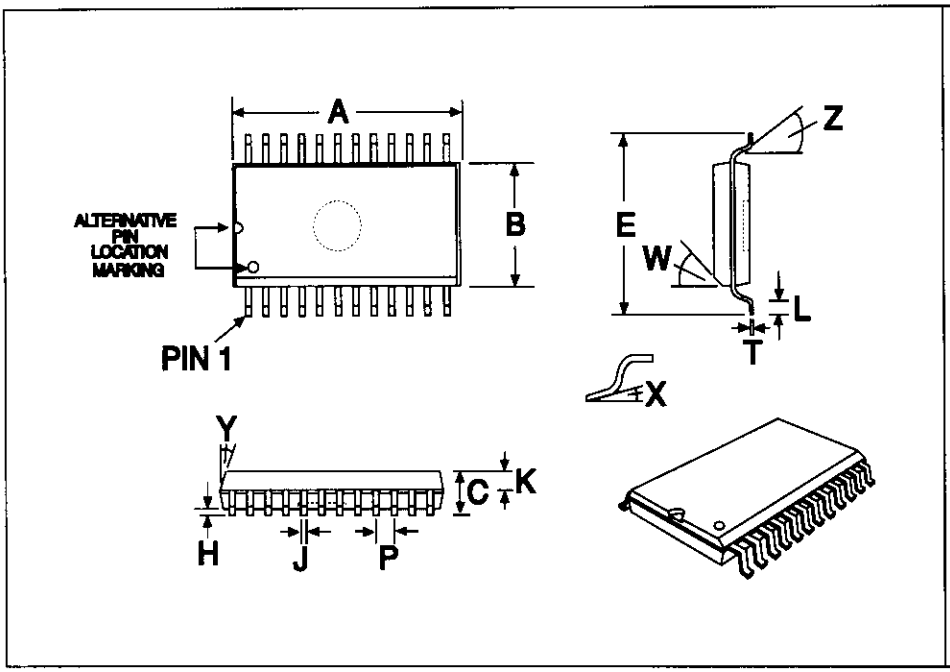


Figure 28: µC Parallel Interface Timings

6.2 Packaging

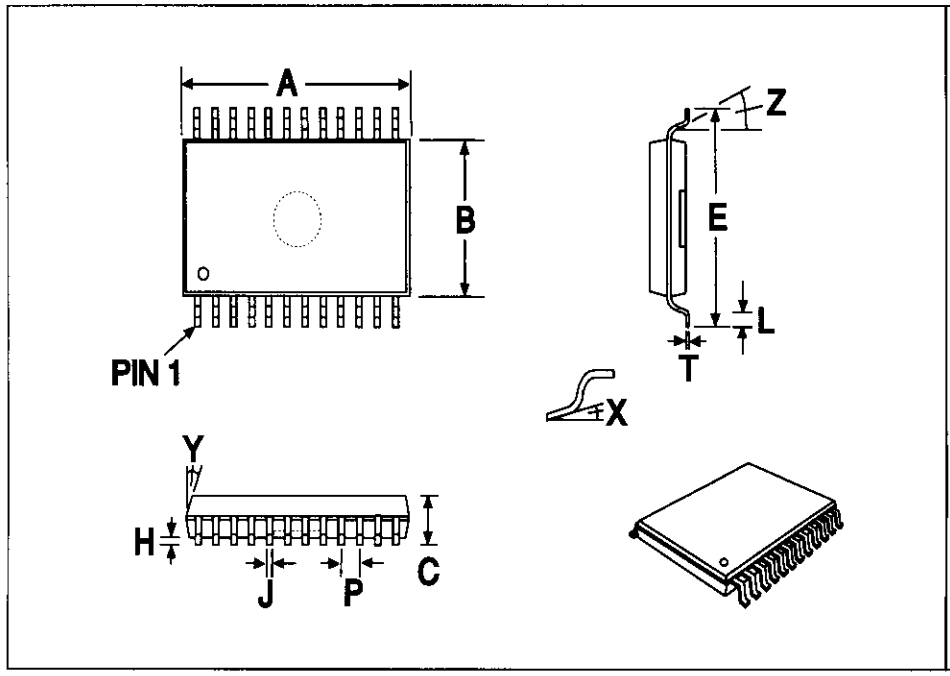


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 30: 24-pin SOIC Mechanical Outline: *Order as part no. MX919BDW*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 31: 24-pin SSOP Mechanical Outline: *Order as part no. MX919BDS*

6.1.6 Typical Bit Error Rate

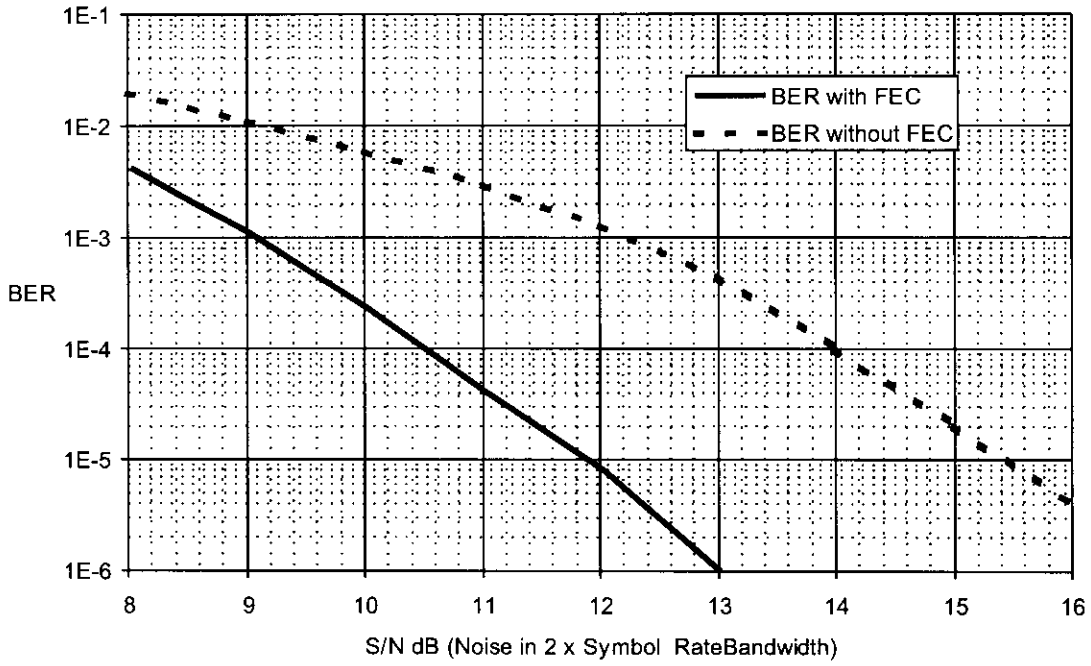


Figure 29: Typical Bit Error Rate With and Without FEC

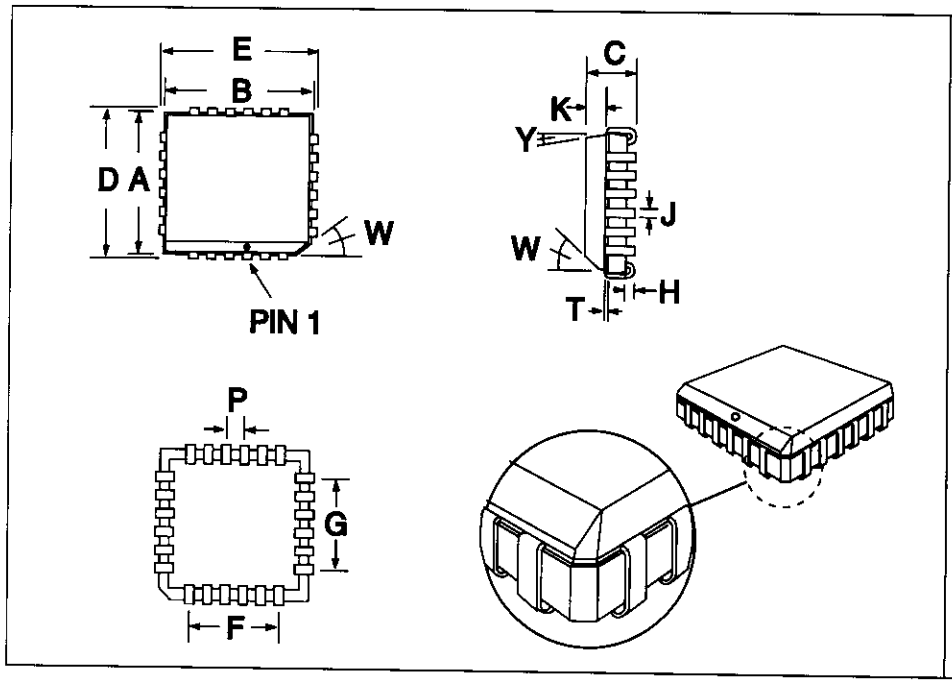
Measured under nominal working conditions, LEVRES bits set to 'Level Track' or 'Slow Peak Detect' and PLLBW bits set to 'Medium' or 'Narrow' Bandwidth, Command Register TXIMP bit set to '0' or '1' (same for Tx and Rx devices), with pseudo-random data.

Note: S/N calculates as $20\log_{10}(\frac{\text{Signal Voltage}}{\text{Voltage Noise}})$

Where: Signal Voltage is the measured V_{RMS} of a random 4-level signal.

Noise Voltage is the V_{RMS} of a flat Gaussian noise signal having a bandwidth from a few Hz to twice the symbol rate e.g. to 9600Hz when measuring a 4800 symbol/sec (9600bps) system.

Both signals are measured at the same point in the test circuit.

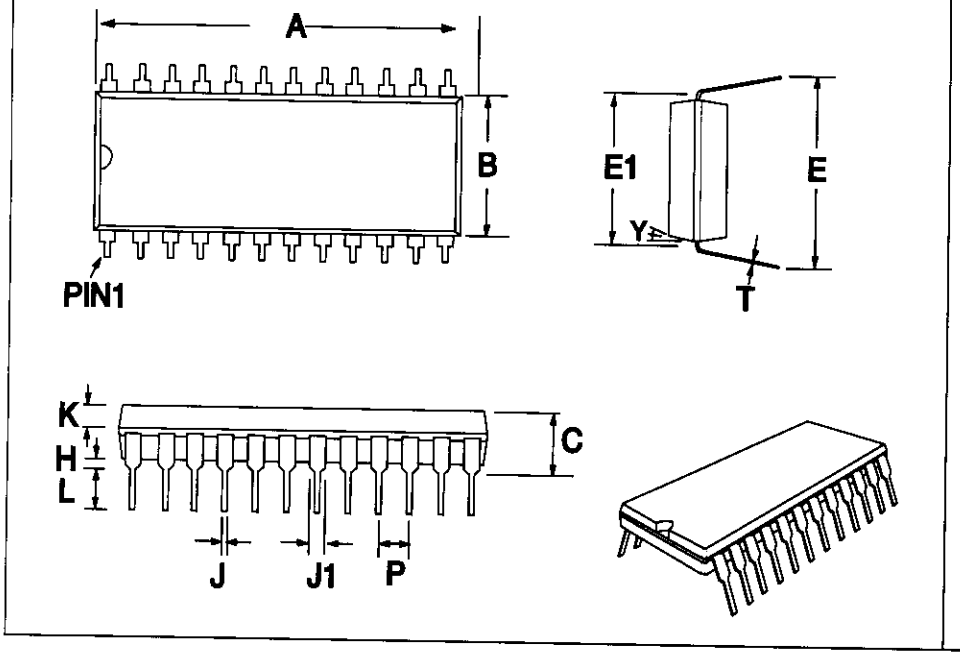


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 32: 24-pin PLCC Mechanical Outline : *Order as part no. MX919BLH*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 33: 24-pin PDIP Mechanical Outline: *Order as part no. MX919BP*

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