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Operations and Maintenance Manual

**Model 1150A Doppler
VHF Omirange (DVOR)**

571150A-0002 Rev - November, 2008

SELEX Sistemi Integrati Inc.
11300 West 89th Street
Overland Park, KS U.S.A. 66214

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SAFETY SUMMARY

The following are general safety precautions that are unrelated to specific procedures and therefore do not appear elsewhere in this publication. These are recommended precautions that personnel should understand and apply during through the many phases of operation and maintenance.

ELECTROSTATIC SENSITIVE DEVICES PRECAUTIONS

Since most modules used in all models of equipment have Electrostatic Discharge (ESD) sensitive devices included in them, all modules should be considered sensitive to electrostatic discharge. Handling in the field shall be the same as in the factory. Each system is shipped with a wrist strap that must be worn while maintaining the equipment. The wrist strap shall be fastened to the equipment chassis either in the designated plug-in or attached to the equipment chassis with the alligator clip. The wrist strap must be used before any modules are removed from the equipment and at all times while handling the modules until they are placed in a protective environment such as an anti-static bag. Modules or boards must not be placed on any non-conducting surface such as wooden work benches, painted metal work benches, plastics, or technical manuals. Any work surface to be used must have a conducting mat placed on it and attached to earth ground. The mat and additional wrist straps can be obtained from SELEX Sistemi Integrati Inc.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must at all times observe all safety regulations. Under no circumstances should any person remove any protective covers that expose lethal voltages. Do not replace components or make adjustments inside the equipment with primary power supply turned on. Under certain conditions, dangerous potentials may exist when the power is in the off position, due to charges retained by capacitors. To avoid casualties, always remove power and allow time for the capacitors to discharge before touching it.

DO NOT SERVICE OR ADJUST ALONE

Under no circumstances should any person reach into or enter the enclosure for the purpose of servicing or adjusting the equipment except in the presence of someone who is capable of rendering aid.

RESUSCITATION

Personnel working with or near high voltages should be familiar with modern methods of resuscitation.

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SELEX Sistemi Integrati Inc.

This equipment is supplied by SELEX Sistemi Integrati Inc. For replacement parts and repair service, contact SELEX Sistemi Integrati Inc. using the contact information provided below.

HOW TO ORDER REPLACEMENT PARTS

When ordering replacement parts, you should contact SELEX Sistemi Integrati Inc. by fax, phone or email. Please address the following items (as applicable) in your correspondence to enable us to provide the best possible service.

1. SELEX Sistemi Integrati Inc. model number, type and serial number of equipment.
2. Unit sub-assembly number (where applicable).
3. Item or reference symbol number from parts list or schematic.
4. SELEX Sistemi Integrati Inc. part number and description.
5. Manufacturer's code, name and part number (where applicable).
6. Quantity of each replacement part required.

HOW TO REQUEST REPAIR SERVICE

In order to ensure prompt attention, parts returned for repair should have the following:

1. RMA number (Return Material Authorization number), assigned prior to return when requesting repair service.
2. Unit part number
3. Site location
4. System information
5. Ship-to address for return
6. Contact name and number
7. Date and time of request

CONTACT INFORMATION

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Overland Park KS, 66214, USA

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MANUFACTURER'S WARRANTY
SELEX Sistemi Integrati Inc.

The following warranty is applicable in all cases, except where modified or superseded by specific contract terms. Contact SELEX Sistemi Integrati Inc. if clarification is required.

- A. The Manufacturer warrants to the original Purchaser, subject to the limitations and exclusions stated below, that mechanical and electrical parts of products which it manufactures, (the "Products" will be free of defects in materials and workmanship for a period of (I) one (1) year from the date of installation or (ii) 18 months from the date of shipment, whichever first occurs (the "Warranty Period").
- B. If the Customer believes a Product is defective, notice thereof shall be provided to the Manufacturer's Customer Service Department at the address provided on the cover page and (if applicable) to the selling distributor. A defect in material and workmanship covered by this warranty shall be deemed to have occurred only if, and as of the time when, the Manufacturer is notified in writing by the Customer, within the Warranty Period, that the Product has become defective, and the Manufacturer's personnel verify that the said Product, in fact, does not comply with the warranty provided hereunder and it is determined that:
 - (i) The Products, during the entire Warranty Period, have been operated within normal service conditions, recommended by the Manufacturer and recognized in the industry, and
 - (ii) The Products have been installed and adjusted according to the Manufacturer's procedures as stated in the Instruction Manual or other instructions supplied in writing by the Manufacturer.
- C. Failures caused by lightning or other acts of God, or power surges, are not considered to be defects in materials and workmanship and are not covered under this warranty. Routine Maintenance and calibration are also not considered to be defects in materials and workmanship and are not covered under this warranty. Any change, modification or alteration of the Manufacturer's Products not specifically authorized by the Manufacturer will void this warranty.
- D. If it is determined that the conditions for warranty coverage, as described above, have been satisfied, the Manufacturer shall repair or replace the defective products or parts thereof in accordance with the following procedures:
 - (i) Customer will contact the Manufacturer's customer Service Department which will issue the Customer a Return Authorization (RA) number.
 - (ii) The Component, defective part, or Product, as appropriate, shall be returned to the Manufacturer for inspection, freight prepaid by the customer. The Component, defective part, or Product MUST be packaged with an industry standard anti-static protective bag sufficient to prevent any ESD intrusion during handling and shipment, and MUST ALSO be packaged to protect from damage due to rough handling encountered during shipment. FAILURE TO COMPLY WITH THIS REQUIREMENT WILL VOID THE WARRANTY OF THE RETURNED ITEM. The RA number must be clearly displayed on the exterior of the shipping container. No shipments will be accepted without a RA number. All custom duties, fees, etc. will be paid by the Customer.
 - (iii) If, upon inspection it is determined by Manufacturer's personnel that the Product or component thereof is indeed defective and covered by this warranty, then Manufacturer, at its option, may either repair the Product or defective components thereof and return the same to the Customer or ship a replacement for the defective Product or part thereof, freight paid. All customs duties, fees, etc. will be paid by the Customer. The Product or component thereof will be returned to the Customer utilizing a shipping mode similar to that used by Customer to ship the same to the Manufacturer.
 - (iv) If, upon inspection by Manufacturer, it is determined that the Product or component thereof was not defective or was not covered by this warranty, then the cost of all of Manufacturer's inspections and the return shipping charges will be charged to Customer.
- E. The Manufacturer reserves the right to make modifications and alterations to Products without obligation to install such improvements on, in, or in place of theretofore manufactured products of Manufacturer.

MANUFACTURER'S WARRANTY (cont.)

- F. Manufacturer does not warranty any Products, components, subassemblies, or parts not of its own manufacture. Manufacturer hereby transfers to Customer any and all warranties (if any) which it receives from its suppliers.
- G. Periodic calibration / re-calibration of test equipment is not covered under this or any Seller's warranty, and is the sole responsibility of the Purchaser.
- H. Any and all claims for shortages, missing or damaged items must be presented, in writing, to the Seller within 120 days of the date of shipment from Seller's factory.
- I. This warranty applies only to the original purchaser and, unless Customer receives the express written consent of an officer of Manufacturer, this warranty may not be assigned, transferred, or conveyed to any third party, even if the third party is a bon a fide purchaser of the Products.
- J. **THIS WARRANTY IS EXPRESSLY IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED OR IMPLIED, WHETHER STATUTORY OR OTHERWISE, INCLUDING IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. IN NO EVENT SHALL THE MANUFACTURER BE LIABLE FOR INDIRECT, INCIDENTAL, COLLATERAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES OF ANY KIND, WHETHER ARISING OUT OF CONTRACT, TORT, NEGLIGENCE, STRICT LIABILITY OR OTHER PRODUCTS LIABILITY THEORY.**
- K. **CUSTOMER'S SOLE REMEDY FOR ANY BREACH OF THE WARRANTY SHALL BE THE REPAIR OR REPLACEMENT OF THE PRODUCTS BY THE MANUFACTURER AS PROVIDED HEREIN, AND IN NO EVENT SHALL THE MANUFACTURER BE REQUIRED TO INCUR COSTS FOR THE REPAIR OR REPLACEMENT OF ANY PRODUCT IN EXCESS OF THE PURCHASE PRICE OF SUCH PRODUCT, PLUS ANY TRANSPORTATION CHARGES ACTUALLY PAID ATTRIBUTABLE TO SUCH PRODUCTS.**

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1 GENERAL INFORMATION AND REQUIREMENTS

1.1 INTRODUCTION

This manual provides the data required to operate and maintain the Model 1150A Single or Dual Doppler VHF Omni-range (DVOR) Station. [Figure 1-1](#) is a typical DVOR/TACAN site. [Figure 1-2](#) is a typical DVOR/DME site. The counterpoise structure may vary based upon customer requirements. Included are equipment description and specifications, block diagram level theory of operation, operating procedures, standards and tolerances, periodic maintenance procedures, corrective maintenance procedures, parts list, schematics, and other diagrams.



Figure 1-1 Dual Doppler VHF Omni-range (DVOR) Station with TACAN



Figure 1-2 Dual Doppler VHF Omni-range (DVOR) Station with DME

1.2 EQUIPMENT DESCRIPTION

The DVOR system provides a reference from which aircraft bearing can be determined. To do this, a carrier is radiated in the 108 to 118 MHz band and modulated by two 30 Hz signals. One amplitude modulates and the other frequency modulates (also called the reference phase and variable phase signals, respectively) the carrier signal. This is done in such a way that the phase difference of the 30 Hz signals varies degree for degree with the magnetic bearing around the VOR station.

The DVOR system consists of one electronics cabinet with sub-assemblies, a Portable Maintenance Data Terminal (PMDT), one reference (carrier) antenna and 48 sideband antennas installed on a counterpoise, one field monitor antenna, and interconnecting cables.

The DVOR electronics cabinet standard configuration uses convection cooling. No fans or blowers are installed in the cabinet.

1.2.1 Electronics Cabinet

The 1150A VOR is contained in one (1) electronics cabinet measuring 24" wide, 24" deep and 72" high. It utilizes a standard 19" rack configuration with a front panel door that covers and protects the equipment. The Model 1150A is 100% solid-state. Its internal circuitry is contained on plug-in type printed circuit card assemblies (CCAs) and RF modules.

Refer to **Figure 1-3** through **Figure 1-6** which show the layout of the various modules within the Model 1150A VOR cabinet. The paragraphs on the following pages provide a brief description of each of the modules and its function in the system. Note that the cabinets shown are dual equipment systems. Refer to **Figure 2-2** and **Figure 2-3** for the Model 1150A Doppler VOR system block diagram.

1.2.1.1 Local Control Unit (LCU) (1A1)

The Local Control Unit (LCU) is located in the upper portion of the VOR cabinet and provides station status information. The LCU provides for Transmitter, Monitor and System setup, monitoring and control. Alarm indication from the VOR Monitors initiates transfer or VOR shutdown.

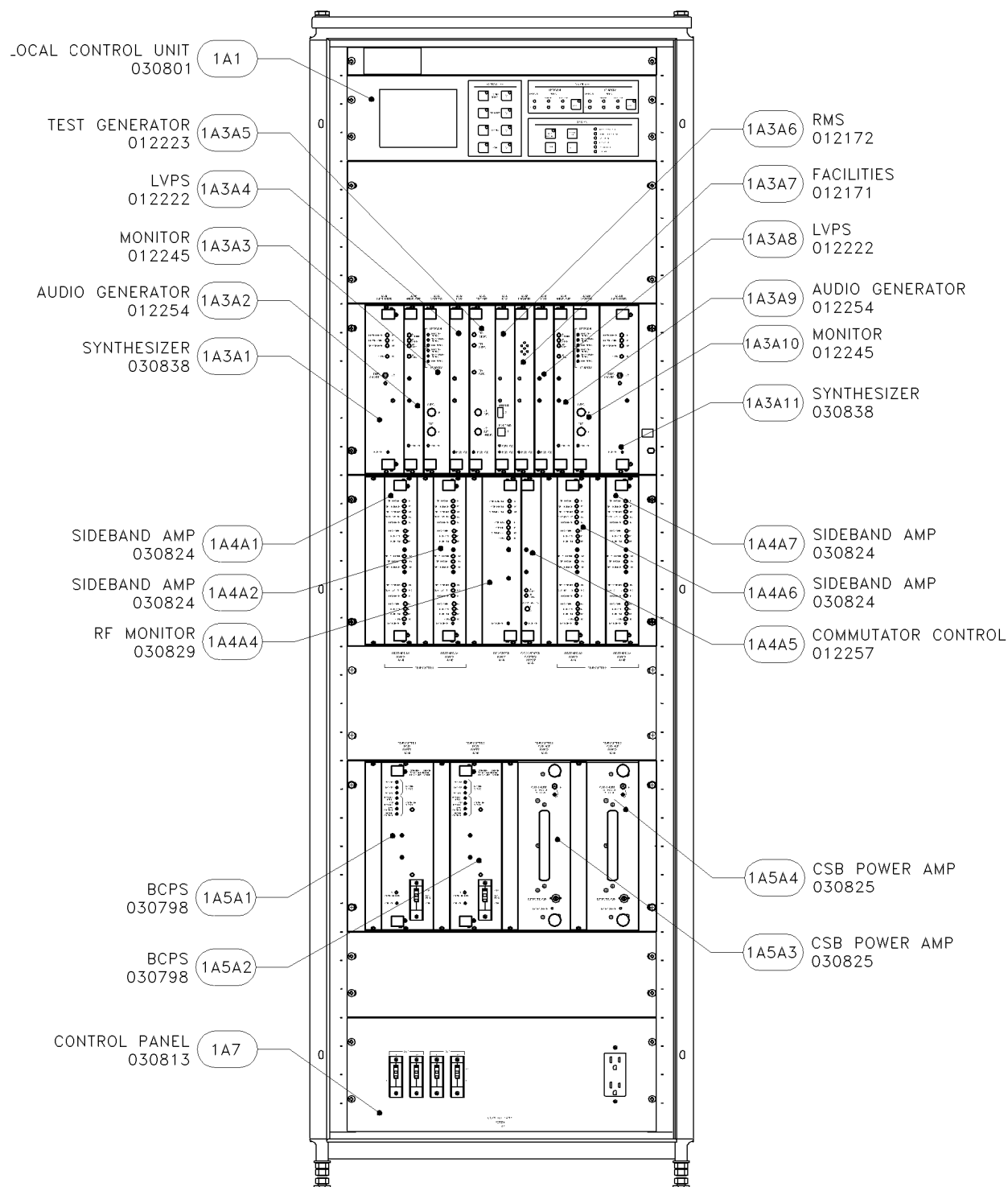
1.2.1.2 Synthesizer Assembly (1A3A1, 1A3A11)

The Synthesizer assembly generates three RF signals (carrier, upper and lower sidebands) for the VOR transmitter. There are three boards in the Synthesizer Assembly. The Carrier board provides the carrier frequency and phase control capability for the Carrier Amplifier. The sideband board generates upper and lower sideband frequencies for the Sideband Amplifier Assemblies. The third board (Interface) provides connectivity to the backplane and includes digital interface circuitry to the Audio Generator and RMS processors.

1.2.1.3 Audio Generator CCA (1A3A2, 1A3A9)

The Audio Generator CCA is responsible for developing and controlling the audio signals, generating the carrier modulation signals and monitoring and controlling RF power level and phase control signals used in the DVOR. In addition, DC analog voltages representing different modulation and power levels of the DVOR RF signals are applied to, and analyzed by, the audio generator to determine carrier power levels, carrier percent modulation, sideband power levels and VSWR. An on-board micro controller and memory circuitry controls all functions within the CCA and communication through the serial connection to the RMS CCA.

Model 1150A DVOR



1150A-0001

CABINET FRONT

Figure 1-3 Location of Major Assemblies in the Electronics Cabinet (Front View)

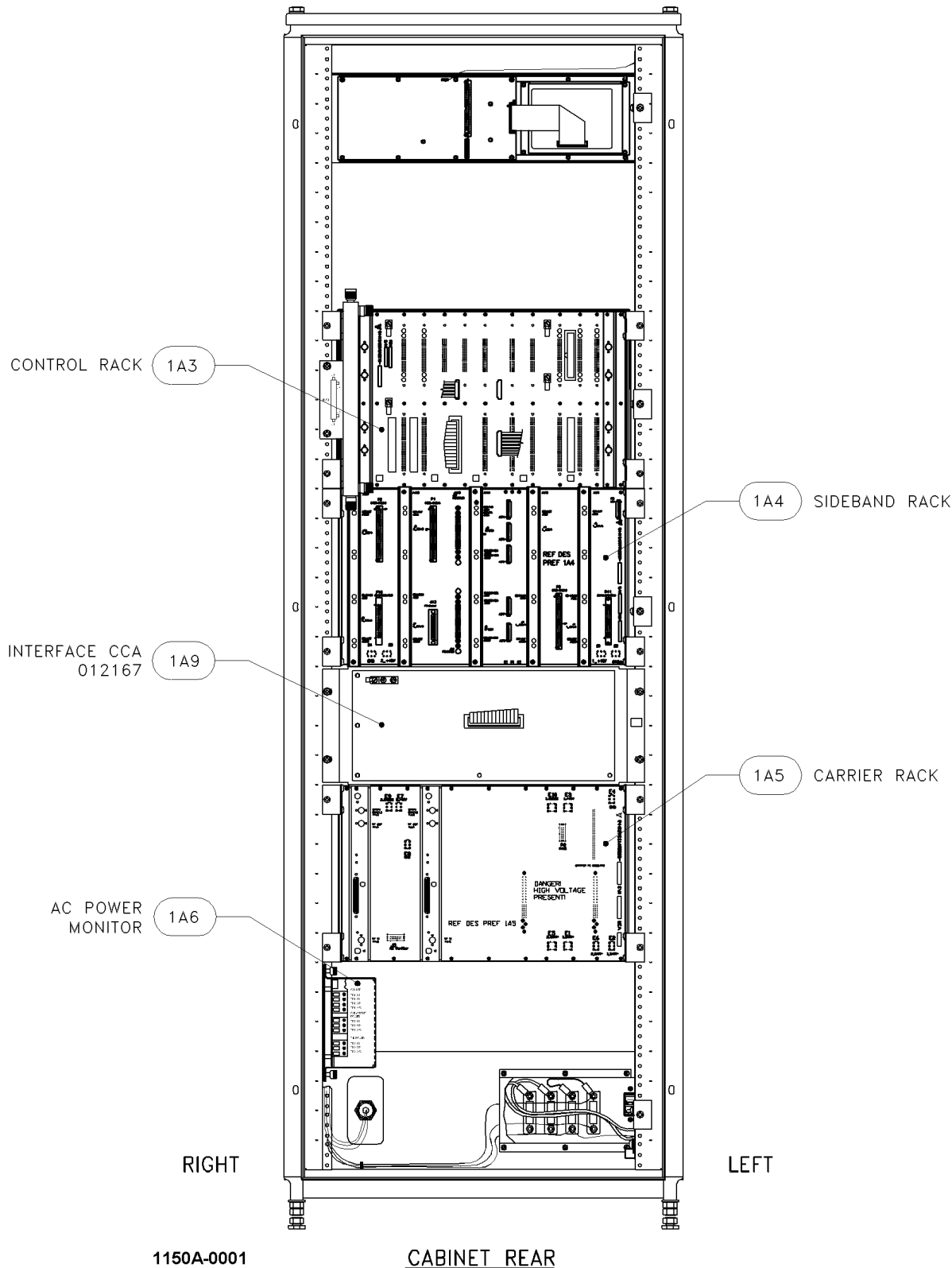


Figure 1-4 Location of Major Assemblies in the Electronics Cabinet (Rear View)

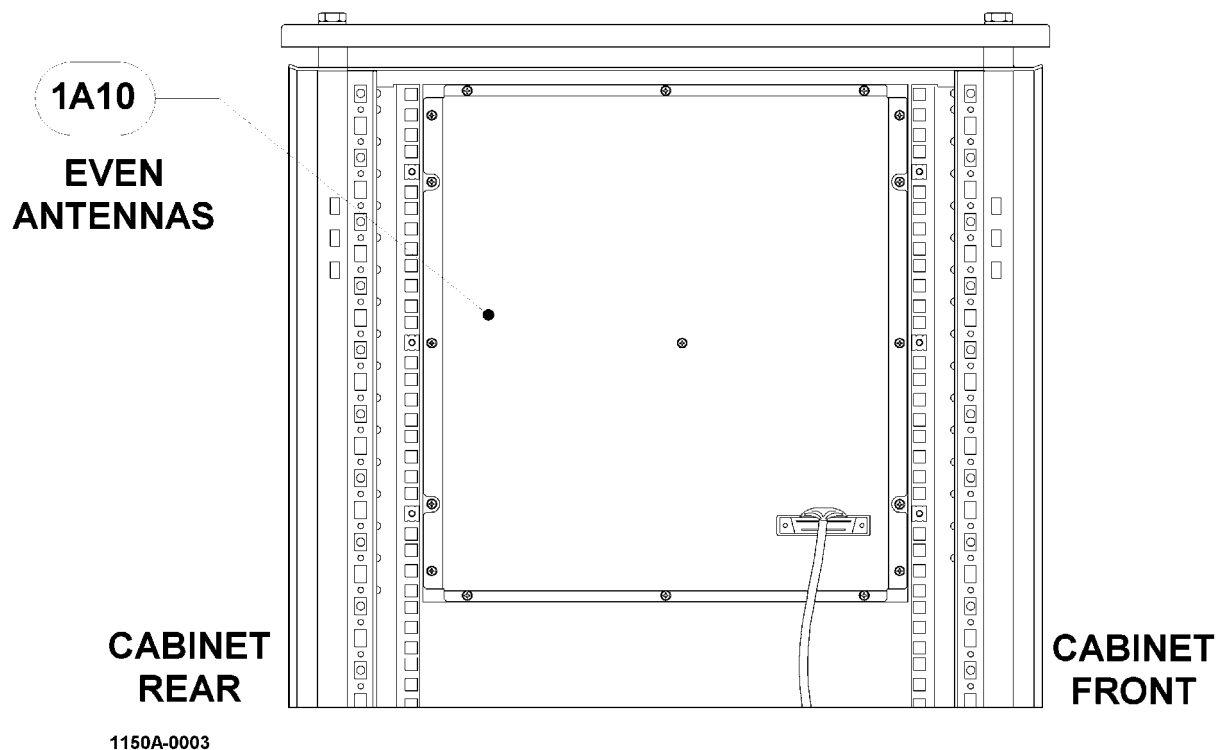


Figure 1-5 Location of Commutator (1A10) Assembly in the Electronics Cabinet (Left Side View)

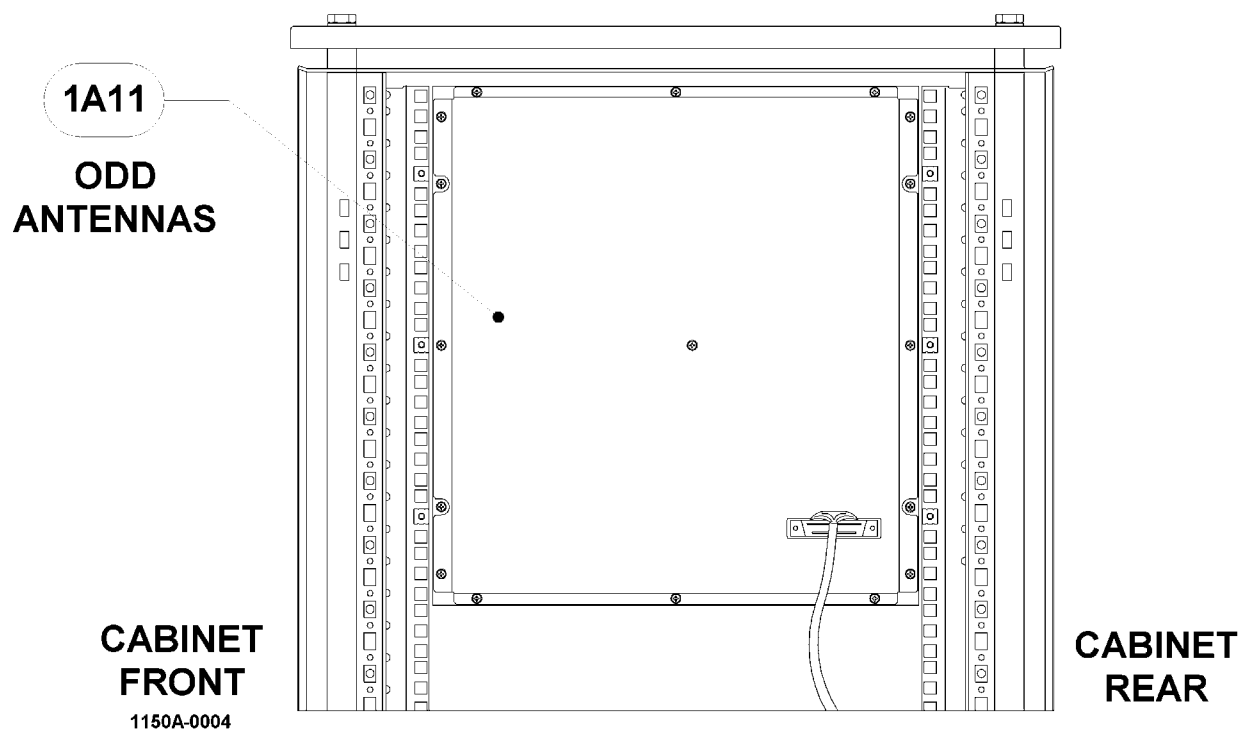


Figure 1-6 Location of Commutator (1A11) Assembly in the Electronics Cabinet (Right Side View)

1.2.1.4 Monitor CCA (1A3A3, 1A3A10)

The Monitor CCA amplifies the RF input from the field monitor antenna, then band pass filters and analyzes the signals. The parametric data is displayed on the PMDT and the Monitor CCA initiates an alarm status indication to the LCU if the DVOR fails to operate within specified limits.

1.2.1.5 Low Voltage Power Supply (LVPS) CCA (1A3A4, 1A3A8)

There are two LVPS assemblies used in the transmitter cabinet. LVPS 1A3A4 is the low voltage power supply for transmitter 1 and 1A3A8 is the LVPS for transmitter 2. Each LVPS is identical in construction and operation. Each is interchangeable with the other.

1.2.1.6 Test Generator CCA (1A3A5)

The Test generator CCA performs two functions. Its primary function is to provide a standard reference signal to the DVOR monitors for calibration whenever directed by the RMS CPU for monitor integrity testing.

The secondary function is an operator maintenance function, which allows test signals to be sent to the monitor(s), as directed by an operator through the PMDT. The operator can vary signal parameters (i.e., voice band audio frequency, percent modulation, phase shift, etc.) to determine if a monitor is functioning properly and will alarm at the required settings.

1.2.1.7 Remote Monitoring System (RMS) Processor CCA (1A3A6)

The Remote Monitoring System (RMS) Processor CCA controls the transmitter and monitoring systems. The RMS CCA performs communications via thirteen serial ports plus a parallel port, and facilitates monitoring/control in a single or dual VOR system. The RMS CCA receives battery-backed DC power from the BCPS.

The RMS CPU contains a micro controller, RAM, EPROM, EEPROM, bus control and power monitor circuitry. It processes the system status, directs communications with the outside world, and communicates with the DVOR monitor and audio generator assemblies.

1.2.1.8 Facilities CCA (1A3A7)

The Facilities CCA provides system I/O for the Remote Monitoring System CCA. Many of the inputs and outputs of the Facilities CCA eventually connect to the Interface CCA after routing through the Control Backplane CCA. System battery-backed power supplies (nominally 48VDC) enter and are regulated down into several lower voltages; including +24V, ±15VDC, ±12VDC, +5VDC, and +3.3VDC.

1.2.1.9 Sideband Amplifier Assembly (1A4A1, 1A4A2, 1A4A6, 1A4A7)

The Sideband Amplifier Assemblies are located in the middle rack (1A4) of the DVOR cabinet. Each Sideband Amplifier contains one CCA and generates two separate RF signals. Both signals are either above the carrier frequency or below the carrier frequency by 9960 Hz.

1.2.1.10 RF Monitor Assembly (1A4A4)

The RF Monitor assembly is located in the middle rack (1A4) of the DVOR cabinet. The RF monitor assembly functions as an RF detector/amplifier and distributor of the detected RF signals. The RF monitor assembly has a high power dummy load for the carrier mounted to a heat sink that is attached to the assembly chassis. There are four sideband dummy loads.

1.2.1.11 Commutator Control CCA (1A4A5)

The Commutator Control CCA connects to a 25 conductor cable on the backplane CCA. This cable originates from one of the two Audio Generators in the Control rack. The output of the Commutator Control CCA exits onto the backplane and to two 40-pin connectors that connect to ribbon cable from the Commutator CCAs.

Capability for the ground performance check of the antennas and commutator switching is provided. This check is automatic after it has been started by the technician and therefore is called an Automatic Ground Check system. When started, the Monitor CCA sends a switch position code to the Commutator control CCA via the 25-pin cable originating at the Control rack.

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The switch positions start at 0 and increment by one until 15. Each position represents 22.5 degrees of antenna rotation from the nominal position. At each position the Monitor CCA determines the azimuth angle at the Field Monitor antenna location. From this data the errors are measured and a Fourier Analysis is performed to generate the display data.

The error as determined during the ground check is analyzed to determine the bias, the duantal error, quadrantal error and octantal error. The bias error is the average error around the station. The duantal error is sinusoidal with a rate of one cycle in the 360 degrees around the station. The quadrantal error is sinusoidal with a rate of two cycles in the 360 degrees around the station. The octantal error is sinusoidal with a rate of four cycles in the 360 degrees around the station.

A 4-pin header on the Commutator Control CCA may be strapped to enable/disable the DVOR automatic ground-check as desired.

WARNING

Enabling the automatic ground-check test changes the signal in space and will cause unsafe conditions for aircraft. A notice to airmen (NOTAM) must be issued prior to starting this

1.2.1.12 Battery Charging Power Supply (BCPS) Assembly (1A5A1, 1A5A2)

The BCPS assemblies provide regulated voltage to the transmitter from either the AC input or the batteries. The BCPS assemblies are located in the third rack. The AC voltage is an input to the BCPS which converts to approximately 50 Volts DC. The BCPS assemblies are also responsible for charging the batteries when AC is present.

1.2.1.13 Carrier Power Amplifier Assembly (1A5A3, 1A5A4)

The Carrier Amplifier has one assembly. The Carrier Amplifier circuit card assembly, which is also the module's I/O, processes the control signals from the Audio Generator to properly control the desired output RF modulation and amplitude. This assembly is capable of providing 100 Watts or more of Carrier power at up to 80% AM modulation.

1.2.1.14 Interface CCA (1A9)

The Interface CCA provides interface connections between the RMS/Facilities/Control Backplane CCAs and the outside world. Examples include spare analog and digital inputs, spare digital outputs, temperature sensors, smoke detector, and intrusion sensor. RS232 communications are provided to RCSU and PMDT terminals as well as an Ethernet module. All signals are protected by transient voltage suppression (TVS) devices on the Interface CCA before exiting.

1.2.1.15 AC Power Monitor Assembly (1A6)

The AC Power Monitor CCA provides a means for the VOR system to measure the AC current and voltage levels of the obstruction lights and of the VOR system itself. Provision for operating with a photo switch is incorporated. A capability to bypass the photo switch for the obstruction lights is provided.

1.2.1.16 Commutator CCA (1A10, 1A11)

Each commutator CCA measures 15-7/8" high and 14-7/8" wide. There are two commutator CCAs installed in the top of the electronics cabinet. They are located on the upper left and upper right side and may be accessed by removing the cabinet side panels. The right (viewed from the front) commutator CCA is used to switch the RF signals to all the odd antennas, and the left commutator CCA drives the even antennas. Each commutator has twenty-six N type RF connectors and two 37-pin D-shell connectors.

1.2.2 Portable Maintenance Data Terminal (PMDT)

The standard PMDT consists of a laptop computer and is the input/output device for controlling and communicating with the DVOR system. Station control, adjustment and monitoring functions are available through the computer, and are accessed via a Windows-based operator interface. An optional external mouse may be used with the laptop computer for ease in operation. An optional desktop PC is available as a substitute for the standard laptop computer. Also, an optional printer is available for use with either the laptop or desktop PC.

Station security control is provided through a three-level password system. Complete access to the system for adjustments and measurements is provided at level 3. Modification of non-critical parameters is available at level 2, and read-only access is available at level 1.

All functions available on the local PMDT are available remotely via a modem and dial-up telephone line to an optional remote laptop or desktop PC running the PMDT software. Refer to [Section 3](#) on the use of the PMDT.

1.2.3 Transmitting Antenna System

The DVOR antenna system consists of a single carrier antenna assembly at the center of the counterpoise, and 48 sideband antenna assemblies spaced equally in a 44' diameter circle concentric with the carrier antenna assembly. All antennas are enclosed in small, weatherproof, fiberglass radomes.

1.2.3.1 Carrier Antenna

Refer to [Figure 1-7](#). Carrier Antenna is a single Alford loop on a support plate. The antenna is supported above the counterpoise by a metal pedestal. This antenna is electrically tuned to the station frequency by means of two large, air-dielectric capacitors. This antenna is designed to function with a collocated distance measuring equipment (DME) or tactical air navigation (TACAN) antenna system. When required, a metal pipe passes through the center of the support plate and center of the antenna. The pipe serves as a conduit for feed lines and cables to a DME or TACAN antenna and obstruction lights, when installed. When collocated with a TACAN, the antenna is enclosed within a larger fiberglass shelter called a “walk in” radome. [Figure 1-8](#) depicts the carrier antenna provided for use without collocated DME or TACAN antennas. The hole through the center is not present and the radome and pedestal are the same as the sideband antennas.

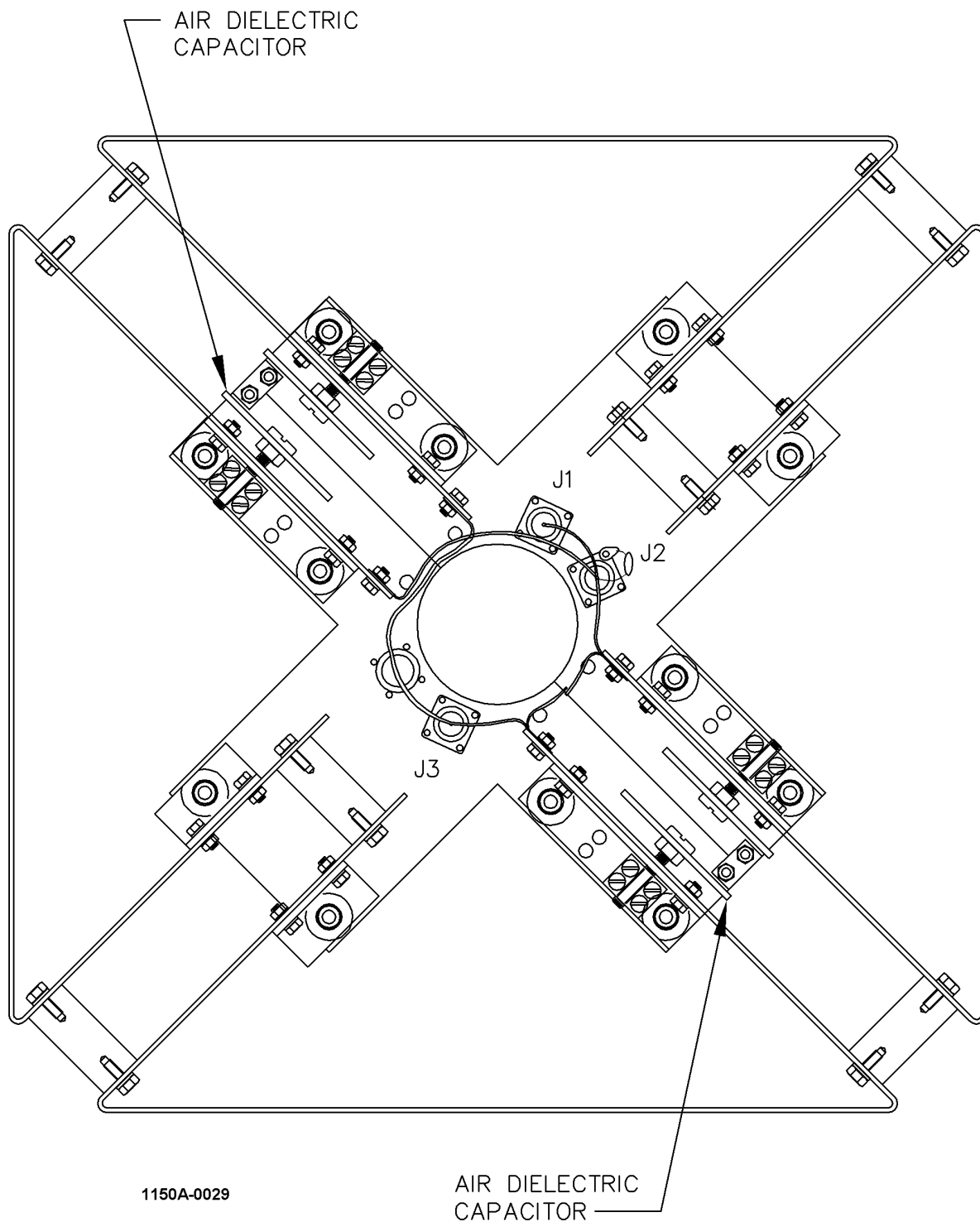


Figure 1-7 Carrier Antenna for collocation with DME/TACAN

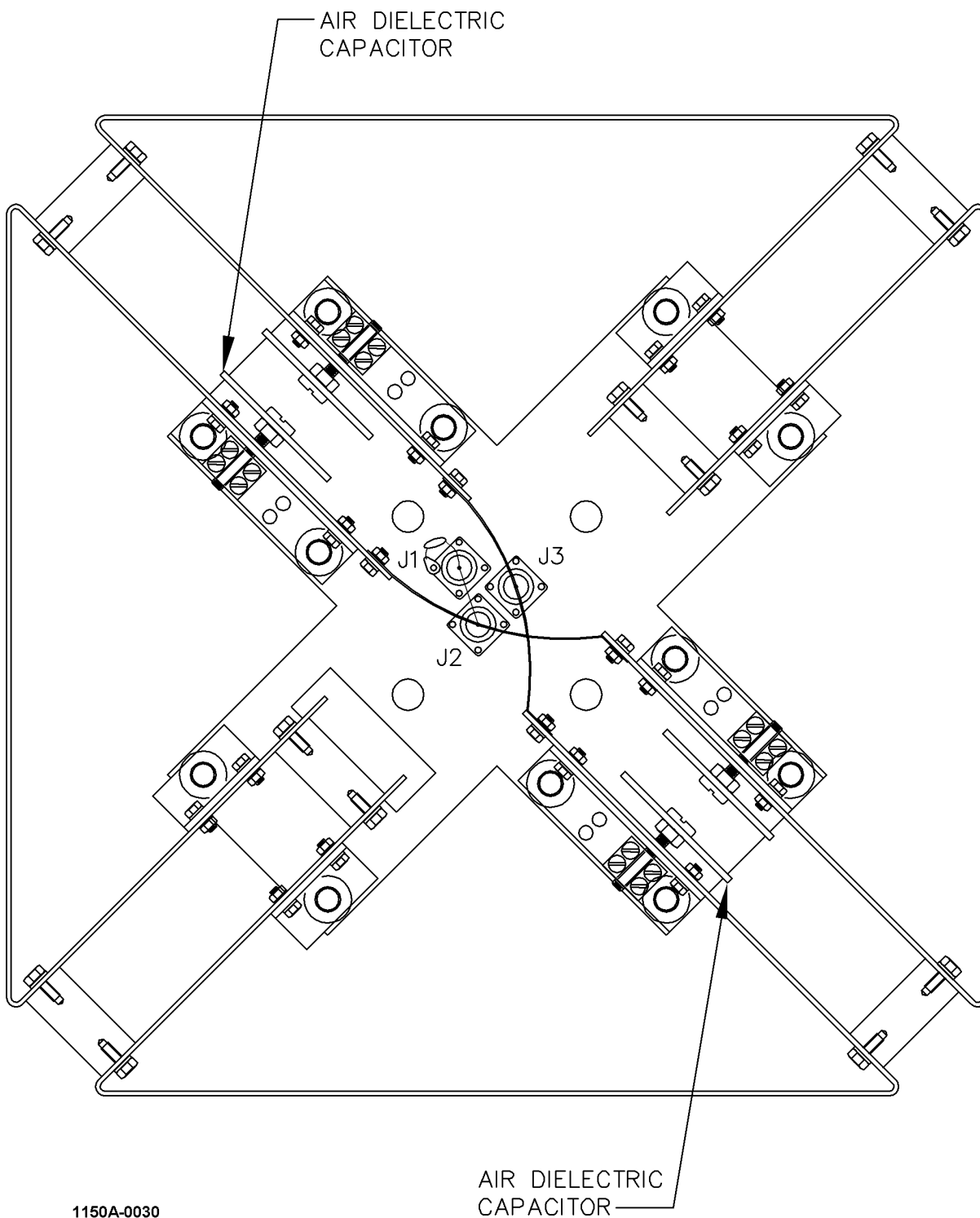


Figure 1-8 Carrier Antenna without DME/TACAN

1.2.3.2 Sideband Antenna

Refer to [Figure 1-9](#). Each sideband antenna is an Alford loop, similar to the carrier antenna but without the large hole in the support plate. This antenna is electrically tuned to the station frequency by means of single high voltage, glass capacitor. The antennas are mounted independently on individual support plates, supported above the counterpoise by metal pedestals equal in height to the carrier antenna.

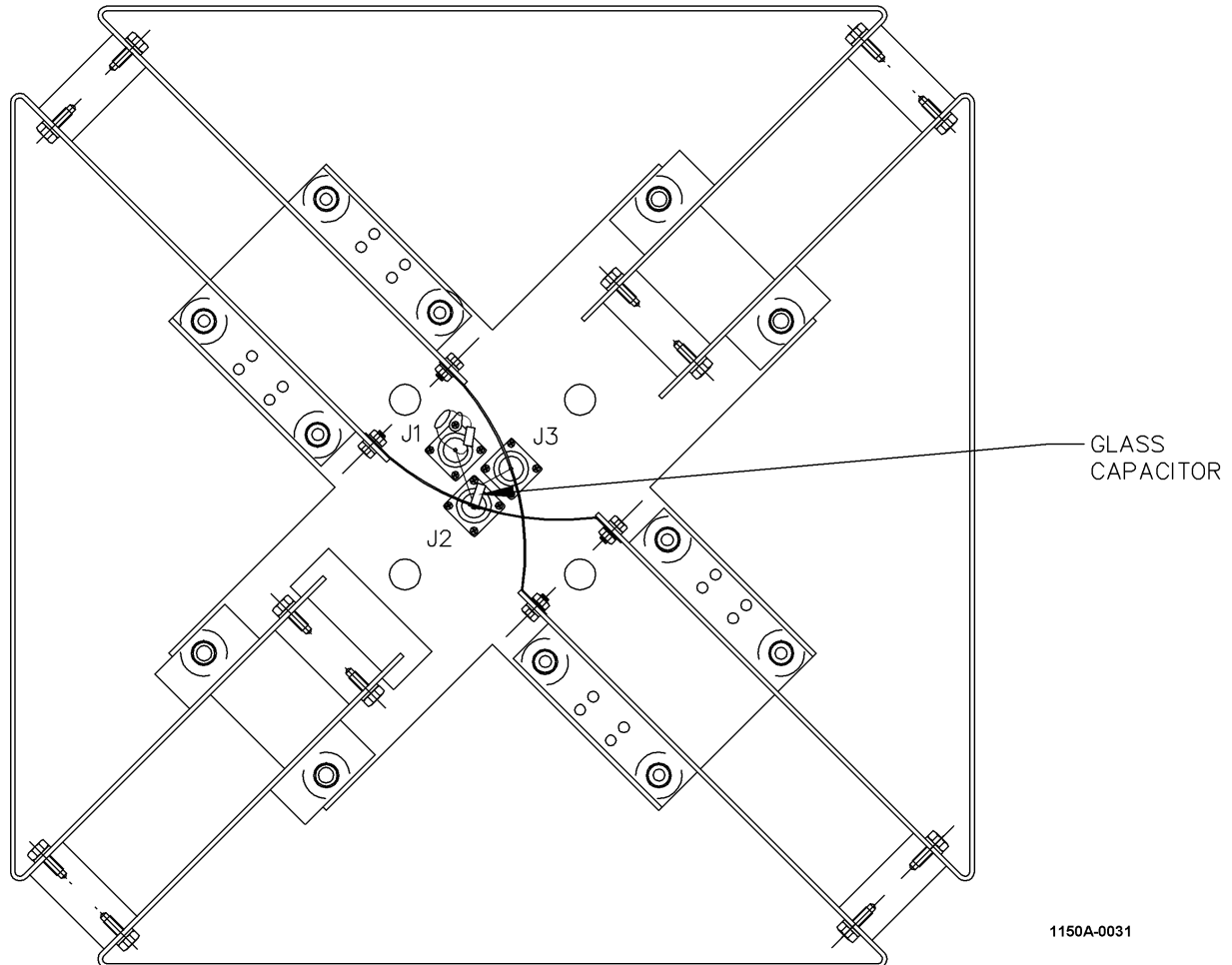
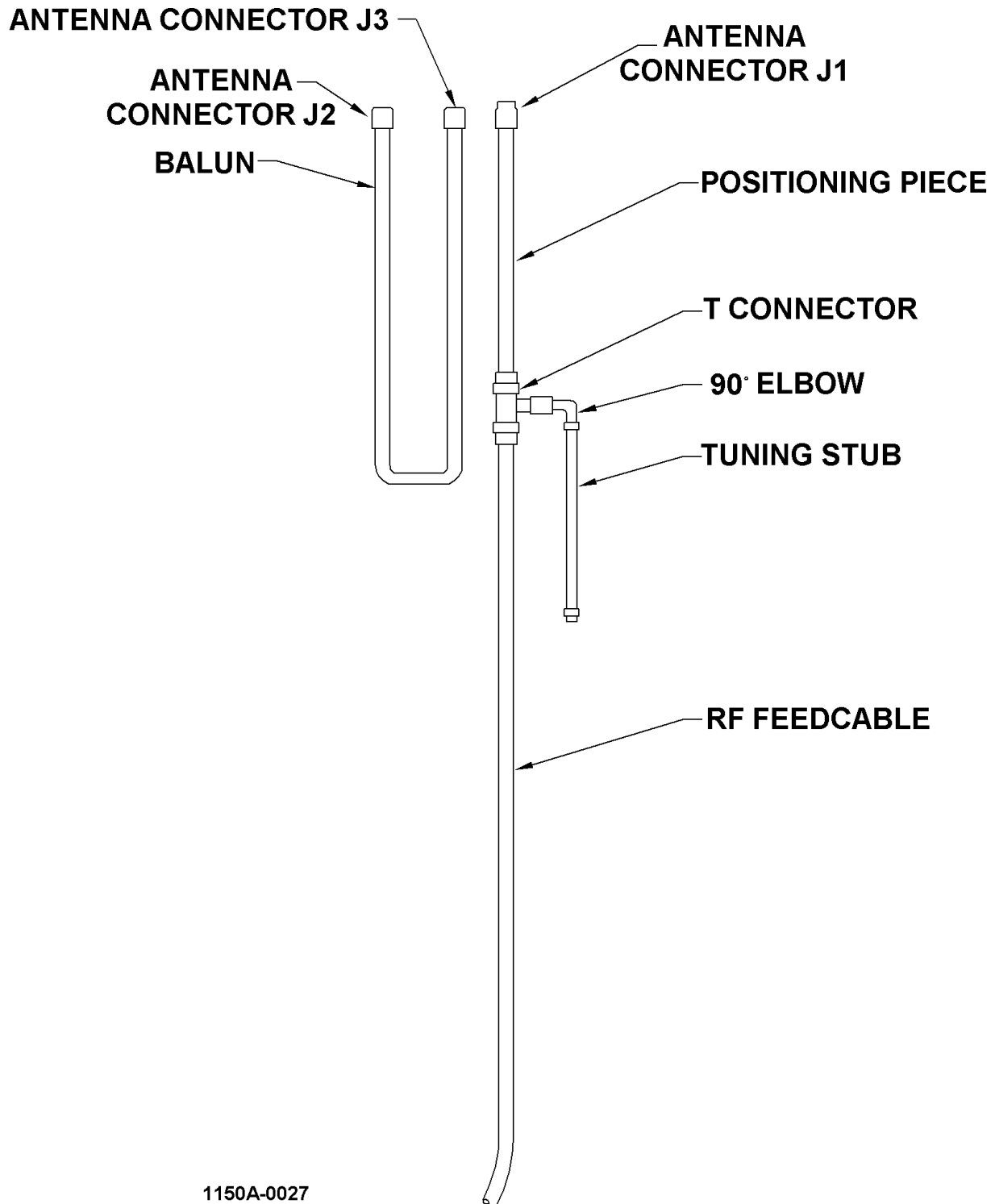


Figure 1-9 Sideband Antenna

1.2.3.3 Balun

Refer to [Figure 1-10](#). The balun is a line section approximately 180 degrees in length that hangs directly under the center of the antenna inside the pedestal and is used to develop a balanced signal output from a coaxial line input.



1150A-0027

Figure 1-10 Balun, Tuning Stub, and Positioning Piece

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1.2.3.4 Tuning Stub

Refer to [Figure 1-10](#). The tuning stub is a line section made out of RG-214 cable with a connector on one end and open at the other end. The function of the stub is to supply the needed capacitive reactance to make the point of the stub attachment pure resistive.

1.2.3.5 Positioning Piece

Refer to [Figure 1-10](#). The positioning piece is a length of RG-214 cable with a connector at each end. The purpose of the positioning piece is to place the tuning stub at a point on the input line where the resistive component of the complex impedance is equal to the characteristic impedance of the line (50 ohms). The length of the positioning piece is factory selected for the frequency band of operation.

1.2.3.6 Pedestal

Refer to [Figure 1-11](#). The pedestal is a 6061-T6 aluminum tube with mounting plates on each end. The pedestal supports the Alford loop antenna and provides a conduit for the feed cable, balun, positioning piece, and tuning stub.

1.2.3.7 Radome

Refer to [Figure 1-11](#). The radome is a fiberglass enclosure that protects the radiating elements of the antenna from the weather and vermin infestation.

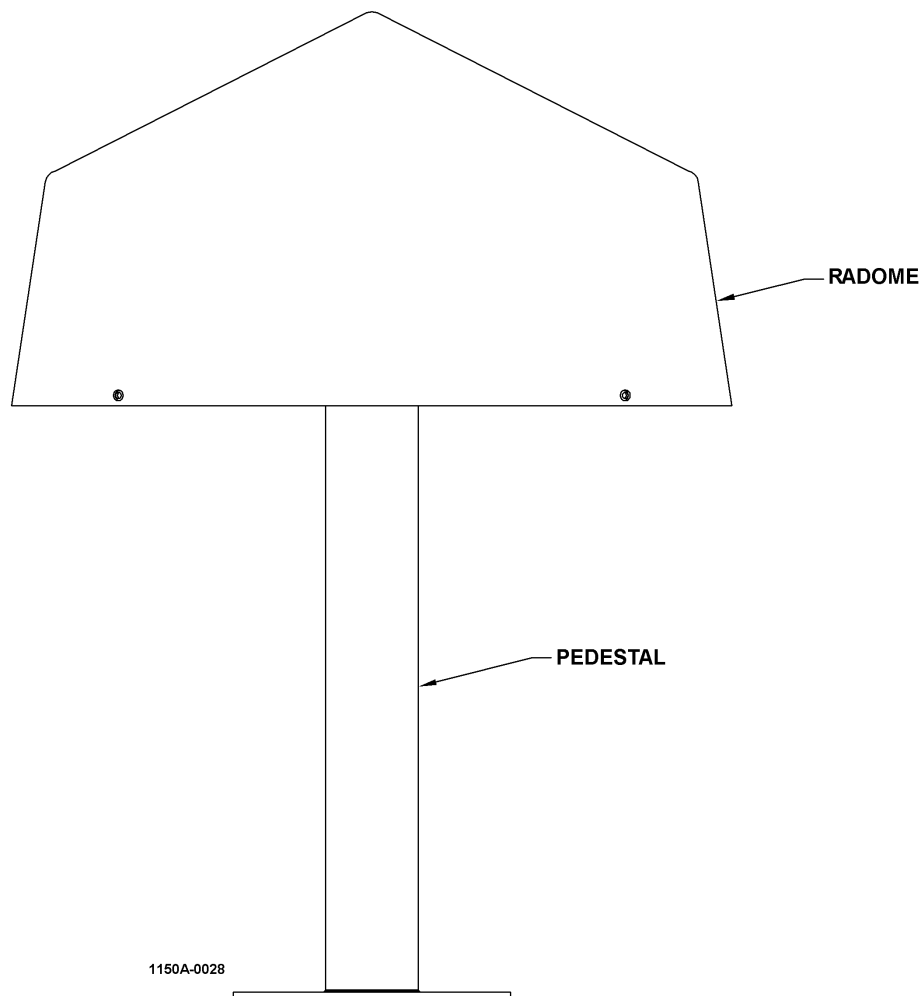


Figure 1-11 Antenna Pedestal and Radome Diagram

1.2.4 Field Monitor Antenna

Refer to [Figure 1-12](#). There are one or two field monitor antennas in each DVOR system. The single dipole antenna is the standard configuration and two antennas are the optional configuration. A cable from the field monitor antenna enters a two way power splitter in the VOR transmitter cabinet. The two outputs from the power splitter are connected to the two Monitor CCAs. The antenna is installed on a support tower 300 to 360 feet from the carrier antenna. The monitor antenna may be installed on any radial.

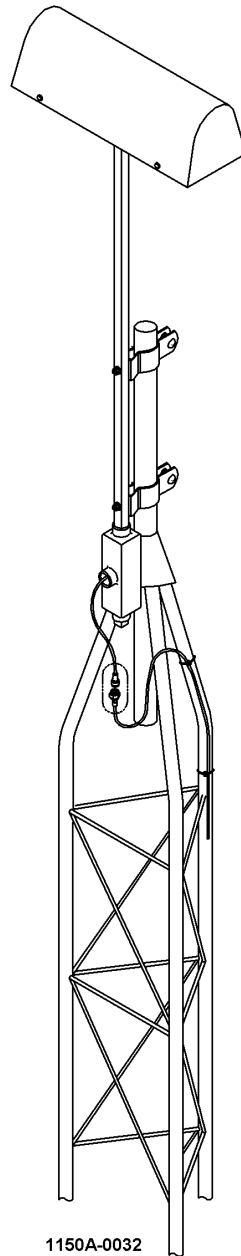


Figure 1-12 DVOR Field Monitor Dipole Antenna

1.2.5 Counterpoise

The counterpoise is a circular, metallic support structure upon which the transmitting antenna system is installed. The counterpoise typically is between 60 and 100 feet in diameter, 8 to 12 feet above ground level. It can be aluminum or galvanized steel and is assembled of segments bolted together.

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1.2.6 Equipment Shelter

The electronic part of the DVOR (transmitter cabinet and commutator rack) is housed in a shelter environmentally-controlled with heating, cooling and ventilation. Normally, the shelter is installed below the counterpoise and directly underneath the carrier antenna.

1.2.7 Battery Backup Unit (Optional)

The battery backup supply contains two battery boxes each containing two lead-acid maintenance-free batteries in a 48VDC configuration. Additional backup capacity can be achieved by adding additional groups of four batteries.

1.3 EQUIPMENT SPECIFICATION DATA

Equipment specifications are listed in [Table 1-1](#).

1.3.1 Transmitter and Antenna System

1.3.1.1 Transmitter

Table 1-1 DVOR Equipment Specifications (Transmitter)	
Parameter	Specification
Carrier Frequency Range:	108 to 118 MHz with 50 kHz channel spacing.
Frequency Control:	Synthesizer
Carrier Frequency Tolerance:	$\pm 0.0005\%$ (5 PPM)
Carrier Output Power:	Transmitter output power adjustable from 25 to 100 Watts (14 to 20 dBW) in 1 Watt increments
Effective Radiated Power:	23 dBW minimum with a transmitter output of 100 Watts
Carrier Level Shift:	less than 0.5% for modulation depth up to 80%
Duty Cycle:	Continuous
Spurious Outputs:	greater than 77 dB below the carrier at 30% modulation
Harmonic Radiation:	Meets or exceeds U.S. FCC requirements. Harmonics of 9960 Hz meet or exceed: Second harmonic >30 dB lower than fundamental Third harmonic >50 dB lower than fundamental Fourth and higher harmonics >60 dB lower than fundamental
Hum and Noise:	With voice, VOR reference and identification inputs, hum and noise on the carrier are more than 30 dB below the audio level equivalent of 30% modulation.
Maximum Range:	Line-of-sight, 175 nautical miles at 37,500 feet (11,433 M) above the facility.
Accuracy:	When site meets requirements of ICAO, bearing information on the horizontally-polarized radiation is within $\pm 1.0^\circ$ (at a distance of approximately 1000 feet (300 meters) for all elevation angles between 0 and 60 degrees, measured from the center of the VOR antenna.

Table 1-1 DVOR Equipment Specifications (Transmitter)	
Parameter	Specification
Reference Phase Signal	(30 Hz AM)
Frequency:	30 Hz $\pm 0.01\%$
Modulation Depth:	30% Nominal, 0 to 40% digitally controlled
Variable Phase Signal	(30 Hz FM)
Frequency:	30 Hz $\pm 0.01\%$
Sub-Carrier Signal	(9960 Hz FM)
Center Frequency:	9960 Hz $\pm 0.1\%$
Deviation Ratio:	16 ± 1 at 115 MHz (based on 44 ft diameter of sideband antennas)
Modulation Depth:	30% Nominal, 0 to 50% digitally controlled
Identification Signal	
Keyer Type:	Solid State
Frequency:	1020 Hz ± 0.01 Hz
Modulation Depth:	0 to 20%, adjustable
Harmonic Distortion:	less than 1.0%
Code:	2,3,4 letters in Morse Code
Rate:	8 words per minute
Repetition:	4 times/30 seconds; 3 times with co-located DME
Voice	
Frequency:	300 to 3000 Hz
Modulation Depth:	0 to 30%, adjustable
Harmonic Distortion:	less than 1%
Input Level:	-30 dBm to +2 dBm
Environmental	
Operating Temperature	
Indoor Equipment:	-10° to +55°
Outdoor Equipment:	-50° C to +70°
Relative Humidity	
Indoor Equipment:	95% (non-condensing) at +50° C.
Outdoor Equipment:	100% at +70° C
Wind	More than 100 mph (85 knots) (160Km/hr) with shelter and counterpoise on concrete foundation
Ice and Snow	5cm (2 in.) Ice coating causes negligible course error
Altitude	0 to 4500m (0 to 15,000 ft.)

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1.3.1.2 Antenna System

Table 1-2 DVOR Equipment Specifications (Antenna System)	
Parameter	Specification
Type:	Alford loop
Frequency Range:	108 to 118 MHz, field-tunable
Polarization:	Horizontal
Antenna System Bearing Error:	less than 0.5°
DME Co-Location:	Permits coaxial mounting of DME antenna above carrier
Weather Protection	Fiberglass radome
Blending Function:	$\cos^{.836} X$
Number of Antenna:	48 Sideband, 1 Carrier
Modulation Type:	Double-Sideband
Commutator Type:	Solid-State
Frequency Range:	108-118 MHz broadband, no tuning
Blocking Attenuation (Switches Off)	Greater than 80 dB
Insertion Loss:	0.5 dB maximum
Difference in Insertion Loss:	Less than .05 dB
Phase Balance	Less than 2 degrees
VSWR:	Less than 1.15:1
Lightning Protection	Provided on each Commutator output

1.3.1.3 Field Monitor

Table 1-3 DVOR Equipment Specifications (Field Monitor)	
Parameter	Specification
Antenna Type:	Dipole
Number of Antennas:	1 Standard, 2 Optional
Frequency Range:	108 to 118 MHz
Output:	Composite VOR signal, RF
Installation:	Located at minimum of 91.4m (300 ft) from center of counterpoise and level with counterpoise
Position:	Any azimuth angle
VSWR:	$\leq 1.5:1$ at 112 MHz

1.3.2 Monitor

Table 1-4 DVOR Equipment Specifications (Monitor)	
Parameter	Specification
Configuration:	Dual (“And”, “Or” user selectable)
Azimuth Measurement Resolution:	$\pm 0.01^\circ$
Azimuth Measurement Range:	0 to 360°
Azimuth Measurement Accuracy:	$\pm 0.02^\circ$
Azimuth Readout Indication:	Digital, on the Local Touch Screen display and on the station computer (PMDT)
Phase Shift Control:	Calibrated against test generator
Monitoring of VOR Signal:	At any desired azimuth angle
Adjacent Channel Rejection	> 50 dB
Monitor Limits	
Bearing:	0.1 to $\pm 5^\circ$ from any radial, 0 to 360°
30Hz AM Amplitude:	$\pm 2\%$ from 30% nominal, adjustable, 21 to 39%
30Hz FM Amplitude:	± 2 from nominal ratio 16, adjustable, 12.6-19.4 (ratio)
9960 Hz Subcarrier Amplitude:	$\pm 2\%$ from 30% nominal, adjustable, 21 to 39%
Level Alarm:	± 3 dB from nominal carrier power, adjustable ± 9 dB from nominal
Identification:	Incorrect code, lack of ident, continuous ident, or level change of $\pm 3\%$
Stability of Alarms	
Phase Shift:	better than $\pm 0.1^\circ$
Amplitude:	better than $\pm 0.1\%$
Alarm Time Delay:	Adjustable, 4-99 seconds
VSWR Measurement:	Continuous measurement and display of individual sideband antenna VSWR. Maintenance alert if limit exceeded.
VSWR Alarm Limit:	1.0 to 3.0:1
Notch Monitor	50% from reference value, adjustable 0 to 100% nominal

1.3.3 Mechanical and Electrical

Table 1-5 DVOR Equipment Specifications (Mechanical and Electrical)	
Parameter	Specification
Size of Cabinet:	72" H x 24" W x 24" D (183cm H x 61cm W x 61cm D)
Weight of Cabinet:	450 lb (205 kg) maximum
Mounting	Floor mount
Primary Power:	85 to 264 VAC, 47 to 63Hz, single phase
Standby Power:	Standard 48 VDC no-break battery backup system (four 12V-65Ah batteries) with charger provides approximately 4.0 hours of operation. Optional 48VDC no-break battery backup system (four 12V-100Ah batteries) with charger provides approximately 6.0 hours of operation.
Power Consumption:	Single Stations: 375VA (typical), 625 VA with maximum battery charging. Dual Stations: 500VA (typical), 750VA with standby transmitter operating for test purposes.
Duty Cycle:	Continuous

1.3.4 Remote Control System

1.3.4.1 Design Features

The optional remote control system consists of a Model 2238 or Model 2240 Remote Control and Status Unit (RCSU) and one Remote Slave Unit (RSU). The 2238 RCSU is designed for installation in a standard 13.33 cm (5.25") rack panel space in a Control Tower Equipment Room. The 2240 RCSU is designed for installation in a standard 6.66 cm (2.12") rack panel space in a Control Tower Equipment Room and the RSU's are designed for installation at a controllers' position in the Tower Cab. The 2238 RCSU contains provisions for six ILS Localizer, Glideslope, Outer Marker and Middle Marker and DME and VOR stations. The 2240 RCSU contains provisions for up to three ILS Localizer, Glideslope, Outer Marker, Middle Marker, DME, or VOR stations. Each of the respective stations is connected to the RCSU by an RF data link or a single dedicated telephone line pair. The RSU is then slaved to the RCSU by interconnecting cables.

1.3.4.2 RCSU Controls and Indicators

Table 1-6 RCSU Controls and Indicators	
<u>Indicators</u>	<u>Controls</u>
Main On	System On/Off
Standby On	System Transfer
Off	RMS Reset
Maintenance Alert	
System on Batteries	
Primary AC Power Fail	
System on Local Control	
Monitor #1 & #2 Normal Alarm Bypass	
Monitor Mismatch	
Aux Equipment On/Off	
Comm Fail	
Common on RCSU	
Low Volume	RSCU Alarm Silence
Audible Alarms	Lamp Test
	I/O Status & Control
	Volume Controls
Control Functions/Indicators for Associated RSU	
Operational Status	
RSU Module Power Status	
Comm Failure w/RSU Module	

1.3.4.3 RSU Controls and Indicators

Table 1-7 RSU Controls and Indicators	
<u>Indicators</u>	<u>Controls</u>
VOR System	Alarm Silence/Cancel
Main On	Alarm Volume Up/Down
Main Alarm/Off	Self Test
Standby On	Lamp Intensity Up/Down
Standby Alarm/Off	
Maintenance Alert	
DME System (Co-Located w/VOR)	
Main On	
Main Alarm/Off	
Standby On	
Standby Alarm/Off	
Maintenance Alert	
Aux 1 On/Off	
Aux 2 On/Off	
RSU AC Power Ok/On Batteries (when optional Battery Backup is installed)	
RSU Communications Failure	
Audible Alarm	

1.3.5 Remote Maintenance Monitoring System (RMM)

1.3.5.1 Design Features

The Remote Maintenance Monitoring (RMM) system operates in conjunction with the local control system and Portable Maintenance Data Terminal (PMDT). The RMM is an integral part of the DVOR system and consists of the various embedded sensors, internal monitoring points, microcomputers and built-in test equipment to remotely monitor, control, record and certify proper operation of the system.

The RMM system is accessed locally through the built-in RS-232 port, and remotely through a dial-up telephone line, fiber optic line, radio link or GSM telephone connection, and a Portable Maintenance Data Terminal (PMDT). The telephone line, fiber optic line, radio link, or GSM telephone connections are all optional. The choice of which communication system is to be utilized for a particular installation, and who is to supply it, is determined by individual contract.

In addition, the Remote Control and Status Unit (RCSU) computer and modem may be utilized for dial-up access to the RMM system.

1.3.5.2 RMM Functions

The RMM system provides the following key functions:

- a. System control.
- b. Adjustment of transmitting parameters.
- c. Monitoring of system performance and certification parameters. Compares the outputs of each of the monitoring devices at least once per second to determine alarm and alert status by comparing the monitored values to pre-determined limits.
- d. Adjustment of all alarm and alert monitoring limits.
- e. Monitor Certification through the system test generator.
- f. Storage of monitor alert and alarm data, control settings, operational parameters and limits, initialization data, data files and fault history locally within the RMS. Storage of parameters is backed by either lithium battery or EEPROM for a non-volatility of 90 days or greater. DVOR parameters may be stored to and retrieved from the PMDT for a permanent record.
- g. System Fault Diagnostic routines with result reporting and storage in memory. "On-Air" diagnostic routines may be initiated either locally at the station or remotely. By default, diagnostic routines which require the station to be NOTAMed out of service must be run locally. The station may be user re-configured, if desired, to allow all diagnostic routines to be run from a remote location.
- h. Monitoring of routine maintenance parameters including voltages and currents and antenna VSWR.
- i. Monitoring of environmental parameters (when optional sensors are installed).
- j. Monitoring the presence or absence of Primary AC Power applied to the system.
- k. Printing of menus and all display/parameter values (when optional printer is supplied).
- l. Provide clock calendar function within the RMS. The display is date, hours, minutes and seconds. The current time and date may be set from the PMDT. The RCSU provides the master clock update at periodic intervals. The accuracy is to within 15 seconds per month and retains the clock/calendar function even when power is lost by the use of a lithium battery. The lithium battery can maintain the operation of the clock for up to 180 days.
- m. Provide building security monitoring (optional). For this system, an intrusion sensor is installed on the DVOR equipment shelter door. If the door is open longer than 0.25 seconds, and the security feature has not been bypassed through the PMDT within a programmable period of 0 to 5 minutes, an alarm message is generated. Disconnecting the PMDT starts a 0 to 30 minute programmable timer before the intrusion sensor is reset. The default settings are 5 minutes for the bypass period and 30 minutes for the reset period. Activation, disabling, reset and bypass of the Intrusion sensor is supported both locally and remotely.
- n. Provide monitoring of an optional ionization type smoke detector. Detection of smoke generates an alarm message.

1.4 EQUIPMENT AND ACCESSORIES SUPPLIED

Table 1-8 is a list of all major equipment and accessories supplied.

Table 1-8 Equipment and Accessories Supplied				
Quantity	Nomenclature	Unit Number	Dimensions (in inches)	Weight
1	Electronics Cabinet	1	72" H x 24" W x 24" D (183cm H x 61cm W x 61cm D)	450 lbs (205kgs)
49	Transmitting Antennas	E1 thru E49	20.25"W x 20.25"D x 5.5"H each	13 lbs (5.9 kgs)
1	Field Monitor Antenna	4	Prior to assembly: 5.5"W x 13"D x 6.5"H	20 lbs (9.1 kgs)
1	Portable Terminal (PMDT)	3		
	Consisting of:			
	IBM Compatible laptop computer		13"W x 13.25"D x 3"H	10 lbs (4.5 kgs)
	PMDT Software			
1	Battery Backup System (12V-65Ah)		36"H x 18" W x 18" D	231 lbs (105kgs)

1.5 OPTIONAL EQUIPMENT

Table 1-9 and Table 1-10 contain a list of optional equipment that can expand the capabilities of the VOR system or aid a technician in maintenance and troubleshooting.

Equivalent test equipment can be substituted for that recommended.

Table 1-9 Optional Test Equipment		
Quantity	Nomenclature	Part No.
1	Oscilloscope	950259-0000
	Oscilloscope; Dual Trace, BW $\geq$ 25 MHz	
	Delayed Sweep	
1	Frequency Counter	950260-0000
1	RF Wattmeter	950258-0000, Bird Model 43
1	5-W Wattmeter Element	950552-0301, Bird 5B
1	100-W Wattmeter Element	950552-0405, Bird 100C
1	250-W Wattmeter Element	950552-0306, Bird 250B or 950552-0406, Bird 250C
1	RF Sampler Element	950262-0000, Bird 4274-025
1	Digital Multi-meter	950257-0000
	3-1/2 Digit	
1	Torque Wrench	399003-0000
	(For SMA RF Connectors)	
1	Adapter, BNC Female to Phone	180218-0000
2	Dummy Load, 5-Watt, Type N-Male	950270-0000, Bird 5-T-MN

Table 1-10 Optional Station Equipment		
Quantity	Nomenclature	Part No.
1	Battery Backup System 12V-100Ah	470639-0003
1	Environmental Sensors (Smoke, Temperature, Intrusion)	470357-0003
1	Extender Cables	470449-0001
1	Wattmeter Bodies Kit	470451-0001
1	Field Monitor	
	Obstruction Lighting	
	Incandescent - 120V	470630-0001
	- 240V	470630-0002
	LED - 120V	470630-0003
	- 240V	470630-0004
1	Printer – Universal AC Input	950311-0003

2 TECHNICAL DESCRIPTION

2.1 INTRODUCTION

The Model 1150A DVOR system is a dual transmitter system, with dual monitoring facilities. It is designed for terminal and en route navaid operation. The VOR is identified by a specifically assigned two to four letter Morse code identity and may also include voice identification. In addition automatic terminal information service (ATIS) information may be modulated onto the VOR signal with a standard input connection. The DVOR can be collocated with DME to provide distance information in addition to bearing data.

The DVOR concept is based on the 360° radials which originate from a transmitting station and on the airborne equipment which resolves the particular radial data from the station. The resolved radial, called line-of-position (LOP) is the displacement angle between magnetic north and the aircraft, as measured from the DVOR antenna. Therefore, regardless of its heading, an aircraft which is on the 0° radial is north of the DVOR station. The magnetic course to the station is the reciprocal of the radial. In addition, to/from orientation data, relative to the DVOR station, is also resolved by the airborne equipment.

2.2 OPERATING PRINCIPLES

Operation of the DVOR is based on the phase difference between two 30 Hz signals modulated on the carrier, called the reference phase and the variable phase.

The reference phase signal is obtained by amplitude modulating the carrier with a 30 Hz sine wave signal. This amplitude modulated (AM) signal is radiated omni-directionally in the horizontal plane by the central, carrier antenna. The radiation pattern is a circle, and produces in the aircraft receiver a 30 Hz signal with a phase independent of azimuth.

NOTE

DVOR system requires separately radiated upper and lower sideband frequencies which are displaced ± 9960 Hz from the carrier frequency. The Model 1150A DVOR has synthesizer controlled frequencies which are assigned as follows: carrier (on-channel) station frequency, carrier frequency plus 9960 Hz, carrier frequency minus 9960 Hz.

The variable phase signal is obtained from the 9960 Hz frequency modulated subcarrier which amplitude modulates the carrier. This amplitude modulation of the carrier is often referred to as the space modulation, since it is obtained by adding in space the omni-directionally radiated carrier and the separately radiated upper and lower sideband signals emanating from the ring of sideband antennas. The upper and lower sideband signals are displaced, on average, 9960 Hz above and below the carrier respectively and, when added in correct phase to the carrier, will produce a resultant signal which is amplitude modulated at 9960 Hz.

The subcarrier is frequency modulated at a 30 Hz rate. The sideband signals are sequentially distributed to and radiated from the 48 sideband antennas in such a way as to simulate two diametrically opposed antennas, rotating counterclockwise about the circumference of the sideband antenna ring at 30 revolutions per second, with one antenna radiating the upper sideband signal and the other the lower sideband signal. Since the effective length of the path of travel between the rotating sideband sources and the distant point of reception varies at a 30 Hz rate, the observed frequency of the sideband signals varies also at a 30 Hz rate (i.e., the sidebands) and therefore, the subcarrier is frequency modulated at 30 Hz.

The amount of frequency deviation is proportional to the diameter of the sideband antenna ring expressed in wavelengths at the operating frequency. Setting the diameter to 44.0 feet (13.4 meters) produces peak frequency deviation of 480 Hz at a frequency of 113.85 MHz, 454 Hz at 108 MHz and 497 Hz at 118 MHz. [Figure 2-1](#) depicts a typical RF spectrum of a DVOR with an operating frequency of f_c . The corresponding deviation ratio varies therefore from 15.13 at 108 MHz to 16.57 at 118 MHz.

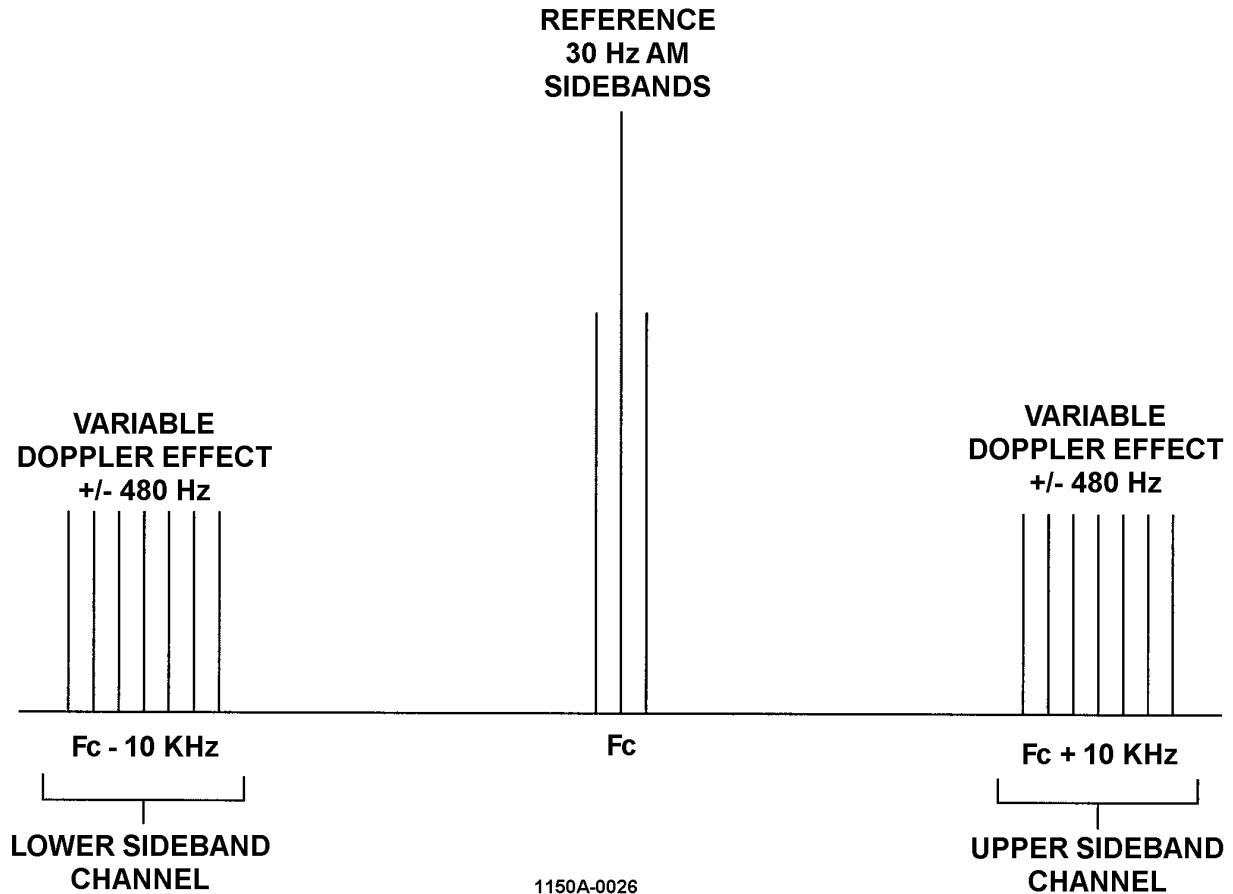


Figure 2-1 RF Spectrum of a Doppler VOR

The deviation frequency is determined by the formula:

$$f_d = \omega \lambda \pi$$

Where: f_d equals the deviation frequency in hertz.

ω equals the angular velocity of the signal (30 Hz).

λ equals the diameter of the ring in wavelengths.

π equals 3.14.

$$r_d = \frac{f_d}{30}$$

In the aircraft receiver, a 30 Hz signal is extracted from the 9960 Hz FM subcarrier. The phase of this second 30 Hz signal varies linearly with the change of the azimuth bearing of the receiving point; for each degree of azimuth change, the phase of the 30 Hz variable phase signal changes by one degree.

The sequential energizing of the sideband antennas and the 30 Hz amplitude modulation of the carrier are time related in such a way that the reference and the variable phase 30 Hz signals are in phase at zero degrees (0) magnetic from the DVOR station. As the receiving point is moved clockwise around the station, the variable phase signal (30 Hz FM) begins to lead the reference signal (30 Hz AM). For example, for the observer west of the DVOR, the 30 Hz FM signal leads the 30 Hz AM signal by 270 degrees. The aircraft receiver determines the phase difference between the two 30 Hz signals and thus it's bearing in degrees (magnetic), relative to the station, as the number of degrees by which the 30 Hz AM signal lags the 30 Hz FM signal.

2.2.1 DVOR Antenna Principles

The DVOR antenna system simulates a rotating arm with a transmitting antenna at each end, radiating the upper sideband signal from one end and the lower sideband signal from the other end. This is achieved electronically by using 48 antennas spaced equally around the perimeter of a circle 44 feet (13.4 meters) in diameter, with an antenna in the center of the circle radiating a reference carrier.

Consider the effect of simulated antenna rotation on an airborne receiver. When the upper sideband source is moving toward the aircraft, the Doppler effect causes the airborne receiver input frequency to become higher than $f_c + 9960$ Hz, and for the lower sideband source, which is moving away, the frequency becomes less than $f_c \pm 9960$ Hz, f_c being the carrier frequency. The frequency difference changes sinusoidally due to the simulated rotation. The difference is at a maximum when the line joining the two radiating antennas is perpendicular to the radial to the aircraft. The difference is equal to zero when the two sideband sources align with the radial to the aircraft since, at that moment, the distance between each sideband source and the receiver does not vary.

The moment of zero frequency deviation is different for different positions of the aircraft around the station. Therefore, the recovered 30 Hz FM signal will have a different phase for each of these different positions. For the receiver North of the DVOR station, the 30 Hz FM signal must be in phase with the 30 Hz AM signal; both signals passing through their positive zero crossings at the same time. To achieve this, the following has to be observed: At the moment that the 30 Hz amplitude modulation of the carrier is passing through its positive zero crossing, the simulated rotating antennas shall align with antenna number 1 (at North) and antenna number 25 (at South), with the North antenna radiating the peak of the lower sideband signal and the South antenna radiating the peak of the upper sideband signal. The lower sideband frequency will be decreasing; the upper increasing. The subcarrier frequency will be increasing from exactly 9960 Hz up and the 30 Hz FM signal will be passing through its positive zero crossing.

2.3 DVOR TRANSMITTER THEORY OF OPERATION

The following paragraphs provide a technical description of the Model 1150A DVOR, its individual components and accessories. Refer to [Figure 2-2](#) for simplified block diagram of the DVOR Transmitter System and [Figure 2-3](#) for a detailed block diagram of the DVOR system.

2.3.1 Simplified System Block Diagram

Refer to [Figure 2-2](#). The transmitter (main and standby) consists of a frequency synthesizer assembly, CSB power amplifier assembly, directional coupler, audio generator CCA, and two sideband generators,

The frequency synthesizer assembly produces the three interrelated RF signals used by the DVOR. The on-channel carrier RF signal drives the CSB power amplifier assembly. The upper and lower sideband RF signals drive the two sideband generator assemblies.

The CSB power amplifier assembly amplifies and modulates the carrier RF signal to the operational output level.

The CSB power amplifier also provides a sample portion of the RF energy to be used as an error correction that is sent back (feedback) to the frequency synthesizer assembly.

The bi-directional coupler obtains a sample of the forward and reflected RF carrier power. The sampled forward and reflected power is directed to the RF monitor assembly where the signal is used in the detection and analysis process circuitry.

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The RF monitor assembly functions as an RF detector/amplifier and distributor of the detected RF signals. The assembly also contains the dummy load for the standby transmitter carrier RF signal. The RF Monitor includes built-in dummy loads for the four sideband signals.

The Audio Generator CCA generates and processes all of the modulation signals transmitted by a DVOR transmitter and generates the power level and phase control signals needed to operate the transmitter and commutator. It is also responsible for monitoring the operational status of the transmitter.

The DVOR system uses two sideband generator assemblies for each transmitter. Each sideband generator contains one Sideband Generator CCA.

The Sideband Generator amplifies the CW RF signal from the frequency synthesizer to the operational output power levels.

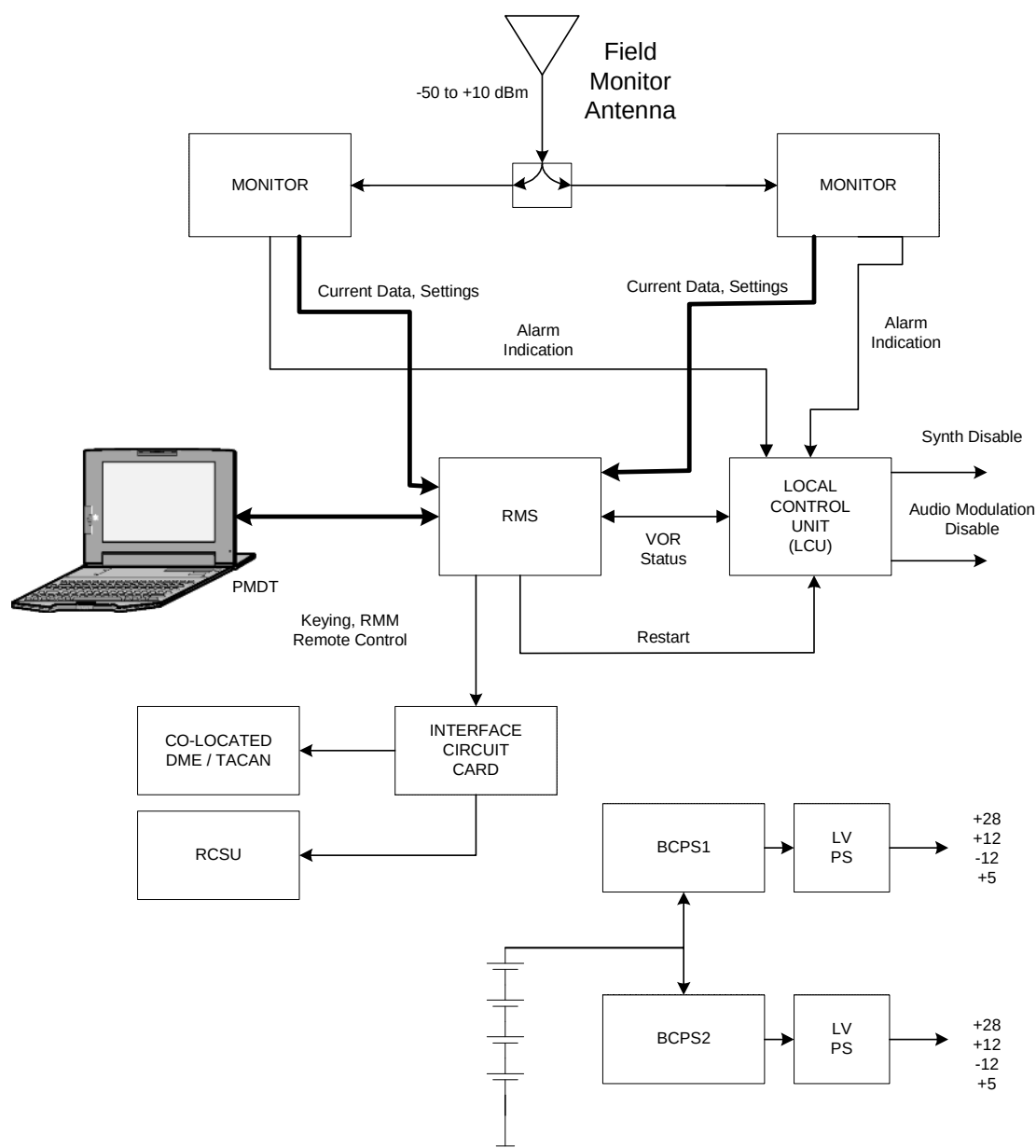


Figure 2-2 Simplified DVOR Control and Monitoring Block Diagram

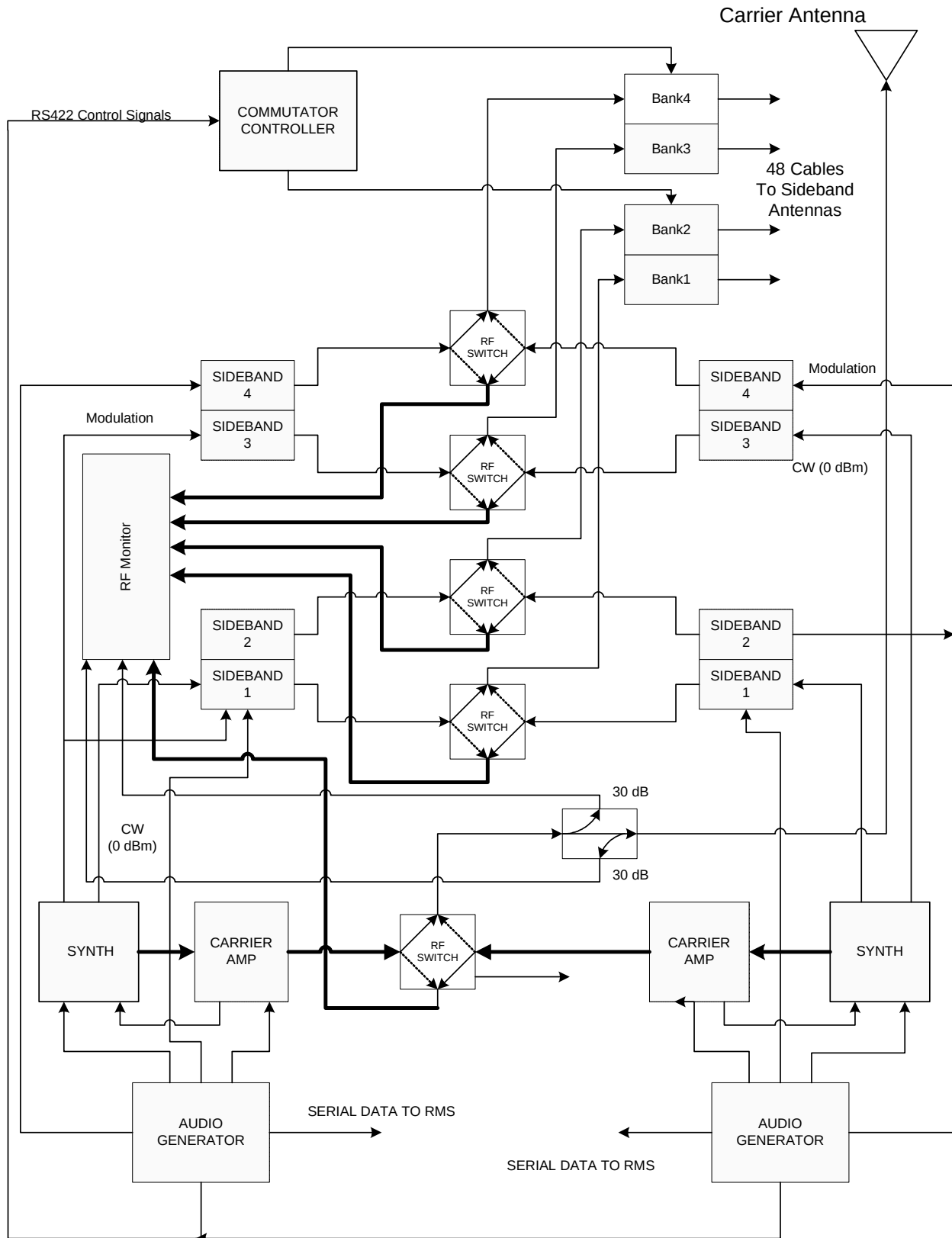


Figure 2-3 Simplified DVOR Transmitter Block Diagram

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Refer to [Figure 2-3](#). The Remote Maintenance System Processor (RMS) handles all command, control, communications and information for the DVOR system.

A monitor antenna located on any radial in the far field provides an RF signal which is equally divided and sent to the VOR monitors for processing and analysis.

The VOR monitor CCA works independently from the transmitter and from each other; however, the alarm control features of both monitors can be organized to function in a logical AND or logical OR arrangement.

The Local Control Unit (LCU) is responsible for turning off the transmitters and transferring from Main to Standby transmitters. The LCU contains hardware logic that acts on alarm inputs from the Monitors. The LCU has two controls to each transmitter to remove radiation in case of out-of-tolerance conditions. The LCU is responsible for controlling the transfer relays and reporting the current state of the relays as to which transmitter is connected to the antenna.

The transmitter cabinet contains the assemblies needed to control the electronic switching of the sideband antennas.

2.3.1.1 Electronics Cabinet (Unit 1)

The VOR electronics cabinet assembly contains all of the electronic assemblies that generate, control, and monitor the DVOR modulated radio frequencies. The cabinet contains three separate card cage assemblies that hold the transmitter and RMS modules. It provides the means to physically secure the modules within the electronics cabinet and provides for the interconnection of the modules. Attached, but independent from it, are the five coaxial latching relays mounted to the middle card cage directly behind the RF monitor assembly. The relays are latched by applying a ground pulse to either the latch or release coil. The relays are powered from a common 28 volt source. The relays switch the ten RF inputs (main and standby) between the antenna system and the dummy loads. They also provide DC logic signals which are used by the Monitors and Audio Generators to sense which transmitter system is connected to the antenna system. The DC logic signal is supplied to the Audio Generator to enable commutator switching signals and identification to be applied from the on-air Audio Generator CCA.

2.3.2 System Block Diagram Theory

Refer to [Figure 2-2](#) and [Figure 2-3](#). The DVOR system block diagram depicts the main components (both optional and required) of a functional station and identifies primary signal, control and voltage paths within the station.

The DVOR system is contained in an electronics cabinet assembly. Connected to this DVOR cabinet are the PMDT, carrier antenna, sideband antennas, field monitor antenna, and optional backup batteries.

The electronics cabinet is next broken down into its main components which are a Local Control Unit (LCU), RMS, main and standby transmitters, VOR monitor CCAs, RF monitor, changeover relays, battery charger power subsystems (BCPS).

The LCU contains the displays that provide a visual indication of the status of the VOR system along with control to change the operational states of the DVOR.

The RMS group handles all command, control, communications, and information for the station.

The main transmitter consists of a frequency synthesizer assembly, CSB power amplifier assembly, directional coupler, audio generator CCA, and two sideband generators. Supplying the voltage for the main transmitter is a stand-alone battery charger power subsystem, and a Low Voltage Power Supply (LVPS).

The frequency synthesizer assembly contains three CCAs. They are the carrier CCA, the Sideband CCA and the Interconnect CCA. This assembly produces the three interrelated RF signals used by the DVOR. The on-channel carrier RF signal drives the CSB power amplifier assembly. The upper and lower sideband RF signals drive the two sideband generator assemblies.

The Audio Generator CCA generates the carrier modulation signals, monitors and controls power levels, and directs the RF phase control signals for the DVOR transmitter.

Each sideband generator contains one CCA within the assembly. Functionally, each sideband generator has two sideband amplifiers on the one sideband amplifier CCA. Each sideband amplifier is designed to amplify and modulate one of the four individual sideband signals used by the DVOR system.

The CSB power amplifier contains one CCA. The CSB power amplifier assembly amplifies the carrier RF signal to the operational power level of the station and modulates it with the specified audio signals. A sample of the RF energy to be used as an error correction feedback signal that is sent to the frequency synthesizer assembly. A second sample of the RF is provided on the front panel test point on the CSB power amplifier assembly. A directional coupler in the carrier feed-line allows sampling of the forward and reflected RF energy.

The RF monitor processes the main and standby RF signals for use by the audio generator and VOR monitor CCAs. The RF monitor contains all the dummy loads, for use by the standby transmitter.

The field monitor antenna cable enters the two way equal power splitter in the cabinet. The outputs of the power splitter feed each of the two VOR monitors for processing and analysis. Each VOR monitor CCA works independently from the main transmitter and from each other; however, the alarm control features of both monitors can be organized to function in a logical AND or logical OR arrangement.

2.3.2.1 Frequency Synthesizer (1A3A1, 1A3A11)

The Synthesizer assembly generates a three RF signals (carrier, upper and lower sidebands) for the VOR transmitter. There are three boards in the Synthesizer Assembly. The Carrier board provides the carrier frequency (see [Table 9-4](#)) and the phase control capability for the Carrier Amplifier. The long term phase is kept constant in the carrier amplifier by means of a phase control loop in the synthesizer. The phase control loop also removes unwanted phase modulation in the carrier amplifier due to amplitude modulation.

The sideband board generates the upper and lower sideband frequencies for the Sideband amplifier Assemblies and provides the ability to adjust the sideband generator phase over 360 degrees relative to the carrier. This eliminates the need to cut the antenna cables during installation.

2.3.2.1.1 Frequency Synthesizer Block Diagram Theory

Refer to [Figure 2-4](#). The function of the Frequency Synthesizer Assembly is to create the Carrier, Upper Sideband, and Lower Sideband radio frequencies radiated by the VOR Transmitter. The Synthesizer Assembly is used in both CVOR and DVOR system configurations. The Synthesizer Assembly generates the Carrier Signal using a synthesized PLL and control loop to lock the frequency. In addition to the PLL synthesized RF Generator, there is another phase lock loop in the Synthesizer. This loop is used to maintain the carrier phase relative to the reference RF signal, and correcting for amplitude modulation induced phase mod on the VOR Carrier Transmitter output signal. There are three boards (CCAs) in the 030838-0001 Frequency Synthesizer Module, the 012258 Sideband CCA, the 012262 Interface CCA, and the 012263 Carrier CCA. The majority of the circuitry is located on the 012258 Sideband CCA and the 012263 Carrier CCA; with the test port buffer amplifier and audio generation circuitry on the 012262 Interface CCA.

There is a temperature compensated crystal oscillator, or TCXO, on the 012262 Interface CCA that generates a 10.000 MHz reference signal. This signal is buffered and divided by 50 to create a 200 KHz loop reference signal for the carrier PLL. The 10.000 MHz reference signal is also buffered and sent directly to the Direct Digital Synthesizer (DDS) for processing of the 9960 Hz signal generation.

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Refer to [Figure 2-4](#). The carrier frequency is generated by a PLL synthesizer, referenced to the precision 200 KHz signal. A voltage controlled oscillator, or VCO, generates the RF signal. This signal is buffered, and a portion of the signal fed back to the PLL controller, where it is divided by a programmable divider. The divided output is compared to the precision 200 KHz reference signal in the PLL controller's phase comparator. The phase comparator generates an error voltage signal that is filtered and applied to the voltage control input of the VCO, thus locking the VCO output frequency to the reference. VOR channel selection is accomplished by changing the divide ratio of the PLL controller's divider. This divide ratio is programmed into the PLL controller by a serial port interface (SPI) located in the audio generator CCA. The output of the carrier synthesizer is split and routed to the carrier phaser, the carrier phase reference, the front panel test port buffer amplifier, and the sideband board in the synthesizer assembly.

The test port buffer amplifier is located on the 012262 Interface CCA, on the backside of the frequency synthesizer module. The output of this buffer is attenuated to provide the 10 mW typical carrier frequency output signal available on the front panel SMA connector. The attenuator also serves to provide a resistive load for the buffer when no external load is connected to the SMA connector. The 012262 boards serve as an interface with the Synthesizer (012258) and Carrier (012263) boards to communicate with the system through the backplane. The 012262 board also contains circuitry for sideband generation and power supplies for each of the boards mounted. The 012258 and the 012263 board each have a 30 pin header for connecting to the 012262 Interface board. The 012258 and 012263 boards are mounted in a housing to provide isolation between the carrier and sideband signals.

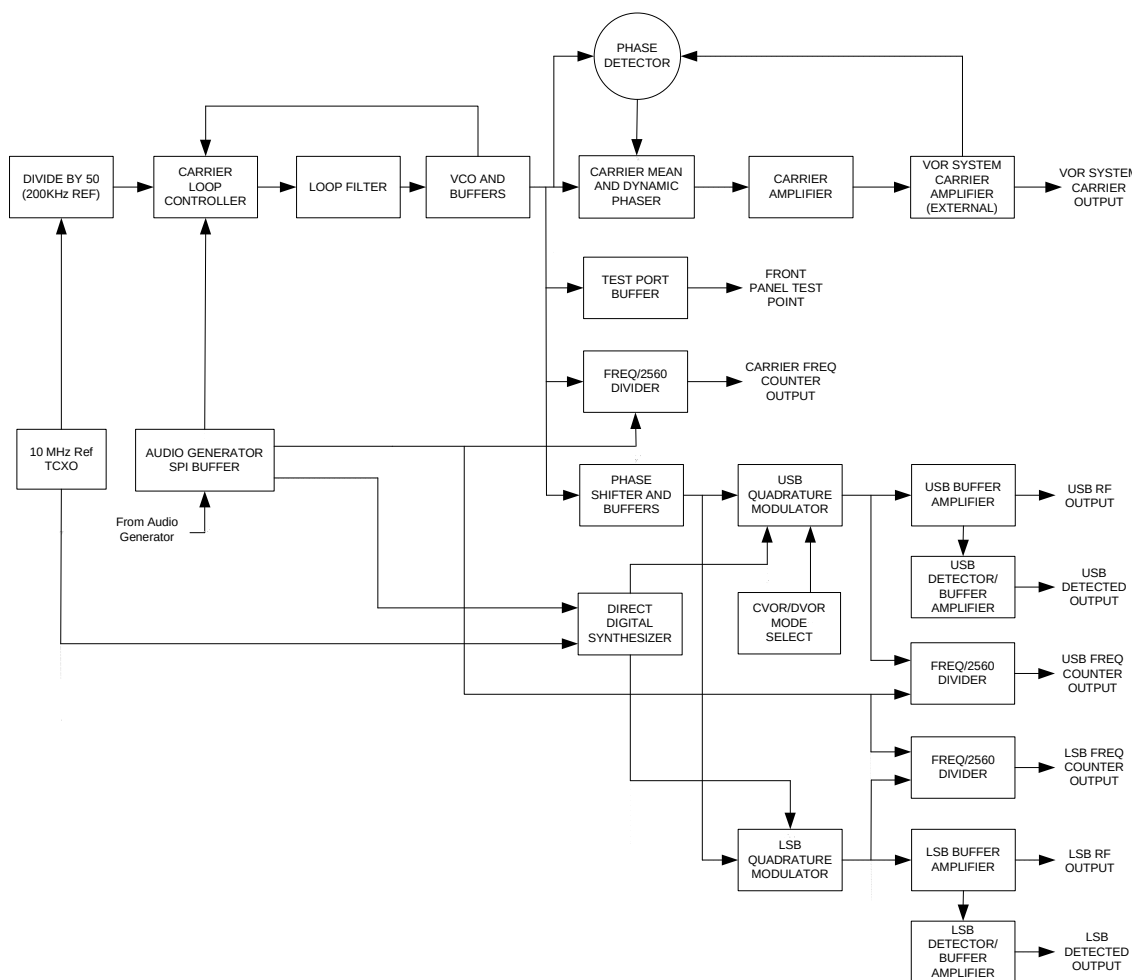


Figure 2-4 Synthesizer Block Diagram

The output of the carrier phaser is amplified by the carrier buffer amplifier, and feeds the high power carrier amplifier module in the VOR system. In the process of amplitude modulation, the VOR carrier amplifier generates undesired phase modulation of the output signal. In addition, the transfer phase of the RF amplifier chain will drift due to temperature. The carrier phaser is used to counter both of these effects. Feedback from the VOR carrier output signal is routed back to the Frequency Synthesizer module. This feedback is representative of the final RF carrier output signal, and has both the 30 Hz amplitude modulation, and the undesired phase shift information.

This carrier feedback signal is first passed through a limiter in the Frequency Synthesizer module to remove the 30 Hz AM information. The output of the limiter is applied to a phase detector where it is compared to the direct output of the carrier PLL synthesizer. The output of this phase detector is a phase error signal, which is amplified and filtered to drive the carrier phaser. The carrier phaser is modulated to maintain the error voltage at zero volts, hence countering the undesired phase shift and phase modulation effects of the VOR carrier RF amplifier.

There is a DC offset input to the carrier phase error amplifier that has the effect of shifting the phase of the VOR carrier output signal with respect to the reference phase in the frequency synthesizer module. This allows for phase adjustment of the carrier to sideband output RF signals to optimize the signal in space characteristics of the VOR radiated signal.

The carrier frequency counter divider is also programmed by the SPI interface from the audio generator board. It provides a fixed divide by 2560 CMOS compatible output for carrier frequency monitoring.

In a DVOR system configuration, the upper and lower sideband frequencies are generated in the synthesizer on the Sideband 012258 CCA. The 012258 CCA derives the upper and lower sideband signals from the carrier signal using two quadrature modulators. The modulators use the 9960Hz signals from the Direct Digital Synthesizer (DDS) on the interface board to mix with the carrier signal. Each sideband signal is generated when the In phase (I) port of the quadrature modulator is 90 degrees out of phase with respect to the quadrature (Q) port of the quadrature modulator. The upper sideband is generated when the I-port is +90 degrees with respect to the Q-port. The lower sideband is generated when the I-port is -90 degrees with respect to the Q-port. This allows the upper and lower sideband signals to always be 9960 Hz offset from the carrier frequency no matter what channel the VOR system is transmitting on.

In a CVOR configuration, only the lower sideband path is used. The upper sideband quadrature modulator is disabled and the lower sideband quadrature modulator is configured to pass only the carrier signal without any frequency offset. This allows only software programming to determine a CVOR/DVOR system configuration using the same module.

Both the upper and lower sideband PLL synthesizers have fixed divide by 2560 dividers that operate in the same fashion as the carrier PLL synthesizer to provide for upper and lower sideband frequency monitoring. In addition, there are detectors on each of the carrier, upper sideband, and lower sideband signals for power detection and monitoring of the synthesizer assembly.

The synthesizer assembly also contains phase control circuitry to digitally step the phase in 90 degree increments referenced from the carrier signal for a coarse phase adjustment. A fine adjustment is made with an analog phaser. The analog phaser is capable of a minimum of +/- 45 degrees of adjustment range. This allows a total adjustment range of 360 degrees for the sideband signal referenced to the carrier signal and reduces cable cutting to phase the VOR system.

2.3.2.1.2 Frequency Synthesizer (1A3A1, 1A3A11) Detailed Circuit Theory

2.3.2.1.2.1 Frequency Reference Circuitry

Refer to [Figure 11-12](#). Oscillator Y1 is a temperature compensated crystal oscillator, or TCXO, which provides a precision 10.000 MHz CMOS compatible signal at its output. Potentiometer R27 is a trim adjustment for Y1 on the 012262 CCA used to make fine adjustments to output frequency and to compensate for possible crystal aging.

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The output of Y1 routes to buffers U15:A and U15:B. The buffer U15:B routes to 1/2 of a dual decade counter U16:A. This counter divides the input signal by 5, then routes it to U16:B, the other half of this IC. Here it is divided by 10 again, creating a 200 KHz signal. The 200 KHz signal is provided to the PLL circuit on the 012263 CCA. The 200 KHz signal is used as a reference for the PLL circuit.

The output of buffer U15:A is the 10.000 MHz reference clock for the direct digital synthesizer (DDS), U17.

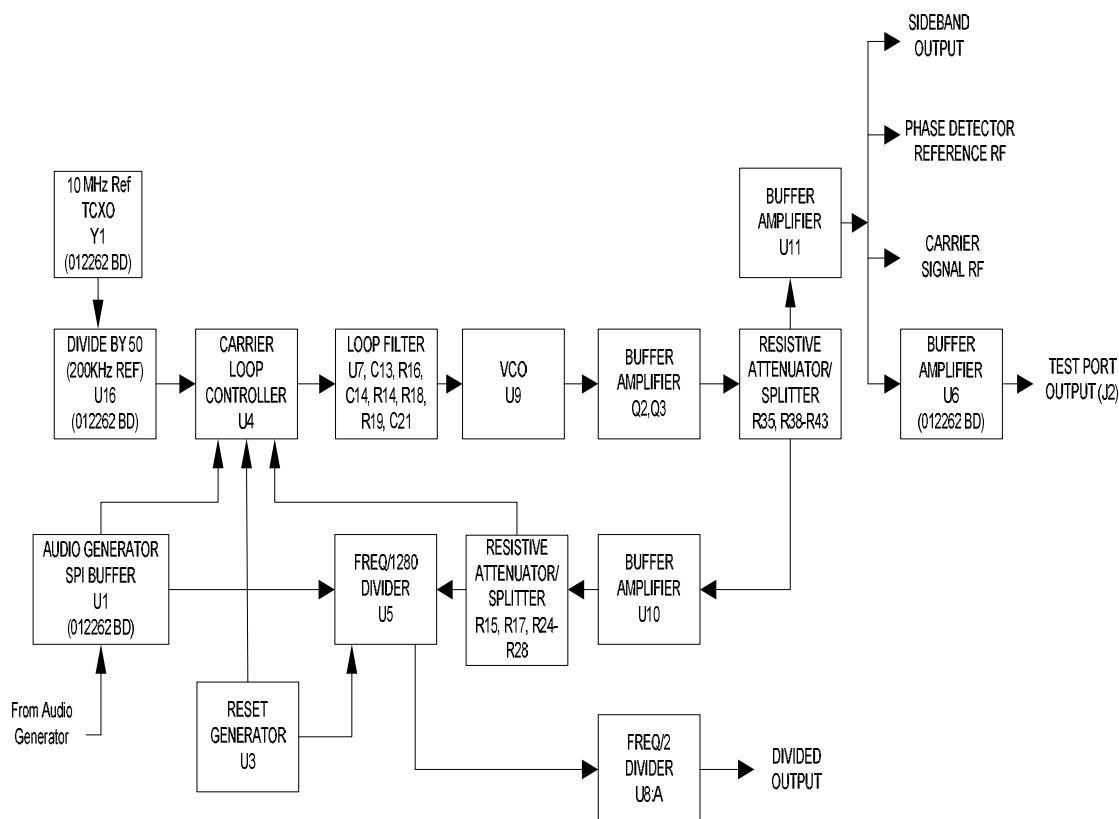


Figure 2-5 Carrier RF Generation Loop

2.3.2.1.2.2 Carrier PLL Synthesizer Circuitry

Refer to Figure 2-5, the Carrier RF Generation Loop block diagram. The carrier radio frequency is generated by a phase lock loop synthesizer. The loop is comprised of a voltage controlled oscillator, or VCO, buffer amplifiers and power splitters, and a loop controller IC with an SPI interface bus.

Voltage regulator U6 provides a +12V supply to Q1 for a low-noise +10V line used by the VCO, U9. This regulator provides isolation from sources of power supply noise which would adversely affect the RF spectrum of the VCO output.

U9, the VCO is an oscillator that generates a RF signal, the frequency of which is proportional to a control voltage at pin 5, the tuning input. The output of this oscillator is applied to a cascode buffer amplifier circuit composed of Q2, Q3, R30 – R32, R34, R36, R37, C27, C30, C35, C36 and L3. The amplifier provides low phase noise and good isolation to external noise influences. Buffer amplifier U11 provides gain to bring the signal back up to approximately +15 dBm, as well as providing additional reverse isolation to prevent signal degradation from noise.

The output of the cascode buffer amplifier is applied to a resistive power splitter / attenuator combination made up of R35, R38 – R43. The output of R35 is amplified by U10, where it is again split and attenuated. The output of R24 is applied to U4, the synthesizer loop controller IC. The output from R43 is amplified by U11.

Voltage regulator U2 provides a +5 volt source for U4, the carrier loop controller IC. By using a separate +5V source, the sensitive charge pump output of U4 will not be affected by other VOR system +5V circuitry.

U4 provides a number of functions. It contains the programmable divider network used to set the operating frequency of the phase locked loop, the phase comparator, the charge pump output used to drive the loop low pass filter, lock detection circuitry, and a programmable divider on the loop reference frequency input. In this application, since the reference frequency is 200 KHz applied to the oscillator input of U4, the reference divider is programmed to divide the reference frequency by 4 to provide a 50 KHz loop reference frequency.

The variable frequency feedback signal from U10 is applied to the variable frequency input (Fin) of U4. This signal is divided in a programmable divider to match the loop reference frequency, or 50.00 KHz. For example, if the desired VOR channel is 113.000 MHz, the programmable divider will divide the incoming RF signal by 2,260. If the desired channel is 117.950 MHz, the programmable divider will divide this input signal by 2,350.

After the variable RF signal is divided by the programmable divider, it is applied to U4's internal phase comparator, where it is compared to the 200.00 KHz reference signal. If the variable RF signal phase slightly lags the 200.00 KHz reference signal, U4's charge pump output (CPO) is driven high, causing the voltage at the VCO control input to increase. This will increase the frequency of the VCO, until the phase difference between the variable signal and the reference signal is near zero. In the same manner, if the variable RF signal phase slightly leads the 200.00 KHz reference signal phase, the charge pump output is driven low, causing the voltage at the VCO control input to reduce, lowering the VCO output frequency, until the difference between the variable signal phase and the reference signal phase are near zero. This has the effect of locking the output frequency to the precision 200.00 KHz reference signal, multiplied in frequency by the number programmed into U4's input divider network.

When the variable phase and reference phase within the loop controller IC are locked together, U4 provides an output indicating that the phase locked loop synthesizer is in the locked state.

The information for programming the dividers within U4 is provided by the SPI interface bus from the audio generator CCA. The audio generator CCA determines the channel frequency, calculates the required programmable divider settings, and creates the serial data stream, clock signals, and data latch signals used to program U4, the synthesizer loop controller IC.

When U4 determines that the loop is indeed locked, it switches the lock detect output high, illuminating CR3 on the 012262 interface board and providing a logic low output used to indicate carrier RF generation loop lock. If U4 senses that the carrier RF generation loop is unlocked, it switches the logic high output to a logic low indicating loop unlock, extinguishes CR3, and the signal is sent to the audio generator to re-initialize the loop controller IC.

RF signal is routed through the signal splitter / attenuator parts R15, R17, and R26 where it is applied to the carrier frequency divider U5. U5 is actually the same type part as U4, the carrier synthesizer loop controller IC. In this application, however, U5 is used simply as a frequency divider, dividing the RF signal by 1280. U5 is programmed by the audio generator CCA to operate as a fixed divide by 1280, with the output provided at pin 14, FO/LD. This output is a short duration pulse, occurring at 1/1280 of the programmed VOR channel frequency. This pulse is applied to flip flop U8:A, where it is divided by two to create a square wave signal at the carrier frequency divided by 2560. This output is used elsewhere in the VOR system to monitor the frequency of the carrier synthesizer.

The output of amplifier U11 is split in a resistive power splitter / attenuator combination and is used in four separate functions. RF output is taken from R53, applied to amplifier U18, then routed through an attenuator (R83, R84, R85) where it is applied to phase detector HY1 as the reference RF phase for the carrier phase correction loop (not to be confused with the carrier RF generation loop). RF output is taken from R50 and routed via jumper J2 to the carrier phase shift network.

RF signal is routed through R55 and C45 to E1. E1 is a one pin connector that provides a RF feed through to the 012162 interface CCA. The RF signal from E1 is amplified by U6 (on the 012162 board), passes through an attenuator made up of R14, R15, and R16, then made available on the front panel of the synthesizer module via J2, Carrier Frequency Output.

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While serving as an interconnect board, the 012262 CCA also contains a temperature sensor, U12 and an EEPROM, U10. These are serial interface circuits that use a port expander, U9 digital gates to select the devices. The port expander U9 along with U8:B, U11, U13, and U14 allows serial communication using a single chip select signal. U1, U2, U7, U8:A, U21, and U22 are buffers for the digital signals coming into the 012262 CCA. L4 and C59 serve as a filter on the reset line for the digital circuits. U18 and U23 function as a window comparator for the power supply voltages. CR19 is a visual indicator on the front panel of the synthesizer assembly to display the status of the voltages monitored by the window comparator circuit.

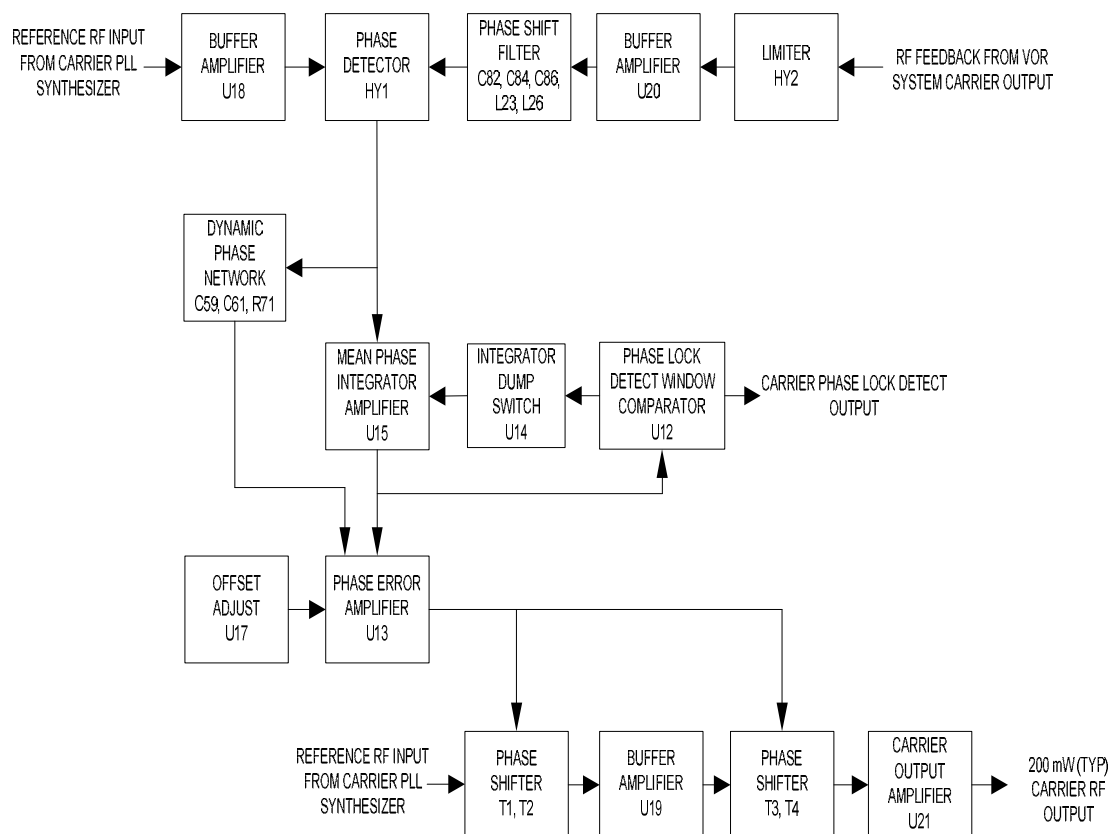


Figure 2-6 Carrier Phase Control Loop

2.3.2.1.2.3 Carrier Phase Control Loop

Refer to [Figure 2-6](#), Carrier Phase Control Loop Block Diagram. RF from the carrier frequency PLL synthesizer is applied to buffer amplifier U18, and then routed to the reference phase input of phase detector hybrid HY1.

The VOR system takes a sample of the carrier transmitter output from the carrier amplifier assembly. This sample of the modulated carrier output signal is brought into the 030838 Synthesizer Assembly via connector J3 on the back panel. The signal passes through limiter hybrid HY2, which serves to remove the 30 percent amplitude modulation, but leaving the phase distortion information intact. This limited signal then goes through buffer amplifier U20, a phase shift network consisting of C82, C84, C86, L23 and L26. This phase shift network provides approximately 180 degrees of RF phase shift to the signal. The signal is then applied to the variable phase input of phase detector HY1.

HY1 provides a DC output that is proportional to the phase difference between the reference input signal and the variable input signal. When the two signals are in quadrature (the normal operating condition), the output is zero volts. Output voltage increases with the variable phase input signal delayed with respect to the reference phase, and decreases with the variable phase input signal advanced with respect to the reference phase. Resistor R87 provides the proper terminating impedance for the hybrid phase detector output.

The output of the phase detector hybrid HY1 takes two paths. One is referred to as the “mean phase” correction path, the other the “dynamic phase” correction path.

The mean phase path is DC coupled, with a very low frequency bandwidth. This path serves to correct for any long-term phase drift with temperature, etc, within the carrier power amplifier assembly in the VOR system. The phase error voltage developed by phase detector HY1 is applied to the inverting input of integrator amplifier U15. This amplifier provides a very high gain to DC signals, with limited gain for AC components.

The output of integrator U15 is low pass filtered further by R65 and C55, then applied to the phase error amplifier U13:A. The output of U13:A controls the tuning voltage on the varactor diodes contained in the phase shifter network. This control voltage causes the phase shifter network to provide the proper phase shift to the synthesizer module carrier output signal to force the output of the phase detector hybrid HY1 to zero volts. This locks the DC component of the system carrier power amplifier output phase to the reference phase within the synthesizer module.

When the VOR system carrier power amplifier amplitude modulates the carrier output signal, it also causes inadvertent phase modulation. In the DVOR system, this appears as a 30Hz phase modulation, with components at harmonics of 30 Hz. This is referred to as the dynamic phase shift.

The output of phase detector HY1 is AC coupled through capacitor C59 and phase lead network C61/R71 to the non-inverting input of phase error amplifier U13:A. The high pass frequency response of this network is chosen to provide adequate gain to the 30 Hz and above components of the phase error signal, but minimal low frequency (down to DC) gain to avoid interaction with the mean phase signal processing described above.

This AC coupled path is referred to as the dynamic phase correction path. The dynamic phase error signal is amplified by U13:A, applied to the phase shift network, and provides a “counter modulation” effect to minimize the phase distortion in the VOR system carrier output signal.

Carrier frequency RF signal from the Carrier PLL Synthesizer is applied via J2 to the input of the carrier phase shift network, or phaser.

For additional details on the carrier phase shift network (phaser), refer to sheet 2 of the 012263 schematic diagram, [Figure 11-11](#). RF from the carrier synthesizer loop is applied to pin 3 of transformer T1. Transformer T1 along with capacitors C62 and C65 function as a 4 port hybrid, or 90 degree power splitter. RF energy applied to pin 3 is split equally into two parts at pins 1 and 2, with 90 degrees of phase difference between pin 1 and pin 2. Pins 1 and 2 are terminated with series LC circuits consisting of L9/CR3 at pin 1, L11/CR4 at pin 2. Inductors L10 and L12 are RF chokes, providing high RF impedance with DC connections to ground for varactor diode control voltage reference. The capacitance of the varactor diodes is changed by varying the control voltage applied to the cathodes, with a RF ground provided by C64. With the purely reactive load presented to pins 1 and 2 by the two series LC networks (L9/CR3 and L11/CR4), the RF energy is reflected back into pins 1 and 2, with the phase of the reflected signal changed by the variable reactance on these pins.

The reflected signals from pins 1 and 2 are 180 degrees out of phase from each other at pin 3, the input port, and in phase at pin 4, the output port. The signals add together at the output port, and cancel at the input port. This has a net effect of a minimal loss broadband phase shift network, with the output signal shifted in phase by the varying reactance of the varactor diode / inductor networks.

The other three phase shifter networks function in a manner identical to the T1 circuit described above. Attenuator networks between T1 and T2, T3 and T4 serve to provide consistent RF impedance matching as the varactor control voltage is changed. Amplifier U19 provides gain and isolation between the sections of the phase shift network.

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The output of T4 is then routed to buffer amplifier U21. Amplifier U21 feeds signal to the carrier amplifier in the VOR system. C102 couples a small RF sample from the output of U21 and is sent to the detector U22 and a buffer amplifier for monitoring of the output power to the carrier amplifier. U22 is a detector integrated circuit that generates a voltage on the output proportional to the RF input power. There is sufficient gain compression in U21 to minimize any changes in attenuation due to the small changes in loss of the phaser network with varying control voltage.

U17, R76, and R77 are used to provide a DC offset in the output of U13:A. This offset is adjusted so that the error voltage seen at the phase control loop integrator U15 output is a nominal zero volts, maximizing the useful control range of U15. This error voltage is available at a test point (TP1) on the front panel of the synthesizer module. U17 is a digital potentiometer that requires the use of the SPI bus from the audio generator and software to program the part. U17 is adjusted to set the phase error voltage as measured at TP1 to a nominal zero volts, +/- 0.050 volts when the synthesizer module is installed in the VOR system cabinet.

Note that in some cases, due to the large available phase shift of the phaser network (>450 degrees) U17 can be adjusted to achieve zero volts at TP1 at two separate points. The actual phase loop control voltage (output of U13:A) is measured at TP2 on the synthesizer front panel. U17 should be adjusted with the use of software to provide zero volts error voltage at TP1 between 2 and 8 volts as seen at TP2. If a zero volt phase error is achieved below 2 volts or above 8 volts, re-adjust U17 to see if a lock condition can be found between these two points.

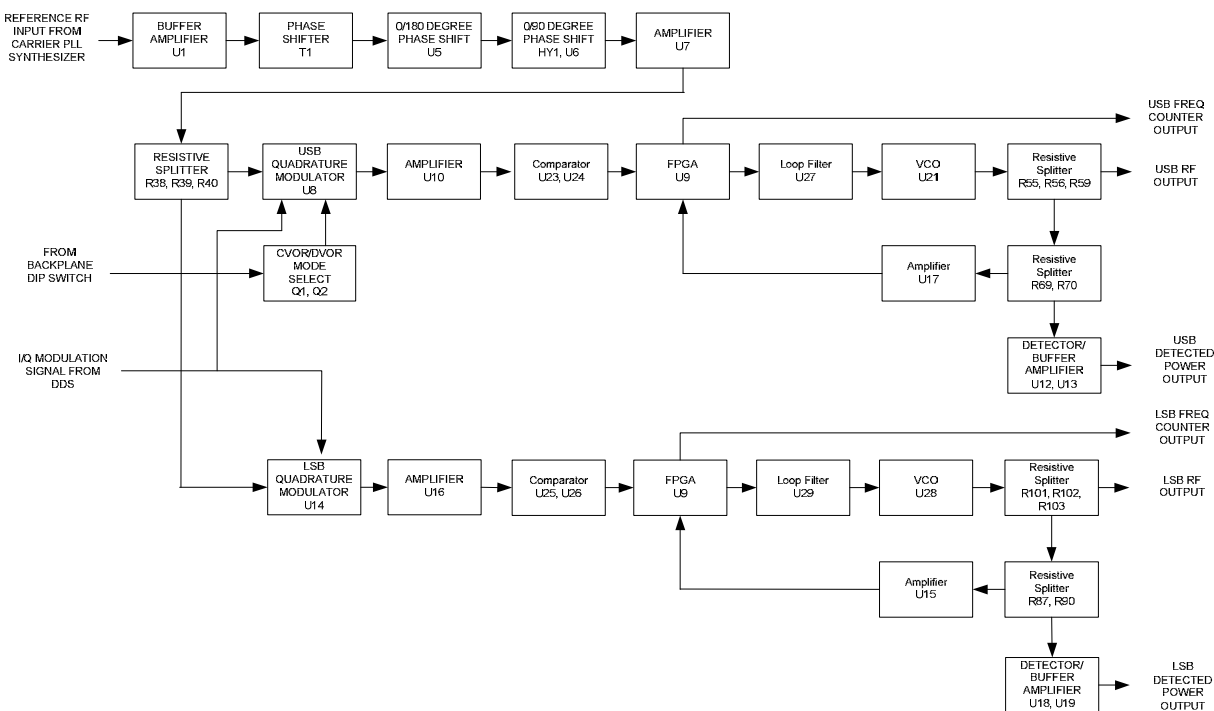


Figure 2-7 Sideband RF Generation Loop

2.3.2.1.2.4 Sideband RF Generation Loops

The block diagram in Figure 2-7 depicts the sideband loop. Refer to Figure 2-7, Sideband RF Generation Loop.

The synthesizer CCA (012258) within the synthesizer module generates the sideband signals necessary for CVOR or DVOR system configuration. Connector J3 provides the input RF signal from the carrier CCA (012263) within the synthesizer assembly. From the J3 connection RF is routed through a resistive attenuator (R1, R2, R3). The attenuator provides a resistive load to the U21 amplifier from the carrier CCA (012263). U1 is a buffer amplifier used to amplify the input signal and to provide isolation between the carrier CCA and the sideband CCA.

The RF signal is attenuated after the U1 amplifier and sent through a phase shift network similar to the phase shift networks in the carrier CCA (012263). The phase shifter provides a fine adjustment for the carrier to sideband phase relationship. The phase shifter provides a minimum of ± 45 degrees of phase shift. The control signal for the phase shifter is amplified through U2:B. Filtering is done through R5, C8, R11, and C10. Resistors R13 - R15 provide a resistive load for the phase shifter. The RF signal is then applied to U5, which is a bi-phase modulator. The bi-phase modulator is used with U4 to provide a 180 degree phase shift from the reference input on pin 4 of U5. This allows a single digital bit for 180 degrees of adjustment referenced to the carrier signal. The signal is applied to HY1 attenuated and to U6. HY1 is a coupler that is used to provide a 90 degree phase shift to the RF signal. U6 is an RF switch used to switch either the 0 degree path or the 90 degree path with resistive attenuation to provide a load to the coupler.

The RF signal is then routed to an amplifier U7 and a resistive power splitter. The signal is split to an upper and lower sideband path. Both sideband paths are identical with the exception the upper sideband disables the DC power to quadrature modulator U8 in a CVOR system configuration. This accomplished through R47, Q1, R48, and Q2. Since both sideband paths are identical, only the lower sideband path will be discussed.

The lower sideband path is attenuated and routed to the quadrature modulator U14. The quadrature modulator uses the 9960 Hz audio signal generated from the DDS, U17 on the 012262 CCA within the synthesizer assembly. There are two 9960 Hz signals that are 90 degrees apart fed into the I/Q ports of U14. This allows carrier and sideband suppression, leaving only the desired sideband for the output signal. Depending if the in-phase (I) signal is $+90$ or -90 degrees with respect to the quadrature (Q) signal, the output signal will yield the upper or lower sideband respectively. The phase shift is controlled by the DDS on the 012262 CCA within the synthesizer assembly.

In a CVOR system configuration, the DDS from the 012262 CCA provides only a differential DC signal to the quadrature modulator in order to pass only the carrier frequency to the lower sideband out without any modulation.

The quadrature modulators provide the sideband output that becomes the reference frequency for the clean-up loop. The clean-up loop is there to filter out the undesired frequency components generated by the quadrature modulators. From the quadrature modulators the signal is routed to a buffer amplifier and then to a comparator circuit to generate a square signal from a sine wave input. You will notice in the block diagram above that the FPGA block has the same U9 reference designator for each of the upper and lower sidebands. This is because the upper and lower sideband signals are routed to the same FPGA. Each signal is then treated independently inside the FPGA. The FPGA serves as the PLL controller for each of the sideband signals while also providing frequency monitor outputs that are a sample of the output frequency divided by 2560. This signal is used in the VOR system to provide monitoring capability of the sideband frequencies. The FPGA has tri-state outputs that are connected to loop filters (U27, U29). The loop filters drive the VCO circuits for each of the upper and lower sideband channels. A sample of the output frequency is split to provide a sample back to the FPGA for the phase control and a sample provided to a detector for monitoring the output power of each of the sideband signals. The output voltage of the detector is proportional to the input RF power.

2.3.2.2 Audio Generator CCA (1A7, 1A23) Theory

2.3.2.2.1 Audio Generator CCA Block Diagram Theory

Refer to [Figure 2-8](#). The Audio Generator CCA is responsible for supplying the audio signal to the carrier amplifier, sourcing four modulated sideband outputs for a DVOR or two modulated sideband outputs for a CVOR, making two bi-phase outputs to the sideband amplifier, generating six DVOR commutator switching control lines, and programming the Synthesizer CCA frequency, phase, and DDS (9960 Hz) signals. In addition, the Audio Generator CCA monitors carrier forward / reflected powers, up to four sideband forward / reflected powers, phase locks of the synthesizer and sideband amplifiers, and frequency lock of the synthesizer.

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All signals and power supplies of the Audio Generator CCA enter and exit through right-angle DIN connectors P1 and P2; which connect to the Control Backplane CCA. Digital Signal Processor (DSP) U6 communicates to the RMS CCA through UART U12 and TTL-RS232 converter U14. Oscillator Y1 clocks the DSP U6 while uP supervisor U13 monitors the watchdog strobe, external $\sim$ MRESET, and on-board power; resetting DSP U6 if necessary. DSP U6 utilizes memory which includes flash ROM U1 / U2, synchronous DRAM U4, and non-volatile RAM U3.

DSP U6 also has serial ports available at debug header JP1 and spare header JP2 that are only used at the factory. Configuration switches on the Control Backplane CCA are read by DSP U6 through buffers U29 and U30. Synthesizer and sideband digital I/O is controlled through latch U27 and SPI / SPORT buffers U28 and U24.

Coder / Decoder (CODEC) U51 contains two analog-to-digital (ADC) converters and two digital-to-analog (DAC) converters. One ADC / DAC pair is used for voice and ident processing while the other ADC converts over 24 channels of powers, phases, and audio levels switched through multiplexers U54 and U48. CODEC U51 responds to DSP U6 SPORT and Timer2 controls.

Channel selection of Multiplexers U54 and U48 is controlled by DSP U6 through programmable logic device (PLD) U40.

DSP U6 also has direct read / write access to the 32Kx16 of carrier audio RAM (CARRAM) U41 and U42 as well as the 32Kx16 of sideband audio RAM (SBRAM) U43 and U45 through PLD U40. Once the CARRAM and SBRAM have been initialized, DSP U6 can command PLD U40 to cycle through the contents of the RAM at a rate determined by oscillator Y2.

The contents of the CARRAM are transferred to carrier DAC U44 as reference modulation while the contents of the SBRAM are clocked into SB1/3 DACs U18 and SB2/4 DACs U20 as audio outputs. The power levels of DACs U44, U18, and U20 are set by DACs U31 and U32. DACs U31, U32, and U33 are directly written by DSP U6. DACs U32 and U33 establish sideband and carrier phase control.

PLD U40 offsets the CARRAM addresses by 7.5 degrees if appropriately strapped at header JP3 and ground-check commanded by the Monitor CCA. PLD U40 synchronizes its internal audio RAM counters to that of the other Audio Generator CCA if logic U19 and U39 indicate that this Audio Generator CCA is not actively on the antenna and a new cycle is beginning.

The DVOR / $\sim$ CVOR configuration input of PLD U40-126 determines if the SB1/3 and SB2/4 bi-phase signals repeat at 720 or 30 hertz rates. Both of these outputs from PLD U40-19 and U40-18 are buffered by U25-8 and U25-9 as SIN_BIPHS and COS_BIPHS.

Commutator switch controls DVSC0 through DVSC5 are generated by PLD U40 during audio RAM cycling. They are converted from digital to RS422 levels by U21 and U22. DVSC5 is also buffered by U46 and presented to the front panel as SYNC on test point TP3.

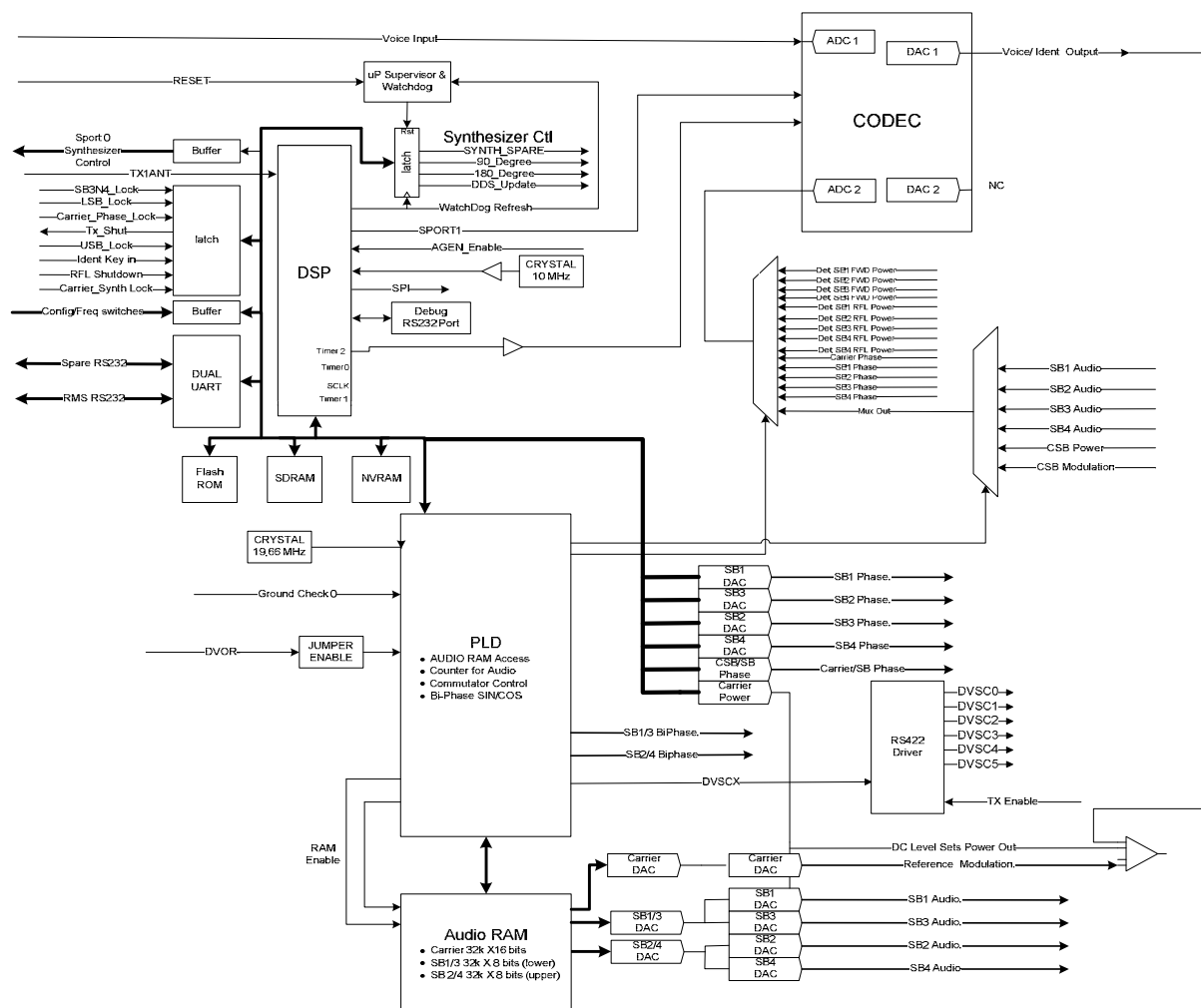


Figure 2-8 Audio Generator CCA Block Diagram

2.3.2.3 Audio Generator CCA Detailed Circuit Theory

Refer to [Figure 11-13](#). All signals and power supplies of the Audio Generator CCA enter and exit through right-angle DIN connectors P1 and P2; which connect to the Control Backplane CCA.

The +5V from connector P1-C1 is filtered by capacitors C48 and C51 as well as inductor L4 to create +5VA for powering analog circuitry. +5V is also regulated by U17 to create +3.3V for powering digital circuitry. The +12V from connector P1-A31 is filtered by capacitors C49, C53, and C55 as well as inductor L2 to make +12ANA for powering analog circuitry. The -12V from connector P1-C32 is filtered by capacitors C50, C52, and C54 as well as inductor L3 to make -12ANA for powering analog circuitry.

The +12ANA is regulated by reference U15 and adjusted by potentiometer R185 to create +VREF. The +VREF sets the level on DACs U31-4, U33-1, and U33-2. Finally the -12ANA is regulated by U16 to make -5VA for powering analog circuitry. Diode CR8 helps prevent latch-up upon power-up.

DSP U6 communicates to the RMS CCA through UART U12 and TTL-RS232 converter U14 as signals AGCN_TX (U14-10) and AGCN_RX (U14-11) to connector P1-A3 and P1-A4. Factory-only RS232 communication ports DEBUG and SPARE are also available on headers JP1 and JP2.

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Oscillator Y1 (available at test point TP22) clocks DSP U6-10 and UART U14-13 at 10 MHz through buffers U5D, U5E and U5C. Supervisor U13 will reset (~RESET) DSP U6-13 if the +3.3V supply drops too low, if ~EXTERN_RESET is active on SPI header J1-2 (factory only), if ~MRESET is active on connector P1-B16 (filtered by inductor FL1 and capacitor C65), or if watchdog (WDOG) from DSP U6-50 doesn't transition often enough.

The ~RESET output (available on test point TP7) also restarts flash RAM U1-10 / U2-10, latch U27-1, DACs U31-28 / U32-24 / U33-24, and PLD U40-127. Finally the ~RESET output (U13-7) is inverted to RESET (U5F-12) for initializing UART U12-36 and decoder U26-5.

DSP U6 utilizes external memory which includes 512Kx16 of flash ROM (U1 and U2), 16Mx16 of synchronous DRAM (U4), and 32Kx8 of non-volatile RAM (U3) as well as some internal cache memory. The internal memory as well as other parts of DSP U6-25 are powered by +1.2V (available at test point TP26) which is created by charge-pump transistor Q1, diode CR2, and capacitor C34. DSP U6 status is indicated on the front panel by CPU_OK LED CR3.

The address and data busses of DSP U6 are buffered by buffers U7-U11 before distribution to the most of the CCA. Only SDRAM U4 is unbuffered to DSP U6 address and data busses due to its communication rates of up to 100 MHz. Emulator header J2 provides accessibility to DSP U6 for in-factory testing.

Decoder U26 defines address spaces for several components of the CCA. Configuration switches on the Control Backplane CCA are read by DSP U6 through buffers U29 and U30. Synthesizer and sideband digital I/O is controlled through latch U27 and SPI / SPORT buffers U28 and U24.

CODEC U51 contains two 16-bit analog-to-digital (ADC) converters and two 16-bit digital-to-analog (DAC) converters. One ADC / DAC pair processes voice input MIC+ from connector P1-C3 and voice / ident output through op-amps U52A and U50 (available at front panel test point TP2) and op-amps U52B and U53 as CARR_MOD+ and CARR_MOD- at connector P1-A12 and P1-B12. The other ADC of CODEC U51 converts over 24 channels of power levels, phase levels, and audio levels switched through multiplexers U54 and U48.

CODEC U51 responds to DSP U6 SPORT0 (U6-72, U6-74, U6-75, U6-69, and U6-68) and Timer2 (U6-77) controls. The +AVCC power supply of CODEC U51-20 is created by the filtering of +3.3V by inductor L6 and capacitors C135, C136, C137, and C139.

Channel selection of multiplexers U54 and U48 is controlled by DSP U6 through PLD U40 signals MA0 through MA5. MA4 (U40-121) is the output enable of multiplexer U54-18 while MA5 (U40-112) is the output enable of multiplexer U48-18. MA0 (U40-87), MA1 (U40-86), MA2 (U40-111), and MA3 (U40-60) select one of sixteen channels on each multiplexer but only the enabled multiplexer output is switched to buffer U50A before routing to CODEC U51. Op-amps U47A and U47B condition the CARR_FWD+/- and CARR_RFL+/- signals before multiplexer U48-19 and U48-20 while the SBx_FWD and SBx_RFL signals are passively filtered before entering multiplexer U48.

DSP U6 has direct read / write access to the 32Kx16 of CARRAM U41 / U42 as well as the 32Kx16 of SBRAM U43 / U45 through PLD U40. The address / data bus and control signals of DSP U6 are piped directly through PLD U40 to the RAMs when not in cycling mode. When in cycling mode, the RAMs address and control lines are connected to internal counters of PLD U40. The internal counters of PLD U40 read the contents of every location of the RAMs in 1/30 of a second; a time division of the 19.6608MHz oscillator Y2 into PLD U40-125.

While the contents of an accessed CARRAM address are on the data bus, PLD U40 activates the ~CARDAC signal; writing the data into DAC U44. Op-amp U37A-1 gains the DAC U44 outputs to create REF_MOD; which inputs to op-amp U52B (mentioned previously) and eventually as part of the CARR_MOD+/- signals.

While the contents of an accessed SBRAM address are on the data bus, PLD U40 activates the ~SBDAC and SBDAC_A1 signals; writing the lower byte of data into DACs of U18 and the upper byte of data into DACs of U20.

The outputs of DACs U18-6 and U18-8 are input to op-amps U34C-10 and U34D-12 as SB1_MOD and SB3_MOD. The outputs of DACs U20-6 and U20-8 are input to op-amps U34A-3 and U34B-5 as SB2_MOD and SB4_MOD.

The power levels of DACs U44-16, U18-1 / U18-2, and U20-1 / U20-2 are set by DACs U31-6, U32-3, U32-4, U32-5, and U32-6. DACs U31, U32, and U33 are directly written by DSP U6. DACs U32 establish the sideband modulation levels while DACs U33 set the sideband phase levels. The DACs U32-2 and U32-1 reference inputs are programmed by DAC U32-5 while DAC U33-2 and U33-1 reference inputs are programmed by +VREF (mentioned previously).

The SBOx_LEVEL outputs of DAC U32 are summed into op-amps U34A, U34B, U34C, and U34D and further conditioned by op-amps U35A, U35B, U35C, and U35D before routing to connector P1-C21, P1-C22, P1-A21, and P1-A22 as SBx_AUDIO. The corresponding SBOxAM signals are available on test points TP18 through TP21.

The SBxPH outputs of DAC U33 are current-limited by resistors R55 through R59 before routing to connector P1-A28, P1-A30, P1-A32, and P1-B28 as SBx_PHS. The SBxPH outputs of DAC U33 and the SBOx_LEVEL outputs of DAC U32 route to multiplexer U54 for monitoring by DSP U6.

PLD U40 internally adds an offset to the CARRAM addresses of 7.5 degrees if header JP3-4 / JP3-3 pins are connected and ground-check signals GSC0+ (P1-C10) and GSC0- (P1-C11) from the Monitor CCA are translated as logic high by RS422-TTL converter U38-2. PLD U40 clears its internal audio RAM counters if logic U19 interprets that this Audio Generator is not on the antenna (U19-4 as ~TX_IND is logic high) and a rising edge of AUD_SYNC (output of RS422-TTL converter U39-2) is detected on PLD U40-40. The rising edge of AUD_SYNC indicates the start of a new cycle by the other Audio Generator (which is on the antenna).

The DVOR_B configuration input (a buffered DIP switch from the Control Backplane via connector P1-B16) of PLD U40-126 determines if the SB1/3 (U40-19) and SB2/4 (U40-18) bi-phase outputs cycle at 720 Hz DVOR or 30 Hz CVOR rates. Both of these outputs are buffered by buffer U25 as SIN_BIPHS and COS_BIPHS before routing to connector P1-C31 and P1-C29.

Commutator switch controls DVSC0 (U40-10) through DVSC5 (U40-23) are generated by PLD U40 during audio RAM cycling. They are converted by TTL-RS422 converters U21 and U22 if this Audio Generator is on the antenna (U19-4 as ~TX_IND is logic low) and transient-voltage protected by TVS CRN1 and CRN2 before routing to connector P1. DVSC5 (U40-23) is also buffered by U46 and presented as SYNC on front panel test point TP3.

PLD U40 is factory programmed using in-system programming (ISP) header J3.

DSP U6-35 can shut down the transmitter by taking TX_OFF high; turning on transistor Q3 and taking ~TX_SHUT of buffer U25-17 and connector P1-A27 low. DSP U6-47 can read transmitter on/off status signal ~TX_SHUTB from buffer U25-3.

2.3.2.4 CSB Power Amplifier Assembly (1A5A3, 1A5A4)

2.3.2.4.1 CSB Power Amplifier Assembly Block Diagram Theory

Refer to [Figure 2-9](#). The Carrier Amplifier amplifies and amplitude modulates the input RF carrier to a level that is acceptable for a 100 watt output at the top of the VOR transmitter cabinet. The modulation is done with 9960 Hz, 30 Hz, keyed 1020 Hz, and voice as needed. The carrier amplifier assembly is made with a single board layout. The layout consists of all necessary local power supplies that are converted from a single +48V nominal input. The amplifier assembly has all necessary shutdown signals to stop transmission in case a fault should occur. The Carrier Amplifier Assembly takes the low level signal from the synthesizer assembly, amplifies, modulates, and filters it, then applies it to the output for antenna distribution. The Carrier Amplifier Assembly accomplishes the amplification and modulation using two LDMOS type RF FETs.

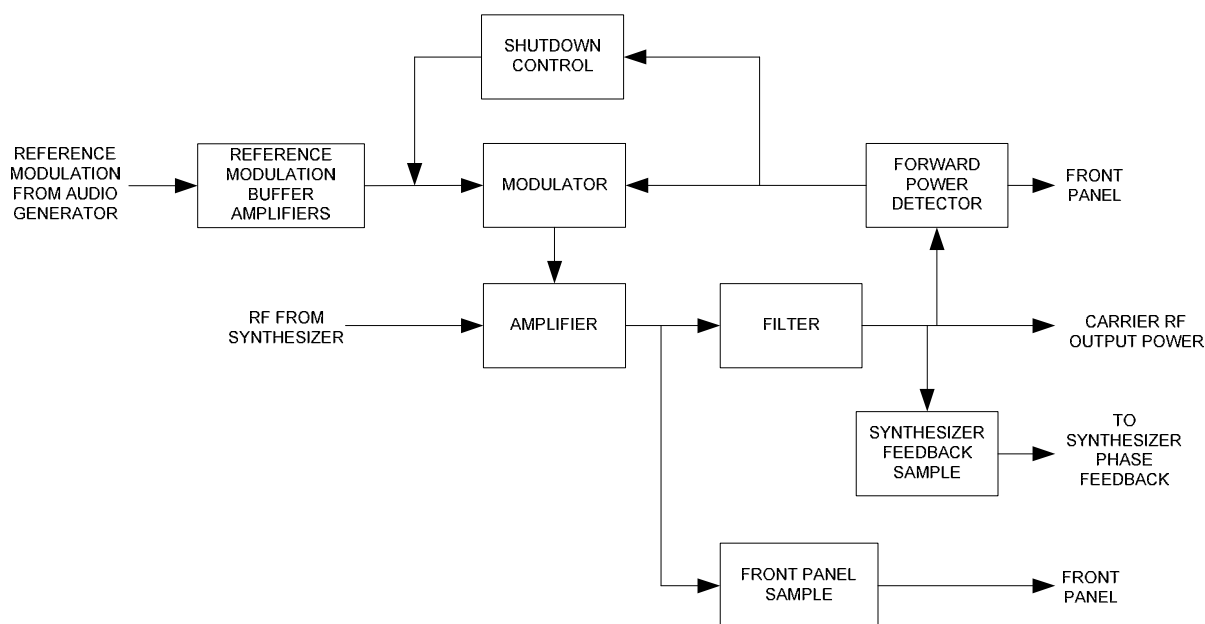


Figure 2-9 Carrier Amplifier Assembly Block Diagram

2.3.2.4.2 Power Amplifier Assembly Detailed Circuit Theory

Refer to [Figure 11-19](#) An input CW RF signal is generated from the VOR synthesizer module with a minimum output power level of 100mW. The RF is sent through a cable to the carrier amplifier assembly. Once the RF enters the amplifier, it is attenuated through a 3 dB attenuator before entering the driver stage of the amplifier. The 3 dB attenuator serves to provide a resistive load for the synthesizer module. The RF is modulated with the Q6 driver stage. The driver is an LDMOS type RF FET with high gain and good linearity. Q6 is modulated using a gate modulation technique. The gate of Q6 is voltage-varied, which modulates the RF signal. This is accomplished by using a feedback circuit that samples the output of the amplifier using C80, C81, and R42. The feedback signal is attenuated through R69, R70, and R71. This signal is routed to the detector, U21 where the audio is detected and buffered through U22:D. The input to the detector circuit is a 14 dB attenuator, R69, R70, and R71 followed by a coupling capacitor C116 into U21. U21 is a high linearity, true power, single chip detector. U12:A is an error amplifier used to compare the input reference signal to correct for non-linearity in the RF amplifier. From the driver stage, the RF signal is attenuated using AT1 to help balance any slight impedance differences between the driver and final RF stages. Attenuator AT1 also helps with a wider bandwidth. The signal is then routed to the final amplifier stage, Q7. The Q7 amplifier is another LDMOS type RF FET with high gain and good linearity. The Q6 amplifier is biased at approximately 850mA. The biasing of the stage is set with potentiometer R36, U13, R35, and CR5 to adjust the quiescent (no RF applied) current level to produce a voltage drop of 17mV across test points TP7 and TP8. Diode CR5 provides thermal compensation for Q6. The minimum gain from the final amp stage is +20 dB.

A small RF sample is coupled from the output of the final amplifier stage through C67. The sample is low pass filtered and sent to the front panel of the module for a test equipment test point. The front panel sample is intended to replicate the high power output filter of the amplifier.

The RF output of the final amplifier stage is then capacitive coupled through C66 to the output filter. The output filter C69, L24, C71, L26, C72, C74, L28, C76, C78, and L29 is a low pass filter designed to remove harmonics from the carrier RF signal.

A small RF sample is coupled from the output of the low pass filter through C84. The small sample is the carrier feedback to the RF synthesizer via J3.

Another RF sample is coupled from the output of the low pass filter through C80. The sample is sent to the detector circuit for detection of forward transmitted power.

From U21 the demodulated signal is sent through a non-inverting unity gain buffer amplifier, U22:D. The output of U22:D is split into three different paths: CSB Power, Reflected Shutdown, and Detected.

The CSB Power circuit is non-inverting amplifier (U22:C) circuit that uses R85 and R87 to set the gain of the circuit. Potentiometer R87 is adjusted to set the voltage level at TP20 to 3.0V with a 100W output CW RF power. The output of the CSB Power circuit is split into two signals, one is sent to the backplane via the DB37 pin connector, the other is sent through a non-inverting unity gain buffer amplifier, U22:A, to the front panel of the module for an easily accessible test equipment connection point.

The demodulated signal from U22:D is sent through a voltage divider network R84 and R81. After the signal is divided down, it is sent to the positive input of the voltage comparator (U23:C). The reflected carrier demodulated signal is sent from the backplane via the DB37 connector to a differential amplifier U22:B. The gain is set for U22:B with the potentiometer R76 and resistor R73. From the differential amplifier, the signal is amplified and sent to the negative input of the voltage comparator (U23:C). The comparator is set such that a 3V reflected input voltage will trip the comparator. The reflected input voltage is routed from the RF monitor, which scales the voltage that is used for the reflected shutdown circuit within the power amplifier module. When the comparator trips, the output voltage travels to a low state causing the one-shot timer U24:A to take the output low for a time period of 33 mS. The time constant for U24:A is set with R92 and C124. The Reflected Shutdown output is connected to the backplane via the DB37 connector, to the reflected shutdown control, and to the latch U8:A for monitoring the reflected shutdown through a serial interface.

The demodulated signal from U22:D serves as a feedback signal to the negative input of the error amplifier U12:A. The positive input of the error amplifier is the reference that is generated by the audio generator CCA within the VOR system. There is a shutdown control circuit consisting of U11, and Q1-Q5 for the input reference signal in the event a fault in the power amplifier should occur. The carrier modulation voltage is routed from the backplane via the DB37 connector to a differential amplifier, U10:A. The differential amplifier can be configured for single mode using the J5 selection. The audio signal may be a sine wave input with a DC offset up to 10 KHz. The amplitude of the sine wave may be a level capable of producing a minimum of 50% modulation on the output of the carrier amplifier module. The output of the U10:B buffer amplifier is then sent to the input of R18 for scaling the input audio signal for a 100W output. The output of the U11 analog switch shutdown circuit will travel to a ground potential in the event a fault should occur in the amplifier module. The faults monitored for a shutdown to occur within the amplifier assembly are Over Temperature, Over Power, and Carrier Reflected. The Q2, Q3, and Q4 fault transistors are connected in series to the gate of Q1. If any of the fault transistors stop conducting, the gate of Q1 is pulled high, pulling the gate of Q5 low and to a non-conducting state. The gate of Q5 may also be pulled low externally to shut down the power amplifier assembly.

The SPI interface communicates with the amplifier assembly through U1:A. U1:A is used as a buffer for the SPI bus. The SPI uses the general purpose I/O expander U2 along with U4, U6, and U7 for address decoding for serial communication to the EEPROM, U3 and temperature sensor, U5. U1:B is only used for the SPI serial out of the amplifier assembly. The general purpose I/O expander U2 in conjunction with U8 and U9 reports the status of faults that have occurred in the power amplifier assembly.

The Over Power shutdown circuit serves to protect the amplifier assembly if an over power condition should occur. The over power circuit consists of a voltage comparator U23:A and a one-shot timer circuit U24:B. The CSB power signal from the detector is sent to the negative input of the voltage comparator. The negative input of the voltage comparator also contains a low pass filter circuit R98, R99, and C128 that serves to reduce the modulation on the line to for an average output power. The positive input of the voltage comparator is set with R100 and R101 voltage divider. Once the power level out of the amplifier assembly reaches approximately 200 watts, the comparator output will go low. The negative edge from the comparator triggers the one-shot timer low pulse for approximately 33mS. The pulse time for the one-shot timer is set with R109 and C51. The over power signal is sent to the back plane, Q3, and U8:B for an error status signal. When the over power circuit pulses low, Q3 will stop conducting and disable the amplifier from transmitting for the period set by the one-shot timer.

The over temperature shutdown circuit consists of a voltage comparator U23:B with positive feedback R104 for hysteresis purposes. Thermistor R108 is thermally connected to the amplifier heat sink. The value of the thermistor

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is approximately 10K ohms with the amplifier at 25 degrees C. R108 has a negative temperature coefficient, meaning as the temperature of the heat sink rises, the resistance of R108 reduces. In the event of excessive heat sink temperature, the output of comparator U23:B will travel to a low state. When the comparator goes low, this will make Q2 stop conducting, disabling transmission. The comparator will not reset until the temperature of the heat sink cools down. The over temperature shutdown signal is also sent to U9:B for monitoring purposes.

The amplifier assembly contains four different local power supplies that are converted from the +48Vdc nominal input. The power supplies are: +15Vdc, +10Vdc, +5Vdc, and +3.3Vdc. The +15Vdc supply is directly converted from the +48Vdc input. R45 and R47 along with U14 set the output voltage for the +15Vdc supply. The +15Vdc supply is a switching supply only used to convert the +48Vdc input to a level suitable for linear regulation of the +10Vdc supply. From the +10Vdc supply, the +5Vdc supply is linear regulated and the +3.3Vdc linear regulates from the +5Vdc supply.

All power supplies within the module are monitored with voltage comparators U18A, U18B, U18C, U18D, U19B, U19D, U20C, and U20D. The comparator circuits are powered directly from the +48V input through R51, R52, and CR10. Diode CR10 provides a +10Vdc reference for powering the comparator IC's and providing a reference voltage for the voltage divider resistors. The power supply monitor circuit is the only circuit in the module assembly that is not fused. This was intentional for monitoring the power supplies without degrading performance in the power supply monitoring circuit. A logic low on any of the power supply monitoring comparators will cause the output of U19:A to travel to a high impedance state. This will prevent the power ok LED (CR11) from conducting. Comparator U19:C will also travel to a high impedance state for monitoring the power supplies externally.

2.3.2.5 Bi-Directional Coupler (1DC1)

The Bi-Directional Coupler is used to obtain a representative sample of the forward and reflected RF powers of the carrier signal (refer to [Figure 2-2](#), DVOR system block diagram). The coupler has negligible insertion loss between the input and output connectors. Internal directional pickup loops couple a portion of the forward and reflected powers to the output sampling ports. These ports provide a fixed ratio of the sampled powers to the RF monitor assembly for detection and analysis processing.

2.3.2.6 Sideband Generator Assembly (1A4A1, 1A4A2, 1A4A6, 1A5A7)

The DVOR uses two Sideband Generator Assemblies for each transmitter system. Each generator contains one sideband amplifier CCA part number 012218-0001. The Sideband Generator may be plugged into one of four positions within the DVOR cabinet. Position 1A4A1 is for transmitter 1 Sidebands 1 and 2 signal generation of two lower sideband outputs (Carrier -9960 Hz). Position 1A4A2 is for transmitter 1 Sidebands 3 and 4 signal generation of two upper sideband outputs (Carrier +9960 Hz). Position 1A4A6 is for transmitter 2 Sidebands 1 and 2 signal generation of two lower sideband outputs (Carrier -9960 Hz). Position 1A4A7 is for transmitter 2 Sidebands 3 and 4 signal generation two upper sideband outputs (Carrier +9960 Hz).

2.3.2.6.1 Sideband Generator Assembly Block Diagram Theory

Refer to [Figure 2-10](#). The Sideband CCA (PN 012218-0001) is responsible for developing the sideband amplitude modulated signals that are sent to the commutator. The commutator only acts as a selection switch to the sideband antenna array and performs no modulation.

RF enters the Sideband Generator at P1D from the frequency synthesizer upper or lower sideband output. The signal is CW and at approximately 0 dBm. The signal is split and then enters either sideband 1 or sideband 2 circuits. The two sidebands are identical so only one will be described.

After the RF splitter the CW signal enters the manual phaser. This phaser is controlled with an operator setting in the PMDT. This phaser is used to align all four sidebands in a DVOR to the same RF phase in order to get maximum sideband modulation. The signal then passes through a buffer and then enters the bi-phase modulation. The bi-phase modulator can be set to provide 0 or 180 degrees of RF phase shift. In a DVOR this is directly controlled by J11. This jumper allows for either a setting of 0 or 180 degrees based on the frequency of operation and described in the alignment procedures.

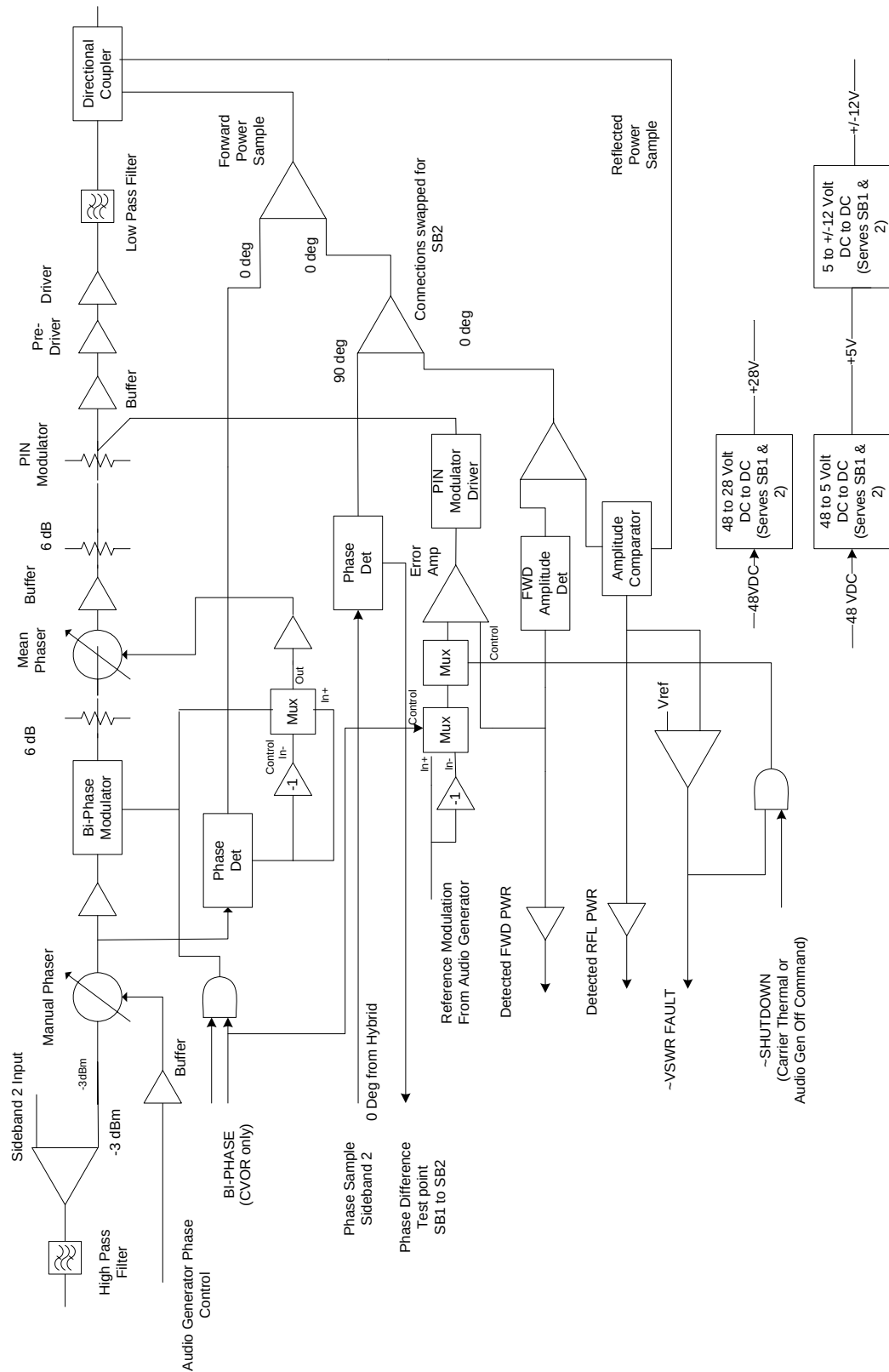


Figure 2-10 Sideband Generator Block Diagram

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The signal then enters a buffer then a passes through a 6 dB fixed attenuator. The signal then passes through a voltage controlled phase shifter with up to 360 degrees of phase shift. This phase shifter is used in a control loop to correct for any phase shift due to temperature, and aging so that the output phase remains constant. After the phase the signal passes through a buffer then a fixed 6 dB attenuator and then a voltage variable attenuator used to amplitude modulate the RF signal.

The signal then passes through a buffer then a pre-driver and then the final amplifier. The signal then passes through a low pass filter to eliminate the higher harmonics of the RF signal. The signal then passes through a dual directional coupler. Both forward and reverse RF paths are provided from the coupler.

The phase control loop maintains the output phase of the sideband generator the same relative to a sample of the input phase. A sample of RF signal is taken after the manual phaser. This is considered the reference phase. Another sample of RF signal is taken from the directional output and 3 dB two way splitter. A phase detector strips the modulation from the signals and compares the phase and produces an error voltage that is used to control the mean phasor in order to keep the input to output phase constant.

The amplitude control loop receives a sinusoidal signal from the Audio Generator. The amplitude of this signal sets the output power of the Sideband Generator. The sinusoidal signal is rectified and used for the reference signal to the amplitude control loop. A sample of the amplitude modulated signal is derived from the directional coupler forward port and split by the 3 dB two way power divider. The signal then enters the forward power linear detector. The output of the detector is fed into the error amplifier. The error amplifier is used to drive the voltage controlled attenuator. The error amplifier makes sure that the input and output signals are the same.

The reflected power monitor compares a sample of the forward signal and sample of the reflected signal from the directional coupler to determine the VSWR of the circuits following the Sideband Generator.

The power applied to the Sideband Generator is approximately 48 Vdc. The power supply circuitry is common to both sidebands on the board. A 48 V to 28V converter module is mounted to the back side of the board. This module supplies most of its output power to the final amplifier transistors. Another power supply is comprised of discrete components and generates +5 Vdc from the 48 Vdc input. The 5 Vdc is used by another switching power supply to generate the +12 and -12 Vdc supply voltage.

The sideband generator has an on board temperature sensor that is monitored by the RMS processor.

2.3.2.6.2 Sideband Generator CCA Detailed Circuit Theory

There are two Sideband Generators on the circuit card. Only one will be described along with the circuitry common to both Sideband Generators.

The CW RF enters on connector P1:D at approximately 0 dBm. The signal is equally split by he -3 dB power splitter formed by L1, L2, C2, C7 and R7. The signal then passes through high pass filter formed by C8, C10 and L3.

The signal then enters the phase shifter formed by T2, C12 and C16. This phase shifter has a range of approximately +/- 60 degrees of range and is the manual phase shifter. This phase shifter is used to align all the sideband amplifiers to the same phase. The diodes CR1 and CR2 are varactor diodes that vary in capacitance based on the voltage applied. The operational amplifier U1 amplifies the SB1_PHS signal that originates at the Audio Generator. This voltage is controlled from the PMDT as a Sideband Phase offset setting

After the manual phase shifter the signal is split by a 6 dB splitter formed by R15, R17 and R18. A sample (SB1_REF_PHASE) is provided to the phase comparator circuit described later. The signal then enters a phase shifter with transformer T4, controlled by the Phase control loop voltage (SB1_MEAN_DYN_PHASE). After the phase shifter the signal is amplifier by U3 with a fixed 20 dB gain.

The signal then enters the Bi-phase modulator circuit. This circuit provides either 0 or 180 degrees of RF phase shift. In a DVOR the selection is controlled by jumper J11 (SB1_BI_PHASE_CVOR is low) to allow operation over the band from 108 to 118 MHz. In a CVOR the SB1_BI_PHASE_CVOR changes from low to high with each sinusoidal lobe of modulation signal. This technique is used to remove the carrier from the sideband signal (carrier suppression) necessary for a CVOR sideband signal. Analog multiplexer U4 switches between the S1 and S2 inputs to alternately provide +12 or -12 Vdc to R23 and the control pin of the U6 modulator.

After the bi-phase modulator the signal passes through a 6 dB attenuator formed by R26, R28, and R30. The signal then passes through phase shifters formed by T5, T7, and T9 which are controlled by the phase control loop. The signal is then amplified by U9 with a fixed gain of 20 dB.

The signal then passes through a 6 dB attenuator formed by R55, R56, and R58. The signal then enters the voltage controlled attenuator circuit. The SB1_PIN_MOD signal controls the voltage that Q2 applies through R73 and the current through PIN diodes CR22, CR24, CR27 and CR28. The capacitance of the diodes varies with the current through the diodes and therefore the attenuation changes with current. The other half of diodes CR22, CR24, CR27 and CR28 are biased on continuously to provide a nominal voltage at R60, R70, R74 and R81.

After the PIN diode attenuator the signal enters the U11 amplifier with a fixed gain of 20 dB. The signal (SB1_DRIVER_RF) passes through a 3 dB attenuator and is amplified by FET Q3. The output level is about 2 watts peak. The Potentiometer R137 sets the gate bias level. This is normally set for 250mv across R141. The gate bias is turned off with Q15 and Q16 when the shutdown signal (~TX_SHUT) is low to reduce power dissipation.

After amplification by Q3 the signal passes through a 3 dB attenuator formed by R145, R146, and R147. The signal is then amplified by the final FET Q4. The gate bias is set with R150 to approximately 50mV across R156. The gate bias is turned off with Q15 and Q16 when the shutdown signal (~TX_SHUT) is low to reduce power dissipation.

The signal then passes through a low pass filter to remove second and higher harmonics of the carrier. The signal then passes through directional couplers DC1 and DC2 before exiting the board at P2:E. Directional coupler DC1 provides a sample of the forward power to the phase and amplitude control loops. Directional coupler DC2 provides a sample of the reflected power to the Phase/Magnitude circuit U33 through a 22 dB attenuator. A sample of the forward power passes through the 30 dB attenuator and into the Phase/Magnitude circuit U33. The levels are set so that U33 provides 0.9 VDC at the VMAG output when the return loss is 20 dB. The VMAG output is buffered by U31B and enters the comparator U30a. The positive input to the comparator is a sample of the reference voltage from U33 divided by 2. If the negative input to the comparator is above the reference then the output of U30A goes low triggering the one shot U29B and sets the ~SB1_VWSR_ALARM line low. This line goes out of the CCA to the Audio Generator CCA and reports the indication on the PMDT.

The modulation signal (SB1_Audio) from the Audio Generator is a sinusoidal signal at 30 Hz for a CVOR or 360 Hz for a DVOR. This signal passes through DC blocking cap C251 and through buffer U38C. The output of buffer U38C feeds both inverter U38D and the analog multiplexer U25. The SIN_BIPHS signal that originates from the Audio Generator is high when the SB1_AUDIO signal is positive and low when it is negative. Multiplexer U25 switches between the positive (U38C) and negative (U38D) inputs to generate a rectified sin wave signal. Multiplexer U26 passes the signal when the SB1_ENABLE line is high. Potentiometer R142 is used to add an offset to the output of U26 and set in the factory. Operational amplifier U27A provides a gain of 3 with high frequency attenuation. The signal enters error amplifier U27B which drives the PIN diode modulator circuit. A sample of the forward power is detected by linear detector U32 and buffered by U31A and applied to the inverting input of the error amplifier U27B for reducing the modulation harmonics of the sideband output. Amplifier U34 drives the front panel test point TP2 and the SB1_FWD signal sent to the Audio Generator. Potentiometer R2 is used to calibrate the output level to match external test equipment value for output power.

Model 1150A DVOR

Refer to page 2 of [Figure 11-21](#). Circuit U22 is a phase comparator circuit that forms part of the phase control loop of the Sideband Generator. The reference phase (SB1_REF_PHASE) is the unmodulated CW signal that is sampled after the manual phaser. The SB1_RF_SAMPLE1 signal is a sample of the final output signal from the forward power coupler DC1. The phase detector is most accurate when the Input A (INPA) and Input B (INPB) ports are separated by 90 degrees. The output at VPHS is 0.9 Vdc when the phase difference is 90 degrees. The voltage is 0 volts at 0 degrees and 1.8 volts at 180 degrees. Circuit U20A buffers the detected phase signal. A sample of the U22 voltage reference of 1.8 VDC is applied to resistors RN1E and RN1G which divide this to 0.9 Vdc. Circuit U20 inverts the detected phase. Analog multiplexer U18 is not active in DVOR mode. In CVOR mode the SB1_BI_PHASE_CVOR signal is used to switch between the inverted and non-inverted detected phase signals to remove the bi-phase modulation created by U6.

The output of U18 is applied to the phase error amplifier U14A. The non-inverting input of U14A is connected to the 0.9 Vdc created from the U22 voltage reference. Error amp U14A drives the output at pin 1 so that the input at pin 2 equals 0.9 V. The multiplexer U16 is normally open from pin 1 to the S1 output. The switch closes making the error amplifier a unity gain buffer when the phase loop is unlocked in order for the voltage to move through the entire range to find the correct lock voltage.

Operational amplifier U14B provides a gain of 2 and adds a DC offset from R1. This sets the normal operating voltage of the phasers in the control loop. This set point will be different for each operating frequency and must be adjusted during alignment. The output (SB1_MEAN_DYN_PHASE) is routed to each of the phase shifters. Comparators U12A and U59A compare the error voltage from the U14A output to a fixed voltage of 3.4 V. If the error voltage is between 0.8 Vdc and 3.4 VDC then the loop is locked and the U12A and U59A outputs are high. If the voltage falls outside 3.4 and 0.8 Vdc then the output is low and C109 is discharged. R88 then charges the voltage back high in order to stretch the unlock time. Comparator U12B output goes low when the loop is not locked and causes U16 to close.

Refer to page 6 of [Figure 11-21](#). The 48 VDC enters the Sideband Generator and enters fuses F1 and F2. Fuse F1 feeds DC to DC converter PS2. The output of PS2 is 24 VDC that primarily supplies the operating voltage for the final transistors Q4 and Q6 through L91.

The +48 Vdc signal is applied to fuse F2 and then applied to the switching voltage regulator U42. Regulator U42 provides a rectangular pulse train at the VOUT pin. Inductor L85 and C273 filters the pulse train into a DC voltage. A sample of the DC voltage is applied to the FB (feedback) pin of U42 which allows correction of the pulse train pulse width to provide +5 VDC at the output. Diode CR32 along with R231, C269 and Q8 provide over voltage protection. If the voltage exceeds 5.6 volts then Q8 is turned on which will blow the fuse F2.

Linear regulator circuit U44 provides regulation of the +5 Vdc to +3.3 Vdc. DC-DC Converter PS1 converts the 5 Vdc to +15 VDC and -15 Vdc. Linear regulator U45 converts the -15 Vdc to -12 Vdc. Linear regulator U46 converts the +15 Vdc to +12 Vdc.

Refer to sheet 6 of [Figure 11-21](#). Resistors R249, R250 and diode CR44 provide a precise +10Vdc source for the voltage monitor circuits. Voltage comparators U49A and U49B monitor the 5 Vdc supply and if the voltage exceeds the range 4.5 to 5.5 Vdc then one of the comparator outputs will go low turning off both Q11 and Q12. Voltage comparators U49C and U49D monitor the 12 Vdc supply and if the voltage exceeds the range 10.8 to 13.2 Vdc then one of the comparator outputs will go low turning off both Q11 and Q12. Voltage comparators U50A and U50B monitor the 24 Vdc supply and if the voltage exceeds the range 22.3 to 26.3 Vdc then one of the comparator outputs will go low turning off both Q11 and Q12. Voltage comparators U50C and U50D monitor the -12 Vdc supply and if the voltage exceeds the range -10.9 to -13.1 Vdc then one of the comparator outputs will go low turning off both Q11 and Q12. FET Q11 provides an output to the Facilities CCA that is low when the power is ok and high when the power is out of tolerance. FET Q12 control the front panel power OK LED. When power is normal the gate of Q12 is high and the drain is low turning the LED CR45 on. The lamp test input (~TEST) goes low when the switch on the LCU is depressed and causes the LED CR45 to go on.

The Sideband Generator contains a temperature sensor U56 attached close to the heat sink to monitor the temperature of the heat sink. The RMS has the ability to read the temperature through the SPI interface. The signal SPI_SCK is the clock used to clock in and out the serial data. The SCK signal is buffered by U43 and U53A. The SPI_MOSI (master out slave in) line is serial data coming from the RMS. Data on this line enters U53A pin 2 and is buffered and exits at the Y1 output. The signal ~SPI_CSXX is active low when the Sideband Generator board is being addressed by the RMS. Clock and data information is always present but ignored by the Sideband Generator when the ~SPI_CSXX is high.

Buffer U53B is used to buffer the SPI_MISO data out of the Sideband Generator to the RMS. The output at Y1 is tri-stated when the data is a high and active low when the data at the ~OE goes low. This allows for many of the other modules to use the same SPI_MISO line back to the RMS. Resistor R273, R270, R272, and U54 are used to decode the addressing of the RMS so that the Sideband Generator responds to the correct ~SPI_CSXX and address. The circuit U54 provides for parallel input output from the RMS SPI port. This allows for selection of either the temperature sensor U56 or EEPROM U55. The EEPROM is used to read and write data from the RMS. This EEPROM holds the Sideband Generator serial number and revision information programmed by the technician through the PMDT screens.

Phase detector U51 compares a sample of the output of Sideband 1 and Sideband 2 through quadrature hybrids couplers HY1 and HY2. The two samples are 90 degrees out of phase due to the coupling of the two hybrids. Therefore when the two outputs of sideband 1 and 2 are in phase then the samples to U51 are 90 degrees out of phase and the VPHS output is 0.9 Vdc. Amplifier U52A subtracts 0.9 Vdc so that when sideband 1 and two are in phase front panel test point TP6 is at 0 Vdc. The technician can adjust the manual phasers in the two sidebands to make the test point indicate 0 Vdc.

Refer to sheet 6 of [Figure 11-21](#). Gates U48A and U48B are used to enable the sideband generator if the VSWR is ok and the transmitter is not shut off. Comparator U47B acts as an inverting buffer for the DVOR input. If the DVOR line is high then the BI_PHASE outputs of U28C and U28D go low and the BI_PHASE modulation for a CVOR is stopped.

Gate U48C output is high if both phase lock indications are normal. If either or both go low then U47D goes low discharging C291. Resistor R246 recharges C291 to stretch short time phase lock alarms. Comparator U47C buffers the output to the Audio Generator for monitoring the phase lock indication.

2.3.2.7 RF Monitor Assembly (1A4A4) Theory

The RF monitor assembly functions as an RF detector/amplifier and distributor of the detected analog RF signals. The assembly contains a high power dummy load that is capable of dissipating the 100 watts of RF power from the standby transmitter. There are four additional dummy loads to terminate the output of the standby transmitter sideband generators into loads. The dummy loads are attached to a heat sink to dissipate the power of the standby transmitter while it is operating.

2.3.2.8 RF Monitor Assembly Block Diagram Theory

Refer to [Figure 2-11](#). The assembly contains a high power dummy load that is capable of dissipating the 100 watts of RF power from the standby transmitter. There are four additional dummy loads to terminate the output of the standby transmitter sideband generators into loads. The dummy loads are attached to a heat sink to dissipate the power of the standby transmitter while it is operating. There are RF detectors for the forward power and reflected power for the transmitter connected to the antenna. The transmitter not connected to the antenna is connected to the internal load. A sample of the terminated power is applied to the standby transmitter detector.

The RF Monitor generates power from the 48 Vdc from either transmitter. When either transmitter is on then the RF Monitor is powered. A temperature is located on the RF Monitor and the values are read by the RMS processor. Also data storage is provided on the RF Monitor for the purpose of storing information such as serial number, and revision data entered using the PMDT. This information travels with the module and holds data particular to that module.

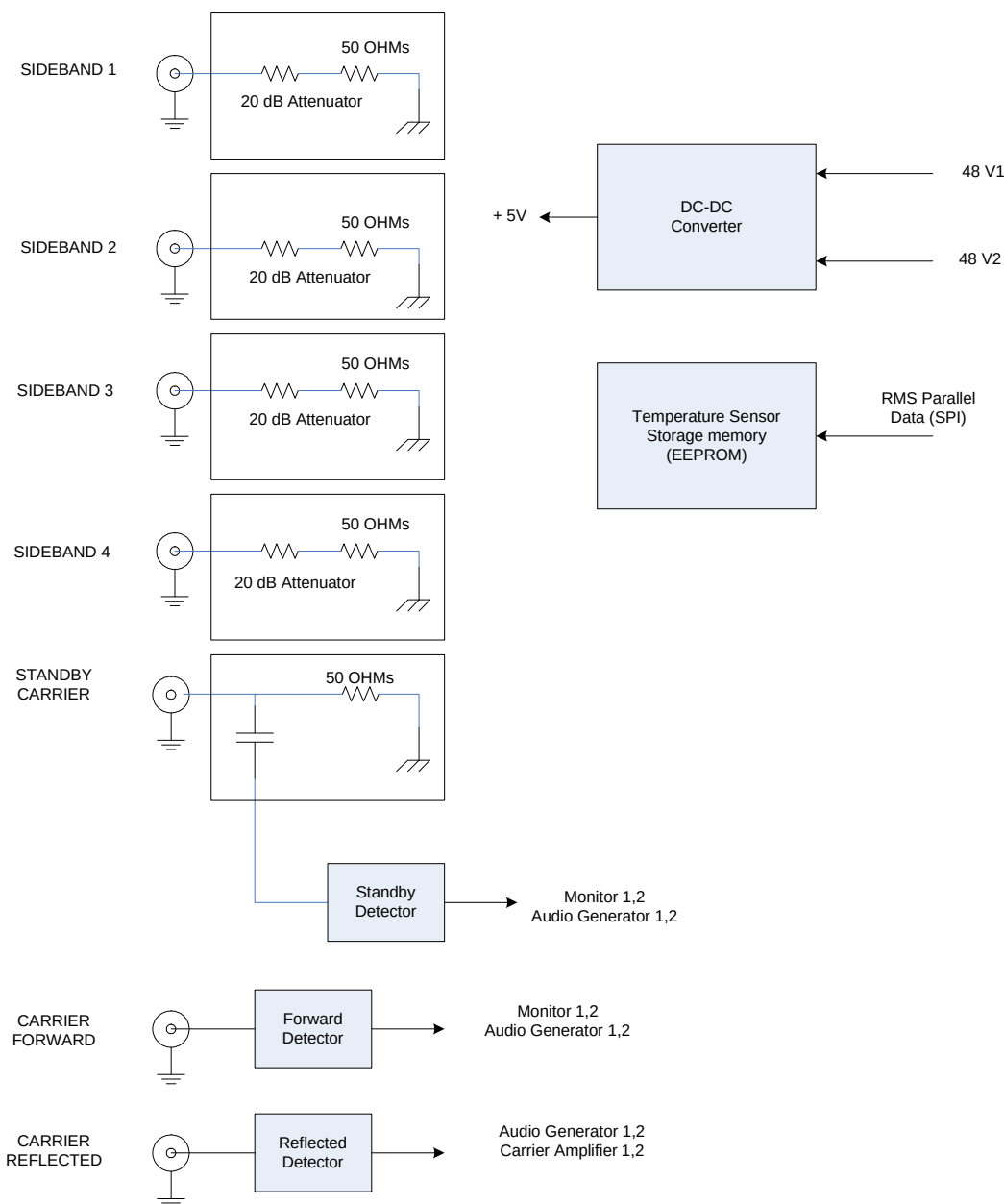


Figure 2-11 RF Monitor Assembly Block Diagram

2.3.2.8.1 RF Monitor Assembly (1A2) Detailed Circuit Theory

The RF Monitor Assembly functions as an RF Detector/Amplifier and distributor of the detected analog RF signals. The assembly contains a high power dummy load that is capable of dissipating the 100 watts of RF power from the standby transmitter. Four dummy loads are mounted to the assembly heat sink in order to dissipate the sideband generator power.

Refer to [Figure 11-22](#). Resistor R84 is the dummy load for the standby transmitter RF carrier power. The RF power enters the assembly via RF connector P1:F. A sample of the RF signal applied through C34 to the 35 dB attenuator formed by R65, R66 and R67. The signal then enters the linear detector circuit U17. The detected voltage from U17 is buffered and amplified by U18A. Potentiometer R3 is located on the front panel of the RF Monitor and allows adjustment of the output level. The technician uses this adjustment to calibrate the Transmitters>>Data>>Standby Power to the same as measured by external test equipment while on the antenna.

Test point TP3 is mounted on the front panel and allows for convenient monitoring of the Standby transmitter composite signal. Differential driver U19 is used to buffer the output signal to the Monitor and Audio Generator. Jumpers JP5 and JP6 provide selection of single ended or differential signals to the Monitor and Audio Generator. In position 1 to 2 the signal is single ended. In position 3 to 4 the signal is differential with the output centered about 2.5 Vdc.

Sideband 1 of the standby transmitter enters at connector P2:F and passes through blocking capacitor C1 and into termination R80. Sideband 2 of the standby transmitter enters at connector P2:D and passes through blocking capacitor C2 and into termination R82. Sideband 3 of the standby transmitter enters at connector P2:G and passes through blocking capacitor C3 and into termination R81. Sideband 4 of the standby transmitter enters at connector P2:E and passes through blocking capacitor C4 and into termination R83.

The forward power RF enters the assembly via RF connector P2:D. This signal originates at directional couple DC1 forward port. A sample of the RF signal applied to the 35 dB attenuator formed by R7, R10 and R11. The signal then enters the linear detector circuit U1. The detected voltage from U1 is buffered and amplified by U3A. Potentiometer R1 is located on the front panel of the RF Monitor and allows adjustment of the output level. The technician uses this adjustment to calibrate the Transmitters>>Data>>Forward Power to the same as measured by external test equipment while on the antenna.

Test point TP1 is mounted on the front panel and allows for convenient monitoring of the Forward power composite signal. Differential driver U4 is used to buffer the output signal to the Monitor and Audio Generator. Jumpers JP1 and JP3 provide selection of single ended or differential signals to the Monitor and Audio Generator. In position 1 to 2 the signal is single ended. In position 3 to 4 the signal is differential with the output centered about 2.5 Vdc.

The reflected power RF enters the assembly via RF connector P2:E. This signal originates at directional couple DC1 reflected port. A sample of the RF signal applied to the 13 dB attenuator formed by R6, R8 and R9. The signal then enters the linear detector circuit U2. The detected voltage from U2 is buffered and amplified by U3B. Potentiometer R2 is located on the front panel of the RF Monitor and allows adjustment of the output level. The technician uses this adjustment to calibrate the Transmitters>>Data>>Carrier VSWR.

Test point TP2 is mounted on the front panel and allows for convenient monitoring of the reflected power composite signal. Differential driver U5 is used to buffer the output signal to the Monitor and Audio Generator. Jumpers JP2 and JP4 provide selection of single ended or differential signals to the Monitor and Audio Generator. In position 1 to 2 the signal is single ended. In position 3 to 4 the signal is differential with the output centered about 2.5 Vdc.

The TX1 +48 Vdc and TX2 +48 Vdc signals are applied to fuse F1 through an OR gate circuit consisting of CR2 and CR3. From F1 the voltage is applied to the switching voltage regulator U7. Regulator U7 provides a rectangular pulse train at the VOUT pin. Inductor L1 and C24 filters the pulse train into a DC voltage. A sample of the DC voltage is applied to the FB (feedback) pin of U7 which allows correction of the pulse train pulse width to provide +5 VDC at the output. Diode CR11 along with R48, C20 and Q1 provide over voltage protection. If the voltage exceeds 5.6 volts then Q1 is turned on which will blow the fuse F1.

Linear regulator circuit U12 provides regulation of the +5 Vdc to +3.3 Vdc. Resistors R36, R37 and diode CR4 provide a precise +10Vdc source for the voltage monitor circuits. Voltage comparators U6A and U6B monitor the 5 Vdc supply and if the voltage exceeds the range 4.5 to 5.5 Vdc then one of the comparator outputs will go low turning off both Q2 and Q3. FET Q2 provides an output to the Facilities CCA that is low when the power is ok and high when the power is out of tolerance. FET Q3 control the front panel power OK LED. When power is normal the gate of Q3 is high and the drain is low turning the LED CR7 on. The lamp test input (~TEST) goes low when the switch on the LCU is depressed and causes the LED CR7 to go on.

Model 1150A DVOR

The RF Monitor contains a temperature sensor U11 attached close to the heat sink to monitor the temperature of the heat sink. The RMS has the ability to read the temperature through the SPI interface. The signal SPI_SCK is the clock used to clock in and out the serial data. The SCK signal is buffered by U8A. The SPI_MOSI (master out slave in) line is serial data coming from the RMS. Data on this line enters U8A pin 2 and is buffered and exits at the Y1 output. The signal ~SPI_CS2X is active low when the RF Monitor board is being addressed by the RMS. Clock and data information is always present but ignored by the RF Monitor when the ~SPI_CS2X is high.

Buffer U8 is used to buffer the SPI_MISO data out of the RF Monitor to the RMS. The output at Y1 is tri-stated when the data is a high and active low when the data at the ~OE goes low. This allows for many of the other modules to use the same SPI_MISO line back to the RMS. Resistor R58, R59, R60, R61 and U13 are used to decode the addressing of the RMS so that the RF Monitor responds to the correct ~SPI_CS2X and address. The circuit U13 provides for parallel input output from the RMS SPI port. This allows for selection of either the temperature sensor U11 or EEPROM U10. The EEPROM is used to read and write data from the RMS. This EEPROM holds the Rf Monitor serial number and revision information programmed by the technician through the PMDT screens.

2.3.2.9 RMS Processor Block Diagram Theory

Refer to [Figure 2-12](#). The Remote Monitoring System (RMS) CCA performs communications via thirteen serial ports plus a parallel port, and facilitates monitoring/control in a single or dual VOR system. The RMS CCA receives battery-backed DC power from the BCPS CCAs at connector J2, through OR'd diodes, and regulated to +5V and +3.3V supplies for use by the RMS CCA to power the microcontroller and all of its associated circuitry.

The U8 microcontroller utilizes external flash ROM, non-volatile RAM (NVRAM), synchronous dynamic RAM (SDRAM), a voltage supervisor/watchdog reset circuit, and an oscillator to form the core microcomputer. The U8 microcontroller also includes a direct memory access (DMA) controller, serial ports, and general purpose input/output (I/O). Microcomputer peripherals include a real-time clock (RTC), universal asynchronous receiver/transmitters (UARTs), a parallel port interface (PPI), a USB host port, a USB slave port, off-board bus buffers, and more general purpose I/O.

The U8 microcontroller's flash ROM is factory programmed using the J4 SPI boot header while factory debug is accomplished using the J3 emulator header, the JP3 debug header, and the JP4 PMDT RS232 header. None of the aforementioned connectors and headers will be used by the customer in the field.

RMS communication to the LCU CCA occurs via the parallel port established by U29 through U32 and connector P1. The LCU also returns system control signals through P1 such as *TEST (lamp test) and *MRESET (master reset). Configuration switches on the Backplane CCA define the system set-up to the RMS when it reads them via the Facilities CCA through the external address/data bus on connector P2.

The U8 microcontroller communicates serially through one internal and twelve external UARTs. The internal UART is the debug port of JP3. The other twelve UARTs control communications to Monitors 1 and 2, Audio Generators 1 and 2, Remote Maintenance Monitor (RMM), Spare #1, Radio Modem, LCD, BCPS, Spare #2, Ethernet, and the PMDT. Two options are possible for local PMDT communications. The PMDT may be connected to USB connector J1 with header JP2 strapped for USB operation. The second option (in factory only) has the PMDT connected to RS232 header JP4 and header JP2 strapped for RS232 operation.

These eleven external UARTs (not including the PMDT) route to connectors P1 and P2. The host USB port of connector J2 is available for possible future options such as connection to a printer.

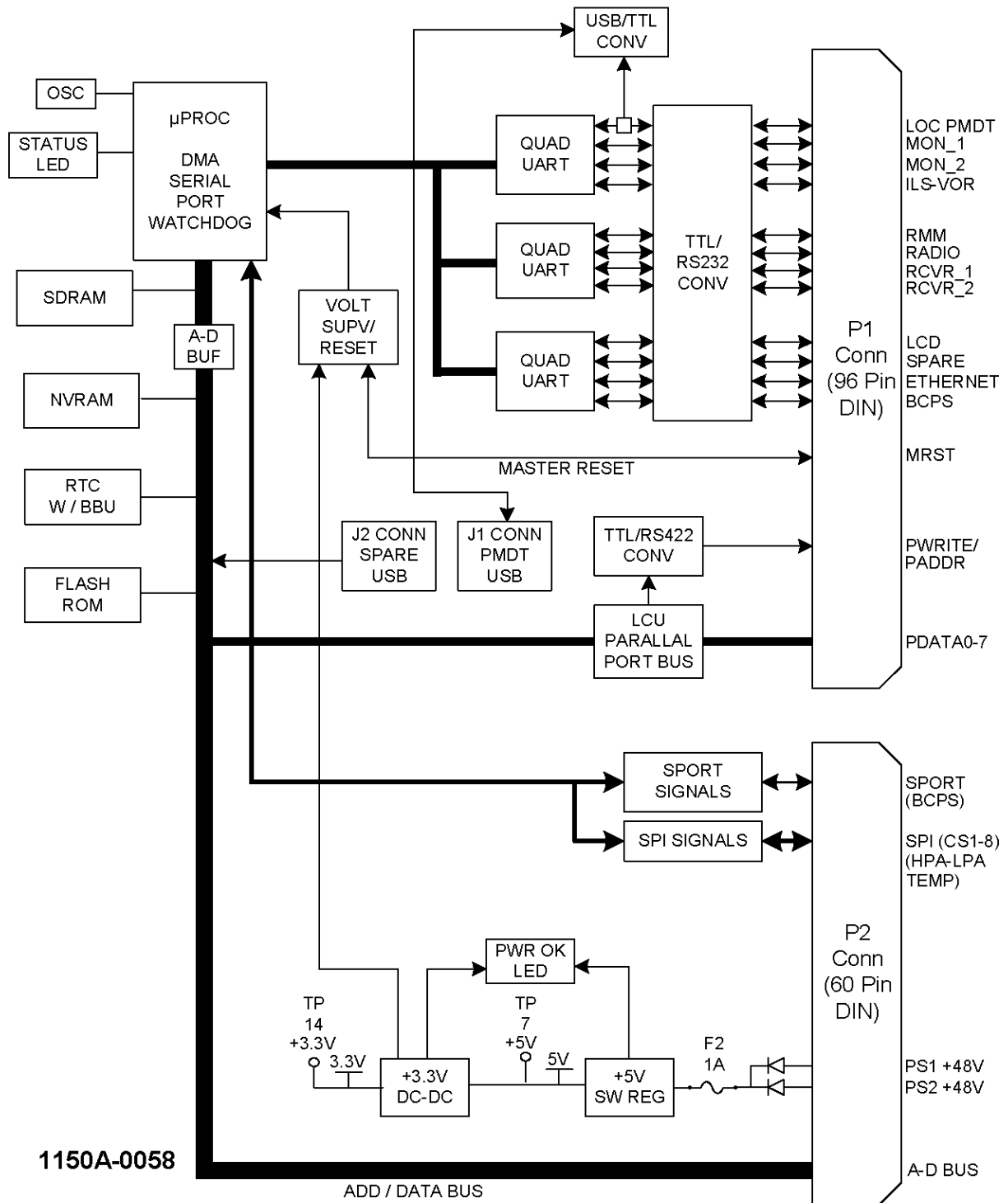


Figure 2-12 RMS CCA Block Diagram

2.3.2.9.1 RMS CCA Detailed Theory

Refer to [Figure 11-17](#). Battery-backed DC power 1_+48V and 2_+48V enter via connector P2-25 and P2-26, diode-OR'D by diodes CR13 and CR14, and fused by F2. This voltage is further regulated to +5V by DC-DC converter U39, diode CR15, and inductor L3. Over-voltage protection for the +5V is provided by SCR Q5, zener diodes CR19 and CR20, capacitor C115, and resistor R65. The +5V supply is further regulated by linear regulator U40 to create DVCC (+3.3V). The +5V is measurable at TP14 while DVCC is available at TP7.

The DVCC and +5V supplies power the U8 microcontroller and its peripherals. The U8 microcontroller acts as a DC-DC converter to create +1.2V (measurable at TP3) for powering its core (VDDINT) by pulse-width-modulating U8-4/5 and using transistor Q1, diode CR2, and inductor L1. Diode CR1 insures proper power supply sequencing during power-up/down.

The U8 microcontroller utilizes 512Kx16 of flash ROM (U1 and U2) for non-volatile program storage as well as 32Kx8 non-volatile RAM (U3) for variable storage. Oscillator Y2 provides the system clock for U8 as well as UARTs U16, U22, and U28 after buffering by U17. The system clock can be measured at test point TP1.

Data buffers U33/U34 and address buffers U35/U36 are decoded by AND gates U47:B, U47:C, and U47:D to activate the buffers only during a valid asynchronous memory select cycle. Resistor networks RN5 through RN9 act as pull-ups on these buffered bus lines. Only the bus lines between U8 and the 16Mx16 SDRAM (U4) are not buffered in some form. The U4 SDRAM is used for program and variable storage and has very fast access/refresh times.

The U8 microcontroller has direct control of the CPU_OK LED (CR5) by utilizing output PF8 (U8-36) and transistor Q2. The ~TEST signal, from the LCU via connector P2-B8, also can light the CR5 LED when active. Zener diode CR17 limits the maximum voltage while resistor R11 limits the maximum current of the CR5 LED.

Buffer U37 is used to buffer address lines A17, A18, and A19, control signals ~AOE and ~AWE, as well as the serial peripheral interface (SPI). The SCK, MISO, and MOSI SPI signals (U8-53, U8-54, and U8-55) along with ~SPI_CS0 (U8-49) are used in conjunction with the SPI Boot header J4 for in-factory programming of flash ROM. Latch U7 and inverter U10 combine to create the SPI chip select signals ~SPI_CS1 through ~SPI_CS8 for communications to off-board serial SPI devices through connector P2-A8 through P2-A16.

Real-time clock (RTC) U15 is clocked by oscillator U9 and battery-backed up by battery B1 if header JP1 is strapped between JP1-2 and JP1-3. The 512 Hertz heartbeat of RTC U15 can be measured at test point TP13. Oscillator U9 is a highly accurate temperature-compensated crystal oscillator (TCXO) whose accuracy eliminates the need for a potentiometer or adjustable capacitor.

Emulator header J3 is used for in-factory testing and development only.

The ~MRESET signal from the LCU enters via connector P2-B16 and is filtered by inductor FL1 and capacitor C39 to create reset signal ~EXT_RES. Signal ~EXT_RES is bi-directional in that either the LCU or the RMS can cause the signal to be active and reset the entire VOR system.

When the LCU pulls ~MRESET (and subsequently ~EXT_RES) low, voltage supervisor / watchdog input U6-1 is low; causing output U6-7 to go low which resets the U8 microcontroller and on-board latch U7 immediately. UARTs U16, U22, and U28 as well as USB host U38 will also be immediately reset by the RESET output of inverter U17:A. Latch U29 will be reset after being delayed by inverters U45:A, U45:B, resistor R13, capacitor C114, and diode CR16.

The RMS can initiate a system reset by activating ARM_SYS_RES (U29-9) and stopping the periodic strobing of voltage supervisor / watchdog input U6-6. A reset from U6-7 will occur approximately one second after the last watchdog strobe; causing inverter U17:A, transistors Q4/Q3 and ~EXT_RES to become active. The reset will clear after ~DELAYED_RESET from U45:B clears latch U29-9 ARM_SYS_RES; which in turn shuts off transistor Q3 and releases ~EXT_RES.

A reset can also be initiated by voltage supervisor / watchdog U6 when the power supply voltage on U6-2 drops too low; causing U6-7 to activate.

Latches U29 and U31, as well as buffer U32, establish an 8-bit parallel port for LCU communications. Latch U29 signals PWRITE, PADDR, ~PREAD_EN, and PIN/~POUT determine a read or write bus access. The PWRITE and PADDR signals are converted to RS422 by U30 before routing to connector P1.

Quad UART U16 provides four serial ports of the RMS CCA; the local PMDT, Monitor1, Monitor2, and Spare #1. The local PMDT has two possible connection means; either through USB connector J1 or RS232 header JP4. PMDT local select header JP2 must be strapped properly for either of them to operate. If the RS232 option is selected (normally only at the factory), U11 performs the RS232-TTL level conversions. If the USB option is selected, U20 performs the USB-TTL translations. U20 is clocked by crystal Y3 and serial EEPROM U5 may be used for USB ID storage. U20 also toggles LEDs CR6 and CR7 to indicate transmission and reception of USB data via the J1 USB-B connector. The ~TEST signal will also light these LEDs through CR8/CR11 when active.

Header JP3 has debug communications that originate as TTL at U8-81/82 before being converted to RS232 by U11. This header is typically used for factory debug / development only.

The Monitor1, Monitor2, and Spare #1 serial ports from U16 are converted to RS232 by U11 and U12 before connection to P1. The interrupt outputs of quad UART U16 are pulled down by resistors R37, R38, R39, and R41 before being combined by OR gates U13:B, U13:C, and U13:A to create UART1_INT. All twelve interrupt outputs of quad UARTs U16, U22, and U28 are logically combined to eventually create UART_INT which connects to microcontroller U8-48. The U8 microcontroller determines the source of the interrupt by polling.

LED_PWR, which originates between diode CR13 fuse F1, sources zener CR22 through current-limit resistors R66, R67, and R68 to create a precision +10V that can be measured at TP15. The precision +10V powers “window” comparators U46:A and U46:B; which compare the +5DIG voltage at U46-4 and U46-7 to the trip points established by resistors R70, R71, and R72 at U46-5 and U46-6. The precision +10V also powers “window” comparators U46:C and U46:D; which compare the DVCC (+3.3V) voltage at U46-8 and U46-11 to the trip points established by resistors R73, R74, and R75 at U46-9 and U46-10.

As long as both the +5DIG and DVCC are within the “window” trip points; the U46-2, U46-1, U46-14, and U46-13 comparator outputs will be pulled-up to +10V through resistor R69; turning on both transistors Q6 and Q7.

Transistor Q6 being on lights the PWR_OK LED (CR25) through current-limit resistor R76 and voltage-limit zener CR24. Transistor Q7 being on pulls the ~PWR_OK signal low through resistor R77. The ~PWR_OK signal is read at microcontroller U8-32 (PF12).

If either +5DIG or DVCC go above or below the “window” trip points, both transistors Q6 and Q7 will shut off; darkening the PWR_OK LED (CR25) and causing the ~PWR_OK signal to go high. The ~TEST signal (when active low) is guaranteed to light the PWR_OK LED (CR25) through diode CR23.

Quad UART U22 provides four more serial ports of the RMS CCA; the RMM, Radio, Audio Generator 1, and Audio Generator 2. These ports are converted to RS232 by U12 and U25 before routing to connector P1.

Quad UART U28 provides the final four serial ports of the RMS CCA; the LCD, the BCPS, the Spare #2, and the Ethernet. These ports are converted to RS232 by U25 and U26 before routing to connector P1.

The U38 USB host controller connects to the U8 microcontroller via an 8-bit asynchronous bus. The J2 USB-A connector is powered by filtered (L2) and fused (F1) supply +5DIG. The U38 USB host is clocked by oscillator Y4 and has transient voltage suppression (TVS) protection provided by U41.

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Decoding of the address space used by the U8 microcontroller is provided by decoders U23, U24, U21, and U18. All decoder outputs are used for on-board devices except for U24-10, named ~EXT_CS. This output defines the address space that is used to decode the Facilities CCA devices. Buffers U43 and U44 establish an 8-bit asynchronous bus for communications to/from the Facilities CCA. The inputs and outputs of buffers U43 and U44 as well as ~EXT_CS route to connector P2.

The U8 microcontroller has a synchronous serial port controller (SPORT) that is used for communications to the off-board battery charge / power supply controller or controllers (Spare Slot). The SPORT signals are buffered by U42 before connection to P2.

2.3.2.10 Facilities CCA Theory

Refer to [Figure 2-13](#). The Facilities CCA provides system I/O for the RMS CCA. Many of the inputs and outputs of the Facilities CCA eventually connect to the Interface CCA after routing through the Control Backplane CCA. System_1 and system_2 battery-backed power supplies (nominally 48VDC) enter connector P2 where they are diode-OR'D together and regulated down into several lower voltages; including +24V, ±15VDC, ±12VDC, +5VDC, and +3.3VDC.

U1 and U7 DC-DC converters regulate the +48V down to +24V and +5V respectively. The +24V supply is routed out connector P2 for powering the Interface CCA. The +5V supply powers several on-board digital and analog integrated circuits as well as powering DC-DC converter PS1 to create ±15VDC. Several linear regulators then create the ±12VDC supplies from the ±15VDC for powering RS232 integrated circuits and the analog signal processing system.

All power supplies, including the system_1 and system_2 supplies, can be monitored by the RMS CCA through the analog-digital converter. The RMS CCA will light on-board PWR_OK indicator CR24 if all supplies are within range. The ~TEST signal, which originates at the LCU CCA and enters on P2-B8, will light all on-board indicators when active. The ~TEST signal will also cause audio to be emitted from speaker SPK1 when active.

The ~MRESET signal, which originates at the LCU CCA and enters via P1-B16, resets U8 when active. U8 outputs ~RESET, which clears the outputs of all on-board latches. ~RESET is also asserted by U8 if the +3.3V supply drops too low.

An asynchronous data and address bus provided by the RMS CCA enters via DIN41612 connector P2. The address bus is decoded into 10 segments for input buffers and output latches. Input buffers are the U27 A-D converter bus, U28 and U29 system configuration switches, U31 amplifier powers status, U32 monitor powers status, U18 frequency configuration switches, and U37 TACAN antenna status (not used). The output latches are U22 A-D converter control, and U23 Ident tone multiplexer control.

As mentioned previously, all power supplies can be monitored by the RMS CCA through on-board U26 A-D converter as well as the U30 voltage reference, exterior and interior temperatures, ten spare analog inputs, and four spare digital inputs. Exterior and interior temperatures originate at the Interface CCA and are conditioned by U19:A and U19:B operational amplifiers. The spare analog inputs and spare digital inputs also originate at the Interface CCA. All of these analog signals are switched through U20 and U21 multiplexers to the single channel A-D converter and read digitally via buffer U27.

The system configuration switch signals, SCON0 through SCON15, originate on the Control Backplane CCA and enter via DIN41612 connector P1. Two of these configuration switches, DIALUP/~EXT and DED/~RADIO, determine whether U12 and U14 on-board modems or external modems connected to the Interface CCA are active. If the U12 and U14 modems are selected, they communicate to the RMS CCA serially once their TTL signals are converted to RS232 by U11 and U13. The U12 and U14 modems each have a speaker output which is multiplexed through U16 to the U15 amplifier and SPK1 speaker. Both U12 and U14 modems have on-board tip and ring transient voltage suppression (TVS) before eventually routed to the Interface CCA and more TVS protection.

U31 and U32 buffer the power OK signals of the Carrier Amplifier CCAs, Sideband Amplifier CCAs, RF Monitor and two BCPS CCAs as well as the A-D status signal, the INTERLOCK signal, the ~FANS_OK signal, the SMOKE_DETECTOR signal, and the INTRUSION_SENSOR signal. All of these signals originate at various cards in the three racks in the VOR except the last four signals, which originate at the Interface CCA.

The U18 buffer reads the frequency select switches, which reside on the Control Backplane CCA and determine the operating frequency of the VOR system.

The U22 latch controls the 32 channels of analog signals through multiplexers U20 and U21 as well as A-D convert/address and PWR_OK indicator. The U23 latch provides the spare digital outputs of the Interface CCA after buffering by U24 as well as the Ident tone multiplexer control and the fans (if installed) on/off signal through transistor Q2. Test header J1 is used for factory testing only.

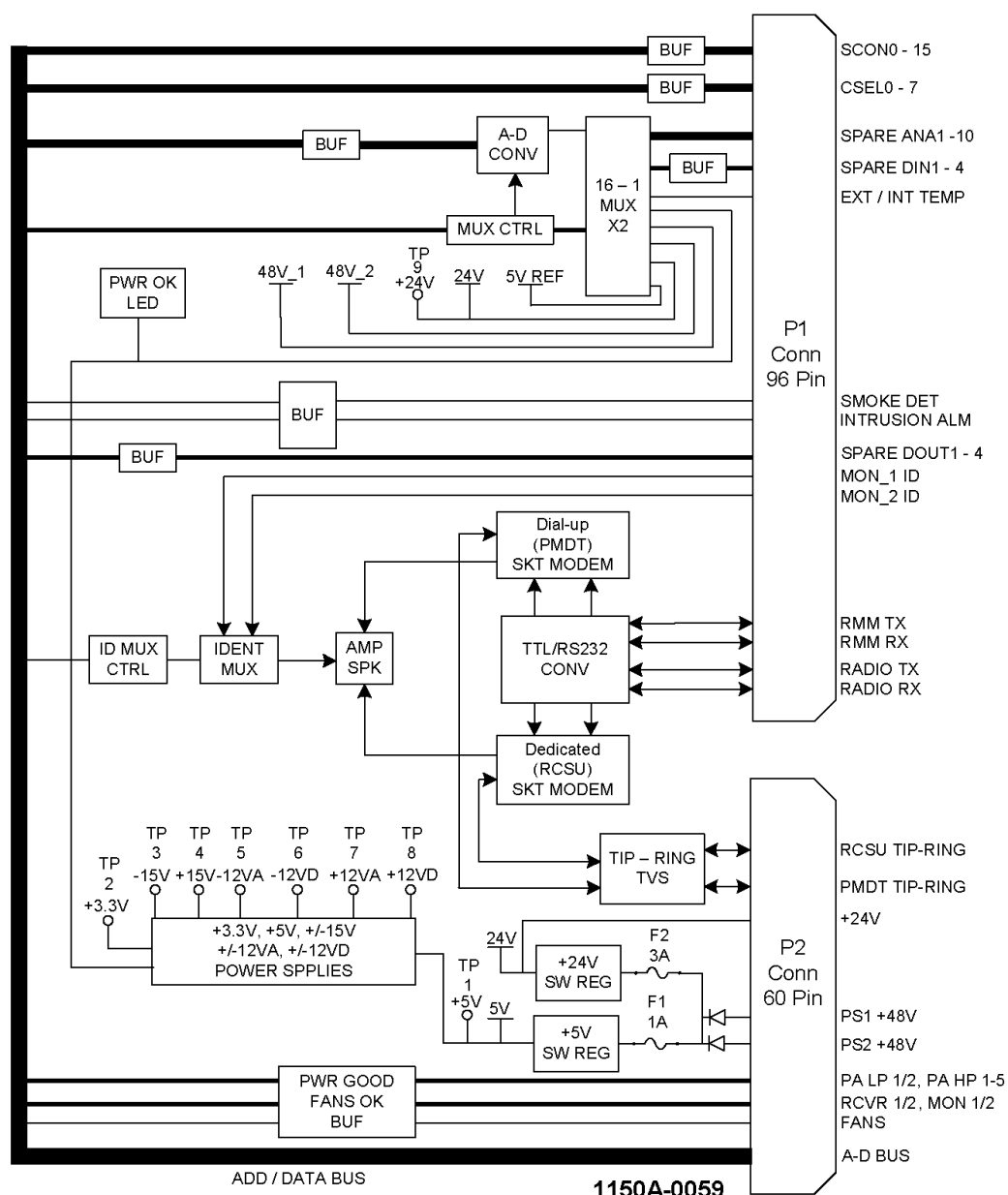


Figure 2-13 Facilities CCA Block Diagram

2.3.2.10.1 Facilities CCA Detailed Theory

Refer to [Figure 11-18](#). System1 and System2 +48V power from connector P2-25 and P2-26 are scaled down by resistor networks RN1 and RN2 for input to the A-D converter as well as diode-OR'D by CR1 and CR2 to create the facilities +48V supply. This supply (also named LED_PWR) lights the CR24 PWR_OK LED when transistor Q1 is turned on under software control by U22-19; indicating all monitored power supplies are within range.

The facilities +48V is fused by F1 and regulated by regulator U1, L1, diode CR3, and C2 to create +5DIG. Zener CR36, R68, and SCR Q3 protect downstream circuitry in the event of an over-voltage event by opening fuse F1. Zener CR37 will short to ground and protect the downstream circuitry if the SCR/Fuse-blowing circuitry fails for any reason.

The +5DIG supply is further filtered and regulated by regulator U2 and capacitors C3 and C4 to create the +3.3V supply. The +5DIG supply is also input to DC-DC converter PS1 to create -15V and +15V supplies. The -15V is filtered and regulated by L2, C8, U3, and C9 to realize -12ANA and by C7, U4, and C10 for -12DIG. The +15V output is filtered and regulated by L3, C12, U5, and C13 to realize +12ANA and by C11, U6, and C14 for +12DIG.

The facilities +48V also feeds fuse F2 and regulator U7. Switching regulator U7, C15, L4, CR4, CR5, R10, C17, and R11 combine to convert 48 volts to +24V. Zener CR38, R69, and SCR Q4 protect downstream circuitry in the event of an over-voltage event by opening fuse F2. Zener CR39 will short to ground and protect the downstream circuitry if the SCR/Fuse-blowing circuitry fails for any reason.

The ~MRESET signal enters via P1-B16, is filtered by FL1/C19, diode-isolated by CR6, and resets U8 when active. U8 outputs ~RESET, which clears the outputs of on-board latches U22, U23, and U38. ~RESET is also asserted by U8 if the +3.3V supply drops too low after R14 and before U8-2.

The ~TEST signal enters on P2-B8 and will light on-board indicators CR13-CR21, and CR24 when active. The ~TEST signal will also cause audio to be emitted from speaker SPK1 when active. The ~TEST signal is transient-voltage-suppression (TVS) protected by CR40.

Asynchronous data and address busses provided by the RMS CCA enter via connector P2 and are pulled-up by resistor networks RN12 and RN13. The address bus is decoded into sixteen segments by U9 and U10; ten of which are used by the Facilities CCA.

The ten spare analog inputs (SPARE_ANA1 through SPARE_ANA10) and four spare digital inputs (SPARE_DIN1 through SPARE_DIN4) enter via connector P1 and are terminated to ground by resistor network RN3 before connection to analog multiplexers U20 and U21.

The DIALUP/~EXT control signal enters via P1-C26. When this signal is high, buffer/converter U11 is enabled and RMM_TX_232, RMM_RX_232, RMM_DTR_232, and RMM_DCD_232 signals will pass through U11 to Dial-up modem U12 to become ~DU_TXDD, ~DU_RXDD, ~DU_DTRD, and ~DU_DCDD. Components R19, R18, CR9, R20, R17, and CR10 convert +5V signal levels to +3.3V between U11 and U12. Dial-up modem U12 lights indicator CR13 when a RING is received. Dial-up modem U12 also lights indicators CR14 through CR17 when serial data and control signals are active.

The tip and ring signals from Dial-up modem U12 are TVS-protected and filtered by CR7, FL2 and FL3 before exiting connector P2-B14 and P2-B15. Audio from U12-64 is scaled by R29 and R31 before audio header JP1-1.

The DED/~RADIO control signal enters via P1-C25. When this signal is high, buffer/converter U13 is enabled and RADIO_TX_232, RADIO_RX_232, RADIO_DTR_232, and RADIO_DCD_232 signals will pass through U13 to Dedicated modem U14 to become ~DED_TXDD, ~DED_RXD, ~DED_DTRD, and ~DED_DCD. Components R22, R24, CR11, R23, R25, and CR12 convert +5V signal levels to +3.3V between U13 and U14. Dedicated modem U14 lights indicators CR18 through CR21 when serial data and control signals are active.

The tip and ring signals from dedicated modem U14 are isolated, TVS-protected, and filtered by T1, CR8, FL4, and FL5 before exiting connector P2-A14 and P2-A15. Audio from U14-64 is scaled by R28 and R30 before audio header JP1-3. Three more sources of audio (other than the modems) are controlled by analog multiplexer U16. MON1_AUDIO_ID and MON2_AUDIO_ID from P1-C1 and P1-C2 (originally from the Monitor CCAs) connect to multiplexer U16-15 and U16-12. The third audio source is generated by 1KHz oscillator CR34, U17:A, C65, and R62 when the ~TEST signal is active. ID_MUX0 and ID_MUX1 (U16-11 and U16-10) select monitor audio through U16 except when ~TEST is active.

Resistors R39 and R38 scale the monitor or test audio output of U16-3 and feed it to AC-coupling capacitor C30. Amplifier U15 amplifies the sum of audio presented through R32, R33, and R34 and drives speaker SPK1 as determined by gain resistor R37. Amplifier U15 (and therefore all audio) is disabled if no jumper is present between audio header JP1-5 and JP1-6. Each modem's audio output can be disabled by either removing jumpers between audio header JP1-1 and JP1-2 or JP1-3 and JP1-4.

The exterior and interior temperature circuitry operates identically. Therefore only the exterior shall be discussed. The exterior temperature sensor signal (EXTERIOR_TEMP) from P1-A21 is converted from current to voltage by R41 and R43 before routing to buffer U19-3. The U19-1 buffered output (EXT_TEMP) is scaled by resistor network RN14-5/12 and RN14-6/11 before connection to the J1 test header and analog multiplexer U21-26 as ETMP_SCALED.

Test header J1 is used for factory testing only.

All on-board power supplies are scaled and presented to both the J1 test header and analog multiplexers U20 and U21. These supplies are DVCC (+3.3V), +5DIG, +12DIG, +12ANA, -12DIG, -12ANA, +15V, -15V, +24V, 1_+48V, and 2_+48V and are scaled by resistor networks RN14, RN4, RN5, RN1, and RN2. Other signals routed to the analog multiplexers are SPARE_ANA1 through SPARE_ANA10, SPARE_DIN1 through SPARE_DIN4, +5Vref created by U30, digital ground, and analog ground.

An individual channel of the 32 possible channels for the U20/U21 analog multiplexer pair is selected by MUX0 through MUX4 from latch U22. Inverter U17:B insures MUX4 enables only U20 or U21. The enabled U20 or U21 multiplexer passes its signal to buffer U25-3. Buffer output U25-6 passes the signal to A-D converter U26-14.

The U26 A-D converts the analog input signal to digital data outputs when commanded by latch U22-15. The end-of-conversion is signaled by U26-28; which is read through buffer U31-9. The digital data outputs of the A-D are pulled-up by RN6 and buffered through U27 to the data bus.

The system configuration switch signals (SCON0 through SCON15) enter via connector P1, are pulled-up by resistor networks RN7 and RN8, and then connect to buffers U28 and U29. Channel select inputs CSEL0 through CSEL7 enter via connector P1, are pulled-up by resistor network RN11, and are buffered to the data bus by U18.

Power OK signals from the Sideband Amplifiers, Carrier Amplifiers, BCPS CCAs, and RF Monitor as well as status signals INTERLOCK and ~FANS_OK connect to buffers U31 and U32 and resistor networks RN9 and RN10. Resistors R16 and R26 provide a high current pull-up for SMOKE_DETECTOR and INTRUSION_SENSOR signals before buffer U32.

Latch U23 drives SPARE_DOU1 through SPARE_DOUT4 through buffer U24 to connector P1. Latch U23-12 drives the FANS_ON signal through inverter U17:C and transistor Q2 to connector P2-B16 while CR42 provides transient protection. Finally, latch U23 controls audio multiplexer U16 via ID_MUX0 and ID_MUX1 (discussed previously).

NOTE

TACAN interfaces are described but not used in the VOR system. The Interface CCA is also used in DME/TACAN systems and common to the VOR product.

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The U37 buffer reads TACAN antenna controller signals which enter through connector P1 and are converted to TTL by U34. The U38 output latch directs activity of the TACAN antenna controller after the U38 latch signals are converted to RS422 by U35 and U36. The U38-19 loop-back signal may be used for fault-isolation purposes to buffer U37-9. Latch U38-16 also controls ~TACAN_RESET through transistor Q5 and TVS diode CR42 before routing to P1-C8.

2.3.2.11 Interface CCA Theory

The Interface CCA provides interface connections between the RMS/Facilities/Control Backplane CCAs and the outside world. Examples include spare analog and digital inputs, spare digital outputs, temperature sensors, smoke detector, intrusion sensor, and a TACAN antenna controller. RS232 communications are provided to RCSU and PMDT terminals as well as an optional Ethernet module. All signals are protected by transient voltage suppression (TVS) devices on the Interface CCA before exiting.

2.3.2.12 Interface CCA Block Diagram Theory

NOTE

TACAN interfaces are described but not used in the VOR system. The Interface CCA is also used in DME/TACAN systems.

Refer to [Figure 2-14](#). All connections between the Interface CCA and the RMS/Facilities/Control Backplane CCAs are accomplished via headers J1 and J2. The J2 and J3 connections will not be used in a VOR system since there will not be a TACAN antenna system controller.

Connectors J5 and J6 are DB9-types which provide interface to the RCSU and PMDT terminals mentioned previously.

Connector J7 is an RJ11 phone jack provided for exterior temperature sensing.

Connector J8 is a header provided for in-factory test purposes.

Connector J9 is an RJ45 jack intended for use as an Ethernet port. The port will be powered by a +3.3V DC-DC converter (PS1).

Terminal block TB1 facilitates connection of up to ten spare analog inputs, four digital inputs, and four digital outputs.

Terminal block TB2 allows connection of the RCSU and Dial-Up modem tip and ring signals. These signals are transient protected by common-mode chokes as well as spark-gaps, sidactors, and power resistors. INTERLOCK and EXT_KEY_IN signals are TVS-protected and optically isolated. True isolation for these signals may be enabled or disabled depending on the strapping of JP1 and JP2. EXT_KEY_OUT signals are optically isolated and TVS-protected before exiting via TB2.

SMOKE_DETECTOR, INTRUSION_SENSOR, ILS-VOR_RX_232, and ILS-VOR_TX_232 signals are TVS-protected before further routing. DET_IDENT1 and DET_IDENT2 signals are scaled as well as TVS-protected before exiting via TB2.

Earth ground lug E1 provides a return path for all transient voltage protection devices on the Interface CCA.

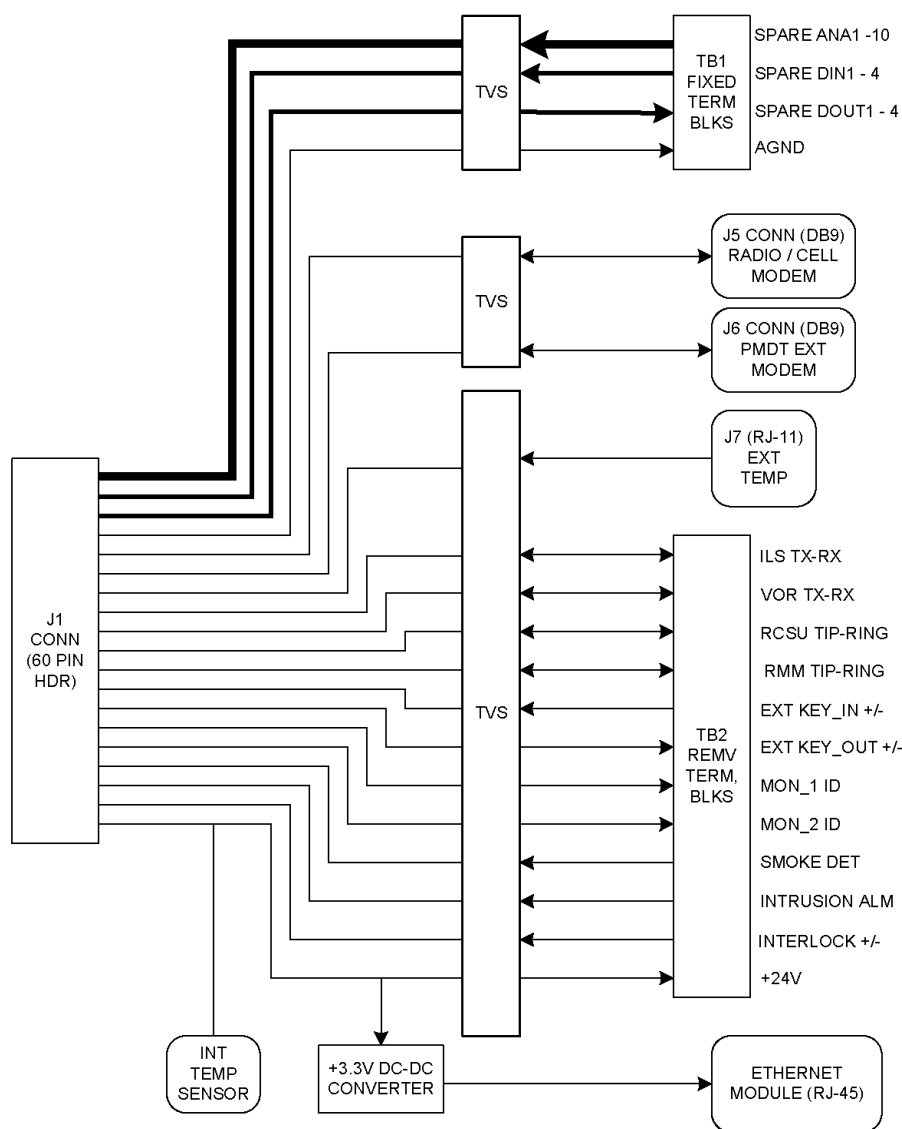


Figure 2-14 Interface CCA Block Diagram

2.3.2.12.1 Interface CCA Detailed Theory

Refer to Figure 11-8. The Interface CCA provides interface connections between the Backplane CCA and the outside world. All signals are protected by transient voltage suppression (TVS) devices. All connections between the Interface CCA and the Backplane CCA are accomplished via headers J1 and J2. The J2 and J3 connections will not be used in a VOR system since there will not be a TACAN antenna system controller.

On-board sensor U1 provides interior (cabinet) temperature while an exterior sensor can be interfaced via RJ11 connector J7. Interior temperature sensor U1 is TVS-protected by diode CR68 while the exterior temperature signal is protected by diode CR29. Earth or chassis ground is connected by lug E1 and inductor L1. Circuit or analog ground is accessible at test points TP4 and TP5.

The +24VDC power, which originates at the Facilities CCA, is indicated present by LED CR71 and resistor R30. The +24VDC is TVS-protected by diode CR44 and available to be measured through resistor R28 and test point TP3. The +24VDC powers the INTERLOCK and EXT_KEY_IN opto-isolators, the optional Ethernet module J9, and an off-board radio/RF modem via terminal block TB2-9.

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Ethernet module J9 has an RJ45 connector, is TVS-protected by U4 through U6, is powered by DC-DC converter PS1, and has its TTL signals converted to RS232 by U7 before routing eventually to the RMS CCA. Diodes CR41 through CR43 insure the proper voltage level before entry into PS1. PS1 converts +24VDC to +3.3VDC and diode CR72 provide TVS protection.

All TACAN antenna system controller signals are TVS-protected by diodes CR45 through CR67 before routed to DB37 connector J3.

Test header J8 is used for factory testing.

The RCSU has two possible paths for communications; either tip-n-ring to terminal block TB2-1 and TB2-2 or RS232 to DB9 connector J5. The active path is configured by a system configuration DIP switch on the Control Backplane CCA. Diodes CR21 through CR24 provide TVS protection for the RS232 signals while resistors R21 through R24, spark-gap V2, sidactor Q3, and balun L2 provide the TVS protection for the tip and ring signals.

The PMDT also has two possible paths for communications; either tip-n-ring to terminal block TB2-3 and TB2-4 or RS232 to DB9 connector J6. The active path is configured by a system configuration DIP switch on the Low Power Backplane CCA. Diodes CR25 through CR28 provide TVS protection for the RS232 signals while resistors R17 through R20, spark-gap V1, sidactor Q2, and balun L3 provide the TVS protection for the tip and ring signals.

Spare I/O terminal block TB1 provides connection to ten spare analog inputs, four spare digital outputs, and four spare digital inputs. All of these signals are TVS-protected by diodes CR1 through CR18. All of these signals eventually route to the Facilities CCA.

External interconnect terminal block TB2 provides connection for the remainder of the signals of the Interface CCA. The SMOKE_DETECTOR and INTRUSION_SENSOR signals are TVS-protected by diodes CR37 and CR38. The ILS-VOR RS-232 signals are TVS-protected by diodes CR19 and CR20.

The INTERLOCK+ and INTERLOCK- signals are connected to opto-coupler U3:A. Full power supply isolation can be achieved by removing jumpers JP1A and JP1B from header JP1 if the customer is willing to provide an external supply. Current is set and steered through the LED of U3:A by resistors R14 through R15 and diodes CR36 and CR69. The transistor output of U3:A is TVS-protected by diode CR39.

The EXT_KEY_IN+ and EXT_KEY_IN- signals are connected to opto-coupler U3:B. Full power supply isolation can be achieved by removing jumpers JP2A and JP2B from header JP2 if the customer is willing to provide an external supply. Current is set and steered through the LED of U3:B by resistors R5 through R7 and diodes CR32 and CR70. The transistor output of U3:B is TVS-protected by diode CR40.

The EXT_KEY_OUT signal is TVS-protected by diode CR35 before routing to pull-down resistor R9 and transistor Q1. Resistors R10 and R11 bias the LED of opto-coupler U2 while diodes CR33 and CR34 transient protect the transistor outputs of opto-coupler U2. The transistor outputs are labeled EXT_KEY_OUT+ and EXT_KEY_OUT- before routed to terminal block TB1.

The MON1_AUDIO_ID and MON2_AUDIO_ID are transient protected by diodes CR30 and CR31 before being voltage-divided by resistors R1/R3 and R2/R4. The lower voltage level signals are called DET_IDENT1 and DET_IDENT2 before being routed to terminal block TB2.

2.3.2.13 AC Power Monitor CCA Theory

The AC Power Monitor CCA provides a means for the VOR system to measure the AC current and voltage levels of the obstruction lights and of the VOR system itself.

2.3.2.13.1 AC Power Monitor CCA Block Diagram Theory

Refer to [Figure 2-15](#). The AC Monitor provides a method of measuring the AC voltage for the Transmitter and obstruction light circuits individually. A step down transformer with a full wave rectifier is provided for each channel. The AC current for the Transmitter and obstruction lights travel through individual current transformers. The resultant AC voltage is provided to the BCPS CCA for rectification and current to voltage conversion.

2.3.2.13.2 AC Power Monitor CCA Detailed Theory

Refer to [Figure 2-15](#). The AC Power Monitor CCA provides a means for the VOR system to measure the AC current and voltage levels of the obstruction lights and of the VOR system itself.

NOTE

The Schematic for the 012186-0001 Circuit Card Assembly differs from the labeling on the mechanical housing. The terminal strips TB4 and TB5 are numbered in the opposite direction on the housing. This theory of operation follows the numbering on the schematic.

T2 is a current-sense transformer in series with the obstruction lights line supply from TB2-1 and TB1-2. AC current through the primary of T2 induces a current in the secondary. The secondary is connected to J1-3. A resistor on the AC Monitor CCA converts this current to voltage for measurement.

T3 is a voltage step-down transformer connected in parallel to the obstruction lights supply at TB1-1 and TB1-3. The transformer primary is strapped to accept a nominal 220 VAC. AC voltage on the primary is stepped-down on the secondary. The secondary is center-tapped and diodes CR1, CR2, CR5 and CR6 act as a full wave bridge rectifier and the rectified output is routed to J1-1.

T1 is a current-sense transformer in series with the VOR's line supply from TB3-1 and TB4-1. AC current through the primary of T12 induces a current in the secondary. The secondary is connected to J1-7. A resistor on the AC Monitor CCA converts this current to voltage for measurement.

T4 is a voltage step-down transformer connected in parallel to the VOR's supply at TB4-1 and TB4-2. The transformer primary is strapped to accept up to 220 VAC. AC voltage on the primary is stepped-down on the secondary and it. The secondary is center-tapped and diodes CR3, CR4, CR7 and CR8 act as a full wave bridge rectifier and the rectified output is routed to J1-5.

An external jumper must be connected at TB1-1 to TB1-2 if a photo cell switch is not connected in series with the obstruction lights. If a photocell is used then a wire must be connected from the output side of the photocell back to TB1-1.

Earth ground is also connected to the AC Monitor CCA via the board's mechanical mounting holes.

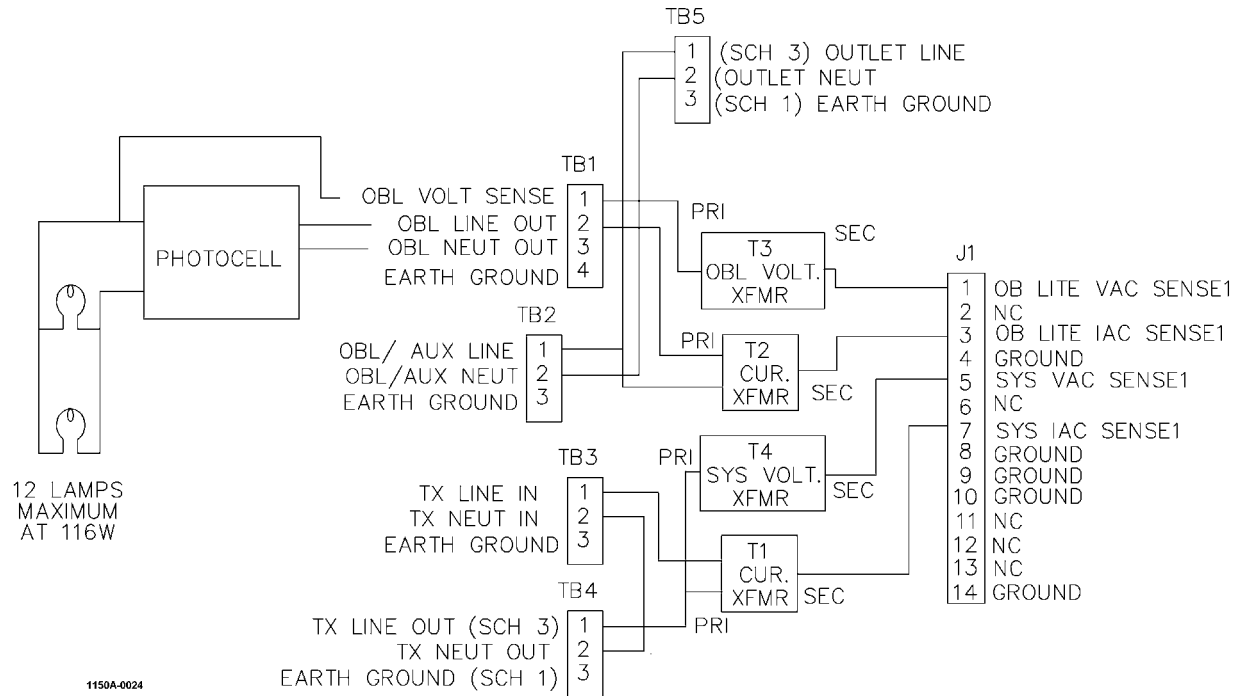


Figure 2-15 AC Power Monitor Block Diagram

2.3.2.14 Local Control Unit Theory

Refer to [Figure 2-16](#). The Local Control Unit (LCU) controls the normal operation of the VOR. All operational functions are performed by the LCU and are controlled by either front panel keyboard when in the local mode or by the Remote Maintenance Subsystem (RMS) through the parallel interface. The LCU is controlled by the Portable Maintenance Data Terminal (PMDT), Remote Control Status Unit (RCSU) or Remote Status Unit (RSU) through the RMS for all remote operator intervention or by the RMS for automatic restart. The LCU receives the alarm outputs from the installed Monitor circuit card(s) and depending on the configuration of the system, uses the results of these signals to determine alarm status. If an alarm is detected, the LCU shuts down the system currently radiating and transfers to the standby system in accordance with the system configuration. The LCU also provides the ability to disable monitors and bypass alarms as required by the operator.

The LCU provides +24V to the two possible synthesizer VCO circuits, the +24V to activate the transfer switch, and the transmit enable clock to the installed Audio Generators.

Status is reported by LED's visible to operator standing in front of the VOR, or through the RMS to the PMDT/RCSU/RSU. An alarm shutdown is reported to the RMS as well as indicated by an audible alarm.

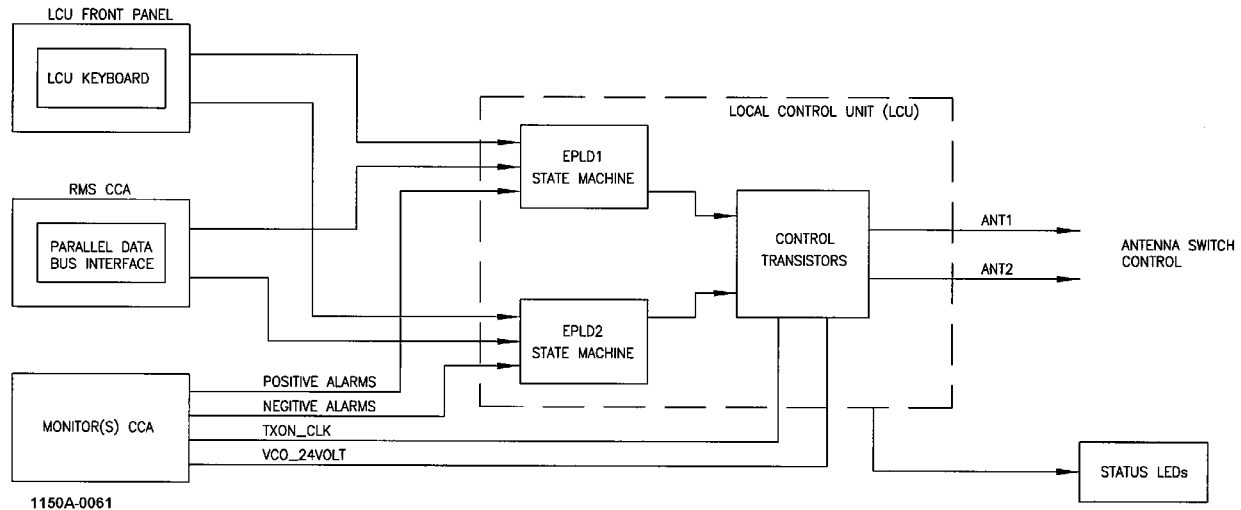


Figure 2-16 LCU Simplified Block Diagram

2.3.2.14.1 Local Control Unit Block Diagram Theory

Refer to [Figure 2-17](#).

2.3.2.14.1.1 DC to DC Converter

The LCU receives +48V from the two independent system power supplies and diode OR's the two sources to provide input power to a DC to DC converter which supplies all required voltages for the LCU.

2.3.2.14.1.2 Power Fail Detectors

Each of the two independent +48V sources is monitored by a voltage comparator to monitor the health and availability of power from each of the sources. These signals are used to determine voting logic for the alarm registers and are reported back to the RMS via the parallel interface.

2.3.2.14.1.3 Key Switch Registers

Front panel switches are de-bounced and held in the Key Switch Registers pending processing by the LCU transfer state machines. Commands received from the RMS via the parallel interface also control the contents of the Key Switch Registers. The registers will hold the last command received until the LCU transfer state machine processes the command.

2.3.2.14.1.4 Parallel Interface

The interface to the RMS is via a parallel data bus consisting of eight (8) data bits, an Address Command line, a Write Command line, and a Read Command line. The sequence to access internal registers within the LCU consist of the address being placed on the data bus followed by the strobing of the Address Command line to latch the address into the internal address register. This is followed by the Read Command line driven true to facilitate a read from the latched address. For a write command, the address is followed by the data to be written to the LCU followed by strobing the Write Command line. Alarm Configuration, Bypass Commands, Key Commands, and basic LCU configuration are some of the bits controlled by the RMS via the parallel interface. State machine Status, Power-fail Status, System Configuration bits (SCON), and Local/Remote status are some of the status bits that are readable by the RMS via the parallel interface.

2.3.2.14.1.5 1.8432MHz Oscillator/Divider Chains

The LCU employs a 1.8432MHz crystal oscillator to produce all frequencies required by the design. The frequency is divided by 512 to produce 3600Hz used to produce the audible alarm tone and the Transmit On clocks driven back to the monitors. The signal is further divided by 8 to produce 450Hz used as the system clock within the design. This signal is divided by 45 to produce 10Hz used in the 20 second delay counter and the Key De-bounce circuits.

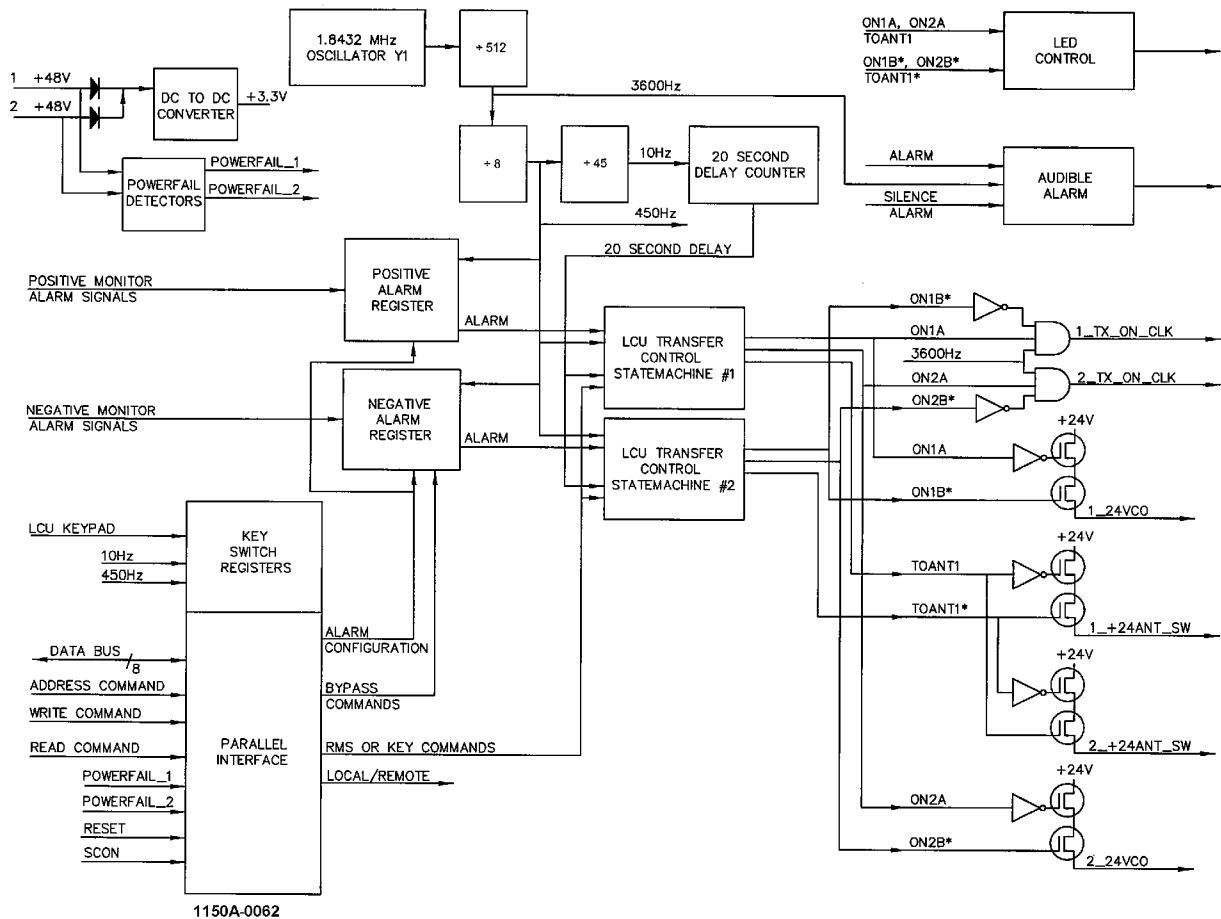


Figure 2-17 LCU Block Diagram

2.3.2.14.1.6 Positive Alarm Register

This register receives the positive (high True) alarms from the two monitors within a system. Depending on the configuration of the alarm voting and bypass logic, the Alarm Register will report an alarm to the transfer state machines if reported by the enabled monitors.

2.3.2.14.1.7 Negative Alarm Register

This register receives the negative (low True) alarms from the two potential monitors within a system. Depending on the configuration of the alarm voting and bypass logic, the Alarm Register will report an alarm to the transfer state machines if reported by the enabled monitors.

2.3.2.14.1.8 20 Second Delay Counter

The 20 second delay counter is activated whenever the system initially powers up or a transmitter has been shut down without transferring to a standby system to ensure that the system will not radiate any signal for a period of 20 seconds following the shutdown.

2.3.2.14.1.9 LCU Transfer Control State Machine #1 and #2 and Discrete Controls

The heart of the LCU is the two redundant transfer control state machines. These are configured by the RMS; receive key commands from the front panel or from the RMS, and process alarms reported by the monitors after being filtered by the Positive and Negative Alarm Registers. Once configured for on air, the state machines will drive out the required signals to enable the transmit on clocks (1_TX_ON_CLK, 2_TX_ON_CLK), enable the +24V power to the synthesizer VCO's (1_24VCO, 2_24VCO), and select the required system to be placed on the antenna (1_+24ANT_SW, 2_+24ANT_SW).

With the redundant state machines, detection of an error assures that the system generating the error will be removed from the air. The LCU transfers to the standby system if configured to do so either immediately for a hot Standby system or after a 20 second delay for a cold Standby system. If further alarms are detected, the LCU transfer state machines will shut the standby transmitter down and block any further transmission for a minimum of 20 seconds. Restarts are under the control of the RMS.

The LCU transfer control state machines report status back to the RMS indicating the state of the state machines, and any shutdowns that have occurred. The LEDs on the front panel reflect the current state of the state machines.

2.3.2.14.1.10 LED Control

Status is fed back to a local operator via the LED's on the front panel of the LCU. These reflect the state of the transmitters and the various alarms as reported by the monitors.

2.3.2.14.1.11 Audible Alarm

If an alarm as reported by the monitors is detected that is not bypassed, the audible alarm is generated. The audible alarm can be reset by pressing the Alarm Silence button on the front panel. In local mode, the audible alarm is disabled.

2.3.2.14.1.12 Monitor Alarm Interface

In order to insure that a monitor alarm signal is communicated to the control logic, redundancy is incorporated into the monitor alarm signals. Each alarm signal is sent as two signals, one active high and the other active low. In the LCU, resistors are used to pull each of their signals to their active (alarm) state. This insures that an alarm condition will be sensed if there is an open in either alarm line. If an alarm line is shorted to its inactive (non-alarm) state, the other line will communicate an alarm condition. If the 1_INT_ALARM+ signal is disconnected, a resistor will pull the input high resulting in an alarm condition being sent to the control logic in the EPLD U3. If the 1_INT_ALARM- signal is disconnected, a resistor will pull the input to a low logic level.

2.3.2.14.1.13 Station Control Logic

The station control logic is duplicated in both U1 and U3. The logic responds to local operator control through the pushbutton switch inputs as well as remote control through the parallel interface. The local operator can perform the following functions:

- a. Specify which VOR transmitter is to be designated as main.
- b. Turn either transmitter ON and connect it to the antenna.
- c. Turn either transmitter ON and connect it to the load.
- d. Turn either transmitter OFF.
- e. Toggle the bypass state of either of the monitored signal sources (Integral, Standby).
- f. Silence the aural alarm (until the next event causes it to sound).
- g. Toggle the state of local control. When local control is set, input from the keypad is enabled.

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The following functions can be performed by the RMS through the parallel interface:

- a. Functions a-g listed above.
- b. Enable or disable the alarm signals from either one of the monitors. When a monitor's alarm signals are disabled, it is functionally equivalent to the monitor producing constant alarms.
- c. Set the "AND/OR" state of the alarm logic when it combines the alarm signals from Monitor 1 with the alarm signals from Monitor 2. When set to "AND", both monitors must provide an alarm from the same source to cause the station to transfer. When set to "OR", Monitor 1 signaling an alarm or Monitor 2 signaling an alarm will cause the station to transfer.
- d. Set the "Maintenance Alert" state. This lights the corresponding LED on the panel.
- e. Set the "Remote Control Fault" state. This lights the corresponding LED on the panel.

In the alarm logic circuitry, the alarms from Monitor 1 alarm status are displayed on the panel. Similarly, the alarms from Monitor 2 alarm status are displayed on the panel. If a given monitor's alarm signals are disabled by the RMS, it is equivalent to all of that monitor's alarm signals being asserted. The state of the AND/OR setting determines whether both or either of the Monitor 1 or Monitor 2 signals are required to produce a transfer condition. If one of the two +48V power fail logic signals goes active, the alarm logic will force an alarm condition for the monitor pair that is powered from the corresponding +48V supply. In order to avoid shutting the VOR station down, the alarm logic is forced to the AND state. This allows the other monitor to monitor the system.

The alarm signals from the monitors have already been given the appropriate transfer delay times within the monitors. This results in an immediate transfer when the combinatorial requirements of the alarm signals are met. When a transfer condition occurs, the present transmitter that is connected to the antenna system is taken off the air. The other transmitter is connected to the antenna system, and turned on (if it is not already on). If the transmitter, not designated as main connected to the antenna system when the transfer condition occurs, the control logic will enter the shutdown state and both transmitters are turned off. Once the control logic enters the shutdown state, no further transfer operations will take place until a local operator or the RMS turns one of the transmitters on and specifies that it is connected to the antenna system. The Station Control Logic controls which transmitter is connected to the antenna system by the status of the +24V ANT outputs.

2.3.2.14.1.14 System Configuration Inputs

In order to reduce the amount of effort required to program various modules within the VOR for the proper configuration, there are eight logic signals that are sent from the RMS to each module to specify the system configuration.

2.3.2.15 Test Generator (1A3A5) CCA Theory

Test generator CCA performs two functions. The primary function is to provide a standard reference signal to the DVOR monitors for calibration whenever directed by the RMS CPU for monitor integrity testing. The secondary function is an operator maintenance function, which is to allow test signals to be sent to the monitor(s), as directed by an operator through the PMDT. The operator can vary signal parameters (i.e., frequency, percent modulation, phase shift, etc.) to determine if a monitor is functioning properly and will alarm at the required settings.

2.3.2.15.1 Test Generator CCA Block Diagram Theory

Refer to [Figure 2-18](#). The Test Generator CCA primary purposes are to generate test waveforms for verification of the Monitor CCAs as well as control of audio recording/play-back.

System1 and System2 +48VDC supplies from connector P2 are diode-OR'd and fused before routing to a +5VDC DC-DC converter. The +5VDC output is linearly regulated to +3.3VDC as well as switched to -5VDC by another DC-DC converter.

Each of the aforementioned output voltages is range-monitored by window comparators. The wired-OR'd outputs of the window comparators assert a power-OK signal and light an LED when all output voltages are within the tolerance windows. The power-OK signal eventually routes to the Facilities CCA for PMDT reporting.

The ~TEST signal when asserted from the LCU via connector P2 will insure the power-OK LED is lighted no matter the output of the window comparators.

Serial signals (SPORT) from connector P2 program the 32Kx16 static RAM (SRAM) via the U1 programmable logic device (PLD) with data to be clocked out to the 14-bit D-A converter. The test waveform from the D-A converter is amplified and buffered before exiting connector P1 and eventually routing to the Monitor CCAs.

The 19.6608MHz oscillator generates the clock for the SRAM and D-A converter as well as the watchdog clock to the reset supervisor through the PLD. The PLD is also reset when the ~MRESET signal from connector P1 is asserted. The PLD is factory-programmed via the J3 In-System-Programmed (ISP) connector.

Audio from the Monitor CCAs via connector P1 routes to the J2 audio jack. If headphones are not plugged into the J2 audio jack, audio is coupled through a transformer and out connector P1 for hook-up on the Control Backplane Voice terminal block.

Audio to the Audio Generator CCAs comes from either of two sources; the microphone input connector J1 through connector P1 or Voice terminal block on the Control Backplane.

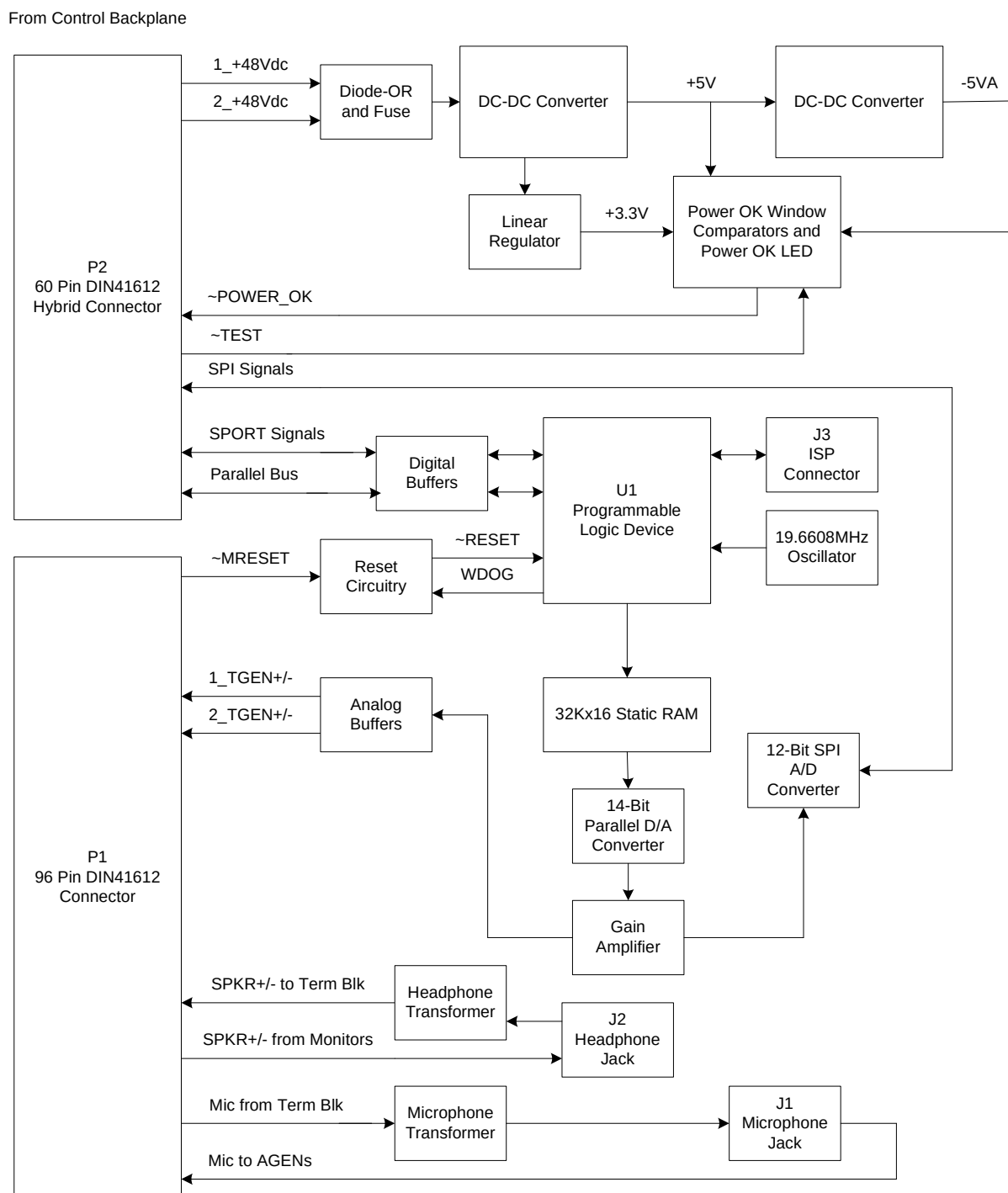


Figure 2-18 Test Generator CCA Block Diagram

2.3.2.15.2 Test Generator CCA Detailed Circuit Theory

Refer to [Figure 11-16](#). System1 and System2 +48VDC supplies from connector P2 are diode-OR'd by diodes CR3 and CR4 and fused by F1 before routing to the U10 DC-DC converter. The U10 DC-DC converter, diode CR6, inductor L3, and capacitor C32 create +5VDC, which is measurable on test point TP11.

Two types of over-voltage protection are utilized for DC-DC converter U10. SCR Q1 in conjunction with CR7, R33, R28, and C30 will activate and open fuse F1 if the output voltage exceeds approximately +6.8VDC. Zener diode CR8 provides redundant over-voltage protection.

The +5VDC supply powers linear regulator U11, which creates the +3.3VDC output. The +3.3VDC output is measurable on test point TP12 and is filtered by capacitor C36.

The +5VDC supply also feeds the U13 DC-DC converter to generate -5VDC. Capacitor C44, inductor L4, and capacitor C46 filter the -5VDC output, which is measurable at test point TP14.

LED_PWR, which originates at the diode-OR'd junction of diodes CR3 and CR4, sources zener diode CR10 through current-limit resistors R39 and R40 to create a precision +10VDC that can be measured at test point TP16. The precision +10VDC powers "window" comparators U19:A and U19:B; which compare the +5VDC voltage at U19-4 and U19-7 to the trip points established by resistors R42, R43, and R44 at U19-5 and U19-6.

The precision +10VDC also powers "window" comparators U19:C and U19:D; which compare the +3.3VDC at U19-8 and U19-11 to the trip points established by resistors R45, R46, and R47 at U19-9 and U19-10.

The precision +10VDC also powers "window" comparators U20:C and U20:D; which compare the -5VDC scaled by resistors R51 and R52 at U20-8 and U20-11 to the trip points established by resistors R48, R49, and R50 at U20-9 and U20-10.

While the +5VDC, +3.3VDC, and -5VDC supplies are within the "window" trip points, the U19-2, U19-1, U19-14, U19-13, U20-14, and U20-13 comparator outputs will be pulled-up to +10VDC through resistor R53; presenting a higher level on U20-4 and U20-6 than that presented by the R54 and R55 voltage-divided +10VDC on U20-5 and U20-7. Thus the U20-2 and U20-1 outputs go low. A low on U20-2 lights the CR11 PWR_OK LED through current-limit resistor R56 and voltage-limit zener diode CR12. A low on U20-1 pulls the ~TGEN_OK signal low, assuming a pull-up resistor after connector P2:A7 at the Facilities CCA.

If any of the +5VDC, +3.3VDC, or -5VDC supplies go above or below the "window" trip points, both U20:A and U20:B comparator outputs de-assert; darkening the CR11 PWR_OK LED and causing the ~TGEN_OK signal to go high, assuming a pull-up resistor after connector P2:A7 at the Facilities CCA.

The ~TEST signal from connector P2:B8, when active low, is guaranteed to light the CR11 PWR_OK LED through diode CR13.

The U1 PLD is factory-programmed via ISP connector J3 and clocked by the 19.6608MHz oscillator Y1. Reset supervisor U3 will reset the U1 PLD if one of three events occurs; the +3.3VDC supply drops too low, an external reset (~MREST) is asserted from connector P1:B16, or the watchdog signal at U3-6 becomes too slow. The watchdog signal is also buffered by U2 and presented as 30Hz SYNCH on front panel test point TP1.

The test generator waveforms are serially loaded into the U1 PLD by the primary and secondary transmit SPORT signals TSCLK1, DT1PRI, DT1SEC, and TFS1. These signals originate at the RMS CCA, enter via connector P2, are buffered by U18, and connect to PLD U1. The test generator data is serially echoed back to the RMS CCA for error-checking by the primary and secondary receive SPORT signals DR1PRI and DR1SEC, also buffered by U18 before exiting connector P2.

The U1 PLD constructs parallel data from the SPORT serial streams and stores the results in the 32Kx16 locations of SRAM U4 and U5. After all waveform data is saved, the U1 PLD cycles through all 32K locations at a 30Hz rate while also clocking D-A converter U6. Thus the digital data is converted to an analog test generator waveform at U6-22, amplified and filtered by U7:A, and presented to front panel test point TP5 as TGEN+.

Analog drivers U8:B, U7:B, U9:A, and U9:B create differential test generator waveform signals which exit via connector P1 and eventually connect to the Monitor CCAs for certification.

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Analog buffer U8:A sends a single-ended test generator waveform to A-D converter U14 for on-board testing and verification. The U14 A-D converter is serially controlled by signals SPI_SCK, SPI_MISO, and ~SPI_CS3X of the RMS CCA via connector P2. The U14 D-A converter has a built-in +2.5VDC reference which is filtered by capacitors C41 and C42, buffered by amplifier U21:A, and presented to the U12 Audio D-A converter.

The audio source is either microphone input MIC+_IN from connector J1 or transformer T2. Transformer T2, which is driven from the Control Backplane voice terminal block via connector P1, is disconnected when a microphone is plugged into connector J1.

Parallel data, address, and control (D0X, A1X, and ~AOEX for example) from the RMS CCA enter via connector P2, are buffered by U16 and U17, and decoded by the U1 PLD to determine the ~EXT signal. The ~EXT signal controls the U17 bus buffer data direction.

Audio output to connector J2 originates at the Monitor CCAs, enters as SPKR+ and SPKR- through connector P1, and arrives at headphone connector J2. If a headphone or speaker is not plugged into J2, audio output couples through transformer T1 as SPKR_XFMR+ and SPKR_XFMR-. These signals exit connector P1 and eventually terminate at the Voice terminal block on the Control Backplane.

2.3.2.16 Low Voltage Power Supply (1A3A4, 1A3A8) CCA Theory

There are two LVPS assemblies used on the transmitter cabinet. The low voltage power supply CCA. LVPS 1A3A4 is the low voltage power supply for transmitter 1 and 1A3A8 is the LVPS for transmitter 2. Each LVPS is identical in construction and operation. Each is interchangeable with the other.

2.3.2.16.1 Low Voltage Power Supply (LVPS) CCA Block Diagram Theory

Refer to [Figure 2-19](#). The LVPS CCA converts +48VDC system power to +28VDC, +5VDC, +12VDC, and -12VDC for eventual use by the Synthesizer, Monitor, and Audio Generator CCAs.

The +48V from connector P2 is fused and feeds two DC-DC converters. One DC-DC converter creates +28VDC while the other generates +5VDC, +12VDC, and -12VDC.

Each of the aforementioned output voltages is range-monitored by window comparators. The wired-OR'd outputs of the window comparators assert a power-OK signal and light an LED when all output voltages are within the tolerance windows. The power-OK signal eventually routes to the Facilities CCA for PMDT reporting.

The ~TEST signal when asserted from the LCU via connector P2 will insure the power-OK LED is lighted no matter the output of the window comparators.

The VCO_EN signal from the LCU via connector P2 is filtered and routed out to connector P2 and eventually the Synthesizer CCA as signal VCO_PWR.

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The VCO_EN signal from connector P2:C7 is filtered by inductor L5 and routed out connector P2:C9 as signal VCO_PWR.

+48VDC, which originates at connector P2:C26, sources Zener CR11 through current-limit resistors R18 and R19 to create a precision +10VDC that can be measured at TP10. The precision +10VDC powers “window” comparators U5:A and U5:B; which compare the +5VDC voltage at U5-4 and U5-7 to the trip points established by resistors R21, R22, and R23 at U5-5 and U5-6.

The precision +10VDC also powers “window” comparators U5:C and U5:D; which compare the +12VDC scaled by resistors R24 and R25 at U5-8 and U5-11 to the trip points established by resistors R21, R22, and R23 at U5-9 and U5-10.

The precision +10VDC also powers “window” comparators U6:A and U6:B; which compare the +28VDC scaled by resistors R30 and R32 at U6-4 and U6-7 to the trip points established by resistors R21, R22, and R23 at U6-5 and U6-6.

The precision +10VDC also powers “window” comparators U6:C and U6:D; which compare the -12VDC scaled by resistors R31 and R33 at U6-8 and U6-11 to the trip points established by resistors R27, R28, and R29 at U6-9 and U6-10.

As long as the +5VDC, +12VDC, +28VDC, and -12VDC supplies are within the “window” trip points; the U5-2, U5-1, U5-14, U5-13, U6-2, U6-1, U6-14, and U6-13 comparator outputs will be pulled-up to +10VDC through resistor R26; turning on both transistors Q3 and Q4. Transistor Q3 turned on lights the CR12 PWR_OK LED through current-limit resistor R35 and voltage-limit zener diode CR13. Transistor Q4 turned on pulls the ~LVPS_OK signal low, assuming a pull-up resistor after connector P2:A7 at the Facilities CCA.

If any of the +5VDC, +12VDC, +28VDC, and -12VDC supplies go above or below the “window” trip points, both transistors Q3 and Q4 will shut off; darkening the CR12 PWR_OK LED and causing the ~LVPS_OK signal to go high, assuming a pull-up resistor after connector P2:A7 at the Facilities CCA.

The ~TEST signal from connector P2:B8, when active low, is guaranteed to light the CR12 PWR_OK LED through diode CR14. Zener diodes CR15 and CR16 provide over-voltage protection to both the ~TEST and ~LVPS_OK signals.

2.3.2.17 Monitor CCA (1A3A3, 1A3A9) Theory

The Monitor CCA amplifies the RF input from the field monitor antenna, band pass filters and analyzes the signals from the field monitor antennas. The parametric data is displayed on the PMDT and the Monitor CCA initiates an alarm status indication to the LCU if the DVOR fails to operate within specified limits.

2.3.2.17.1 Monitor CCA Block Diagram Theory

Refer to [Figure 2-20](#). The monitor CCA is a circuit card assembly designed to monitor and analyze the radiated signal from the DVOR. The monitor checks the monitored signal against the high and low limits and generates the alarm status signals to the LCU if the DVOR fails to operate within specified limits. The Monitor CCA is inserted into the rack which provides the RF connection to the monitor antenna, power input, alarm signals to the LCU and serial communication to the RMS processor.

The DVOR monitors are designed for dual operation in either AND or OR configuration with both monitors checking the signal from the field monitor antenna. The DVOR field monitor is normally connected with one antenna connected to an RF signal splitter that feeds the two Monitors. Operation with two monitor antennas connected to each monitor can be provided as an option.

Refer to [Figure 2-21](#). The antenna is connected to the backplane connector of the Monitor on the DIN female J2 connector. The input is 50 ohms and will accept an input of +10 dBm to -50 dBm.

The signal is routed into the receiver section of the monitor CCA. The signal passes through a selectable 16 dB attenuator on the monitor board. At high signal levels the 16 dB attenuator is switched into the circuit otherwise it is switched out. The user enables this attenuation using the PMDT configuration settings.

The signal then passes through a pre-selector band pass filter that rejects high input level radar and communication band signals. The signal then is amplified by a fixed gain amplifier. The signal then enters mixer MX1 and is mixed by the output of the frequency synthesizer described later. The output is at 45 MHz and is the intermediate frequency signal (IF).

The 45 MHz IF signal then enters the crystal filter which provides a 3 dB bandwidth of 30 kHz. The rejection of the adjacent channel 50 kHz away is greater than 50 dB. The signal then enters a digitally controlled step attenuator that is operator set during installation from the PMDT.

The signal then enters a second mixer that results in a 125 kHz second IF signal. This signal is then sampled by an analog to digital converter. There are two DSP processors the master and the slave. The slave DSP filters the signal and provides a base band audio signal in digital format to the master DSP processor. The Master DSP then digitally processes the signal to generate the individual parameters of the VOR signal.

The Monitor CCA performs supervision of critical VOR system parameters and also performs self-monitoring. The VOR Monitor Certification checks are performed continuously in the background. The current status of the background test may be checked by selecting Monitor 1 (or 2) >> Test Results >> In Process.

The RMS performs the following tests for each parameter using the test generator. Failure of the test three times will cause the RMS to disable the monitor.

1. The parameter is 10% below the lower alarm limit. The monitor must return an alarm indication for this parameter.
2. The parameter is set 10% above the lower alarm limit. The monitor must return a normal indication.
3. The parameter is 10% below the upper alarm limit. The monitor must return a normal indication for this parameter.
4. The parameter is set 10% above the upper alarm limit. The monitor must return an alarm indication.

The Monitor CCA receives battery-backed DC power from the Low Voltage power supply (LVPS) at connector P2. Regulated +5V, +12V and -12V supplies are provided from the LVPS for use by the Monitor CCA to power the microcontroller and all of its associated circuitry. Linear voltage regulators generate -5 VDC and +3.3 VDC for use on the circuit card.

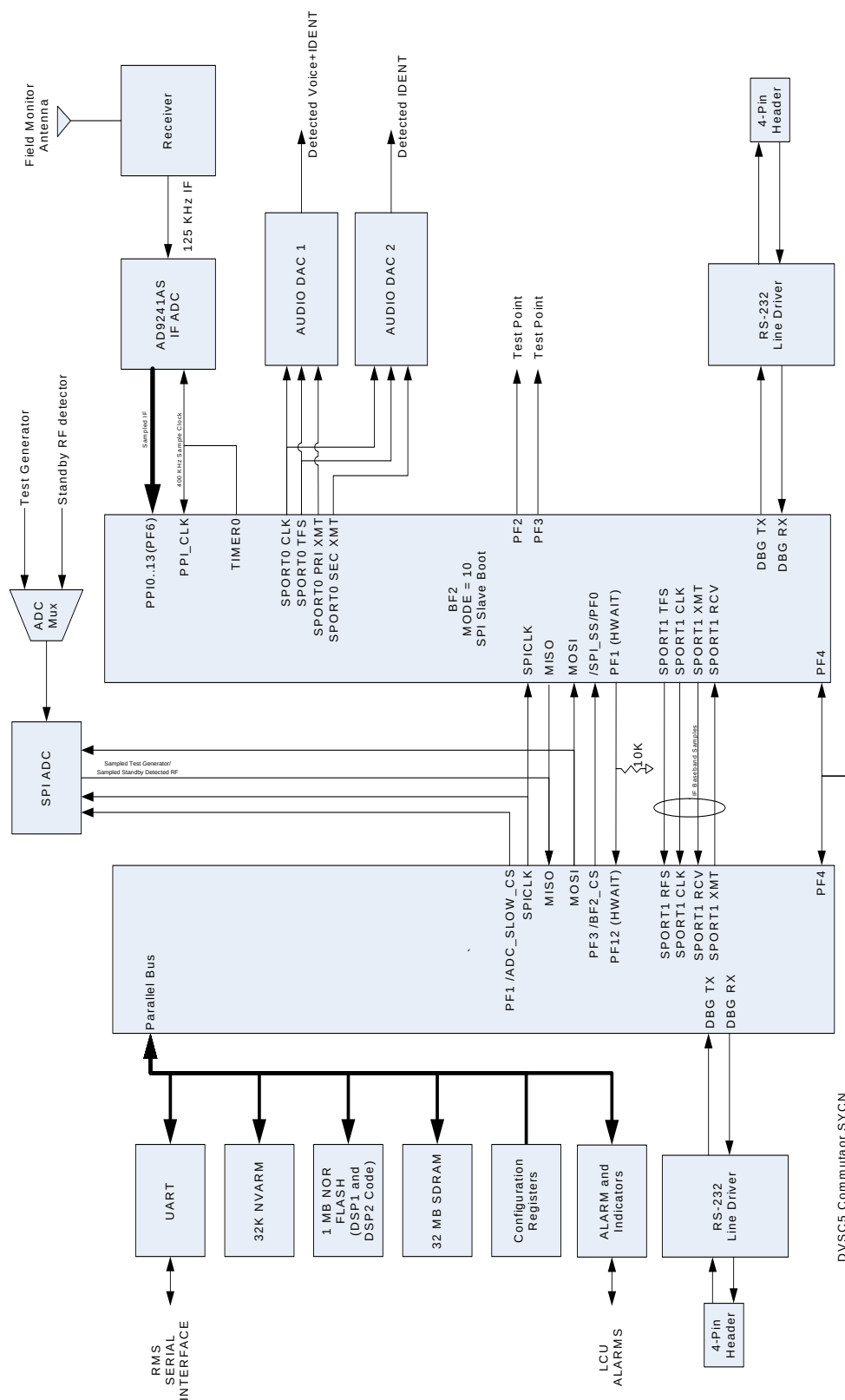


Figure 2-20 Monitor CCA, Block Diagram

2.3.2.17.2 Monitor CCA Detailed Circuit Theory

The microcontroller used on the Monitor CCA is in a product category called digital signal processor (DSP) that utilizes external flash ROM, non-volatile RAM (NVRAM), synchronous dynamic RAM (SDRAM), a voltage supervisor/watchdog reset circuit, and an oscillator to form the core microcomputer. The DSP also includes a direct memory access (DMA) controller, serial ports, and general purpose input/output (I/O). Microcomputer peripherals include a real-time clock (RTC), universal asynchronous receiver/transmitters (UARTs), a parallel port interface (PPI), bus buffers, and more general purpose I/O.

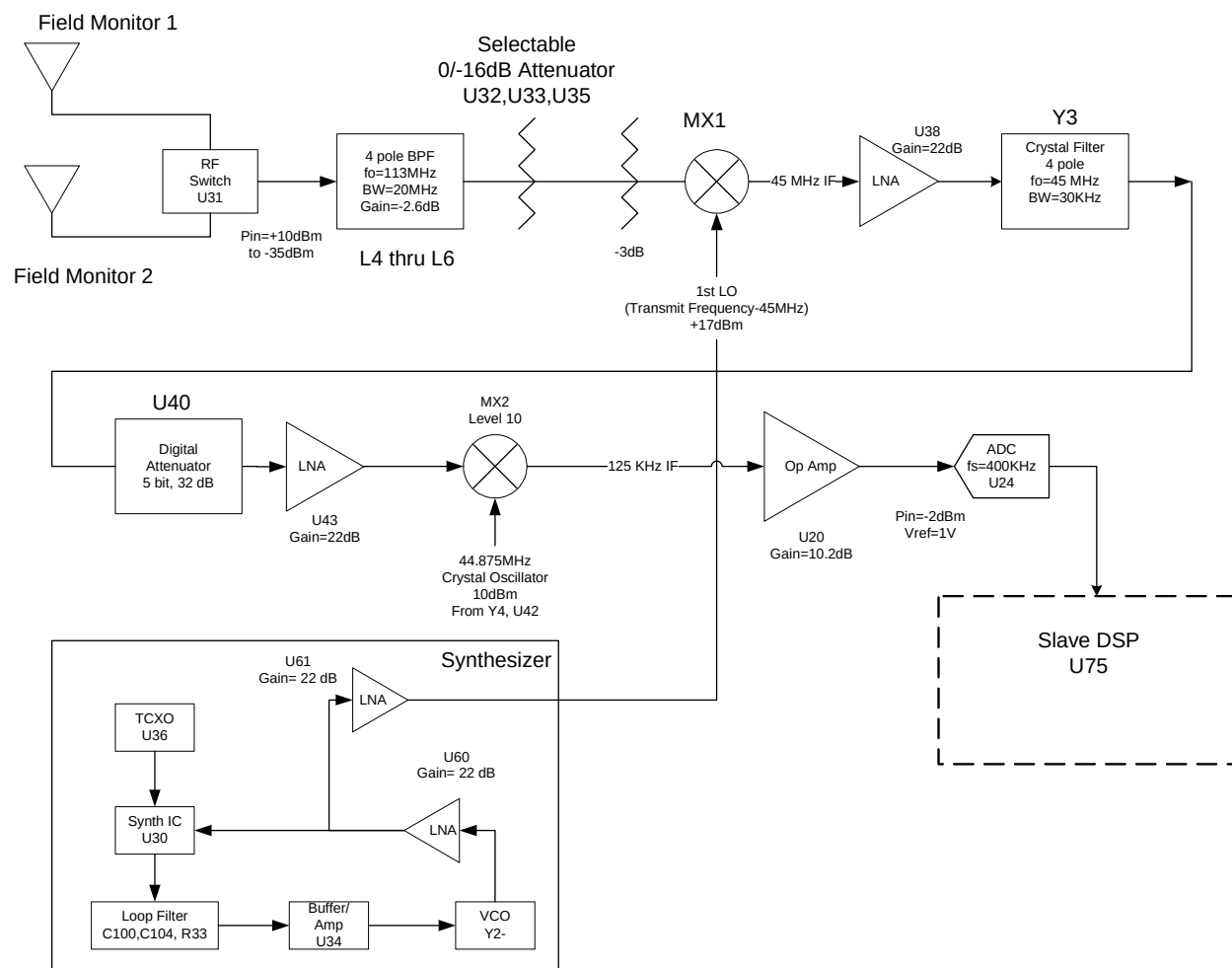


Figure 2-21 Monitor Receiver, Block Diagram

The U6 DSP is one of two DSPs on the Monitor CCA. The U6 DSP utilizes external flash ROMs (U1 and U2) that contain the operating instructions for the DSP. The U6 DSP utilizes NVRAM (U3) that retains settings even without power applied to the Monitor CCA. The U6 DSP also uses SDRAM (U5) for temporary storage and execution RAM. The U6 DSP program instructions are loaded from the flash memory U1 and U2 at power up and then run out of internal RAM within the U6 DSP or in the slower SDRAM (U5). The U6 DSP includes internal, direct memory access (DMA) controller, serial ports, and general purpose input/output (I/O).

The U6 DSP's flash ROM is factory programmed using the J1 SPI boot header while factory debug is accomplished using the J8 emulator header, and the J9 debug header. These connectors and headers are not be used after factory testing is completed.

Buffer circuits U8, U9, U11, U12, and U13 are used to buffer the U6 address and data lines for use within the Monitor circuit card.

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The U6 DSP communicates serially through one internal and two external UARTs (both in U25). The buffer circuit U28 converts the TTL levels to and from RS232 levels (+8 to – 8 Volts Dc) using an internal power supply circuit. The internal UART of U6 is connected to the factory debug port at J9. The other two UARTs control communications to the RMS processor and provide a spare serial port.

The U6 DSP reads the operating frequency setting from the DIP switches on the backplane through the U47 buffer circuit. When selected the A0 through A7 inputs from the backplane switch are presented to the bus. This information is used to set the frequency of the Monitor synthesizer to a frequency that is 45 MHz less than the VOR transmit frequency.

The U6 DSP reads the station configuration setting from the DIP switches on the backplane through the U46 buffer circuit. When selected the A0 through A7 inputs from the backplane switch are presented to the bus. This information is used to determine when the system is a DVOR or CVOR, single transmitter or dual and whether adjustments can be made remotely or only locally. The ~LOCAL signal comes from the LCU and determines if the VOR is being adjusted by a local operator.

The voltage supervisor / watchdog (U45) resets all the digital circuitry when the +3.3V power supply is too low, when the LCU asserts the ~MRESET line, or when the U6 DSP does not refresh the watchdog timer.

The U6 DSP coordinates all subsystems to measure the parameters, sends the measurements to the RMS using RS232 communications, and notifies the LCU (using latch U50) when a critical parameter is out of range using the primary and secondary alarms. Front panel LEDs are controlled by the outputs of latch U52.

After a system reset, the alarm latch outputs (U50 and U52) are in the active state until updated by the DSP. The alarms are updated only when the DSP refreshes the voltage supervisor / watchdog. If there is a DSP failure, the alarms will remain in the last output state until watchdog time-out and the voltage supervisor / watchdog reset activates the alarms. During normal operation, the alarm outputs are read by the DSP using an input buffer (U53) to verify that outputs are not shorted or the latch has failed. The LEDs (CR12, CR14, CR16, CR18, and CR20) are used to signal the alarms and pre-alarms conditions on the front panel. The CPU_OK LED (CR22) is used to indicate that the U6 DSP is operating correctly. The external ~TEST signal coming from the LCU can light all LEDs to verify they have not failed.

The U36 10MHz temperature-controlled crystal oscillator (TCXO) provides an accurate and reliable source of timing for the digital circuitry sections.

Two BNC connectors are on the front panel. The SYNC signal is the trigger for an oscilloscope and the TEST signal is the source signal for the oscilloscope. The PMDT can select which Test signal to display and the Master DSP triggers the oscilloscope when the selected type is been sent

The Monitor provides the ability to measure the operating frequency of Transmitter 1 and Transmitter 2 carrier, upper sideband and lower sideband. The signal “TMR1” is an input to the U6 DSP that has the ability to precisely measure the frequency of the incoming signal. Circuits U19, U21, U63, U64 and U65 are programmable gates used as multiplexers in this application. When control signal “SEL_FREQ_TX is low then the output of gate U21 is selected which originates from transmitter 1. When control signal “SEL_FREQ_TX is high then the output of gate U63 is selected which originates from transmitter 2. When control signal “SEL_FREQ_DIV1 is low then the output of gates U19 and U64 are selected which originates from either the USB or LSB. When control signal “SEL_FREQ_TX is high then the input 1_DIV_F0 of gate U21 and 2_DIV_F0 of gate U63 is selected which originates from the carrier frequency source. When control signal “SEL_FREQ_DIV0, is low then the output of gate U19 is the LSB (1_DIV_LSB) and the output of U64 is the LSB (2_DIV_LSB). When control signal “SEL_FREQ_DIV0, is high then the output of gate U19 is the USB (1_DIV_USB) and the output of U64 is the USB (2_DIV_USB).

The U75 DSP is used to provide high speed data collection and processing of the VOR signals. U6 is considered the “master” and U75 is the “slave”. The U75 DSP does not utilize external flash ROM, NVRAM or SDRAM. The U75 DSP includes an internal direct memory access (DMA) controller, serial ports, and general purpose input/output (I/O). The instruction set for the U75 DSP is downloaded by the U6 DSP at startup. The U75 DSP operates using only internal RAM. Communication between U6 and U75 is accomplished using the PPI (parallel) communication method.

The internal UART of U75 is the debug port at J11. The debug RS232 ports are used only for factory purposes and will not be used by the customer in the field.

Device U59 is a linear regulator that converts the 5 volts DC to 3.3 VDC to run the digital circuitry on the circuit card. Device U37 converts the 12 VDC to 5 VDC to run the PLL and VCO buffer circuits. Device Q10 is a linear regulator that converts the +12 VDC to +10 VDC for the VCO circuit.

Receiver Operation

Refer to [Figure 11-14](#). The input signal enters from one of two antenna inputs P2:D or P2:E. Inductors L2 and L3 remove any DC charge on the antenna lines. Protection devices SG1 and SG2 remove transients from the input line from lightning or ESD. Circuit U31 is used to select one of the two antenna inputs with U6 as the control. The signal then passes through a pre-selector band pass filter. The signal is then routed through a selectable 16 dB attenuator formed by R28, R30 and R32. At high signal levels the 16 dB attenuator is switched into the circuit otherwise it is switched out. The user enables this attenuation using the PMDT configuration setting.

The signal then enters a 3 dB attenuator formed by R48, R49 and R51 and then into mixer MX1 and is mixed by the output of the frequency synthesizer described later. The output is at 45 MHz and is the intermediate frequency signal (IF). The signal is then amplified by fixed gain amplifier U38 with a nominal gain of 20 dB.

The 45 MHz IF signal then enters the crystal filter Y3 which provides a 3 dB bandwidth of 30 kHz. The rejection of the adjacent channel 50 kHz away is greater than 50 dB. The signal is then amplified by fixed gain amplifier U68 with a nominal gain of 20 dB. The signal then enters the digitally controlled step attenuator U40. The settings of the PMDT configuration control the attenuation setting.

Resistor R62 and zener diode CR6 create a -3.3 Vdc source for circuit U40. Circuit U22 switches the -3.3 Vdc source to U40 only after the +5 Vdc source has stabilized.

The signal then is amplified by fixed gain (+20 dB) amplifier U43. The signal then enters mixer MX2 and is mixed with fixed frequency of 44.875 MHz from oscillator Y4. The output of the mixer is 125 kHz enters the differential amplifier U20. The output of U20 enters analog to digital converter U24. The A/D converter U24 continuously samples the input signal and presents the result on the data bus to the DSP U75.

The composite detector is formed by sampling the 45 MHz IF through L37 and C191. Circuit U44 is a linear detector which provides a representation of the modulation to the test point TP16 through U62A and an input to U6 DSP through U62B.

The Synthesizer controller U30 is a single chip that provides reference divider, VCO output divider, phase comparator and charge pump. This chip is programmable from the U6 DSP to set the channel frequency. The output is programmed 45 MHz lower than the station frequency to be monitored. Operational amplifier U34 is part of the loop filter for the VCO control loop. Voltage controlled oscillator Y2 provides an output frequency from 63 MHz to 73 MHz to a 26 dB attenuator. The signal is then amplified by fixed gain amplifier U60 with a nominal gain of 20 dB.

The signal is then split two directions by a 6 dB resistor splitter. One signal, enters a 4 dB attenuator and then is fed back to the PLL circuit U30. The second signal enters fixed gain (20 dB) amplifier U61. This signal is available at TP4 and Mixer MX1.

Model 1150A DVOR

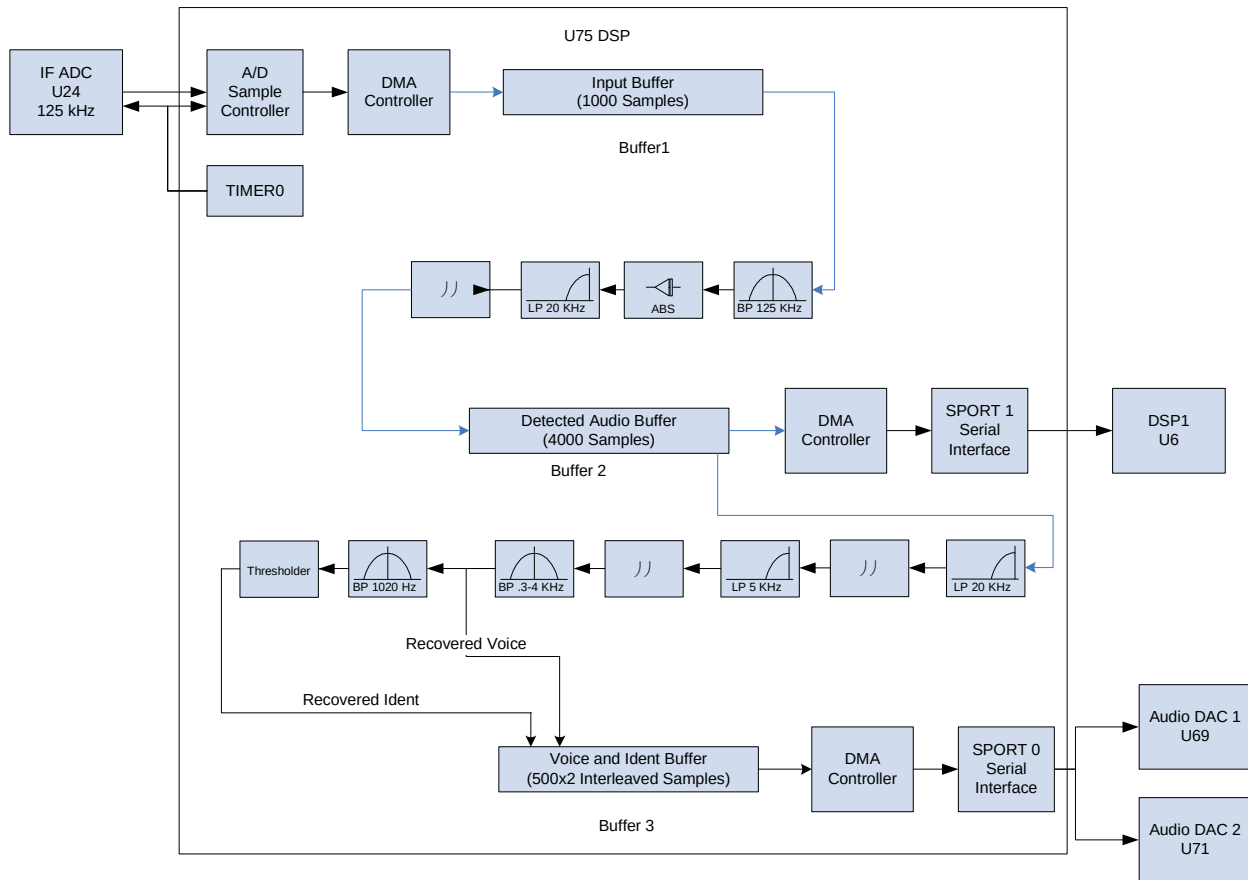


Figure 2-22 Monitor DSP (U75) Signal Processing Diagram

VOR Signal Demodulation

Refer to [Figure 2-22](#). The DSP U75 samples the 125 KHz IF signal using analog to digital converter U24. The DMA controller within U75 synchronizes the sampling of data. The data is stored in internal buffer 1. The data then is bandpass filtered with center frequency of 125 kHz. The data runs through an absolute value calculation which rectifies the signal. The signal is then low pass filtered with a cut off frequency of 20 kHz. The signal is then down sampled by a factor of 5. This signal enters the intermediate buffer 2. This buffer 2 data is serially transferred to DSP U6 for extraction of the VOR azimuth, 9960 Hz modulation, 30 Hz modulation and deviation ratio. The contents of buffer 2 are also sent through a 20 kHz low pass filter. The signal is then down sampled by 2. The signal is then low pass filtered with a cut off frequency of 5 kHz. The signal is then down sampled by 4 and enters a band pass filter with a pass band of 300 to 4000 Hz which contains both voice and identification signals. The voice then enters the buffer 3 Voice and Ident buffer. The voice also enters a bandpass filter centered at 1020 Hz to pass only the ident.

Half of buffer 3 contents are transferred to Audio digital to analog converter U69 for the recovered voice and then through the U16 Audio Amplifier and off the Monitor and eventually the headphone jack on the Test Generator. The other half of buffer 3 contents are transferred to Audio digital to analog converter U69 for the recovered voice and then through U71 then unity gain buffer U72a. This signal leaves the Monitor and then goes to the Facilities CCA for possible connection to the speaker so that the technician can listen to the identification if selected through the PMDT.

Refer to [Figure 2-23](#). The DSP U6 samples three different VOR detected signals. One is the output of the receiver section for mU75. The second is the Test Generator signal. The third is the detected standby transmitter signal from the RF Monitor. One signal at a time is sent to the VOR signal processing routines.

The signal is first changed by removing the DC bias and which provides an RF level value in dB from the nominal set point. The signal is then sent through three separate paths, 30 Hz am recovery, identification recovery, and 9960 Hz recovery.

The 30 Hz am recovery path has a 30 Hz low pass filter. The signal is decimated to 1 KHz then enters a 30 Hz band pass filter. The output is the 30 Hz mod% and the 30 Hz used for the internal audio frequency counter.

The identification recovery path has a 1020 Hz band pass filter. The signal is decimated to 10 KHz then enters a second 1020 Hz band pass filter. The output enters the 1020 Hz mod% detector. The signal is then analyzed for continuous, missing or incorrect identification codes.

The 9960 Hz recovery path has 9960 Hz band pass filter which feeds the modulation detector, the audio frequency counter and the FM deviation detector. The FM detector uses two quadrature mixers mixed with an internally generated 10 kHz signal. The phase angle is computed and sent through a differentiator. This signal is band pass filtered at 30 Hz. The signal is decimated down to 1 kHz and enters a second 30 Hz band pass filter. This output feeds the audio frequency counter and the fm deviation detector.

The azimuth detector takes the 30 Hz am and 30 Hz fm signals and uses a quadrature mixer mixed at 30 Hz to determine the phase of the am and fm signals. The phase angles are subtracted to provide the resulting Azimuth angle.

The DSP U6 then compares the values obtained with the alarm limits. When an alarm condition occurs the front panel LEDs are lit and alarm delay timer is activated. If the alarm continues and the alarm delay timer ends then the alarm outputs to the LCU are activated. The LCU then within 0.5 seconds takes the action of transfer and or shutdown.

Model 1150A DVOR

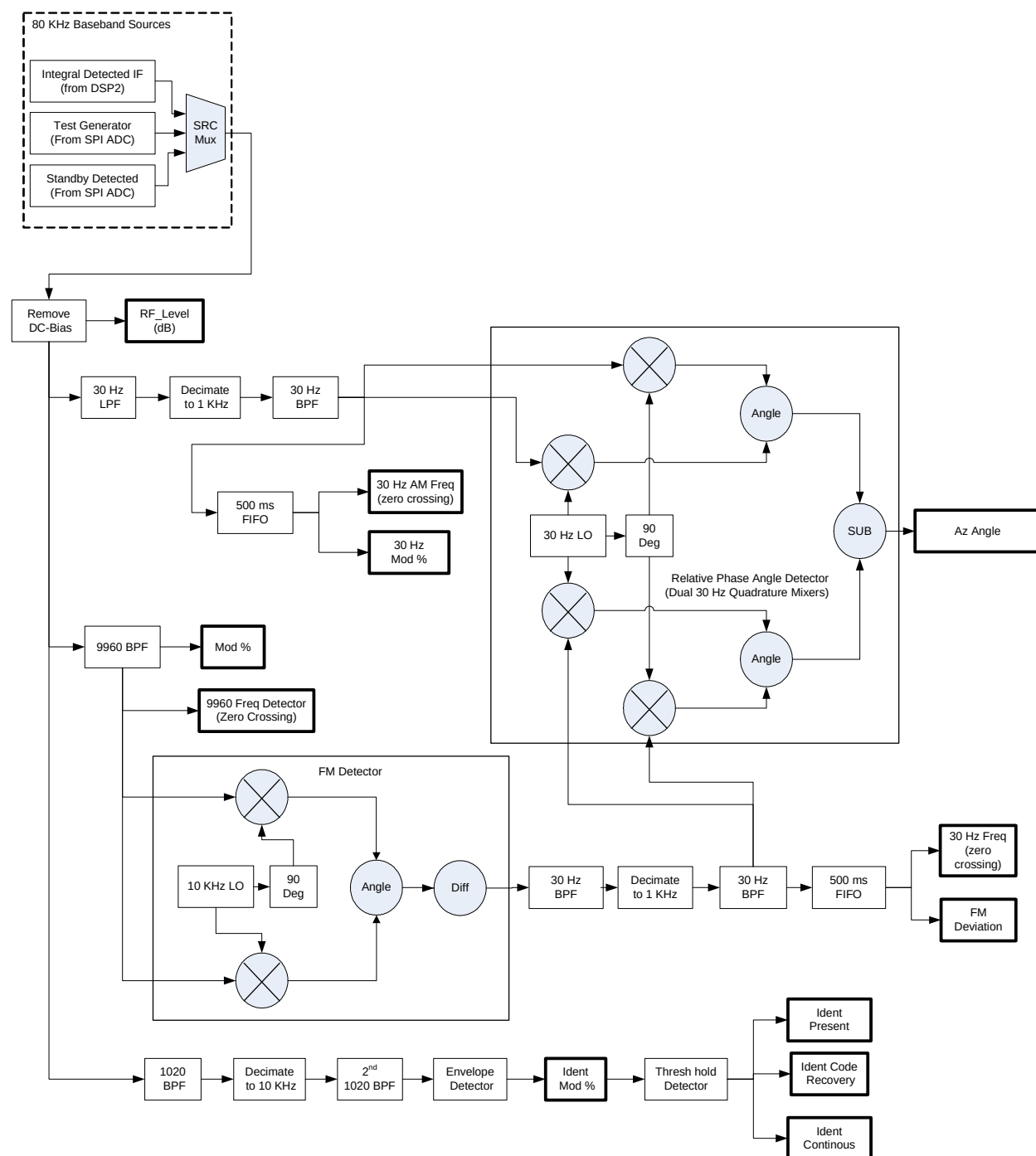


Figure 2-23 Monitor DSP (U6) Signal Processing Diagram

2.3.2.18 Power Panel Theory

Refer to [Figure 1-3](#). The power panel, located on the lower front portion of the electronics cabinet, contains the AC input the Battery input and DC Buss circuit breakers for Transmitters 1 and 2. AC input power for the Transmitters enters the cabinet via the AC Monitor (REF DES 1A6) terminal block 1A9TB3 terminals 1, 2 and 3. AC input power for the Outlet and obstruction lights enters the cabinet via the AC Monitor (REF DES 1A9) terminal block 1A9TB2 terminals 1, 2 and 3. Positive DC input power wires from the optional battery backup (unit 3) enter the cabinet via J1 (blue connector) on the back of the power panel assembly. The negative DC input power wires connect directly to the ground bus bar. Circuit breakers 1CB1 and 1CB4 control the application of AC voltage to Transmitters 1 and Transmitter 2 BCPS systems. Circuit breakers 1CB2 and 1CB5 control the application of battery power to Transmitters 1 and Transmitter 2 BCPS systems respectively. Circuit breakers 1CB3 and 1CB6 control the application of power from the BCPSs to Transmitters 1 and Transmitter 2 racks 1A3, 1A4 and 1A5.

2.3.2.19 Battery Charger Power Supply (BCPS) Theory

The BCPS assemblies provide regulated voltage to the transmitter from either the AC input or the batteries. The BCPS assemblies are located in the third rack. The AC voltage is an input to the BCPS which converts to approximately 50 Volts DC. The BCPS assemblies are also responsible for charging the batteries when AC is present.

2.3.2.19.1 BCPS CCA Block Diagram Theory

Refer to [Figure 2-23](#). The Fanless BCPS CCA provides battery-backed DC power to all associated TX1 or TX2 modules in the cabinet as well as monitor and charge its associated battery stack. The Fanless BCPS CCA connects to the Carrier Backplane CCA through compact PCI (cPCI) connector P1.

100-260VACrms, 47-63Hz power enters through the cPCI connector P1, is fused and RFI filtered before being converted to approximately +51Vdc by brick PS3, then is routed to bridge diode CR1. Bridge diode CR1 OR's this DC output with that of the other BCPS in the cabinet (if optionally wired on the Carrier Backplane) for redundant operation.

The DC output of bridge diode CR1 is measured by op-amp U1 across current-sense resistor R2 and reported to microcontroller U8 through analog multiplexer U11. This DC output (+48BUSS) routes several places.

+48BUSS powers DC-DC converters U15 and PS2 through fuse F1. These DC-DC converters create +5Vdc, +12Vdc, and -12Vdc for powering on-board circuitry.

+48BUSS powers DC-DC converter PS1 through fuse F2 to create +54.2Vdc for charging of the batteries. DC-DC converter PS1 can have its input power switched by transistor Q11 and its output power switched by transistor Q5; both under the control of microcontroller U8. Battery charging is stopped for short times periodically to switch on load transistor Q4 (with load resistors R6, R7, R9, and R10) to test whether batteries are connected or have become too weak.

Battery charging or discharging current is measured by op-amps U4 and U5 across current-sensing resistor R14 and reported to microcontroller U8 through analog multiplexer U11.

Comparator U19 monitors the diode OR'd +51V supplies (scaled by RN1 and named 48VPS_MON) and switches on transistors Q1 and Q2 through isolator U2 when battery back-up is needed (48VPS_MON too low). Comparator U19 will shut off battery back-up if 48VPS_MON is restored or microcontroller U8 will shut off battery back-up by turning on transistor Q3 (which turns off U19, U2, Q1, and Q2) if the battery voltage (scaled by RN3 and named BATT_VOLT) becomes too low; preventing total discharge of and possible harm to the battery.

Charger reset switch S1 provides a means of powering up the board (and the cabinet if the front panel circuit breaker is closed) with no AC power available. Pressing switch S1 turns on transistor Q7 and battery power conducts through current-limiting resistor R91 to +48BUSS.

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System AC voltage and current as well as obstruction light (oblite) AC voltage and current are sensed and scaled on the AC Monitor CCA before arriving at the BCPS CCA. Op-amps U10A and U10D, with potentiometers R29 and R30, calibrate the system and oblite VAC signals. Op-amp U14, with potentiometers R44 and R56, calibrate the system and oblite IAC signals. The calibrated signals pass to analog multiplexer U11 before analog-to-digital conversion by microcontroller U8.

Status of the BCPS is displayed on LEDs CR7 and CR48 through CR54, all of which can be lighted by pressing lamp test on the LCU CCA. The microcontroller U8 reports status digitally to the RMS CCA via RS232 signals through the TTL-RS232 converter U9. The microcontroller U8 may be reset at any time by pressing Reset on the LCU CCA.

After reset, microcontroller U8 uses the BCPS strapping of connector P1-31 (grounded or open on the corresponding Carrier Backplane position) in conjunction with the Synch In and Synch Out signals (P1-29 and P1-30) to determine whether it is BCPS1 or BCPS2 and if another BCPS is active in the cabinet. Microcontroller U8 also reads revision strap inputs U8-9, U8-23, and U8-33 after reset to determine hardware configuration.

Front panel circuit breaker CB1 may be used to disconnect +48 BUSS power from the Carrier Backplane so that other modules in the cabinet on the same transmitter side may be serviced.

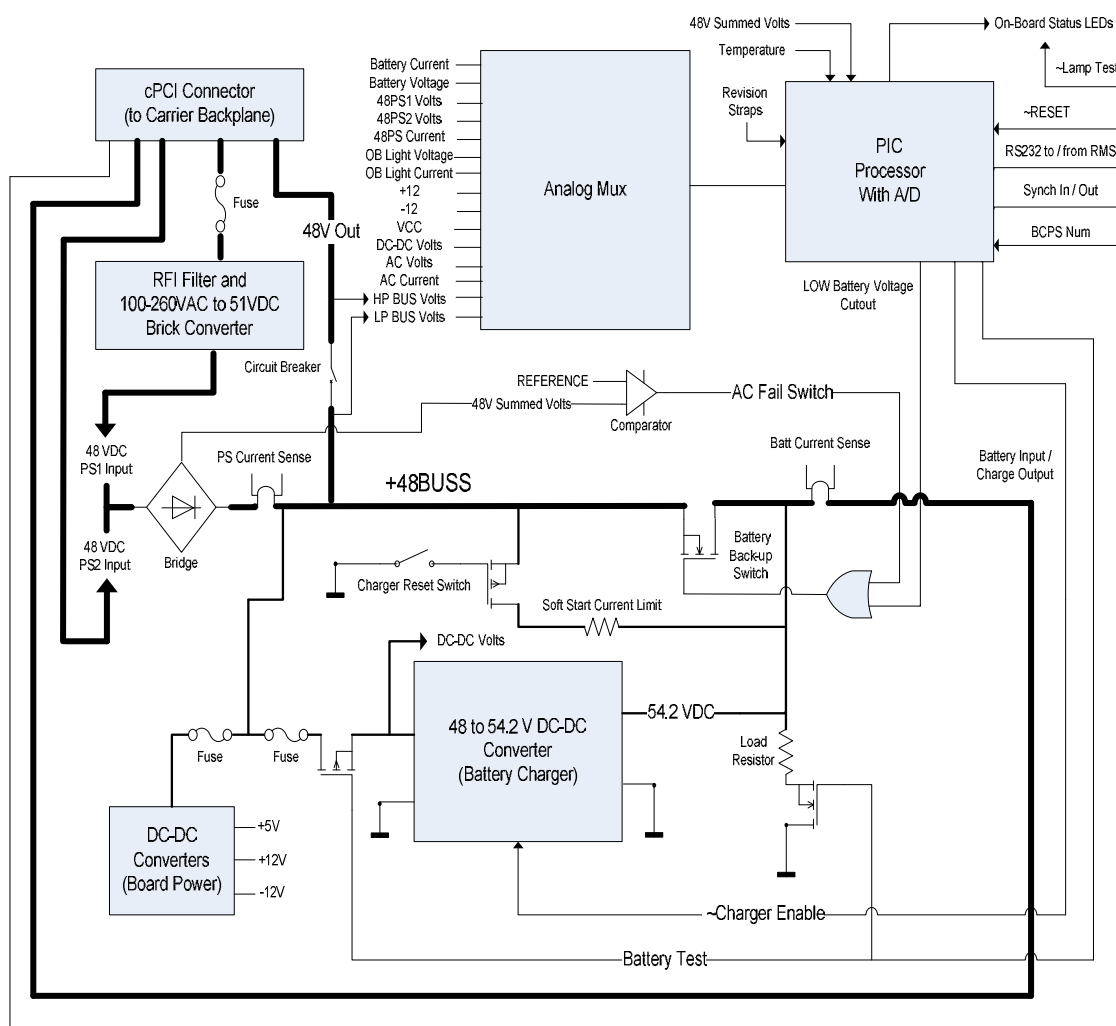


Figure 2-24 Fanless BCPS CCA Block Diagram

2.3.2.20 Battery Charger Detailed Circuit Theory

Refer to [Figure 11-20](#). The Fanless BCPS CCA provides over 700 watts of DC power which may include up to 250 watts of battery charging power. The Fanless BCPS CCA connects to the Carrier Backplane CCA through 47-pin right angle cPCI connector P1.

AC input power (line, neutral, and earth) enters through the cPCI connector P1 and fuse F3 to terminal block TB1. Terminal block TB1 wires through RFI filter FL2 to terminal block TB2 and then to converter brick PS3. Converter brick PS3 uses capacitors C57, C58, C61, C64, and C65 to create an internal +385Vdc which is stepped-down to approximately +51Vdc on the output of converter brick PS3 (48VPS1). Resistor RT1 provides a slow start-up of 48VPS1 upon power-up to prevent nuisance openings of fuse F3.

Capacitors C8, C54, C55, C59, and C56 filter the 48VPS1 output of converter brick PS3 before routing to bridge diodes CR1 and CR45. If another BCPS is present and wired appropriately on the Carrier Backplane, its output (48VPS2) enters via cPCI connector P1-1 to bridge diodes CR1 and CR47.

The OR'd output of bridge diode CR1 is measured by op-amp U1 across current-sense resistor R2. The output of op-amp U1-5 is filtered by resistor R4 and capacitor C49 before routing to multiplexer U11-24. The OR'd output after current-sense resistor R2 is called +48BUSS and routes to several places.

+48BUSS is fused by F1 before powering DC-DC converter U15-1. Capacitors C27 and C28 provide bulk filtering while zener diodes CR37 and CR39, resistors R47 and R68, capacitor C26, and SCR Q6 provide over-voltage protection. Inductor L1 and diode CR36 provide feedback to U15-4 to create the +5Vdc (VCC) output which powers the input of DC-DC converter PS2-3 (as well as many other on-board integrated circuits).

DC-DC converter PS2 creates both +15Vdc and -15Vdc. Resistors R69, R77, R78, and R79 establish a constant load to keep the outputs of PS3 within regulation. The -15Vdc output of PS2-1 is filtered by capacitors C34 and C36 and inductor L2 before linear regulator U16 steps it down to -12Vdc (-12ANA). The +15Vdc output of PS2-8 is filtered by capacitors C35 and C37 and inductor L3 before linear regulator U17 steps it down to +12Vdc (+12ANA). The -12ANA and +12ANA outputs power many other on-board integrated circuits with the +12ANA also powering the reference U18-2. The reference U18-6 output (+5VREF) sets the range of the microcontroller U8-6 internal A-D converter as well as the battery switch voltage level on resistor network RN2-16 and comparator U19-3.

+48BUSS is also fused by F2 before powering DC-DC converter PS1 (if transistor Q11 is on). Microcontroller U8-33 turns on transistor Q11 by turning on transistor Q12. Microcontroller U8 can verify the input power status of DC-DC converter PS1 by reading PS1-4 (DC-DC_VIN) after it's scaled by resistors R101 and R104 on multiplexer U11-4 as DC-DC_SCALED.

The output of DC-DC converter PS1-9 may be turned on by microcontroller U8-26 through transistor Q5; which connects to DC-DC converter PS1-5 (~CHG_ENABLE). When ~CHG_ENABLE is low the output of DC-DC converter PS1-9 is enabled. Resistors R82 and R97 trim the output of DC-DC converter PS1-9 to approximately +54.2Vdc; the desired battery charge level.

Battery charging is stopped for short times periodically to test whether batteries are connected or have become too weakened. Microcontroller U8 takes ~CHG_ENABLE high to shut off the output of DC-DC converter PS1-9 then turns on transistor Q4 (~BATT_DISCHARGE) which places resistors R6, R7, R9, and R10 as a load on the battery. If the battery is not healthy, this load will lower the scaled battery voltage of resistor network RN3 and microcontroller U8 will read it at multiplexer U11-25 (BATT_VOLT). Microcontroller U8-32 will then light the BATT_FAULT LED CR51 through buffer U7.

Battery charging and discharging current is measured by op-amps U4 and U5 across current-sense resistor R14. Op-amp U4-5 reports charging current after filtering by resistor R85 and capacitor C51 as BATT_CURR_CHG at multiplexer U11-26. Op-amp U5-5 reports discharging current after filtering by resistor R86 and capacitor C50 as BATT_CURR_DISCHARGE at multiplexer U11-11.

Model 1150A DVOR

Battery back-up is switched on when the diode OR'd output of diodes CR45 and CR47 (48VPS1 or 48VPS2) is too low; approximately +43Vdc. Comparator U19 monitors this diode OR'd output (scaled by RN1 and renamed 48VPS_MON) at comparator U19-2 and compares it to the scaled +5VREF at U19-3. When 48VPS_MON is too low, comparator U19-7 switches low which turns on isolator U2 and transistors Q1 and Q2; connecting the battery to +48BUSS. Comparator output U19-7 also connects to diode CR11 and resistor R23 so microcontroller U8-7 may read battery switch status as signal ~DC_FAIL.

Battery back-up will remain on until either 48VPS_MON returns or the battery discharges to below approximately +40Vdc. Upon sensing the battery has discharged too much (BATT_VOLT mentioned previously), microcontroller U8-25 turns on transistor Q3 which shuts off comparator U19-7, isolator U2, and transistors Q1 and Q2; disconnecting the battery from +48BUSS. This battery cut-off prevents excessive discharge and possible harm to the battery. The BCPS CCA (and the associated transmitter) will now be completely powered off until either AC power is restored or the charger reset switch S1 is pressed.

Charger reset switch S1 provides a means of powering up the BCPS CCA (and the associated transmitter if the front panel circuit breaker is closed) with no AC power available. Pressing switch S1 discharges capacitor C7 through resistor R15, momentarily turning on transistor Q7. Transistor Q7 momentarily connects the battery through current-limit resistor R91 and diode CR28 to +48BUSS; powering on microcontroller U8. Once microcontroller U8 detects no AC voltage is present, it turns on battery back-up through transistors Q1 and Q2. The BCPS CCA will remain on until either AC power is restored (shutting off battery back-up) or the battery discharges too low (battery cut-off).

System AC voltage and current as well as obstruction light (ob lite) AC voltage and current are sensed and scaled on the AC Monitor CCA before arriving at the BCPS CCA. System AC voltage (SYS_VAC_POS) enters cPCI connector P1-25 and is transient protected by CR23. Current limiter U13, resistor R33 and zener diode CR29 condition the signal to drive the AC_ON LED CR48. Potentiometer R30 scales while resistor R46 and capacitor C21 filter the signal before op-amp U10D buffers it to resistor network RN5-16 and multiplexer U11-19 as SYS_VAC_SCALED.

Obstruction light AC voltage (OB_LITE_VAC_POS) enters cPCI connector P1-23 and is transient protected by CR24. Current limiter U12 and resistor R31 provide a constant load. Potentiometer R29 scales while resistor R34 and capacitor C22 filter the signal before op-amp U10A buffers it to resistor network RN5-12 and multiplexer U11-21 as OB_LITE_VAC_SCALED.

System AC current (SYS_IAC_POS) enters cPCI connector P1-26 and is coupled by capacitor C45, transient protected by CR38, and conditioned by op-amps U14A and U14D. The amplifiers and connected components act as full-wave rectifier and filter averaging circuits. Potentiometer R56 adjusts the final gain to create SYS_IAC which is further scaled by resistor network RN5-14 to create SYS_IAC_SCALED at multiplexer U11-20.

Obstruction light AC current (OB_LITE_IAC_POS) enters cPCI connector P1-24 and is coupled by capacitor C46, transient protected by CR30, and conditioned by op-amps U14B and U14C. The amplifiers and connected components act as full-wave rectifier and filter averaging circuits. Potentiometer R44 adjusts the final gain to create OB_LITE_IAC which is further scaled by resistor network RN5-10 to create OB_LITE_IAC_SCALED at multiplexer U11-22.

Power supplies VCC and +12ANA are scaled by RN4 before routing to multiplexer U11-10 and U11-9. Power supply -12ANA is scaled by RN5 and inverted to a positive voltage by op-amp U10C before connecting to multiplexer U11-8 as -12ANA_SCALED. The -12ANA is inverted because microcontroller U8 can only read voltages in the 0-to+5V range.

Most of the analog signals of the BCPS are connected to the 16-channel analog multiplexer U11. Individual channels are routed to output U11-28 by channel selects U11-17, U11-16, U11-15, and U11-14 which are controlled by microcontroller U8. The multiplexer output signal U11-28 is buffered by op-amp U10B, filtered by resistor R24 and capacitor C13, and clamped by diodes CR9 and CR10 before entering an analog channel of microcontroller U8-3.

Microcontroller U8 contains a multi-channel 10-bit A-D converter. One analog channel of microcontroller U8-8 is used to convert the temperature signal of U21. Temperature circuit U21 is mechanically coupled to the heat-sink with a screw through a mounting hole. Microcontroller U8 reports the temperature along with other data to the RMS CCA via serial communications TX (U8-27) and RX (U8-29). Converter U9 translates these TTL signals to RS232 levels and routes them as BCPS_RX and BCPS_TX to cPCI connector P1-37 and P1-38.

Microcontroller U8 determines its backplane position number (1 or 2) by reading input strap BCPS1 on U8-11 (cPCI connector P1-31). Microcontroller U8 uses SYNC_OUT1_IN2 (P1-28) and SYNC_OUT2_IN1 (P1-29) signals to determine if another BCPS CCA is in the system and if so, synchronize with it. Only one BCPS CCA may transmit at a time to the RMS CCA, thus the converter U9-18 ~shutdown control disables the silent BCPS transmit of U9-15.

Status of the BCPS is displayed on LEDs CR7 and CR48 through CR54. LED CR7 indicates microcontroller U8 is running properly while the other LEDs display power status. All of the LEDs will be lit when the ~TEST signal from cPCI connector P1-34 is active. Diode CR12 protects the BCPS CCA from reverse-powering while resistors R28, R87, and diode CR25 condition the ~LAMPTEST signal to the proper level. When ~LAMPTEST is low, transistor Q10 and buffer U7 are disabled while transistors Q9 and Q8 are enabled; turning on the LEDs through resistors R64, R65, and R66 and diodes CR5, CR15, CR14, CR17, CR18, and CR13.

Microcontroller U8-2 is reset when voltage monitor U6-2 detects a low voltage. A low voltage will occur on voltage monitor U6-2 if either VCC dips through resistor R84 or if the ~MRESET signal from cPCI connector P1-33 is active. Inductor FL1 and capacitor C48 filter ~MRESET while diode CR21 prevents reverse-powering. After ~MRESET is released, microcontroller U8 (clocked by oscillator Y1) will read input straps U8-9, U8-23, and U8-33 to determine its hardware configuration.

Front panel circuit breaker CB1 may be used to disconnect +48BUSS power from the Carrier Backplane. Microcontroller U8 can determine the state of the circuit breaker (open or closed) by reading the scaled signals LP_BUSS_48V (R99 and R102) and HP_BUSS_48V (R100 and R103) on multiplexer U11-6 and U11-5.

ISP connector J2 is used in the factory to program microcontroller U8. Test header J6 is used in the factory for testing. Debug header J3 is used in the factory for software debugging. None of these connectors should be used by the customer.

2.3.2.21 Extender Board Block Diagram Theory

Refer to [Figure 2-25](#). The Extender (Logic) CCA provides the means for a service technician to extend an RMS, Facilities, Monitor, Low Voltage Power Supply, Synthesizer Assembly or Audio Generator CCA outside of the Control Backplane card cage so that measurements can be taken.

The Extender (Logic) CCA extends a 96 pin DIN41612, a 60 pin hybrid DIN41612, and four RF signals through conformable conductors.

The 96 pin (P1 and P3) and 60 pin hybrid (P2 and P4) connectors are bussed straight across the CCA. The RF connectors (P2 and P4: D, E, F, and G) route straight across the CCA via conformable conductors.

Test points TP1 and TP2 allow test equipment connection to circuit ground.

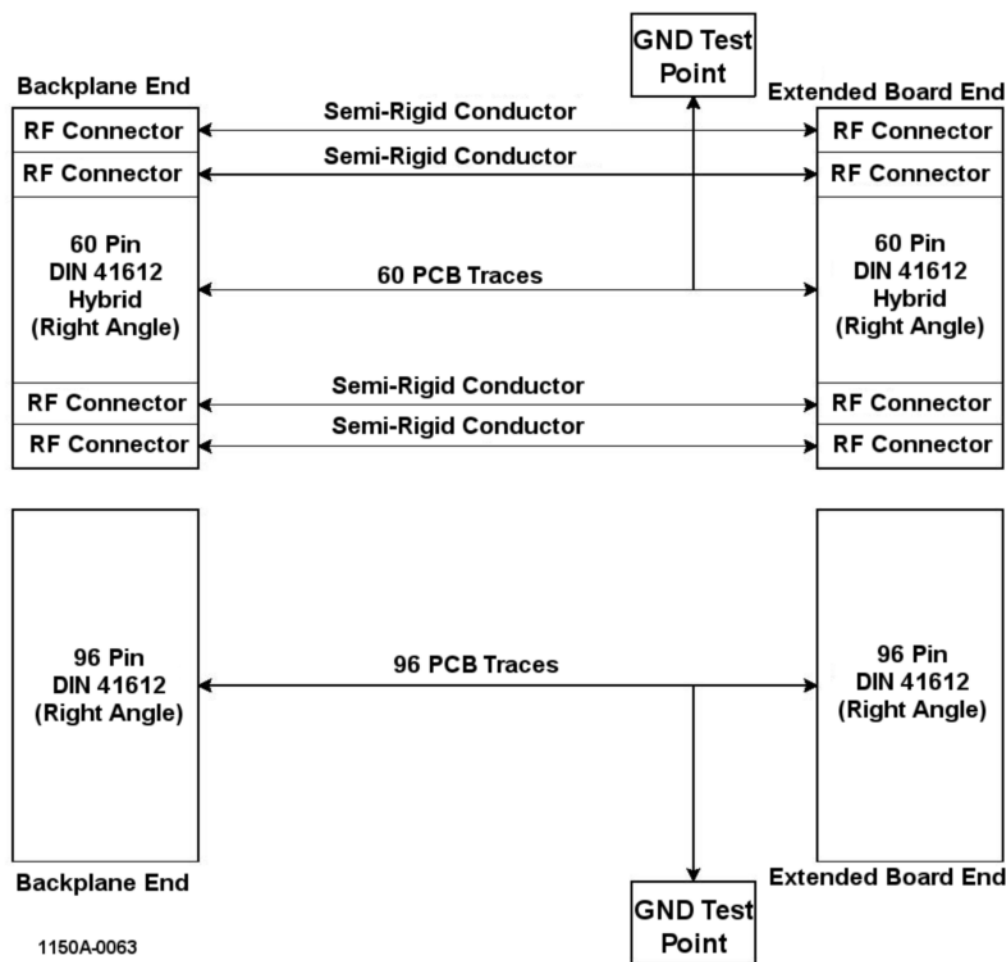


Figure 2-25 Extender Board

2.3.2.22 Commutator Control CCA Theory

The Commutator Control CCA connects to a 25 conductor cable on the Control Backplane CCA. This cable originates from one of the two Audio Generators in the Control rack. The output of the Commutator Control CCA exits onto the backplane and to two 40-pin connectors that connect to ribbon cable from the Commutator CCAs. A 4-pin header on the Commutator Control CCA may be strapped to enable/disable automatic ground-check.

Capability for the ground performance check of the antennas and commutator switching is provided. This check is automatic after it has been started by the technician and therefore is called an Automatic Ground Check system. When started, the Monitor CCA sends a switch position code to the Commutator control CCA via the 25-pin cable originating at the Control rack.

The switch positions start at 0 and increment by one until 15. Each position represents 22.5 degrees of antenna rotation from the nominal position. At each position the Monitor CCA determines the azimuth angle at the Field Monitor antenna location. From this data the errors are measured and a Fourier analysis is performed to generate the display data.

The error as determined during the ground check is analyzed to determine the bias, the duantal error, quadrantal error and octantal error. The bias error is the average error around the station. The duantal error is sinusoidal with a rate of one cycle in the 360 degrees around the station. The quadrantal error is sinusoidal with a rate of four cycles in the 360 degrees around the station. The octantal error is sinusoidal with a rate of four cycles in the 360 degrees around the station.

2.3.2.22.1 Commutator Control CCA Block Diagram Theory

Refer to [Figure 2-26](#). The Commutator Control CCA processes all signal steering for antennas 1 through 48.

Commutator switch control signals from the Audio Generator CCA are applied through connectors P1 and P2 to a differential line receiver circuit on the Commutator Control CCA. The line receiver circuit which consists of line receivers U5A, U5B, U5C, U5D, U6A, and U6B converts the differential signals to TTL signal levels.

From the line receiver circuit the control signals are applied to programmable logic device (PLD) U4. PLD U4 performs decoding and distribution of the antenna and transfer signals.

To simplify discussion, only the odd antenna operation shall be discussed.

The output of PLD U4 is applied to a level converter circuit which consists of U7A, U7B, U7C, and U7D. This circuit converts the antenna select data, which is referenced to TTL levels, to logic levels referenced at -10V to +5 VDC. The output of this circuit is applied to a 4:16 line decoder U12.

PLD U4 also outputs signals to a transfer generation circuit which consists of amplifiers U17A, U17B and transistors Q2, Q3, Q4 and Q1. The outputs of the transfer circuit are the ODD and NOT ODD XFR signals. These are opposite polarity CMOS logic signals that change state every 1/60th of a second.

U12 decodes the antenna select data code to select one of the twelve outputs used in the 48 antenna system. The remaining outputs of U12 are not used. The twelve output lines are normally HIGH (+5 volts). When selected, it is pulled LOW (-10 volts). Each output line is applied to a display driver circuit which consists of drivers U8 through U11, U13 through U16, and U18 through U21. This circuit provides the necessary drive to operate the odd numbered antenna RF signal switching pin diodes (after exiting through connectors P1 and P2) on the upper Commutator CCA. Refer to [Table 2-1](#).

Ground check switch control signals from the Monitor CCA through connectors P1 and P2 are applied to a differential line receiver circuit on the Commutator Control CCA. The line receiver circuit, which consists of line receivers U3A, U3B, U3C and U3D, converts the differential signals to the TTL signal levels.

Automatic ground check may be user enabled to verify operation of the DVOR. The ground check feature is normally disabled. If enabled, the TTL level ground check signals will be added as an offset inside of PLD U4. Refer to [Table 2-2](#).

Memory EEPROM U38 and optional temperature sensor U39 may be accessed by the RMS CCA via SPI I/O port U40. The EEPROM U38 may be used to store system parameters as well as revision / serial number information.

Comparators U43 and U44 monitor the +3.3V, +5V, +12V, and -12V supplies to verify they are within range and light LED CR34 if so. Power status may also be read by the RMS CCA via the SPI I/O port U40.

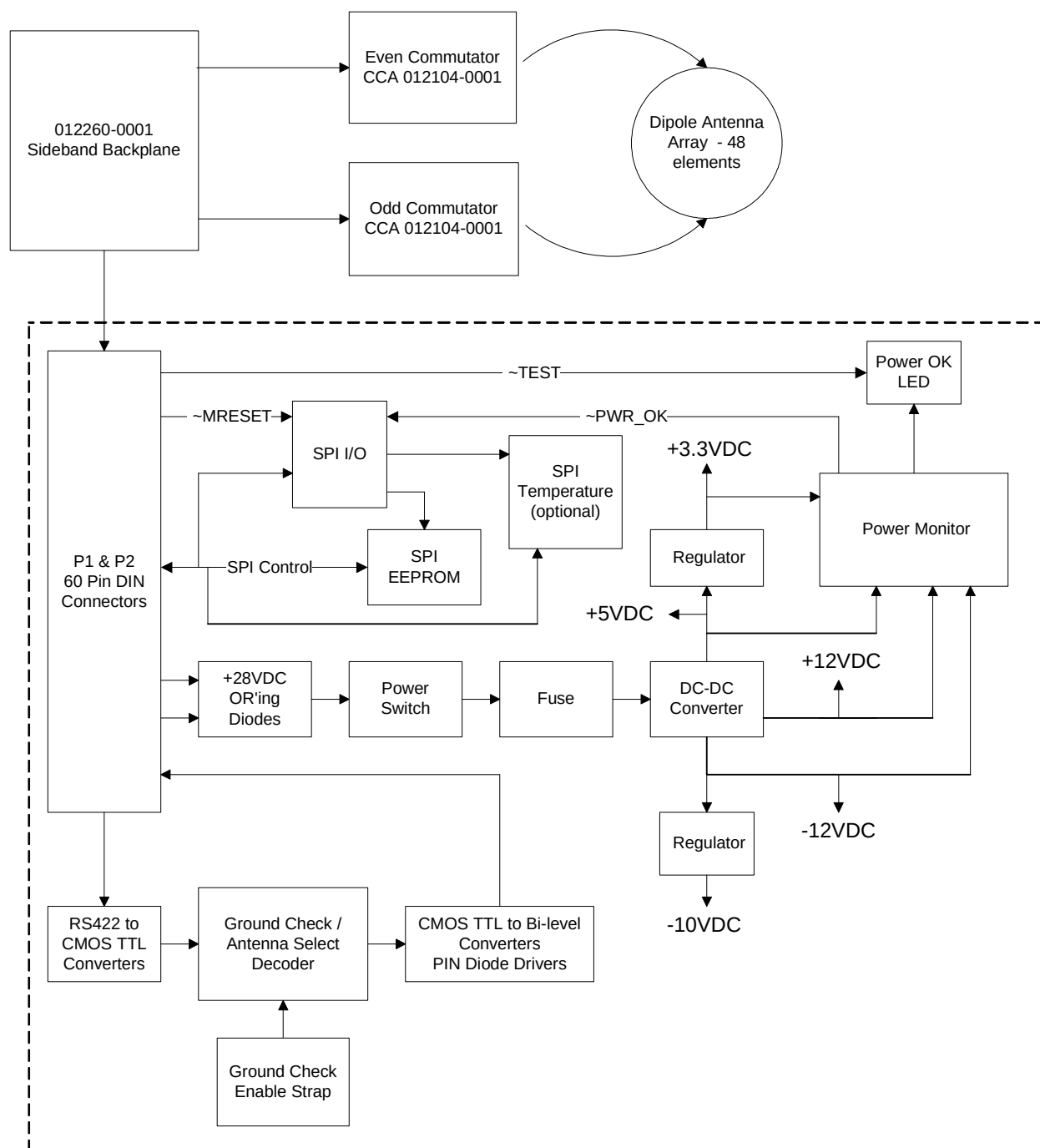


Figure 2-26 Commutator Control CCA, Block Diagram

2.3.2.22.2 Commutator Control CCA Detailed Circuit Theory

Refer to Figure 11-23. Commutator switch control signals from the Audio Generator CCA through connectors P1 and P2 are applied to the inputs of the Commutator Control CCA. These control signals consist of the four balanced antenna select signals, a transfer signal, and a clock signal applied to quad differential line, receivers U5 and U6. Two inputs of U6 are not used and are tied to power or ground.

The antenna switch signals are applied to PLD U4. PLD U4 is programmed to perform all decoding and distribution of the antenna and transfer signals. The clock signal provides a synchronous timing signal for all switching activities.

The ground check switch control lines are translated to TTL levels by differential line receiver U3.

If the automatic ground check feature is enabled at J5, the ground check control lines are added as an offset inside PLD U4. Each increment of the ground check control is added as an offset of 3 to the antenna selected by the DVOR switch control lines.

U4 drives quad converter U7. U7 translates the antenna select data, which is referenced to TTL levels, into CMOS levels (+5V and -10V). The data from U7 is next applied to 4-to-16 line decoder U12.

U4 uses the LOW to HIGH transition of the 720 Hz clock signal to control the timing of the odd antenna switching signals. U4 uses the HIGH to LOW transition of the clock signal to control even antenna switching signals. The time difference is 1/1440th of a second which is the timing difference between a sine and cosine radiated sideband signal.

U12 decodes the antenna select 4-bit data code to select one of the twelve active outputs used in the 48 antenna system. Outputs 13, 14, 15, and 16 are not used. The twelve lines are normally HIGH (+5 volts). When an output line is selected, it is pulled LOW (-10 volts). Each output line feeds the A input of a decoder driver circuit (U6 through U11, U13 through U16 and U18 through U21). The B and C inputs are tied to +5 volts while the D input is tied to -10 volts. The segment driver outputs of each display driver are uniquely paralleled to provide the necessary drive current to operate the RF signal switching pin diodes. Effectively, there are two outputs from each display driver: one is designated the "ON" line, and the other is the "OFF" line. U12 decoder output S0NOT controls display driver U8 which changes the ON and OFF control signals on Commutator antenna control lines OFF 1 and 25, and ON 1 and 25. U12 decoder output S1NOT controls U13 which controls lines OFF 3 and 27, and ON 3 and 27.

OFF 1 and 25 is labeled 1A and ON1 & 25 is labeled 14B on the 012104-0001 Commutator CCA. Also OFF 3 and 27 and ON 3 and 27 are labeled 2A and 15B on the Commutator CCA.

To simplify the discussion of the operation of the decoder driver signals, only the action of U8 will be examined. U8 controls the 1A and 14B ON and OFF lines. If U8 is not selected by U12, then the ON line will have a potential of -10 Vdc and the OFF line will have a potential of +5 Vdc. When U12 selects U8, the ON line switches to +5 Vdc and the OFF line switches to -10 Vdc. This condition exists for the entire time that the selected antenna will radiate, which is 1/720 of a second.

U4 also outputs signals used to generate an ODD_XFR and an ODD XFR NOT signal. PLD U4 outputs a signal to the inverting input of voltage comparator U17A. The non-inverting input of U17A is referenced at approximately 1.5 volts by a voltage divider network which consists of resistors R14 and R15. When U4 outputs a logic LOW, it is inverted by U17A to a HIGH which turns off Q2. When Q2 turns off, Q1 is turned on by self-biasing resistor RN6 section 3-14. With Q1 on, a potential of approximately -10 Vdc is applied to the ODD XFR line to the Commutator CCA.

The LOW output from U4 is also applied to the non-inverting input of U17B. U17B has a +1.5 Vdc bias applied to its inverting input by R14 and R15. The LOW in makes U17B output a LOW which turns on transistor Q4. The emitter of Q4 is tied to VCC. With Q4 turned on, a positive voltage is applied to the base of Q3 and the anode of CR30. The positive bias on the base of Q3 keeps Q3 turned off. However, CR30 becomes forward biased and a positive potential of approximately +5 Vdc is applied to the ODD XFR NOT line to the Commutator.

When the output of U4 changes to a HIGH, Q2 and CR29 in the ODD XFR section are biased on and Q3 in the ODD XFR NOT section is biased. This changes the polarity of the signals on the ODD XFR and ODD XFR NOT lines. The ODD XFR and ODD XFR NOT changes state every 1/60th of a second.

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Scope Synch is available on the ODD XFR signal at test point TP1. Power for the CCA enters via P1-17, P1-18, P1-20, and P1-21. Diodes CR4 and CR6 form an “OR” for the two +28V supplies into Switch S1.

If switch S1 is on and fuse F1 is intact, the DC-DC converter PS1 converts the +28V to +5V, +12V and -12V supplies. Regulator U1 regulates the -12V supply to -10V. Regulator U2 regulates the +5V to +3.3V for powering the PLD U4.

Connector J6 is used for in-system programming of PLD U4 and should not be utilized by the customer.

Connector J7 is used for test of the CCA and should not be utilized by the customer.

Control lines entering via connectors P1 and P2 are surge protected by transient voltage suppressors (TVS) CR9 through CR28. The +28V supply is protected by TVS CR7. The +5V supply is protected by TVS CR2. The auto-ground check enable input is transient protected by TVS CR8.

Zener diode CR1 creates a 10V reference to power comparators U43 and U44 for monitoring of the on-board power supplies. Only the +5V monitor will be discussed further. The 10V reference biases resistors R25, R26, and R29 as a window into comparator inputs U43A-5 and U43A-6. If the +5V supply into U43A-4 and U43A-7 is within the window, the U43A-2 and U43A-1 outputs stay high; indicating the +5V supply is OK.

LED CR34 lights when switch S1 is in the ON position and the +3.3V, +5V, +12V and -12V supplies are all within tolerance, approximately nominal $\pm 10\%$. LED CR34 may be tested when off by pressing the lamp test switch on the LCU CCA.

Power status is also indicated by transistor Q10 into SPI I/O port U40-12 for access by the RMS CCA. Buffers U45 and U37 drive SPI signals to and from SPI I/O port U40, serial EEPROM U38, and optional temperature sensor U39. Strapping resistors R5, R8, R20, and R21 decode a unique address for SPI I/O Port U40. Logic U36, U41, and U42 prevent more than one SPI device from transmitting at once.

The SPI I/O Port U40 is reset through diode CR33 and resistor R19 during power-up or when the reset switch is pressed on the LCU CCA.

Table 2-1 Commutator Driver/Antenna Switch Sequence				
U12 (U27) Decoder Output	Display Driver	Commutator CCA Position	Antenna Number	
			Odd	(Even)
0	U8 (U23)	1A	1	2
1	U13 (U28)	2A	3	4
2	U18 (U32)	3A	5	6
3	U9 (U24)	4A	7	8
4	U14 (U29)	5A	9	10
5	U19 (U33)	6A	11	12
6	U10 (U25)	7A	13	14
7	U15 (U30)	8A	15	16
8	U20 (U34)	9A	17	18
9	U11 (U26)	10A	19	20
10	U16 (U31)	11A	21	22
11	U21 (U35)	12A	23	24
0	U8 (U23)	14B	25	26
1	U13 (U28)	15B	27	28
2	U18 (U32)	16B	29	30
3	U9 (U24)	17B	31	32
4	U14 (U29)	18B	33	34
5	U19 (U33)	19B	35	36
6	U10 (U25)	20B	37	38
7	U15 (U30)	21B	39	40
8	U20 (U34)	22B	41	42
9	U11 (U26)	23B	43	44
10	U16 (U31)	24B	45	46
11	U21 (U35)	25B	47	48

Table 2-2 VOR Ground check Offset Table					
Antenna # (0-47)	Ground Check (GCSC4..1)	Final Antenna # (0 -47)	Antenna # (0-47)	Ground Check (GCSC4..1)	Final Antenna #(0-47)
0	0	0	3	0	3
0	1	3	3	1	6
0	2	6	3	2	9
0	3	9	3	3	12
0	4	12	3	4	15
0	5	15	3	5	18
0	6	18	3	6	21
0	7	21	3	7	24
0	8	24	3	8	27
0	9	27	3	9	30
0	10	30	3	10	33
0	11	33	3	11	36
0	12	36	3	12	39
0	13	39	3	13	42
0	14	42	3	14	45
0	15	45	3	15	0

Table 2-2 VOR Ground check Offset Table					
Antenna # (0-47)	Ground Check (GCSC4..1)	Final Antenna # (0 -47)	Antenna # (0-47)	Ground Check (GCSC4..1)	Final Antenna #(0-47)
1	0	1	4	0	4
1	1	4	4	1	7
1	2	7	4	2	10
1	3	10	4	3	13
1	4	13	4	4	16
1	5	16	4	5	19
1	6	19	4	6	22
1	7	22	4	7	25
1	8	25	4	8	28
1	9	28	4	9	31
1	10	31	4	10	34
1	11	34	4	11	37
1	12	37	4	12	40
1	13	40	4	13	43
1	14	43	4	14	46
1	15	46	4	15	1
2	0	2	\	\	\
2	1	5	\	\	\
2	2	8	\	\	\
2	3	11	47	0	47
2	4	14	47	1	2
2	5	17	47	2	5
2	6	20	47	3	8
2	7	23	\	\	\
2	8	26	\	\	\
2	9	29	47	14	41
2	10	32	47	15	44
2	11	35			
2	12	38			
2	13	41			
2	14	44			
2	15	47			

2.3.2.23 Commutator CCA (1A10, 1A11) Theory

The Commutator CCA measures 15-7/8" high and 14-7/8" wide. There are two Commutator CCAs installed in the electronics cabinet. They are located on the upper left and upper right side of the cabinet and may be accessed by removing the side panels of the transmitter cabinet. The right (viewed from the front) Commutator CCA is used to switch the RF signals to all the odd antennas, and the left Commutator CCA drives the even antennas. Each Commutator has twenty-six N type RF connectors and two 37-pin D-shell connectors.

2.3.2.23.1 Commutator CCA Block Diagram Theory

Refer to [Figure 2-27](#). There are two Commutator CCAs installed in the Commutator rack, one to switch the RF signals to all the odd antennas, and the other to drive the even antennas. Since both CCAs perform exactly alike, the discussion is limited to the odd antenna switch circuit board.

To simplify the interconnection of the signals and antennas used in the 48 antenna system, [Table 2-1](#) is available as an aid. The pin numbers of the 012257 Pin Driver CCA and the 012702 Commutator do not match due to the different styles of connector (i.e. 40 pin dual row on the backplane and 37 pin D type).

Each individual antenna switch circuit on a Commutator CCA is functionally identical with the others. Pin diodes are used to perform the active switching of the RF to the individual antennas, and to swap the LSB and USB signals between each half of a switch assembly.

Each Commutator CCA can be thought of as having two halves; each half is connected to twelve antennas. One half is energized by the LSB RF and the other half by USB RF. The condition of the transfer and NOT transfer lines (from the driver board) determine which half of the Commutator CCA will process the two RF signals.

Each antenna switch on each half is applied RF energy via a common bus. The transfer control switches the two RF signals between the two bus lines, while maintaining complete isolation between them. Since the pin diode switches are operating with either +5V or -10V applied, those voltages insure the diodes are either fully on or off.

When the XFR line is high (+5V) the NOT XFR line is low (-10V), the arrangement turns on A bus pin diode switch 1 and B bus pin diode switch 2. B bus pin diode switch 1 and A bus pin diode switch 2 are biased off. Therefore, the LSB RF signal will be switched to the A bus and the USB RF signal will be switched to the B bus.

When the XFR and NOT XFR signals change polarity, the condition of the A and B pin diode switches change which makes the LSB RF signal be sent to the B bus and the USB RF signal goes to the A bus.

To enable the RF energy to be selectively applied to an individual sideband antenna, and at the same time prevent parasitic re-radiation from an adjacent antenna, a pin diode antenna switch is used. The drive levels are similar to the transfer levels used to switch the LSB and USB RF energy.

Each antenna assembly has twenty-four switches. Twelve are connected to the “A” bus and twelve to the “B” bus. Display driver U8 on the driver board drives both the 1A and 14B positions; display driver U13 handles both the 2A and 15B positions, etc. (see [Table 2-1](#)). This allows opposite paired antennas to radiate the LSB and USB signals.

Each display driver will control two antennas simultaneously. If sideband antenna #1 is a radiating antenna, then sideband antenna #25 is also a radiating antenna. The action of the pin diode antenna switch networks will supply the RF energy from the two buses into antenna #1 and #25 RF feed cables and the RF feed lines of all the other antennas are switched into on-board dummy loads.

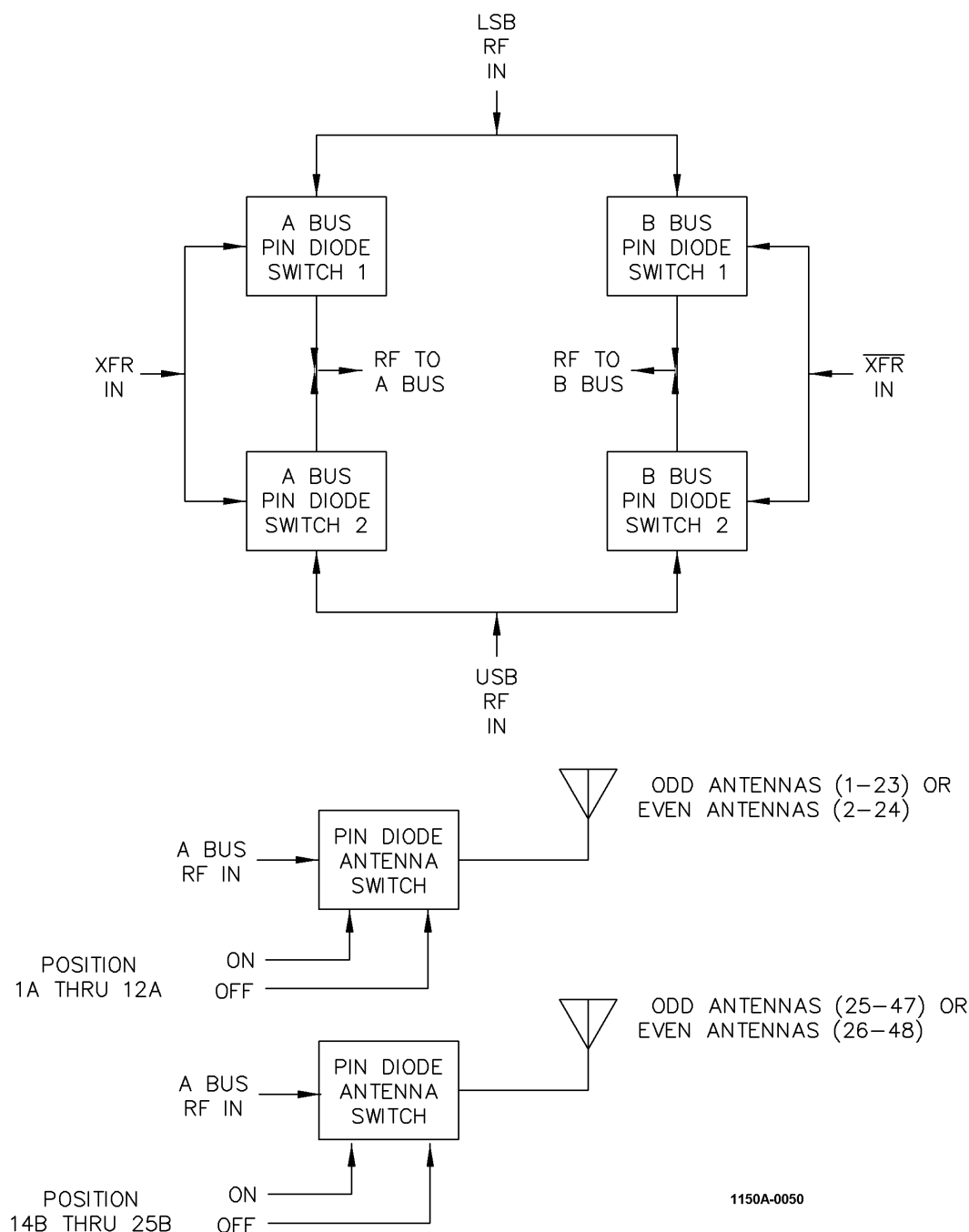


Figure 2-27 Commutator CCA, Block Diagram

Each antenna pair is selectively enabled by the selection of its assigned display driver. Each antenna line is also protected from extreme voltage spikes caused from lightning or other EMF generators by a gas surge suppressor.

2.3.2.23.2 Commutator CCA (2A2, 2A3) Detailed Circuit Theory

Refer to [Figure 11-6](#). There are two Commutator CCAs installed in the Commutator rack; one to switch the RF signals to all the odd antennas, and the other to drive the even antennas. Since both CCAs perform exactly alike, the discussion is limited to the odd antenna switch circuit board.

To simplify the interconnection of the signals and antennas used in the 48 antenna system, [Table 2-1](#) is available as an aid.

Each individual antenna switch circuit on a Commutator CCA is functionally identical with the others. Pin diodes are used to perform the active switching of the RF to the individual antennas, and to swap the LSB and USB signals between each half of a switch assembly.

Each Commutator CCA can be thought of as having two halves, each half is connected to twelve antennas. One half is energized by the LSB sin RF and the other half by USB sin RF. The condition of the transfer and NOT transfer lines (from the driver board) determine which half of the Commutator CCA the LSB and USB RF signals are connected.

Each antenna switch on each half is applied RF energy via a common bus. The transfer control switches the two RF signals between the two bus lines, while maintaining complete isolation between them. The pin diode switches are operating with either +5V or -10V applied, to insure the diodes are either fully on or off.

When the XFR line is HIGH (+5 Vdc), the NOT XFR line is LOW (-10 Vdc). This forward biases diodes CR301, CR302, CR305, CR308, CR311 and CR312. Diodes CR303, CR304, CR306, CR307, CR309 and CR310 are reversed biased. This allows the LSB RF signal to flow through CR311 and CR308 and apply RF to the “A” bus switches. The USB RF signal goes through CR302 and CR305 to the “B” bus antenna switches. Note that CR306 and CR307 are both biased off which provides isolation, while at the same time CR301 and CR312 are biased on to insure any RF in that portion of the circuitry will be shorted to ground.

When the XFR and NOT XFR signal switch, the LSB RF signal is applied to the “B” bus via forward biased diodes CR307 and CR310; the USB RF signal is sent to the “A” bus via forward biased diodes CR303 and CR306.

To enable the RF energy to be selectively applied to an individual sideband antenna, and at the same time prevent parasitic re-radiation from an adjacent antenna, a pin diode antenna switch is used. The drive levels are similar (+5V, -10VDC) to the transfer levels used to switch the LSB and USB RF energy.

Each antenna assembly has twenty-four switches. Twelve are connected to the “A” bus and twelve to the “B” bus. Display driver U8 on the driver board drives both the 1A and 14B positions; display driver U13 handles both the 2A and 15B positions, etc. (see [Table 2-1](#)). This allows opposite paired antennas to radiate the LSB and USB signals.

Each display driver provides two switchable outputs to each antenna pin diode switch. For simplicity, the discussion is limited to the 1A switch circuits. Each antenna pin diode switch circuit has a different reference designator series, starting with 10 and incrementing in groups of 10. Refer to the schematic for all of the group reference designators.

When display driver U8 is selected, the 1A ON line has +5 Vdc applied to it and the 1A OFF line has -10 Vdc on it. This forward biases diodes CR12 and CR14 and reverse biases diodes CR11 and CR13. If LSB RF energy is on the A bus, it will travel through diodes CR12 and CR14 and be applied to the sideband RF cable that feed that sideband antenna.

If U8 is not selected, then the 1A ON line has -10 Vdc on it and the 1A OFF line has +5 Vdc on it. This forward biases diodes CR11 and CR13 and reverse biases diodes CR12 and CR14. CR14 blocks RF energy from the A bus from traveling through the switch circuit. CR11 will pass any RF energy that may appear on the antenna feed cable to 47 ohm resistor R11. Capacitor C12 is a low impedance path at RF frequencies; therefore, resistor R11 is effectively shorted to ground. Each antenna that is not radiating an RF signal is now connected to an on-board dummy load. Additionally, any RF that may leak through CR14 will pass through CR13 to ground also via capacitor C15. Each antenna line is protected from extreme voltage spikes caused from lightning or other EMF generators by a gas surge suppressor.

2.4 PMDT (PORTABLE MAINTENANCE DATA TERMINAL (UNIT 2))

The lap top computer is a commercially obtained computer used for local control, monitoring and maintenance analysis of the DVOR system. The PMDT is typically located on a shelf or desk in the vicinity of the electronics cabinet. The PMDT is interconnected to the VOR via a USB cable to the front of the RMS CCA. The USB cable has a standard USB connector on one end that mates with a connector on the back of the PMDT. The other end of the cable is connected to the front panel of the RMS CCA in the top rack in the electronic equipment cabinet. The PMDT provides the technician access to the DVOR adjustments, tests and measurements. To the greatest extent possible, all indications of voltage, power and monitoring parameters are available through the PMDT. All parameters available locally are also available to a remote computer running the PMDT software. Station security control is provided through a three level password system. Level one is a read-only mode; all screens can be viewed but no changes can be made. Level two provides the capability to execute any commands not effecting the signal in space and includes on, off and station reset. Level three allows complete access, which includes the ability to change all operational parameters. Level four allows permits the change of the security codes.

2.5 BATTERIES (UNIT 3)

Four 12 volt batteries are connected in series to provide the needed 48 volt backup battery voltage used with the UPS in the BCPS. The standard batteries supplied are 65 amp/hour and will normally provide up to 3 hours of emergency operation. As an option higher capacity batteries may be provided to increase the duration of battery operation.

2.6 FIELD MONITOR KIT (UNIT 4)

The Field Monitor Kit contains all components needed to set up a receiving antenna system for the VOR.

For the DVOR, the basic arrangement is one dipole receiving antenna. The RF signal from the dipole antenna is applied to a signal splitter which divides the RF signal into two equal signals. Each portion of the RF is then sent to a VOR monitor. The dipole antenna provides 3 dB gain in the forward direction. The field monitor antenna is located approximately 300 feet from the DVOR antenna array.

3 OPERATION

3.1 INTRODUCTION

The operation of the Model 1150A VOR is controlled by a system of local and remote controls and status displays that provides the following general capabilities:

1. Control of operational parameters and comprehensive display of operational status through the use of user friendly Windows XP™ or VISTA™ based PMDT application running on a standard PC or notebook computer.
2. Control and display of equipment operation in the airport maintenance room and tower cab.
3. Remote control and status via modem and dial-up telephone line with the same displays and control menus as are used with local control.

3.2 REMOTE CONTROL STATUS UNIT (RCSU)

The RCSU provides summary level control and status of the VOR equipment. The RCSU is usually located in the airport equipment maintenance room. The controls and indicators on this panel are described in the RCSU manual (572238-0001 or 572240-0001) specific to this equipment.

3.3 REMOTE STATUS UNIT (RSU)

The RSU displays the summary level status for one pair of opposing approaches and an additional VOR/DME site, but on a smaller panel than the RCSU that is suitable for installation in a console in the tower cab. The controls and indicators on this panel are described in the RCSU manual (572238-0001 or 572240-0001) specific to this equipment.

3.4 REMOTE STATUS DISPLAY UNIT (RSDU)

The RSDU displays the same summary level status as the RCSU, on either a notebook pc, desktop LCD, or a touch-screen controlled display installed in the tower cab or various other locations. The controls and indicators on this display are described in the 2238 RCSU manual (572238-0001) specific to this equipment.

3.5 PORTABLE MAINTENANCE DATA TERMINAL (PMDT)

The PMDT system is comprised of a Microsoft Windows-based desktop or notebook PC and the PMDT control and monitoring software. The PMDT can be used in differing applications including:

1. Local control and status of VOR equipment in the equipment shelter. In this application the PMDT connects directly to the Remote Maintenance Subsystem (RMS) interface on the front of the equipment cabinet.
2. Remote Maintenance Monitor (RMM). The same software and hardware used in the shelter for direct control of the equipment can be used remotely to control and monitor the equipment.

The PMDT software allows the operator to easily select control parameters and monitor thresholds for display and change, and to select operation and status parameters for display. The operator can control the operational state of the equipment for maintenance purposes.

3.5.1 Equipment Turn On

3.5.1.1 Connecting the PMDT

When connecting directly to the VOR, the PMDT PC connects to the J1 PMDT USB port on the front of the RMS CCA using a standard USB A/B cable from one of the PMDT PC's USB ports. This USB cable (SELEX-SI #950915-0000) is supplied with the PMDT PC.

When the PMDT is used as an RMM, the connection is made by connecting the PMDT's internal modem to the TELCO line and using the PMDT software to either call the VOR directly, or call an associated RCSU to establish a PMDT-Passthru link to the VOR via the RCSU. Alternatively to the modem-based RMM connection, the PMDT can connect to the RCSU over a standard TCP/IP network link for RMM operations.

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3.5.1.2 Starting the PMDT Application

To start the PMDT application double-click on the PMDT icon on the desktop or select the Start >> Programs >> SELEX-SI >> PMDT menu item.

Note that the PMDT application is best viewed on a monitor with a resolution of 1024x768 or larger, using the “Normal (96DPI)” font size. Using the “Large size (120DPI)” Windows font will distort some PMDT screen controls making the data hard to read. Refer to the Microsoft Windows XP Display Properties screen for these settings.

3.5.1.3 Turning On the VOR

Turn on both AC switches, and then both DC switches on the BCPS assemblies. Turn on the battery circuit breakers. The system will perform its initialization, delay 20 seconds and then start transmitting. Pressing the Local Mode button will abort the 20 second delay and start the transmitters immediately.

3.5.2 Equipment Shutdown

3.5.2.1 Equipment Turn Off

Log out of the PMDT by selecting System >> Logoff/Disconnect. If the VOR is currently in a non-standard mode of operation, the user will be prompted to correct the issue(s) before continuing with the logoff. Once the PMDT is logged off, turn off both DC circuit breakers, and then both AC circuit breakers.

3.5.2.2 PMDT PC Turn Off

The power to the PMDT PC should not be removed until the Windows Shutdown sequence has been performed. This is done by selecting Start >> Shut Down... >> Shut down >> OK. The PMDT PC should automatically power down.

3.6 PMDT SCREENS

This section describes each of the screens used by the PMDT operator to control and monitor the performance of the VOR equipment.

3.6.1 General

The PMDT is a Microsoft Windows application requiring Windows XP or Windows VISTA. Windows 98, Windows NT or Windows 2000 may be used for direct connections to the VOR but the use of the PMDT over a modem will not be available on these systems.

The PMDT application contains three graphical sections; Menus, the Sidebar, and Screens. The screens are intended to be used with a mouse where the operator positions a cursor on a screen control symbol and clicks the left mouse button to activate the control. Clicking one of the menu items will cause the program to present screens associated with the broad category described by the function (RMS, Transmitter, Monitor, etc.).

NOTE

The VOR allows configuration changes by PMDT with a local connection by default. The DIP Switch S1 Bit 5 “Remote Allowed/Not Allowed” switch on the Backplane may be set to allow configuration change by remote connection also.

3.6.2 Menus

The PMDT functions are arranged in hierarchical menus such that selecting one menu will cause a lower level menu of functions to drop down. A “►” symbol to the right of a menu item indicates that a lower level menu will appear if the cursor is briefly kept on the menu item, or if that menu is selected.

Each menu item contains an underlined character. The menu item can be selected from the keyboard without using the mouse by simultaneously pressing the “Alt” key and the underlined character. This provides an alternate method for making screen selections should a mouse not be available with the PMDT. Similarly, screens containing several controls can be negotiated through the use of the arrow keys, the “Tab” key, and the space bar.

Refer to [Table 3-1](#) for a list of functions available through the PMDT.

Note that throughout this manual, the nomenclature used to indicate the navigation through the PMDT application(s) menus and selections is as follows:

System >> Connect >> Navaid >> Serial/USB Using the mouse (left-click) or keyboard (highlight & press Enter), select the System menu, then the Connect menu item, then the Navaid menu item, then the Direct menu item.

Table 3-1 PMDT Available Functions	
System	
Logon RMS	Log on to the VOR
Logoff/Disconnect	Logs off from the system. Also disconnects the RMM Modem
Configuration Save	Saves the current configuration settings to a specified file
Configuration Load	Loads the configuration settings from a specified file
Configuration Print	Prints the configuration settings to the printer
PMDT Setup	General PMDT application configuration settings – COM port, GUI Language, etc.
Print Setup	Configures the printer output. Refer to the Windows XP help for printer setup
Exit PMDT	Closes the PMDT application
RMS	
Status	Selects the RMS Status Screen
Data	Selects the RMS Data Screen
Logs	Selects the RMS Logs Screen
Configuration	Selects the RMS Configuration Screen
Commands	Opens the RMS Commands Menu
Config Restore	Restore configuration settings from EEPROM
Config Backup	Backup configuration settings to EEPROM
Monitors	
Data	Displays the Integral, Standby and Maintenance Data for both Monitors
Configuration	Settings for limits, delay times and Offset/Scale Factors
Commands	Opens the Monitor Commands Menu
Monitor 1 or 2	
Data	Displays the Integral, Standby and Maintenance Data for both Monitors
Test Results	Selects the Test Results screen
Fault History	Selects the Fault History screen
Offsets & Scale Factors	Configures the Monitor offsets and scale factors
Test Signal Output (J3)	Determines which signal is connected to Monitor connector J3
Transmitters	
Data	Selects the Transmitters Data Screen
Configuration	Selects the Transmitters Configuration Screen
Commands	Opens the Transmitter Commands Menu
Diagnostics	
Power Up Results	Displays the results of the last Power-Up Diagnostic tests
Fault Isolation	Used to run Automatic Fault Isolation and display the results
Info	
About PMDT	Displays PMDT Version and Date information

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3.6.3 System Status at a Glance - Sidebar Status and Control

The Sidebar Status and Control is presented on every screen as shown in [Figure 3-1](#) (Dual Transmitter shown). The portion of the screen under the “Connected” indication is called the “Sidebar”. The Sidebar presents the current status of the VOR. The data is refreshed approximately once every two seconds.

At a glance, the technician can determine the state of the VOR. Buttons (point and click with the mouse) are provided to select Tx1 Main, Tx2 Main, Tx1 Antenna, Tx2 Antenna, Tx1 Load, Tx2 Load, Tx1 Off, Tx2 Off, Monitor 1 Bypass, and Monitor 2 Bypass. The displayed data originates from either Monitor 1 or Monitor 2, depending on which transmitter is on the air.

If a DME is collocated with this VOR, its summary level status will also be displayed at the bottom of the Sidebar.

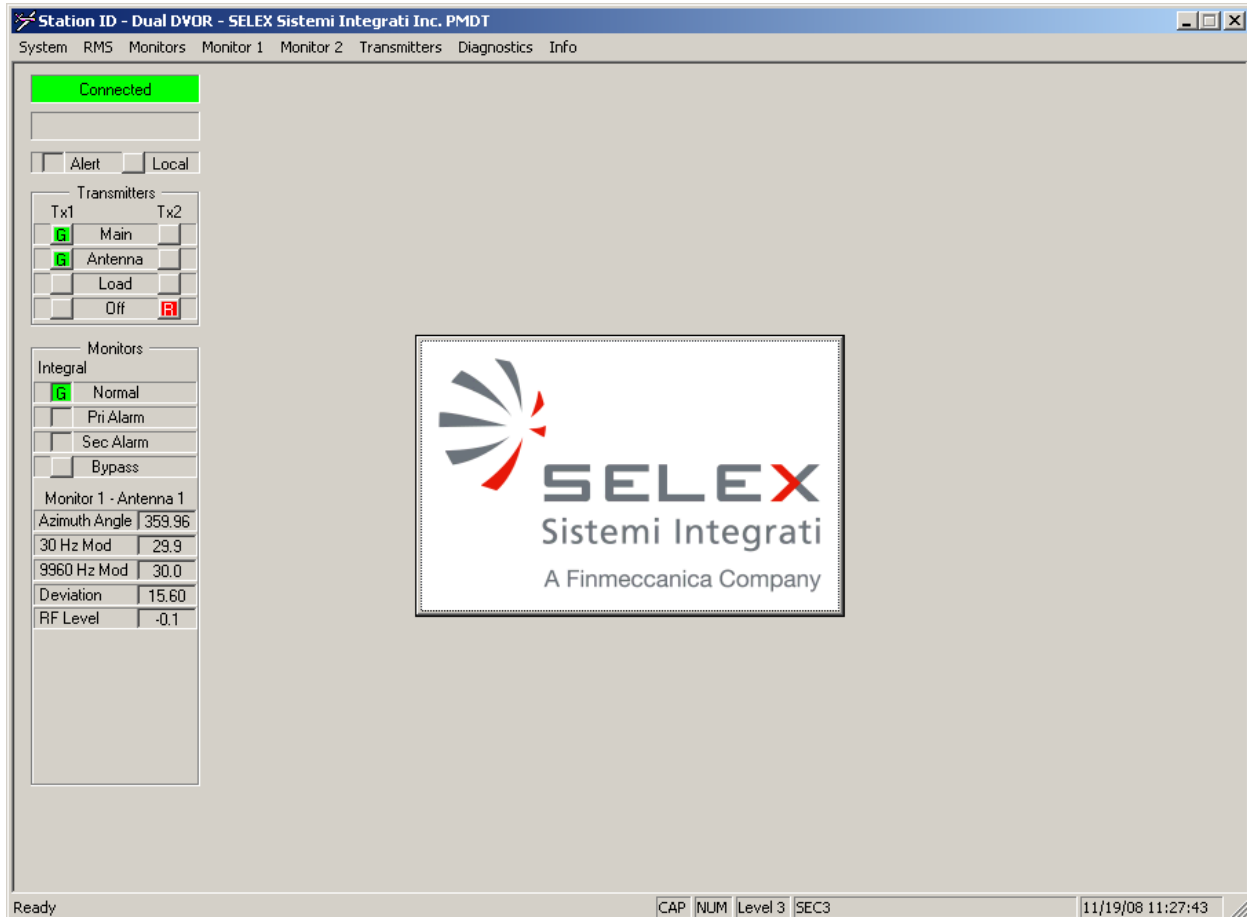


Figure 3-1 PMDT Opening Screen with “Sidebar” Data

3.6.4 Screen Area

The screen area displays selected common parameters and status data. The screen may present tabs and buttons that allow the operator to make further selections.

Shortcuts have been implemented in the PMDT allowing keyboard entry of the Next, Close, Apply, and Reset functions. These buttons are enabled as applicable when navigating through the various PMDT screens. When they are enabled, pressing the following function key results in the specified action:

F5	Next	Move to the next screen in the current group.
F6	Close	Close the current group of screens.
F7	Apply	Save the changes made in the current screen.
F8	Reset	Cancels any changes to the current screen, leaving the data unchanged.

The main PMDT screen also contains two buttons that are used as follows:



Print Screen - Pressing this button sends a copy of the current PMDT screen, including the Sidebar, to the default printer. This will either be a graphical image or a text-based copy of the screen, depending on how the “Print Screens” option is set in the PMDT Configuration screen shown below.



Copy Data to Clipboard - Available only when a block of text is displayed on a screen, such as in the RMS >> Logs screens. Pressing this button copies the text data to the Windows Clipboard, so that the user can paste it into another Windows application such as Notepad.

3.6.5 Configuring the PMDT

The PMDT Configuration screen shown in [Figure 3-2](#) is used to configure the various PMDT options.

The direct connection COM port must be configured before any navaid connection can be established. For the VOR navaid, which has a USB-based PMDT connection, this must be set to the associated USB Serial Port. Note that this USB Serial Port is dynamically installed/uninstalled when the USB cable between the PMDT PC and the VOR is connected/disconnected, as well as when the navaid is powered on/off.

The Print Screens option allows the user to select either a Graphic Image, or a text-based representation of the screen.

The dial-out modem must be selected prior to establishing a modem-based connection to a navaid or RCSU. This should be set to the desired PMDT computer internal modem. Alternatively, a dedicated leased-line modem can be used to establish the RMM link.

The desired language for the PMDT GUI may be selected from the available list.

Typically, the Local RCSU IP Address and IP Port should be kept at the defaults settings shown below. Refer to the facility’s IT department for the proper settings before making any changes to these settings.

The Operational Mode should typically be set to “Normal”. The “Specified Navaid Mode” is used to force the PMDT to connect to a user-specified navaid (eg. Localizer, Glideslope, VOR, etc.) instead of dynamically determining the navaid type during its initial communications with the navaid. Change this setting only if directed by SELEX-SI Customer Service, or the installation instruction in a specialized SELEX-SI RMM equipment kit. When enabled, navaid connection is initiated by selecting the following menu items:

System>>Connect>>Specified Navaid>>Serial/USB [or Modem]>>[the desired navaid]

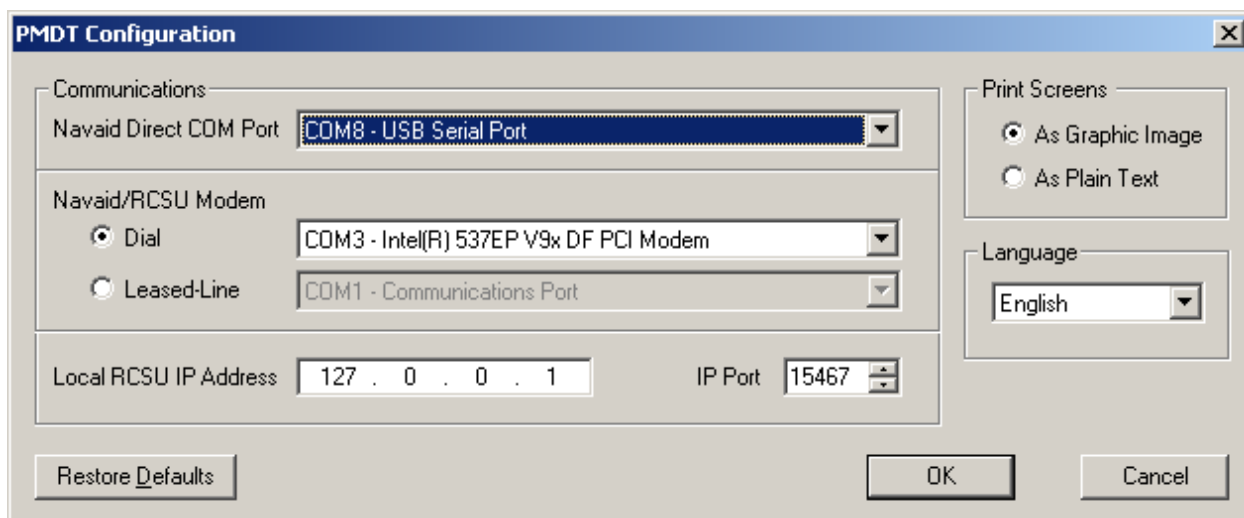


Figure 3-2 PMDT Configuration Screen

3.6.6 Connecting to the VOR

3.6.6.1 Security Levels

Access to the VOR system via the PMDT is restricted through the use of four security levels. Level 1 is the lowest security level, and Level 4 is the highest security level. These security levels are accessed as shown in [Table 3-2](#):

Table 3-2 VOR Security Levels		
Security Level	Accessed by	Permissions
Level 1	Logging on with either: User ID of "GUEST", without a password, or a valid Level 1 User ID and the corresponding Password.	System Status and Parameters. At this level, the user has display-only access to all screens except for the security codes screen. The user has no control over the system.
Level 2	Logging on with: A valid Level 2 User ID and the corresponding Password	Non-Critical Functions. At this level, the user has Level 1 access plus the issuance of discrete commands which do not modify the signal in space. For example, the user can turn the signal on/off, but cannot modify the course position.
Level 3	Logging on with: A valid Level 3 User ID and the corresponding Password	Critical Functions (except Passwords) - The user has access to all functions that are available in the system, except for the Security Screen.
Level 4	Logging on with: The valid Level 4 User ID and the corresponding password.	Critical Functions - The user has access to all functions that are available in the system, including assignment of User IDs, Passwords, and Security Levels in the Security Screen.

The default Level 4 user account information, which is case-sensitive, is:

User Name: SEC4
Password: FOUR

The default Level 3 user account information, which is case-sensitive, is:

User Name: SEC3
Password: THREE

To maintain system security, this default user account information should be changed by the authorized personnel.

NOTES

After 3 failed attempts to logon (ie. invalid User ID or Password), further logon attempts will be blocked for a period of 5 minutes.

The PMDT software contains an Activity Detector feature that will automatically log off a user after 15 minutes of inactivity (either mouse or keyboard activity). This feature is disabled when the system is in Local Mode.

3.6.6.2 PMDT Logon via Direct or Modem Connection

To log on to the equipment directly, select System >> Connect >> Serial/USB. The PMDT Login screen (Figure 3-5) will be displayed. Enter a valid User ID and the associated password and press OK.

To log onto the equipment remotely, select System >> Connect >> Modem. Unless the Leased Line Modem option has been enabled in the PMDT Configuration screen, the System Directory screen will be displayed as shown in Figure 3-3. This directory stores the Station Identifier and Phone Number for the last 100 systems called. Either select an entry from the Contacts list, or press the “Add Entry” button to enter a new phone number.

The “Change Dialing Properties” and “Change Modem Properties” buttons can be used to configure various Windows-based modem properties, such as using a calling card or handling specific area code rules. Refer to Windows Help for the associated screens.

Once the phone number and connection properties have been set, pressing the Dial button initiates the call. Once the PMDT’s modem connects to the navaid’s modem, the PMDT Login screen (Figure 3-5) will be displayed. Enter a valid User ID and the associated Password and press OK.

To remove a contact from the list, select the contact and press the delete entry button.

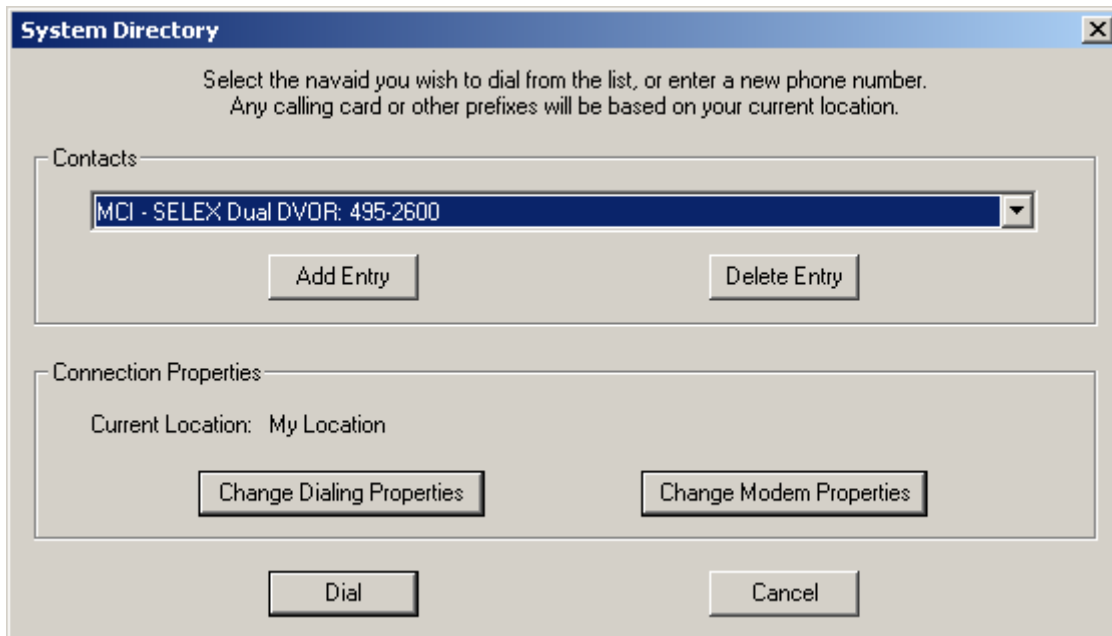


Figure 3-3 PMDT System Directory

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The “Add Phone Number” screen shown in [Figure 3-4](#) is used to specify how the call will be placed. A Windows TAPI-based call allows for the use of a long distance calling card, or handling specific Country Code or Area Code rules, which must be configured using the “Change Dialing Properties” button on the System Directory screen.

For basic phone calls, the phone number can be entered in the “Just dial this Phone Number” field, including any required dialing prefixes such as “9”. A comma can be used to insert a 1 second delay in the dialing sequence if needed.

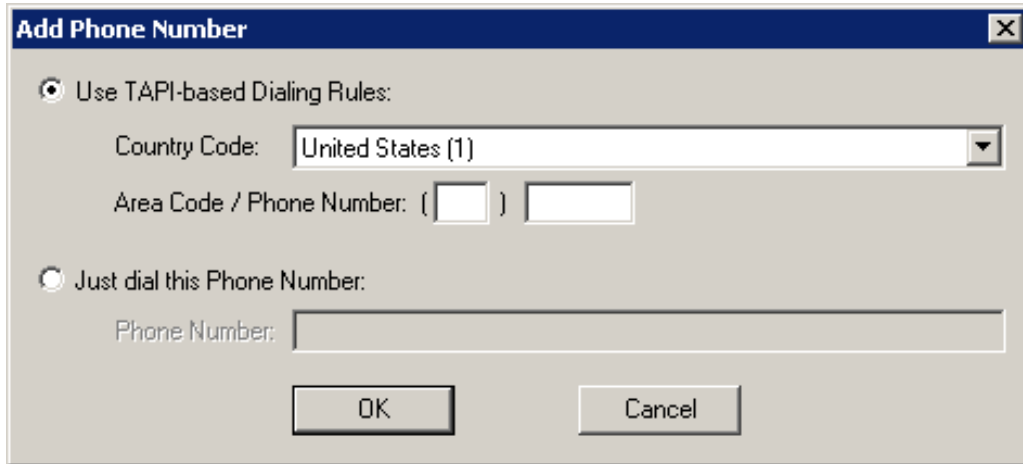
The "Add Phone Number" dialog box has a title bar with the text "Add Phone Number" and a close button. It contains two radio button options. The first option, "Use TAPI-based Dialing Rules:", is selected. Below it, there is a "Country Code:" label followed by a dropdown menu showing "United States (1)". Below that is an "Area Code / Phone Number:" label followed by two input fields: the first is enclosed in parentheses and the second is empty. The second radio button option, "Just dial this Phone Number:", is unselected. Below it is a "Phone Number:" label followed by a single long input field. At the bottom of the dialog are "OK" and "Cancel" buttons.

Figure 3-4 Add Phone Number Screen

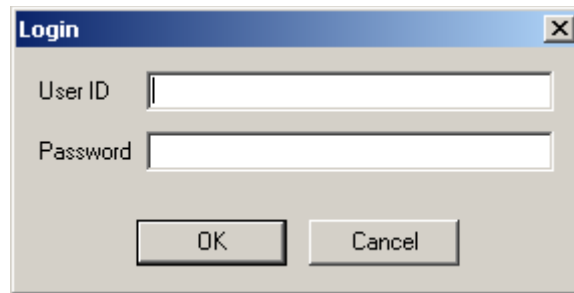
The "Login" dialog box has a title bar with the text "Login" and a close button. It contains two labels, "User ID" and "Password", each followed by an input field. At the bottom of the dialog are "OK" and "Cancel" buttons.

Figure 3-5 PMDT Login Prompt

To obtain Security Level 4 access, select System >> Logon RMS and enter the Level 4 User ID and Password. If the ID and Password were entered correctly, the Initial PMDT screen ([Figure 3-1](#)) will be displayed. If the logon attempt was not successful then the PMDT will display a message indicting an unsuccessful log-on and then display the PMDT Login screen again.

NOTE

The Security Codes Screen will not be displayed for Levels 1, 2, and 3. Some commands and controls will appear in a light grey color to indicate that access to these controls is not available at the current password level.

3.6.7 RMS Screens

3.6.7.1 RMS Status Screens

The PMDT contains the following screens that provide summary level status for the various system modules.

3.6.7.1.1 VOR/DME Status Screen

The VOR/DME Status Screen is shown in [Figure 3-6](#). This screen contains indicators for VOR status provided directly by the Remote Monitoring Subsystem (RMS). If a DME is collocated with this VOR, its summary level status will also be displayed.

The RMS status consists of indicators for Local Control, Maintenance Alert, Power Status, Remote Control configuration, and RCSU connectivity. Status for the associated DME includes Power Status, Alarm, Bypass, Enabled, and Antenna connection.

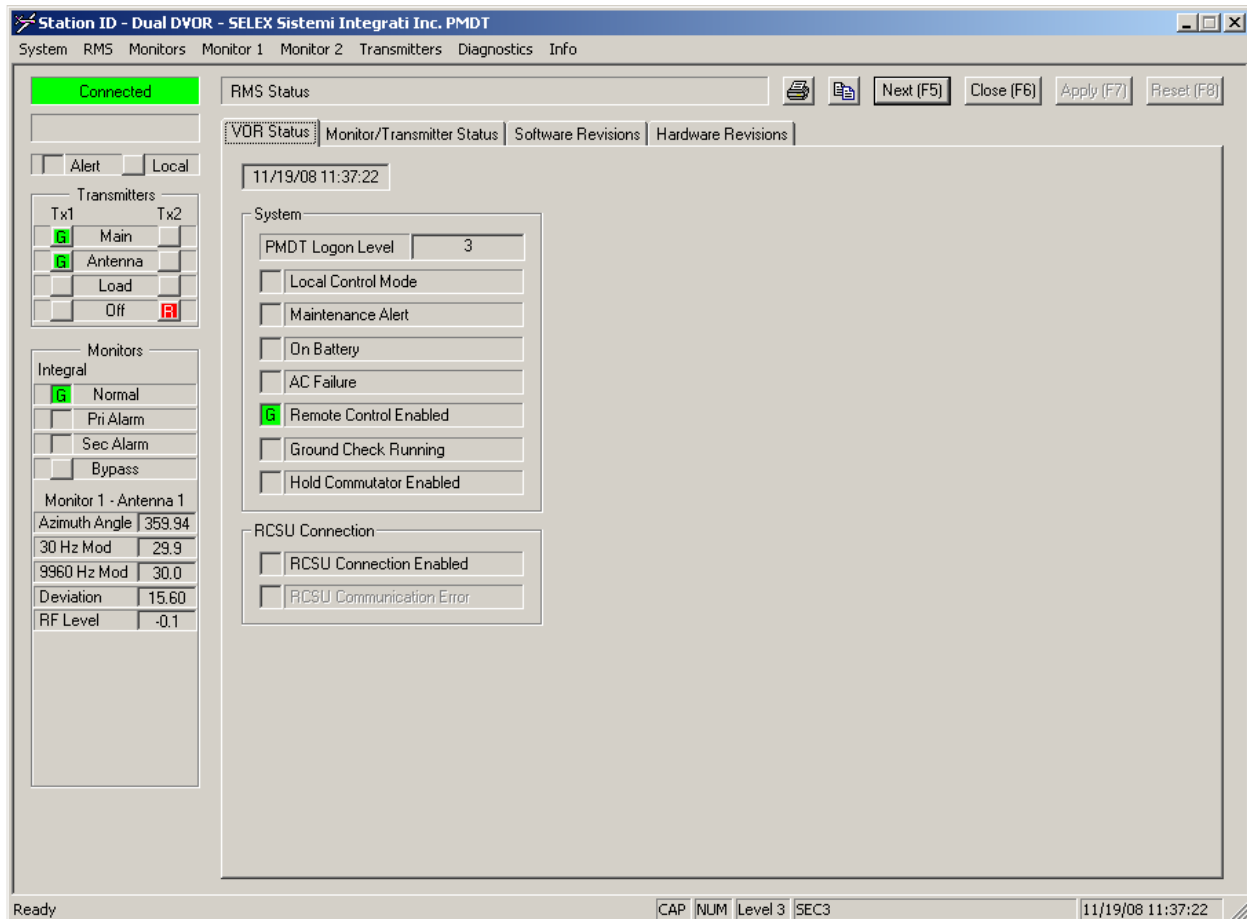


Figure 3-6 VOR Status Screen

3.6.7.1.2 **Monitor/Transmitter Status Screen**

The Monitor/Transmitter Status screen is shown in Figure 3-7. This screen shows the current summary-level operational status of the monitors and transmitters.

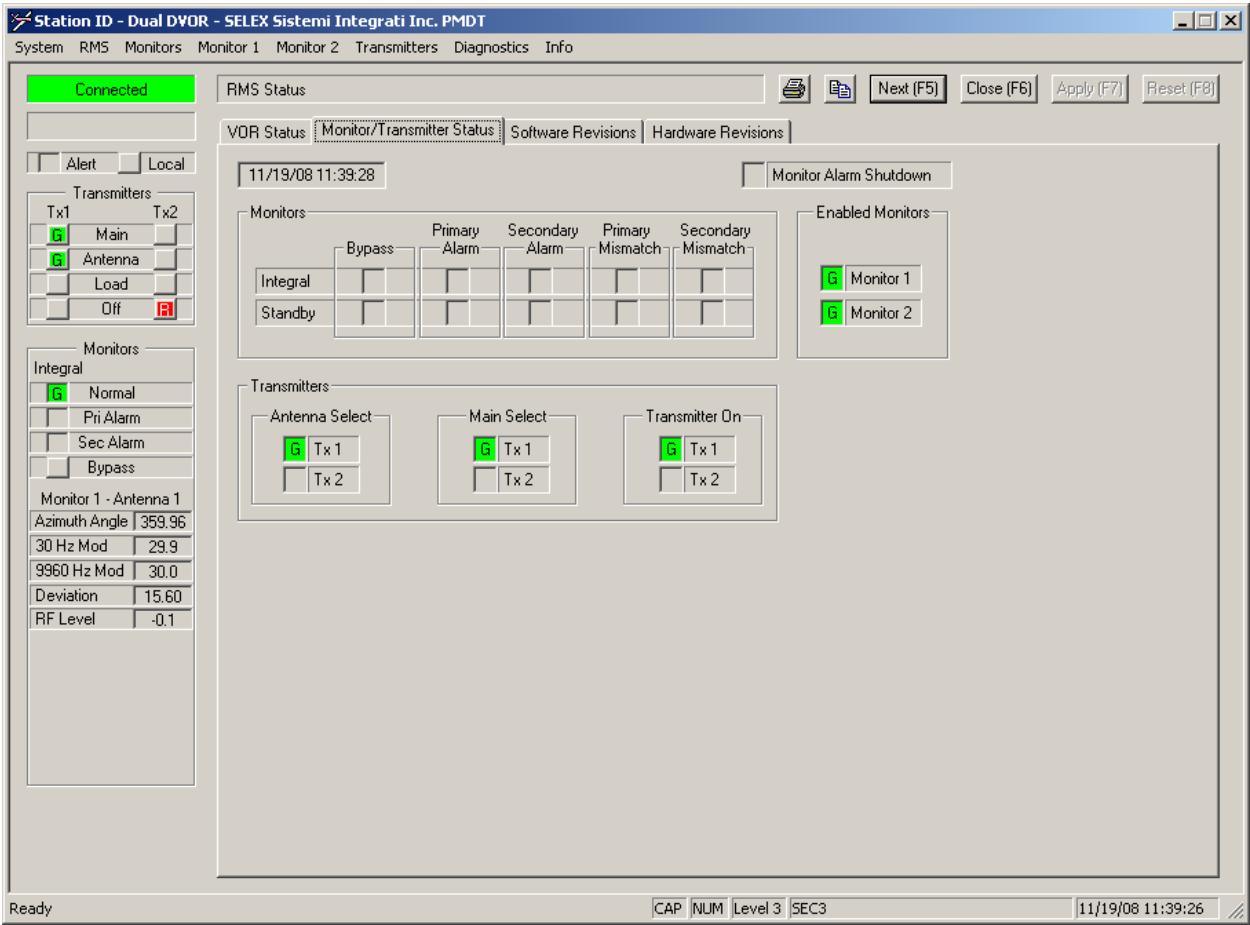


Figure 3-7 Monitor/Transmitter Status Screen

3.6.7.1.3 Software Revisions Screen

The Software Revisions screen is shown in Figure 3-8. This screen contains lists the software revision number for each embedded processor in the navaid.

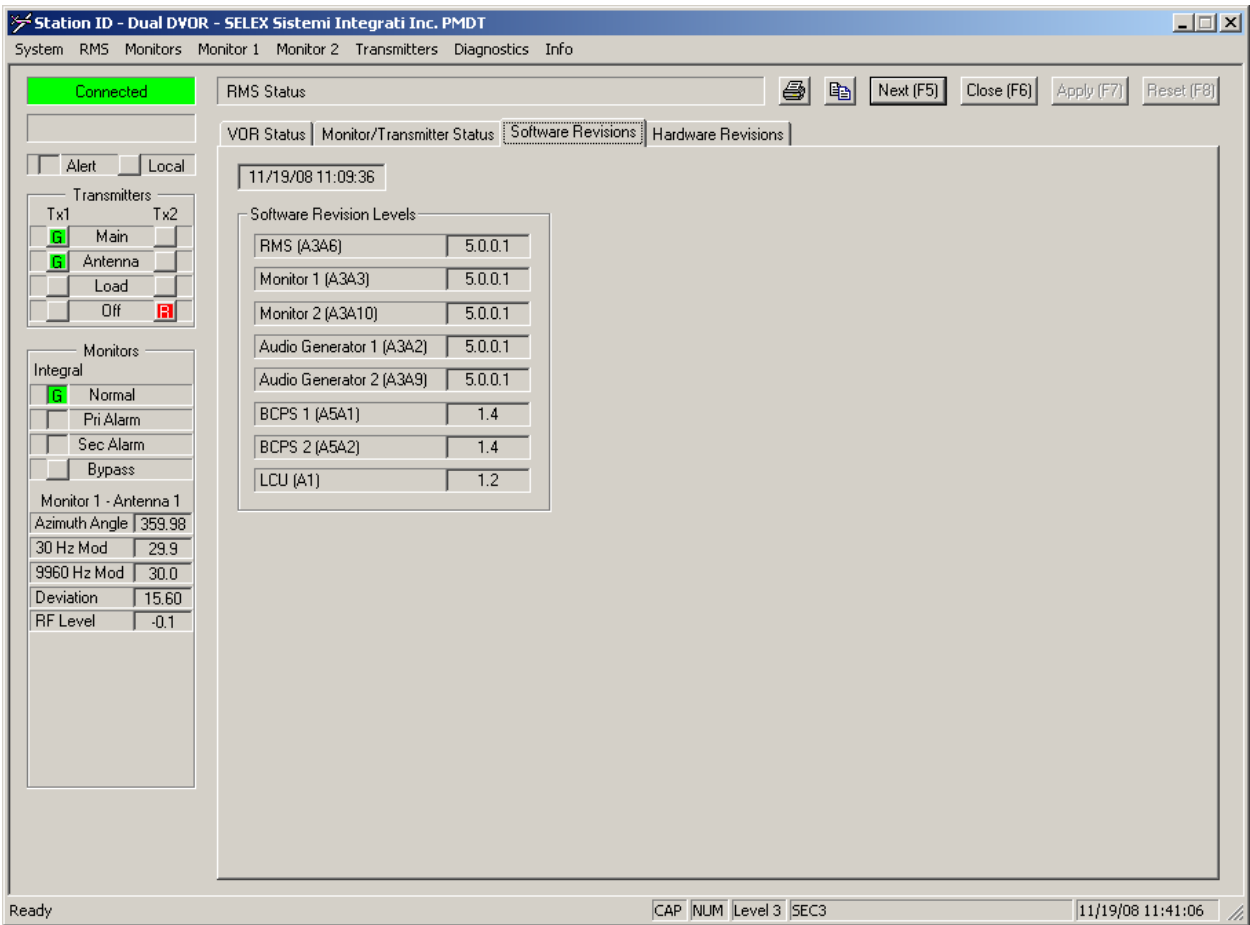


Figure 3-8 Software Revisions Screen

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3.6.7.1.4 Hardware Revisions Screen

The Hardware Revisions Screen is shown in [Figure 3-9](#). This screen is used to maintain configuration management information for each of the installed modules. Data can be entered in each of the available fields by the technician. This data is then written into the on-board memory in the associated module, for use in Customer Service, module history records, and general system maintenance.

[illegible]

Figure 3-9 Hardware Revisions Screen

3.6.7.2 RMS Data Screens

The PMDT contains the following screens to provide detailed system data collected by the RMS.

3.6.7.2.1 RMS Maintenance Alerts Screen

The RMS Maintenance Alert screen is shown in [Figure 3-10](#). This screen shows the source of any maintenance alerts in the system. From this screen the operator can determine the alert/alarm and proceed to the associated screen to observe the specific data driving the alert/alarm. For example, if the RMS Digital I/O Data indicator was on, the operator would go to the RMS >> Data >> Digital I/O screen to see which specific Digital I/O parameter was causing the alert.

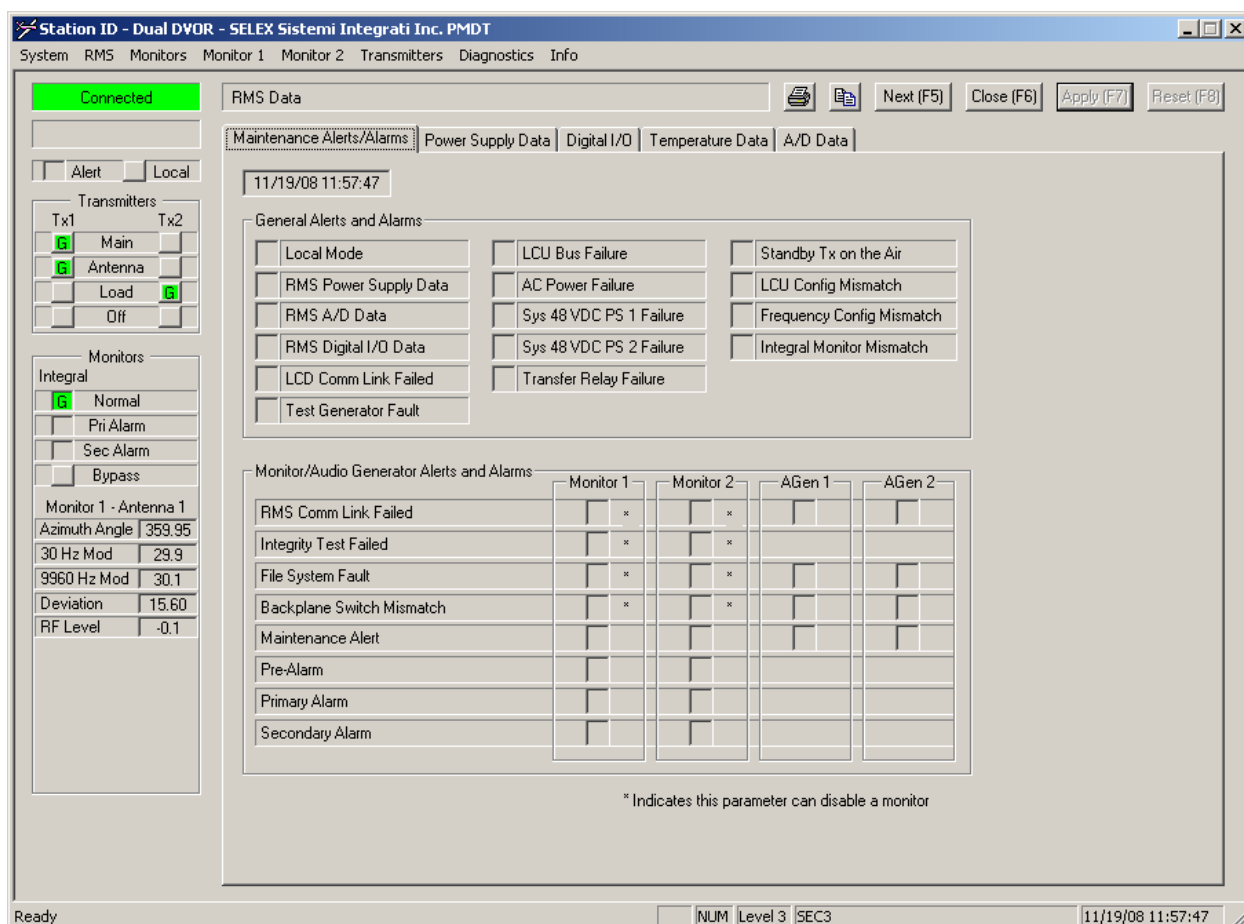


Figure 3-10 RMS Maintenance Alerts/Alarms Screen

3.6.7.2.2 Power Supply Data Screen

The RMS Power Supply Data screen is shown in Figure 3-11. This screen shows the status and limits of each of the system's power supplies. If any parameter is enabled as a maintenance parameter in the associated RMS>>Configuration>>Power Supply Limits screen, and its measured value falls outside of either the Alert Limits or Pre-Alert Limits, the parameter's value will be colored yellow to indicate the alert condition.

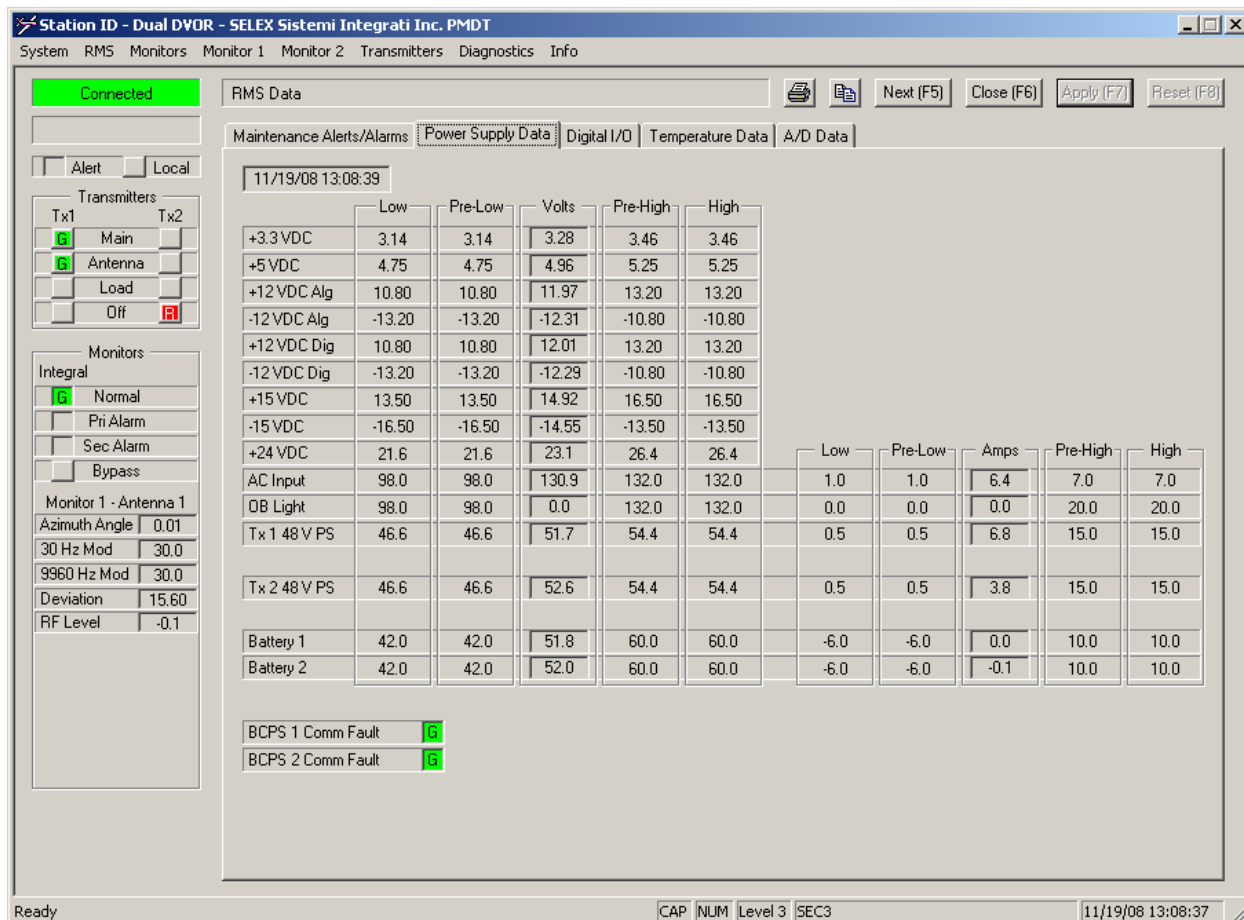


Figure 3-11 RMS Power Supply Data Screen

3.6.7.2.3 Digital I/O Screen

The RMS Digital I/O Data screen is shown in Figure 3-12. This screen displays the current status of the system's digital inputs and outputs. Any abnormal signal will be indicated in yellow or red.

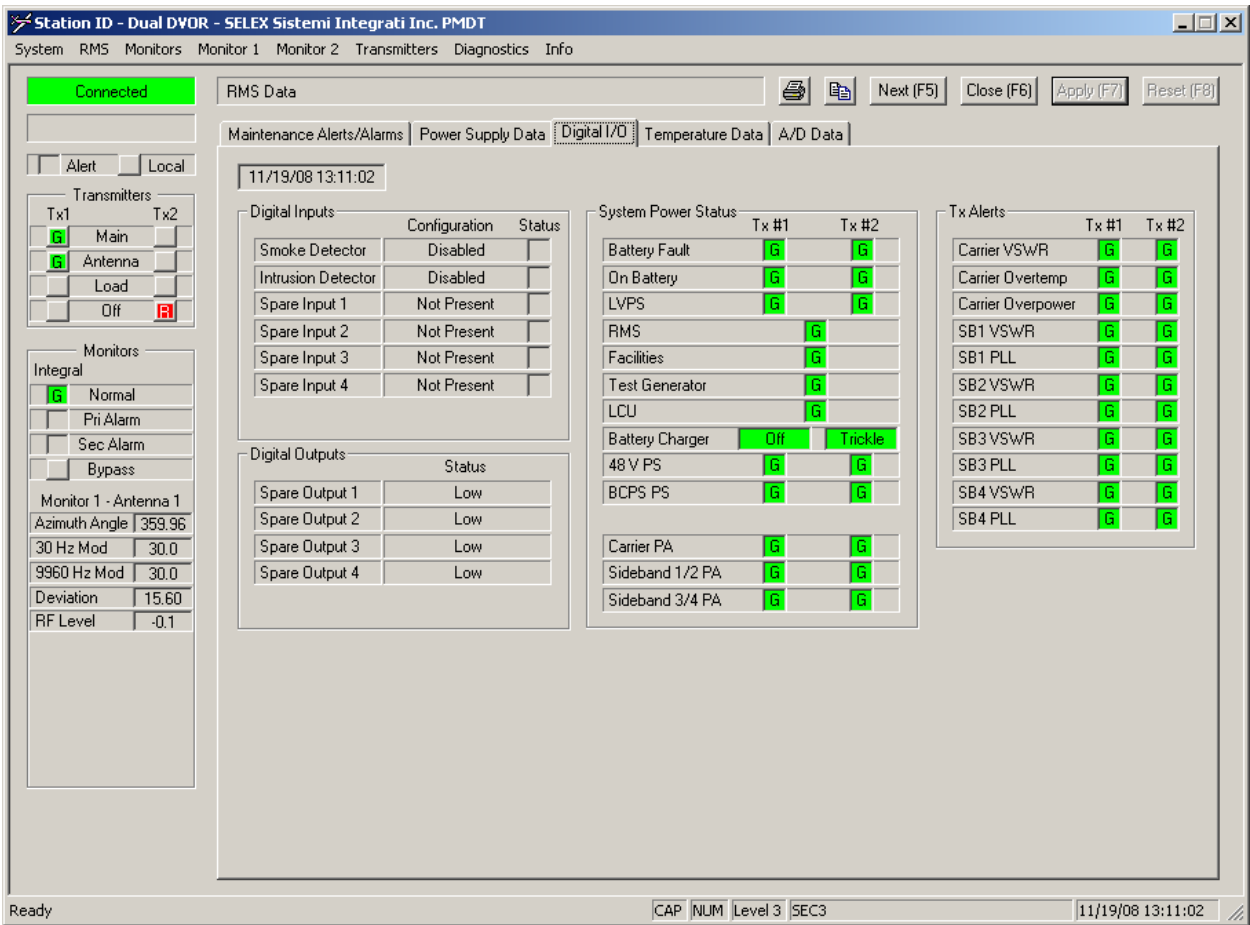


Figure 3-12 RMS Digital I/O Data Screen

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3.6.7.2.4 Temperature Data Screen

The RMS Temperature Data screen is shown in Figure 3-13. This screen displays the current status of the system's temperature sensors. The Cabinet Interface temperature sensor is located on the Cabinet Interface Assembly located at the rear of the cabinet. The optional external temperature sensor module is connected to the Cabinet Interface Assembly. The remaining sensors are located on the individual modules. Any abnormal signal will be indicated in yellow.

Note that when the optional Environmental Sensor Kit is not installed, the Outside Temperature reading will default to its lowest reading of -25°C.

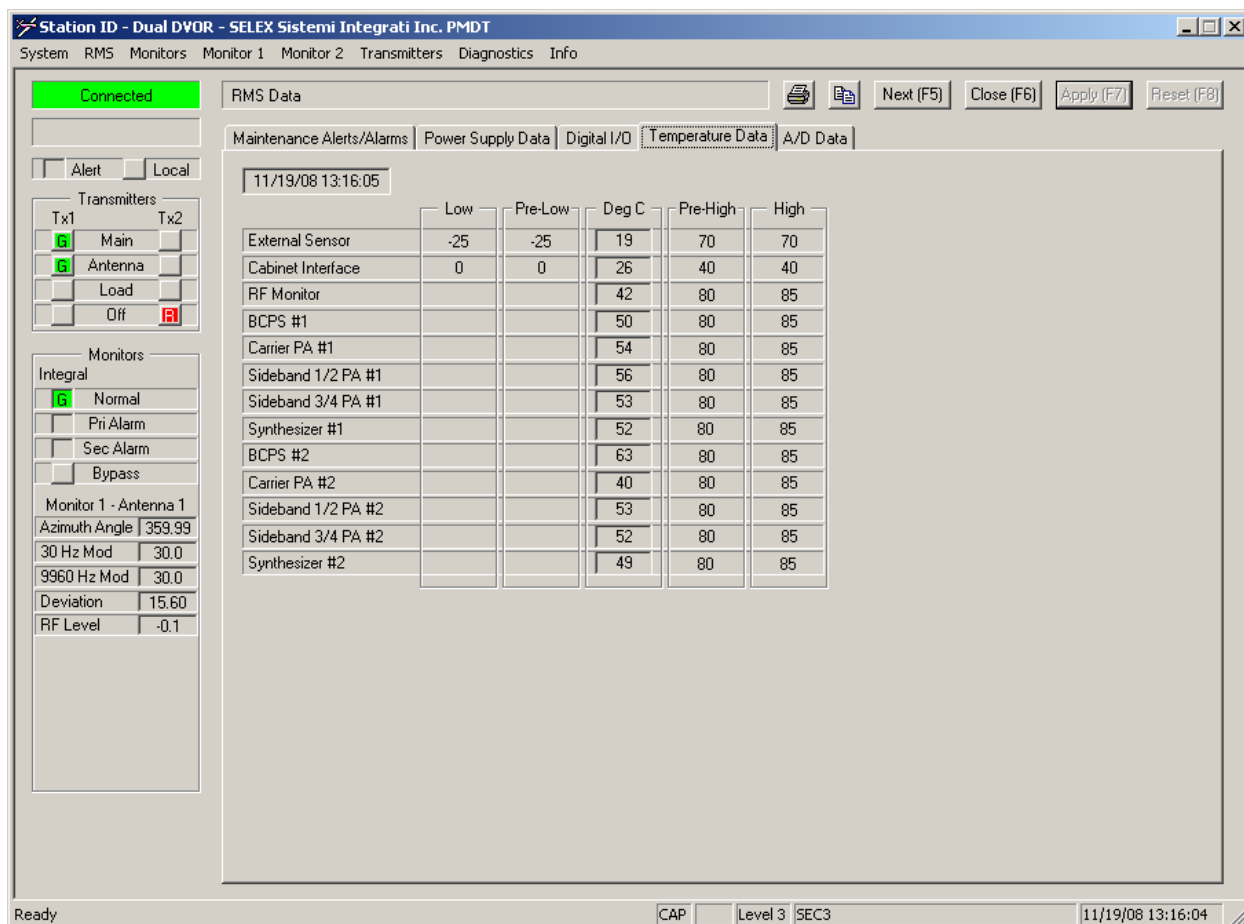


Figure 3-13 RMS Temperature Data Screen

3.6.7.2.5 A/D Data Screen

The RMS A/D Data screen is shown in Figure 3-14. This screen shows the status and limits of each of the Spare Analog signals. If any parameter is enabled as a maintenance parameter in the associated RMS>>Configuration>>A/D Limits screen, and its measured value falls outside of either the Alert Limits or Pre-Alert Limits, the parameter’s value will be colored yellow to indicate the alert condition.

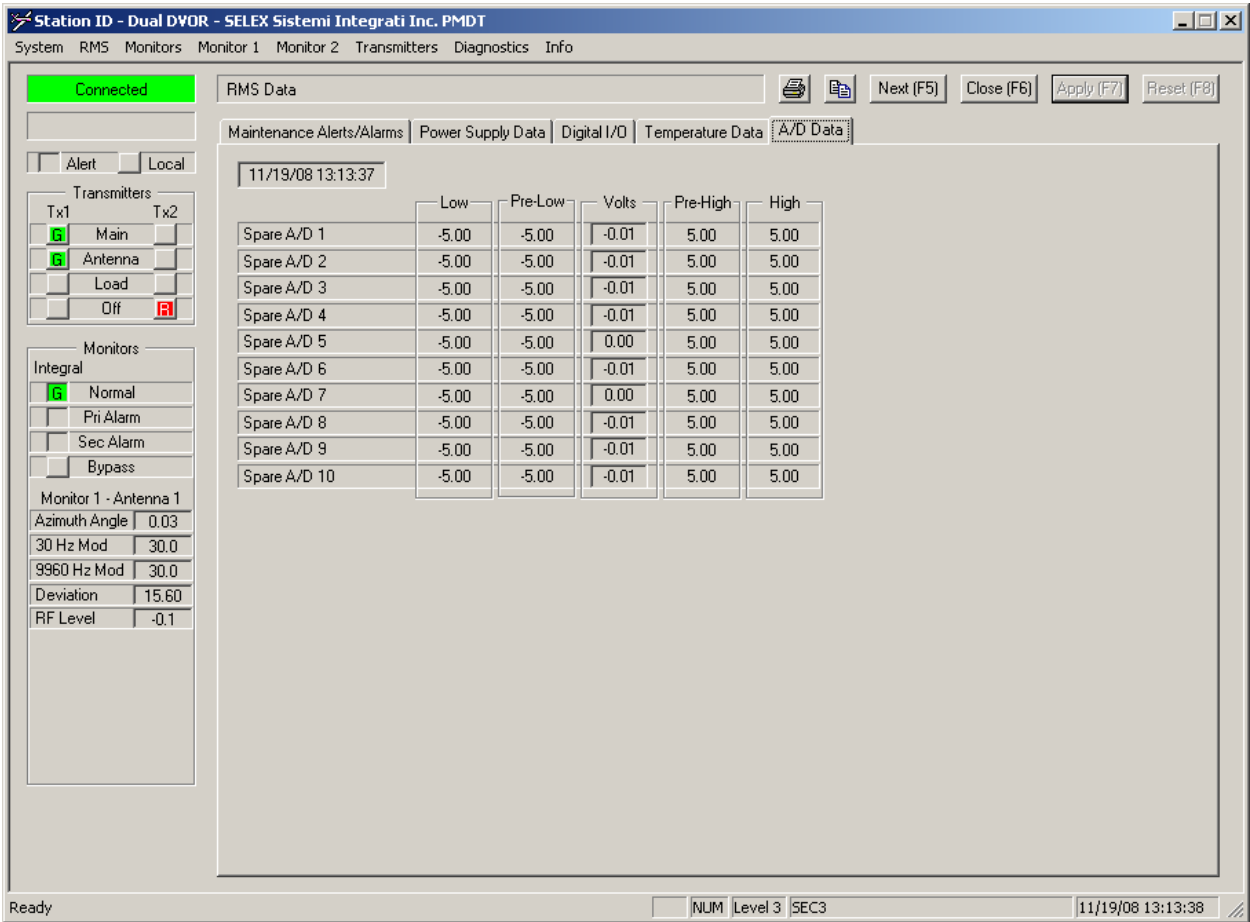


Figure 3-14 RMS A/D Data Screen

3.6.7.3 RMS Logs Screen

The PMDT includes the following log screens that provide time tagged records of changes in the system parameters and operating condition.

3.6.7.3.1 Operational Summary Screen

The Operational Summary Screen is shown in Figure 3-15. This screen presents the duration that each of the transmitters has spent in each operational condition. The Reset Operational Summary button restarts all of the Operational Summary timers.

Station ID - Dual DVOR - SELEX Sistemi Integrati Inc. PMDT

System RMS Monitors Monitor 1 Monitor 2 Transmitters Diagnostics Info

Connected

RMS Logs

Operational Summary | Alarms | Maintenance Alerts | Command Activity | Parameter Change

	Transmitter 1	Transmitter 2	Hours
Normal Operation	0.00	0.00	Hours
Monitor Bypass	0.00	0.00	Hours
Monitor Alarm	0.00	0.00	Hours
Transmitter Off	0.00	0.00	Hours
Hot Standby	0.00	0.00	Hours

Availability 0.0000 0.0000 %

Start Time 11/19/08 13:23:44
End Time 11/19/08 13:23:45
Hours Elapsed 0.0003

Reset Operational Summary

Transmitters
Tx1 Tx2
Main Antenna Load Off

Monitors
Integral
Normal Pri Alarm Sec Alarm Bypass

Monitor 1 - Antenna 1
Azimuth Angle 0.02
30 Hz Mod 30.0
9960 Hz Mod 30.0
Deviation 15.60
RF Level -0.1

Ready Level 3 SEC3 11/19/08 13:23:59

Figure 3-15 RMS Operational Summary Screen

3.6.7.3.2 Alarm Log Screen

The Alarm Log Screen is shown in Figure 3-16. This screen provides the latest 100 alarms state changes that have occurred. When 100 or more state changes have occurred, subsequent alarms will replace the oldest alarm state change in the log. Entries in the log identify the date and time the alarm occurred, the type of alarm event, the test that detected the alarm, and the current status of the alarm condition. The Update button reloads the log file from the RMS and updates the display with any new entries. The Reset button clears the log file in the RMS.

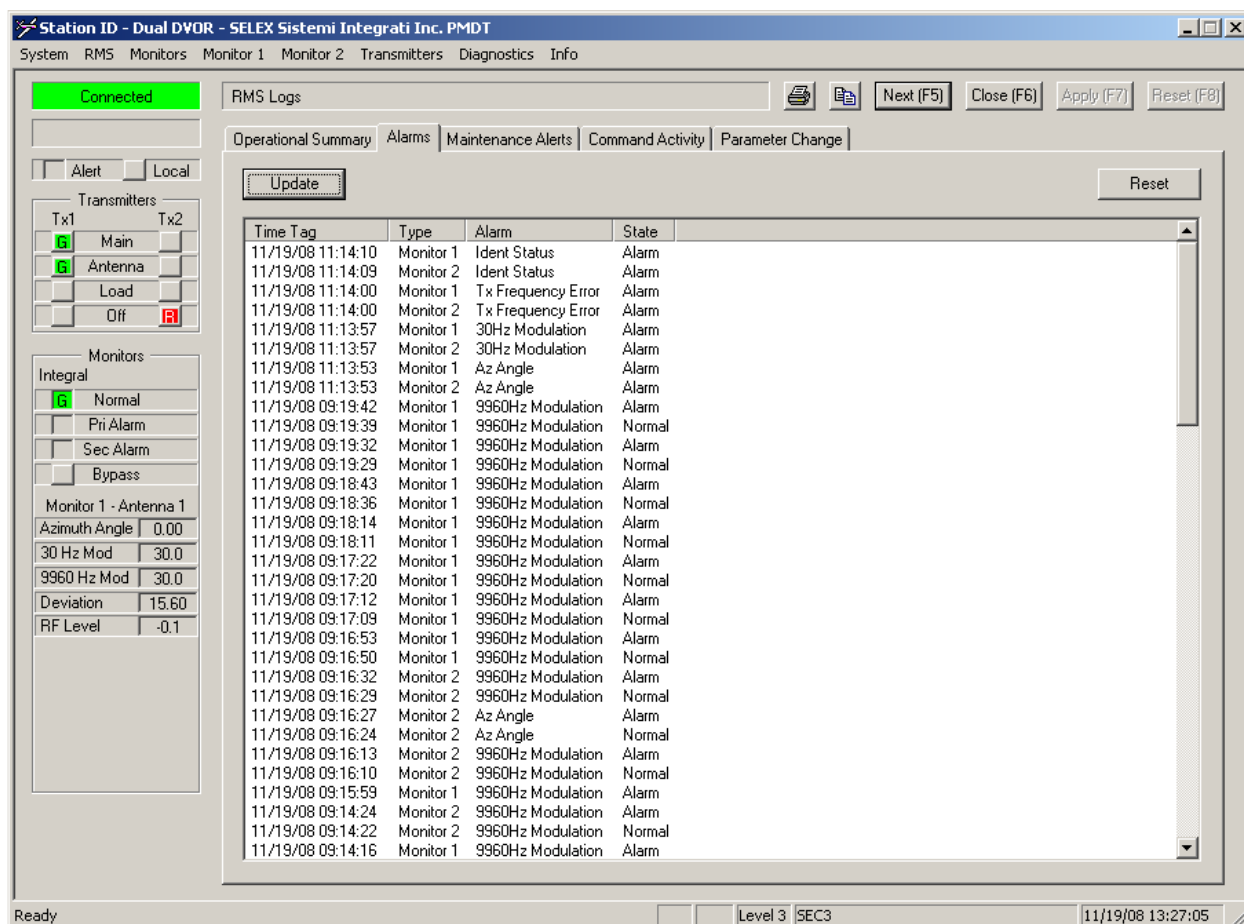


Figure 3-16 RMS Alarm Log Screen

3.6.7.3.3 Maintenance Alert Log Screen

The Maintenance Alert Log Screen is shown in Figure 3-17. This screen provides the latest 100 maintenance alert state changes that have occurred. When 100 or more state changes have occurred, subsequent alerts will replace the oldest events in the log. Entries in the log identify the date and time the alert occurred, the type of alert, and a short description of the alert event, and the current status of the alert condition. The Update button reloads the log file from the RMS and updates the display with any new entries. The Reset button clears the log file in the RMS.

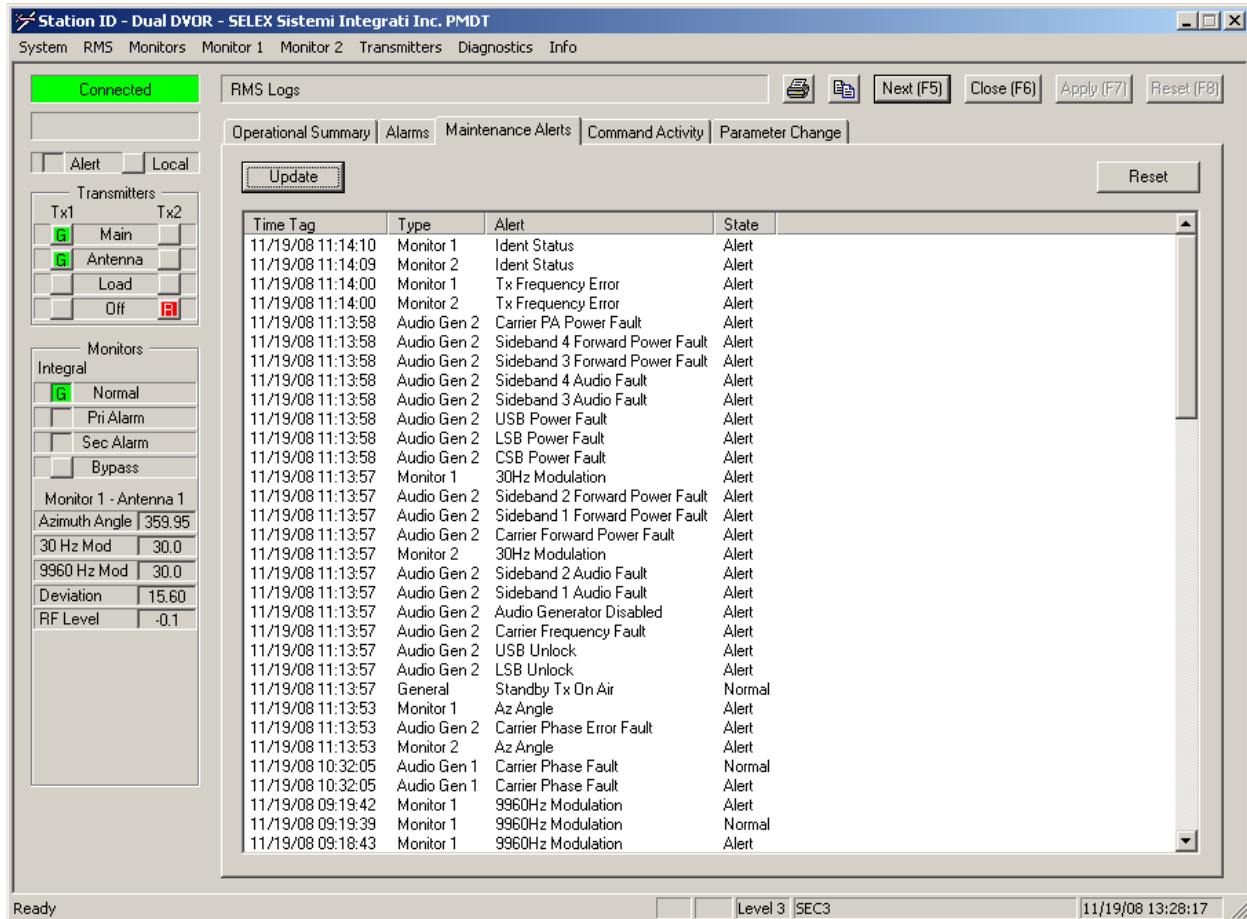


Figure 3-17 RMS Maintenance Alert Log Screen

3.6.7.3.4 Command Activity Screen

The Command Activity Log Screen is shown in Figure 3-18. This screen provides the latest 100 commands issued. When 100 or more commands have been issued, subsequent commands will replace the oldest commands in the log. The Command Activity Log screen specifies the date and time, identifies the operator logged on to the system when the command was issued, and the command that was issued. In addition to the User IDs configured in the Security Screen, the User Name field includes the following names:

Local User	Commands issued through the buttons on the LCU front panel.
GUEST	Commands issued from the default Security Level 1 GUEST account.
RCSU	Commands issued from the Remote Control Status Unit.
Op System	Commands issued from the RMS's Operating System.

The Update button reloads the log file from the RMS and updates the display with any new entries. The Reset button clears the log file in the RMS.

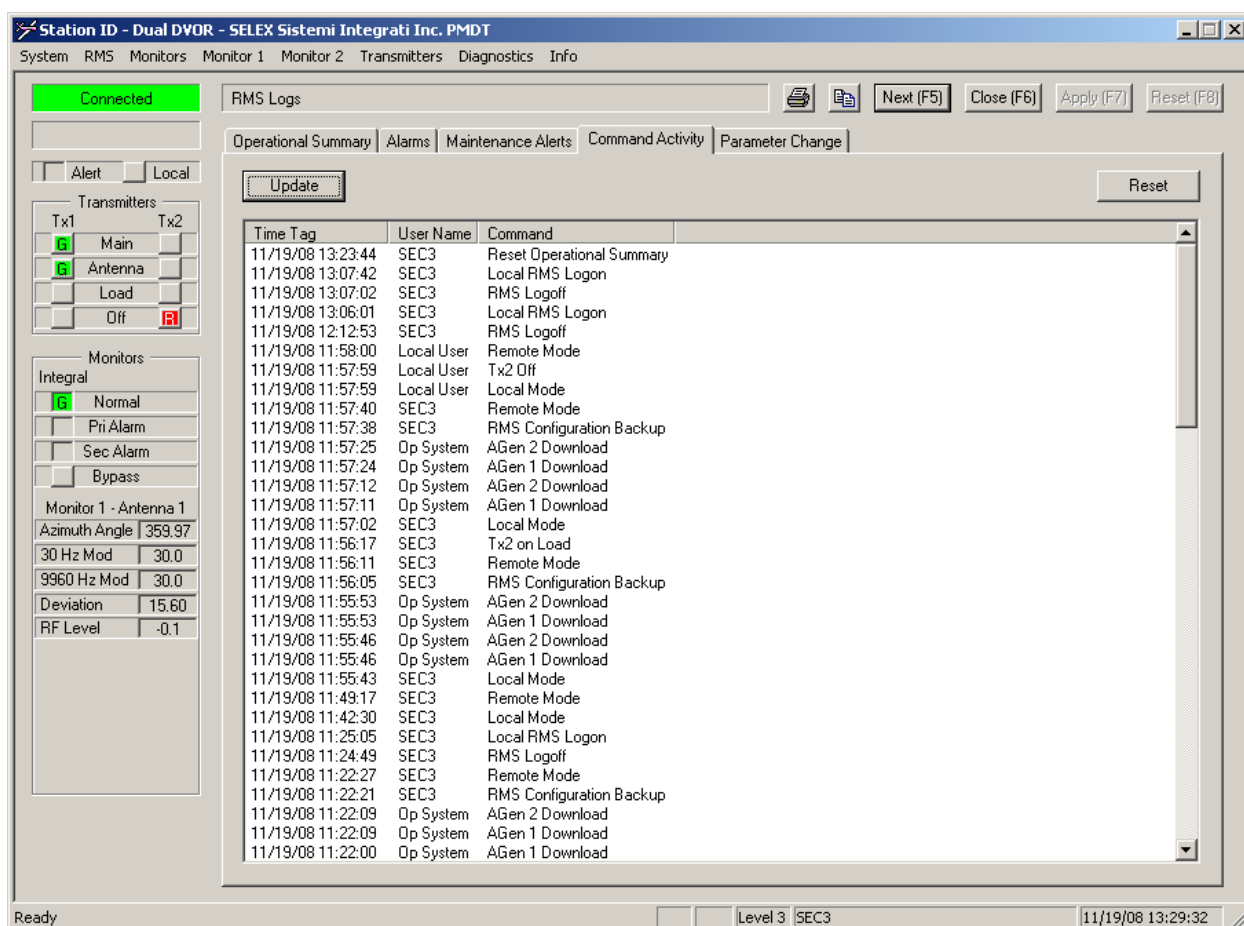


Figure 3-18 RMS Command Activity Log Screen

3.6.7.3.5 Parameter Change Log Screen

The Parameter Change Log Screen is shown in Figure 3-19. This screen provides the latest 100 changes made in the operator parameters. When 100 or more changes have been made, subsequent changes will replace the oldest changes in the log. The Parameter Change screen specifies the date and time, identifies the operator logged on to the system when the change was made, and the file in which the data was changed. The Update button reloads the log file from the RMS and updates the display with any new entries. The Reset button clears the log file in the RMS.

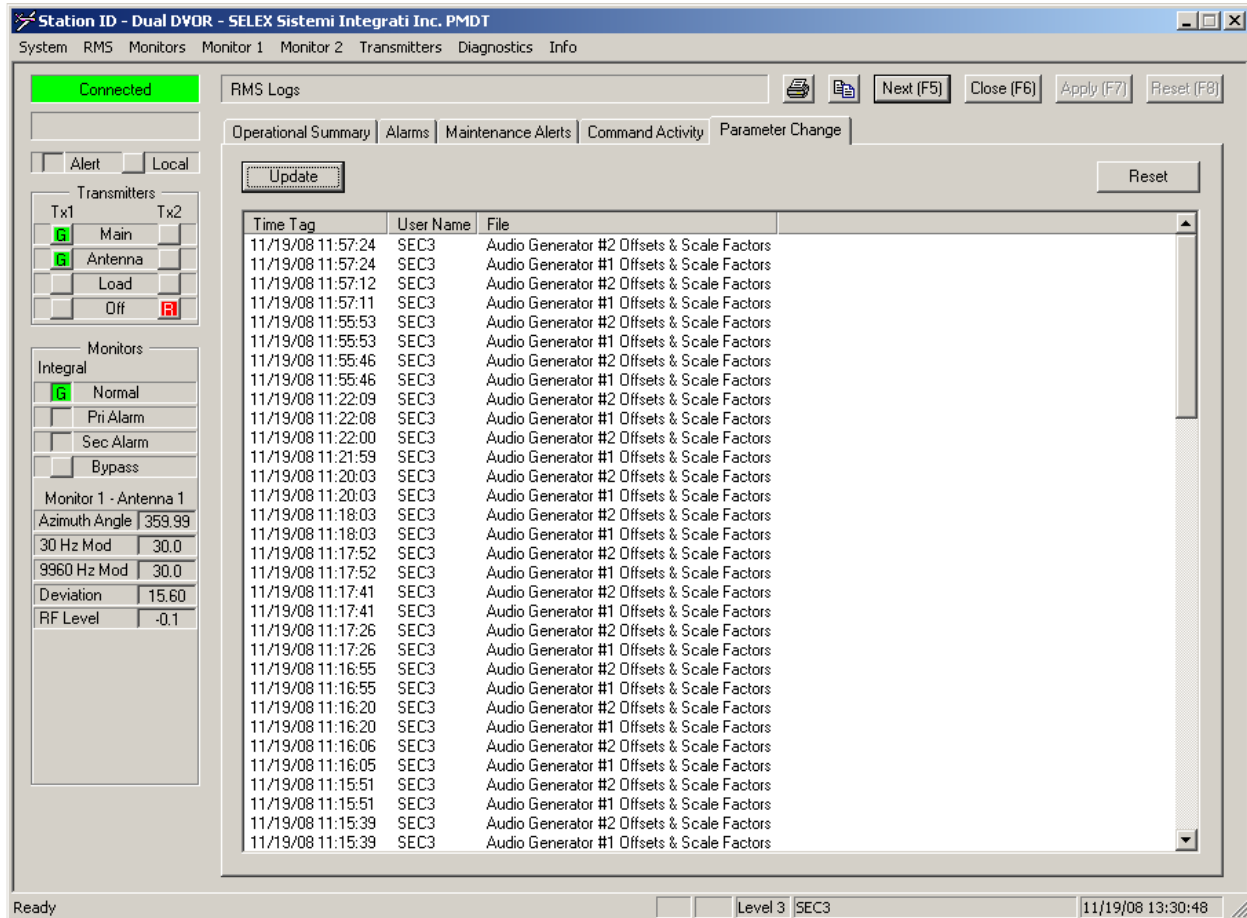


Figure 3-19 RMS Parameter Change Log Screen

3.6.7.4 RMS Configuration Screen

The PMDT contains the following RMS Configuration Screens that are used to define the operating parameters for the RMS.

NOTE

Any changes to the backplane switches must be followed by cycling the DVOR rack power or pressing the Reset on the LCU to make the changes take effect.

Any configuration changes intended to remain after subsequent power cycling or system resetting **MUST** be backed up before cycling/resetting.

To backup the current configuration stored in RAM for non-volatile storage in EEPROM, login to Security Level 3 or higher and select RMS >> Configuration Backup. Press OK at the prompt.

To save the current RMS configuration to a hard drive or other media, select System >> Configuration Save. Select the destination and file name and press Save.

To restore a saved configuration, select System >> Configuration Load, locate the desired configuration file and press Open. When completed, backup the configuration to EEPROM by selecting RMS >> Configuration Backup. Press OK at the prompt.

A hardcopy of the station's configuration can be printed using the System >> Configuration Print menu option.

3.6.7.4.1 General RMS Configuration Screen

The RMS's General Configuration screen is shown in Figure 3-20. This screen allows the operator to configure the general parameters of the VOR system.

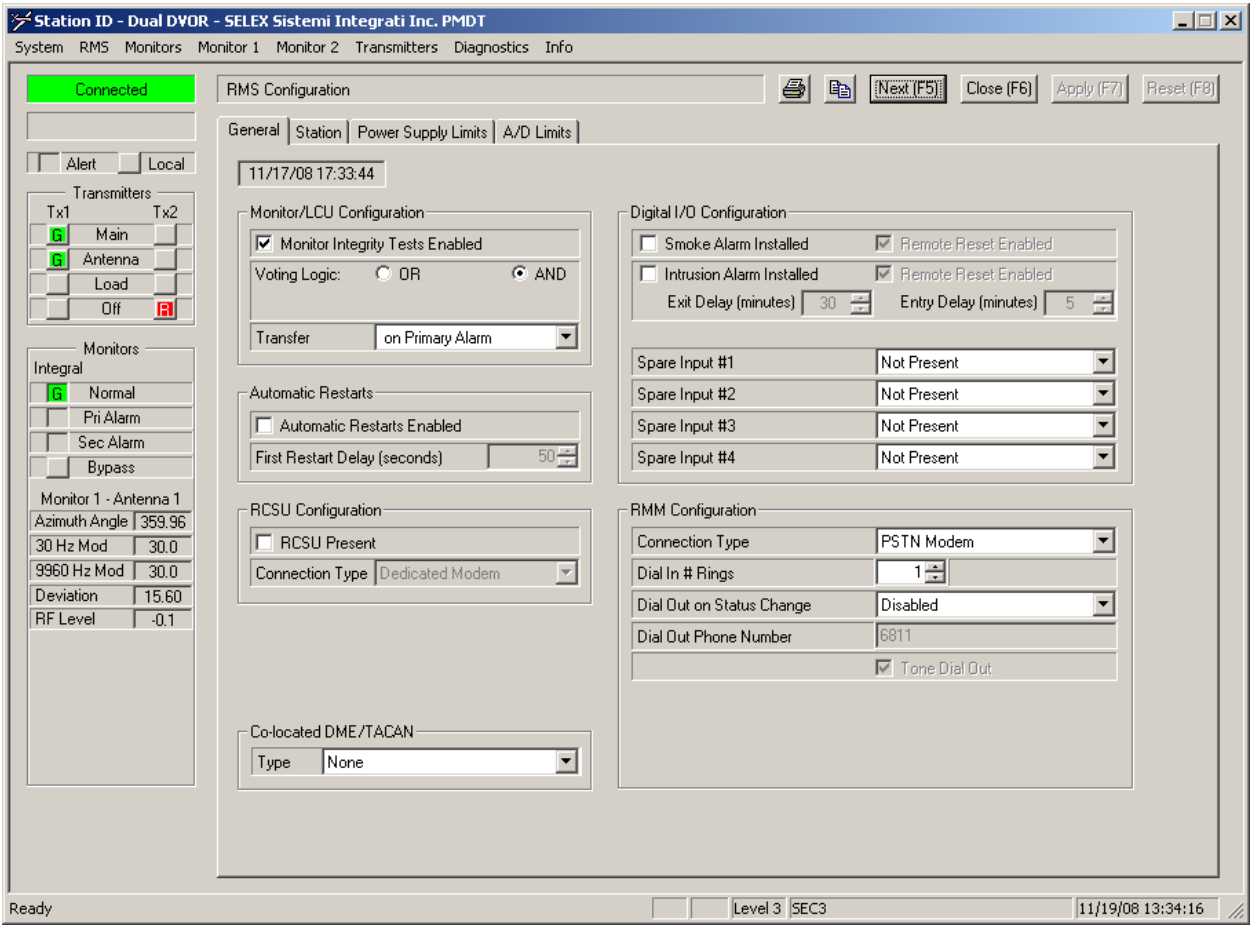


Figure 3-20 RMS General Configuration Screen

The parameters in the General Configuration Screen must be set to correctly correspond to the equipment installation at each site. Refer to the following table for details pertaining to each of the configurable parameters in the General Configuration Screen. Note that some parameters are only applicable to Dual Equipment. In Single Equipment systems, these parameters will not be displayed.

Table 3-3 General Configuration Parameters	
Parameter	Description
Monitor/LCU Configuration	
Monitor Integrity Tests Enabled	Monitor Integrity test is enabled when checked.
Monitor Voting Logic (applies to Dual Monitor/Transmitter systems)	Selects either AND or OR voting logic for multiple monitor systems. When OR voting logic is enabled, the additional option of reverting to AND logic when on Standby is available. This option can be selected to potentially lengthen a system's on-air operational time.
Transfer Logic	Configures a dual system to transfer either on a Primary or Secondary Alarm, or for Best Availability.
Automatic Restarts	
Automatic Restarts Enabled	Both Automatic Restarts (first is adjustable and second fixed) are enabled when the checkbox is checked, and disabled when it is not checked.
First Restart Delay (seconds)	Sets the delay following a shutdown until the system will automatically restart. The system also has an additional 5 minute (fixed) restart delay.
RCSU Configuration	
RCSU Present	When checked, the connection between the RCSU and RMS is enabled.
Connection Type Note: After changing this parameter, the new configuration will not take effect until it has been backed up (RMS >> Config Backup), and the system reset or power-cycled.	Set to "Dedicated Modem" when connecting to the RCSU via the VOR's embedded RCSU Modem. Set to "RF Modem/Fiber" when connecting to the RCSU via the External RCSU Modem port to a serial-based communication link, such as RF Modems, or Fiber Optic converters.
DME Configuration	
DME Type	Enables the optional DME COM link to the specified type of equipment.
Digital I/O Configuration	
Smoke Alarm	Smoke Alarm detection is enabled when checked. Optionally, the smoke alarm can be cleared remotely via the RCSU or PMDT.
Intrusion Alarm	Intrusion Alarm detection is enabled when checked. Optionally, the intrusion alarm can be cleared remotely via the RCSU or PMDT.
Spare #1 Usage	Configures the Spare Input #1 Channel
Spare #2 Usage	Configures the Spare Input #2 Channel
Spare #3 Usage	Configures the Spare Input #3 Channel
Spare #4 Usage	Configures the Spare Input #4 Channel
Modem Configuration	
Connection Type	Selects between Internal Modem or RF external modem
Dial In # Rings	Sets the ring number that the VOR's modem answers incoming calls
Dial Out on Status Change	Allows the VOR to dial out to report a change in status. Either an ASCII text-based message or a SELEX-SI RSMS message can be sent.
Dial Out Phone Number	The phone number to be used for the Dial-out on Status Change feature.
Tone Dial Out	Tone dialing is used to dial out when checked. Pulse dialing is used to dial out when it is not checked.

3.6.7.4.2 Station Configuration Screen

The Station Configuration Screen is shown in Figure 3-21. This screen is used to configure the various system-level parameters for the VOR station: CVOR/DVOR, Dual/Single Transmitter Dual/Single Monitors, Dual Monitor Inputs, and the station’s Transmitter Frequency. The value for each of these settings currently stored in the RMS, Monitors, and Audio Generators is also displayed for reference. Note that any changes under User Configuration must be made while in the “Local” mode and will not take effect until the “Apply” button is pressed. The “Apply” button is “grayed” out until a parameter is changed and then becomes fully visible.

Any discrepancies between the User Configuration, RMS, Monitors, or Audio Generators will be indicated with a red background, and should be corrected by the user. This can be done by verifying the backplane DIP switch settings as detailed below, backing up the configuration (RMS >> Config Backup) followed by a system reset.

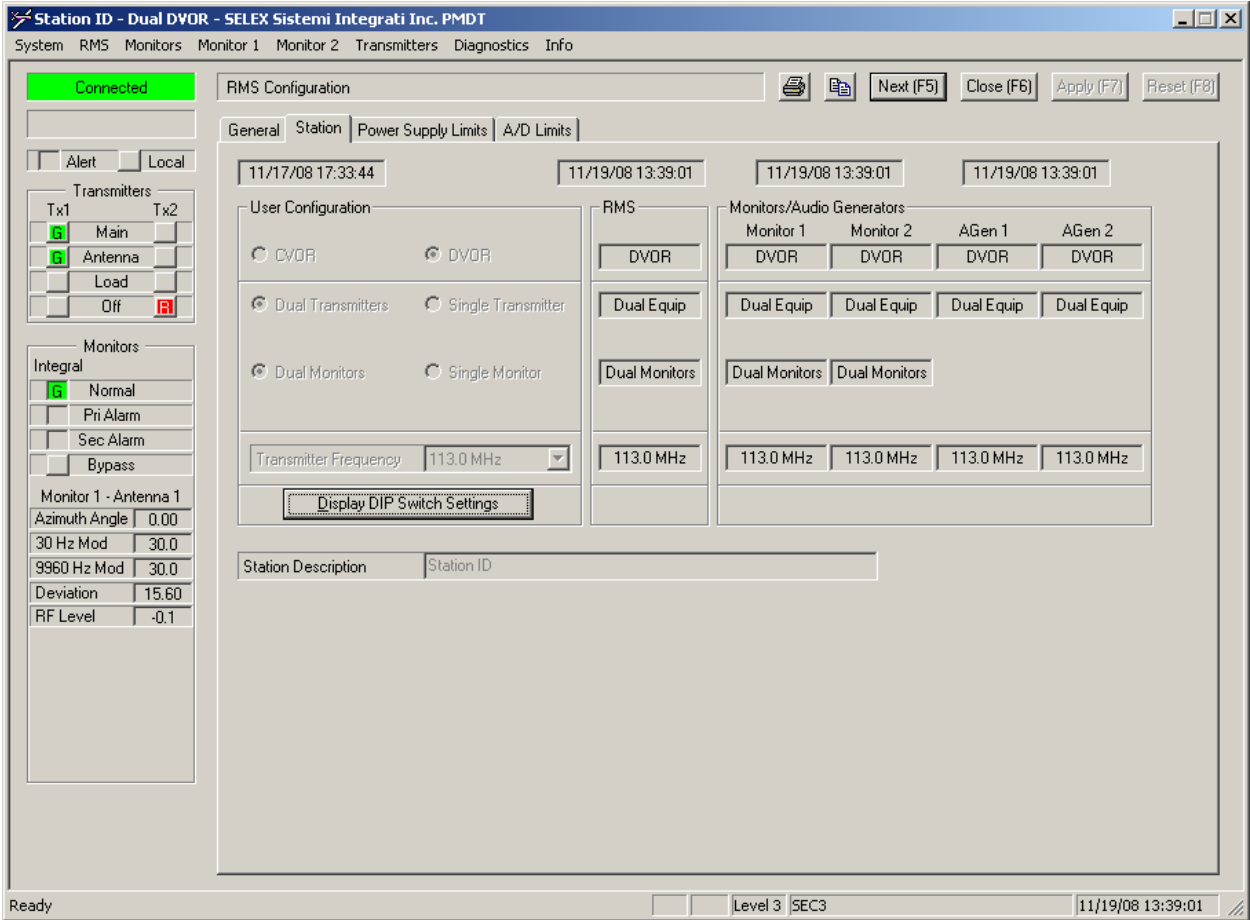


Figure 3-21 Station Configuration Screen

The user should set the User Configuration parameters as required and press “Apply”. Pressing the “Display DIP Switch Settings” button will display the corresponding DIP switch settings for the Backplane DIP switches as shown in Figure 3-22. Review the display. Switches that are not set per the User Configuration are indicated in yellow. These DIP switches should be set according to the displayed information.

Pressing the Update button will refresh the display based on the current DIP switch settings.

Backplane DIP Switches - Required Settings

S3

01	CSEL 0	*
02	CSEL 1	*
03	CSEL 2	*
04	CSEL 3	*
05	CSEL 4	* RF Channel Select
06	CSEL 5	*
07	CSEL 6	*
08	CSEL 7	*

S1

01	SCON 0 - Always Set to On	
02	SCON 1 - Always Set to On	
03	SCON 2 - Dual / ~Single Equipment	
04	SCON 3 - DVOR / ~CVOR	
05	SCON 4 - Always Set to Off	
06	SCON 5 - RMM Read-Only: Disabled / ~Enabled	
07	SCON 6	
08	SCON 7	

S2

01	SCON 8 - RCSU Modem: Embedded / ~External (RF/Fiber)	
02	SCON 9 - RMM Modem: Embedded / ~External	
03	SCON 10 - Power Supplies: Normal / ~Redundant	
04	SCON 11	
05	SCON 12	
06	SCON 13	
07	SCON 14	
08	SCON 15	

OK

Read Switches

Notes:

Switches indicated as or are not in the proper position. Correct this situation, and then press Update to refresh this display.

For switches indicated as refer to Section 9 in the Technical Manual.

For rocker-type DIP switches, the side indicated with should be depressed.

Figure 3-22 Backplane DIP Switches Screen

3.6.7.4.3 Power Supply Limits Configuration Screen

The Power Supply Limits screen is shown in [Figure 3-23](#). This screen is used to configure the upper and lower alarm limits and enable limit checking for the various system power supply voltages and currents. The checkboxes are used to enable the corresponding parameter's Maintenance Alert. If the checkbox is checked, a Maintenance Alert will be generated when the parameter is out of the specified limits.

Station ID - Dual DVOR - SELEX Sistemi Integrati Inc. PMDT

System RMS Monitors Monitor 1 Monitor 2 Transmitters Diagnostics Info

Connected RMS Configuration [Next (F5)] [Close (F6)] [Apply (F7)] [Reset (F8)]

General Station **Power Supply Limits** A/D Limits

11/10/08 10:33:04

Alert Local

Transmitters

Tx1	Tx2
☒ Main	☐
☒ Antenna	☐
☐ Load	☐
☐ Off	☒

Monitors

Integral

☒ Normal

☐ Pri Alarm

☐ Sec Alarm

☐ Bypass

Monitor 1 - Antenna 1

Azimuth Angle	359.97
30 Hz Mod	30.0
9960 Hz Mod	30.0
Deviation	15.60
RF Level	-0.1

Volts

	Low	Pre-Low	Pre-High	High
☐ +3.3 VDC	3.14	3.14	3.46	3.46
☐ +5 VDC	4.75	4.75	5.25	5.25
☐ +12 VDC Analog	10.80	10.80	13.20	13.20
☐ -12 VDC Analog	-13.20	-13.20	-10.80	-10.80
☐ +12 VDC Digital	10.80	10.80	13.20	13.20
☐ -12 VDC Digital	-13.20	-13.20	-10.80	-10.80
☐ +15 VDC	13.50	13.50	16.50	16.50
☐ -15 VDC	-16.50	-16.50	-13.50	-13.50
☐ +24 VDC	21.6	21.6	26.4	26.4

Volts

	Low	Pre-Low	Pre-High	High
☐ AC Input	98.0	98.0	132.0	132.0
☐ OB Light	98.0	98.0	132.0	132.0
☐ Tx 1 48 V PS	46.6	46.6	54.4	54.4
☐ Tx 2 48 V PS	46.6	46.6	54.4	54.4
☐ Battery 1	42.0	42.0	60.0	60.0
☐ Battery 2	42.0	42.0	60.0	60.0

Amps

	Low	Pre-Low	Pre-High	High
☐ 1.0	1.0	1.0	7.0	7.0
☐ 0.0	0.0	0.0	20.0	20.0
☐ 0.5	0.5	0.5	15.0	15.0
☐ -6.0	-6.0	-6.0	10.0	10.0

Ready Level 3 SEC3 11/19/08 13:41:51

Figure 3-23 Power Supply Limits Configuration Screen

3.6.7.4.4 A/D Limits Configuration Screen

The A/D Limits Configuraiton Screen is shown in Figure 3-24 . This screen is used to configure the upper and lower alarm limits and enable limit checking for the Spare Analog voltages and system temperatures. The checkboxes are used to enable the corresponding parameter's Maintenance Alert. If the checkbox is checked, a Maintenance Alert will be generated when the parameter is out of the specified limits.

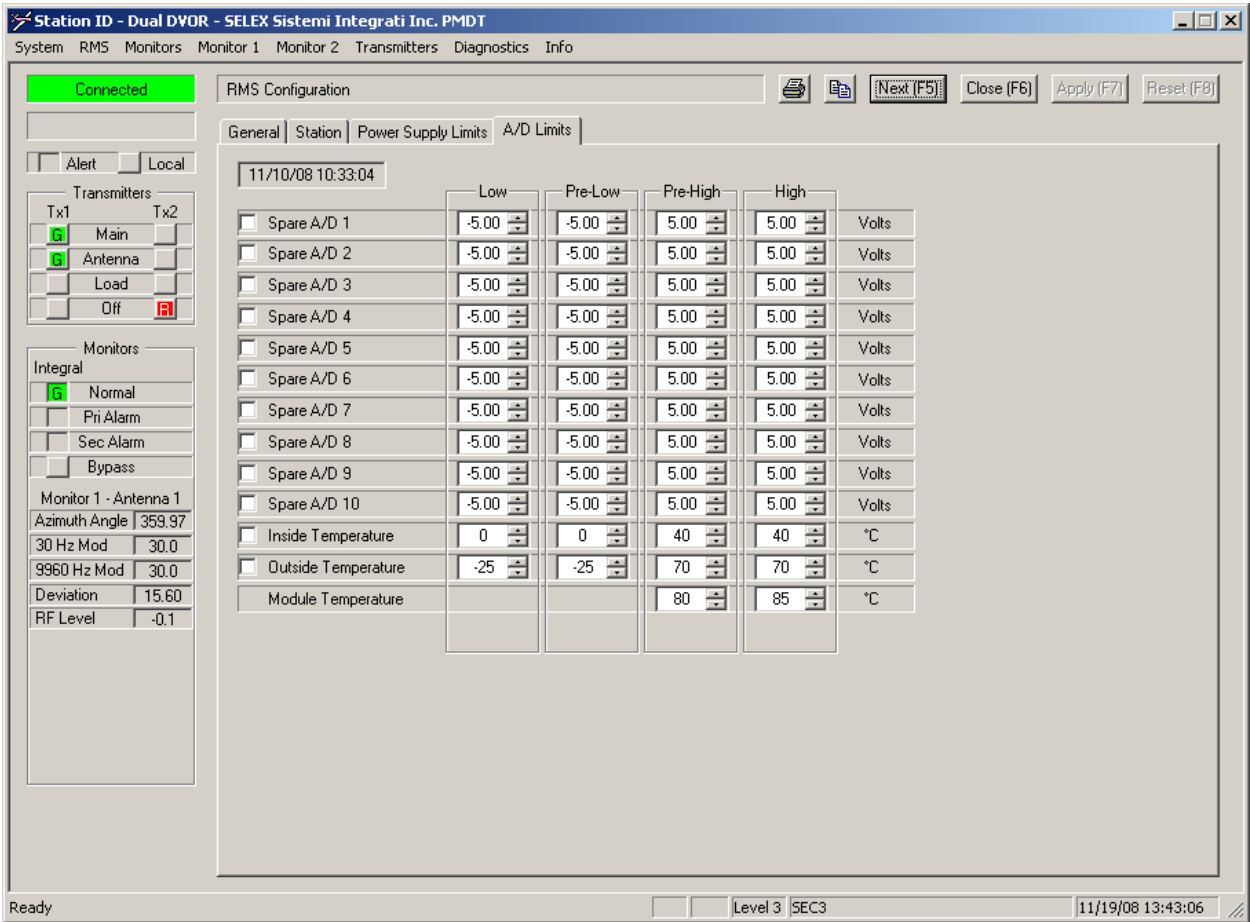


Figure 3-24 A/D Limits Configuration Screen

3.6.7.4.5 Security Codes Configuration Screen

The Security Codes screen is shown in Figure 3-25. This screen is used to configure the security access credentials for each user, including User ID, Password, and Security Level. This User ID/Password information is encrypted and stored in the non-volatile RAM (NVRAM) on the RMS CCA. This screen is only available to the Level 4 user.

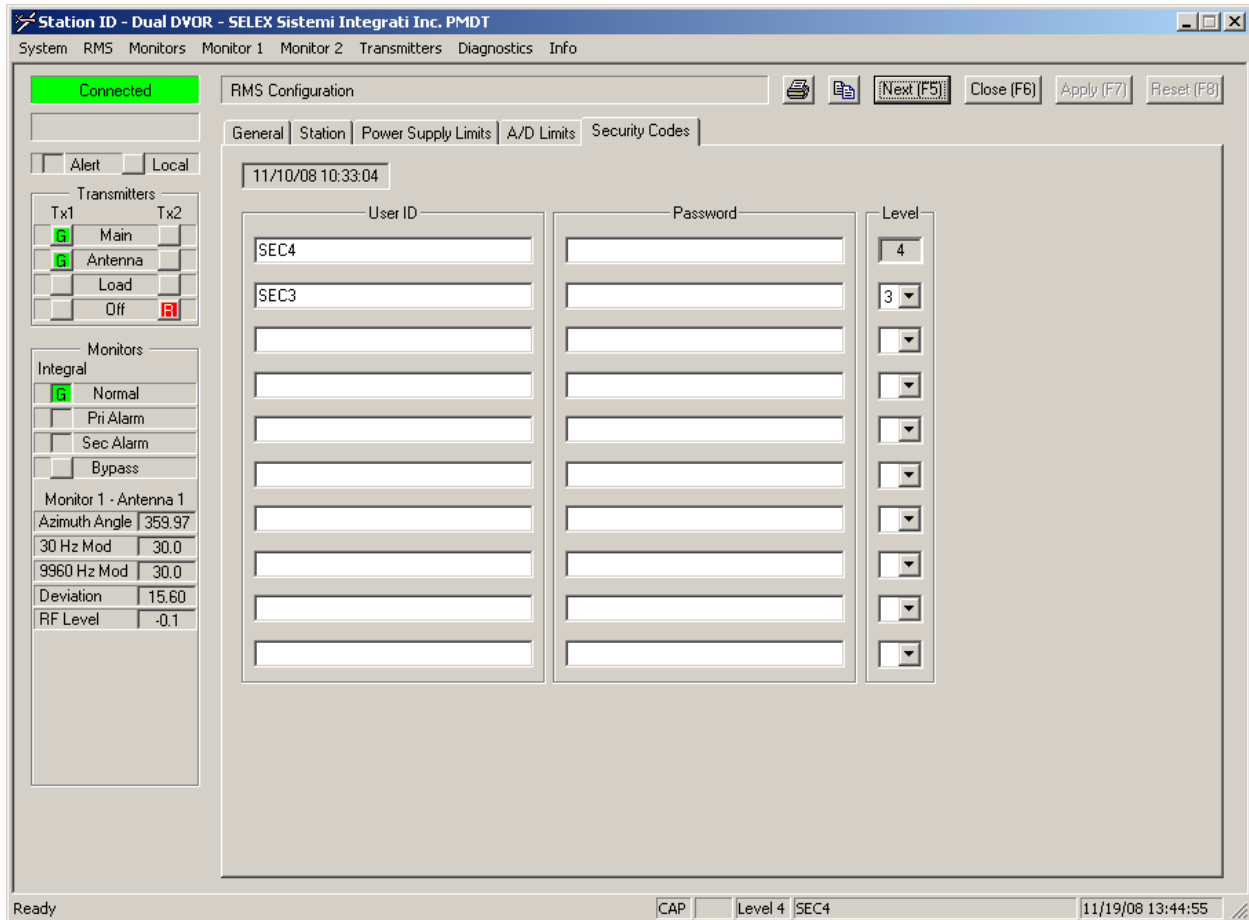


Figure 3-25 Security Codes Configuration Screen

3.6.7.4.5.1 User Account Maintenance

As part of initial configuration, several user accounts should be setup, corresponding to the access levels required. User account maintenance can only be done through a direct connection (i.e. not via a remote modem) in the LOCAL mode, from within Security Level 4, with the exception of changing the current user's password. All users can change their own passwords, when connected directly and the system is in Local Mode, through the RMS >> Commands >> Change Password menu option. Refer to Figure 3-25 for the Security Codes Configuration Screen.

3.6.7.4.5.2 Add a User Account

1. Log on to Security Level 4 and select the RMS >> Configuration >> Security Codes screen.
2. Click on any empty User ID field.
3. Enter the desired User ID. Note that the User ID must be 4 to 32 characters in length, is case-sensitive, and can contain any alphanumeric characters.
4. Press TAB to move to the associated Password field.
5. Enter the desired Password. Asterisks will hide the password on the display. Note that the password must be 4 to 32 characters in length, is case-sensitive, and can contain any alphanumeric characters.
6. Select the desired Security Level for this user.
7. Repeat these steps for any additional users.

8. When all users have been configured, press the Apply button to save the new User Account data. This will clear the asterisks in the password field to hide the length of the password. Note that any changes under User Configuration must be made while in the “Local” mode and not take affect until the “Apply” button is pressed. The “Apply” button is grayed out until a parameter is changed and then becomes fully visible
9. To store the new account information in the RMS’s NVRAM, select RMS >> Config Backup. If this is not done, the user data will revert to the values stored in the NVRAM following the next system reset or power-cycle.

3.6.7.4.5.3 Change a User’s Password

All User account information, including passwords, is accessible from Security Level 4 as follows:

1. Log on to Security Level 4 and select the RMS >> Configuration >> Security Codes screen.
2. Select the Password field associated with the desired User ID.
3. Enter the desired Password, which is case-sensitive. Asterisks will hide the password on the display. Note that the password must be 4 to 32 characters in length, and can contain any alphanumeric characters.
4. Press the Apply button to save the new User Account data. This will clear the asterisks in the password field. Changes must be made while in the “Local” mode and not take affect until the “Apply” button is pressed. The “Apply” button is grayed out until a parameter is changed and then becomes fully visible.
5. To store the new account information in the RMS’s NVRAM, select RMS >> Config Backup. If this is not done, the user data will revert to the values stored in the NVRAM following the next system reset or power-cycle.

From other Security Levels, only the current user’s password can be changed. This is done as detailed below:

1. Log on directly (not via a Modem connection) and press the Local Mode button on the LCU.
2. Select the RMS >> Commands >> Change Password menu item.
3. Enter the Current Password and press TAB to move to the next field.
4. Enter the New Password, which is case-sensitive. Asterisks will hide the password on the display. Note that the password must be 4 to 32 characters in length, and can contain any alphanumeric characters. Press TAB to move to the next field.
5. Re-enter the New Password and press OK to save the new password.
6. A message box will be displayed, indicating that the password has been changed. Press OK to clear this message.

3.6.7.4.5.4 Delete a User’s Account

1. Log on to Security Level 4 and select the RMS >> Configuration >> Security Codes screen.
2. Select the desired User ID field.
3. Delete the User ID in this field, leaving it blank.
4. Press the Apply button to save the new User Account data. Changes must be made while in the “Local” mode and not take affect until the “Apply” button is pressed. The “Apply” button is grayed out until a parameter is changed and then becomes fully visible
5. To store the new account information in the RMS’s NVRAM, select RMS >> Config Backup. If this is not done, the user data will revert to the values stored in the NVRAM following the next system reset or power-cycle.

Model 1150A DVOR

3.6.7.5 RMS Commands

The RMS Commands menu, shown in Figure 3-26 through Figure 3-30, provides system level controls for setting the time and date of the VOR station to the PMDT PC's current settings, changing the current user's password, setting the system's Fan Control, setting the level of any of the Spare Digital Outputs, controlling the BCPs, resetting the Intrusion and Smoke Detectors, resetting the RMS hardware, and basic control of a co-located 1118/1119 DME if so equipped.

Refer to Figure 3-26. Note that if the VOR is connected to an RCSU, the Set Time and Date command will not be available, since the RCSU updates the current time to all of its associated nav aids to its system clock. If the displayed time is incorrect, set the correct Time and Date at the RCSU itself.

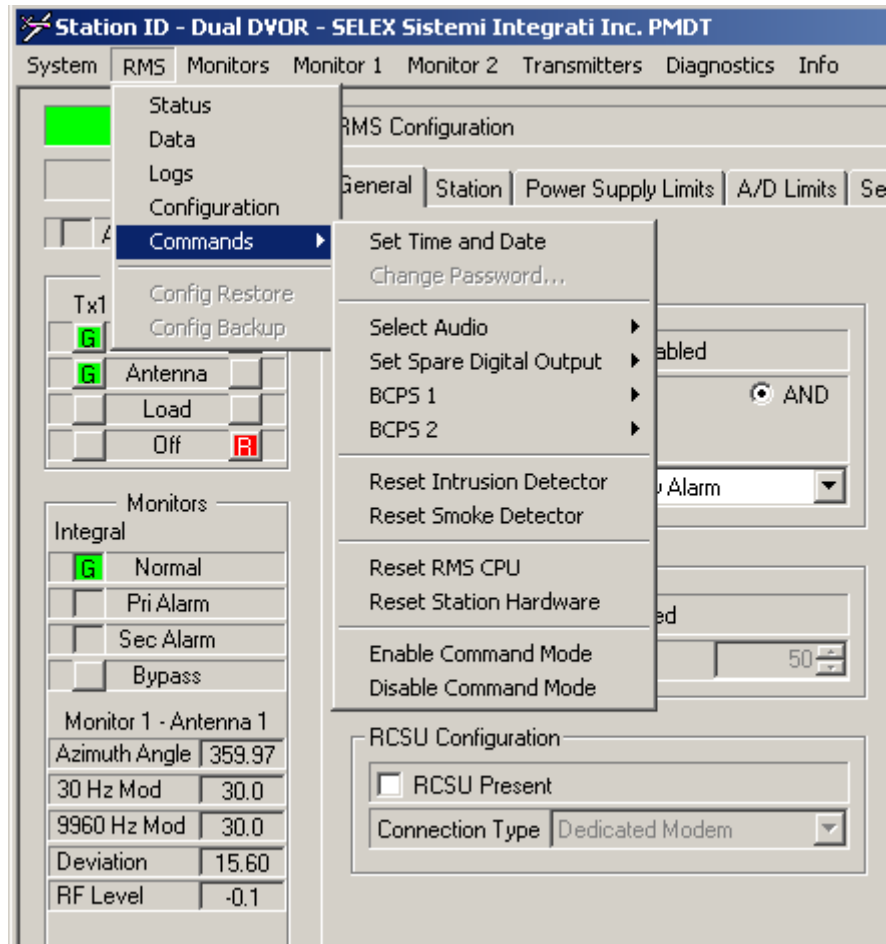


Figure 3-26 RMS Commands

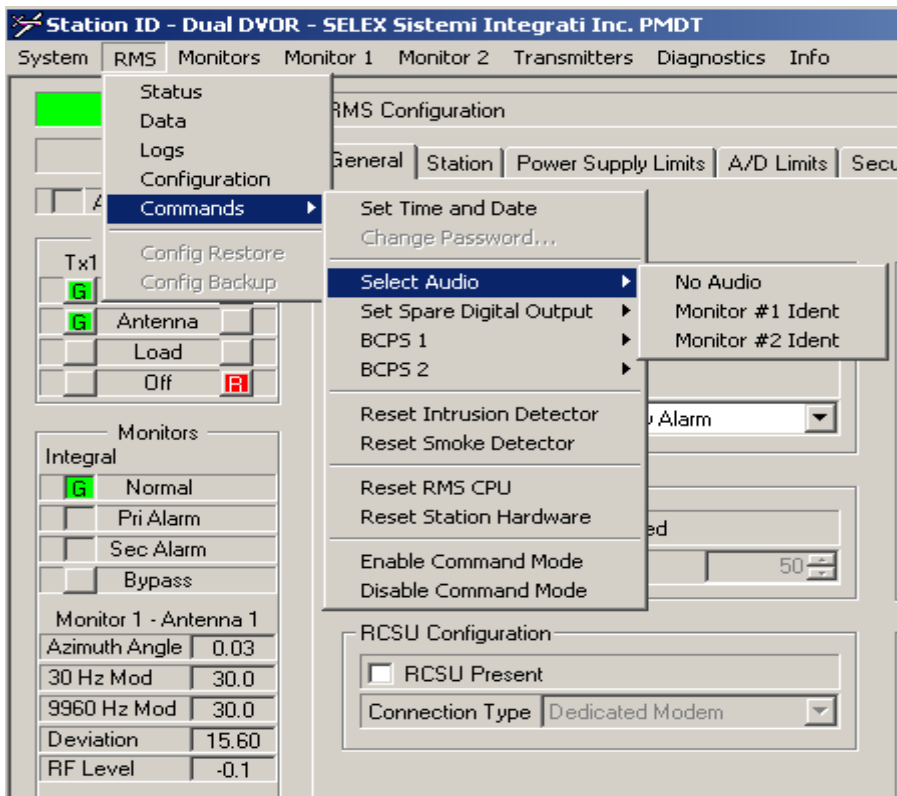


Figure 3-27 RMS Commands – Selection of Digital Output Level

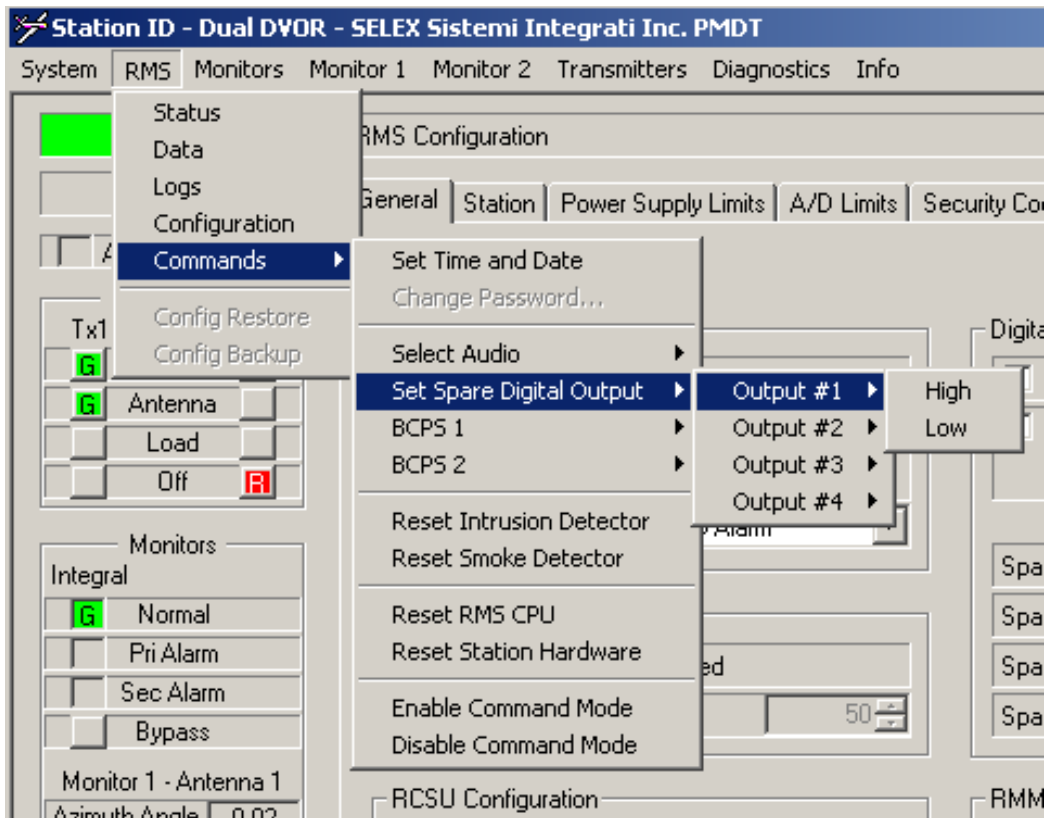


Figure 3-28 RMS Commands – Selection of Digital Output Level

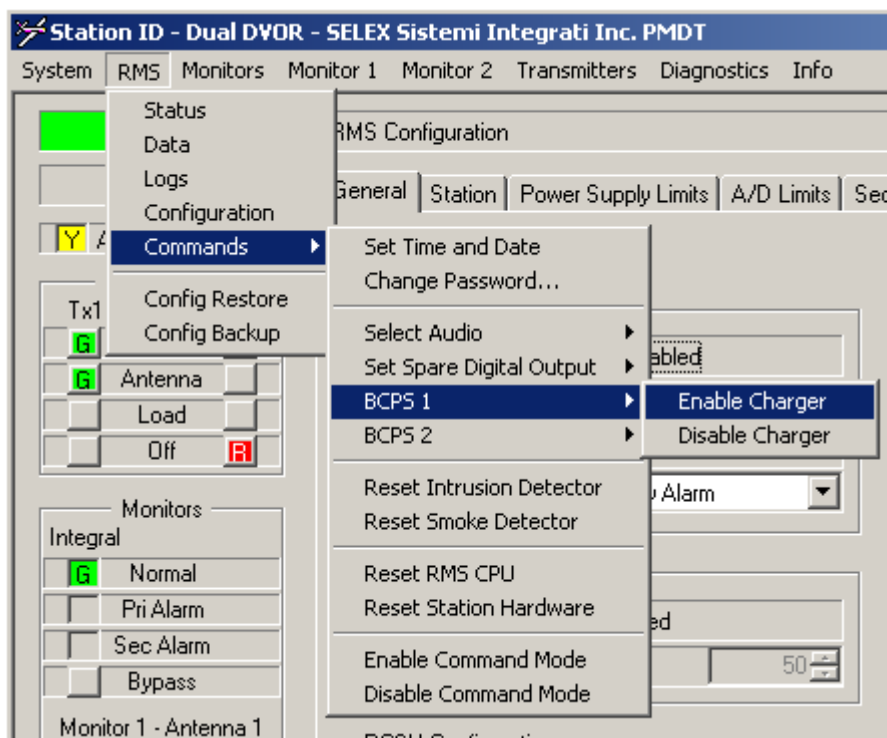


Figure 3-29 RMS Commands - BCPS Charger Enable and Disable

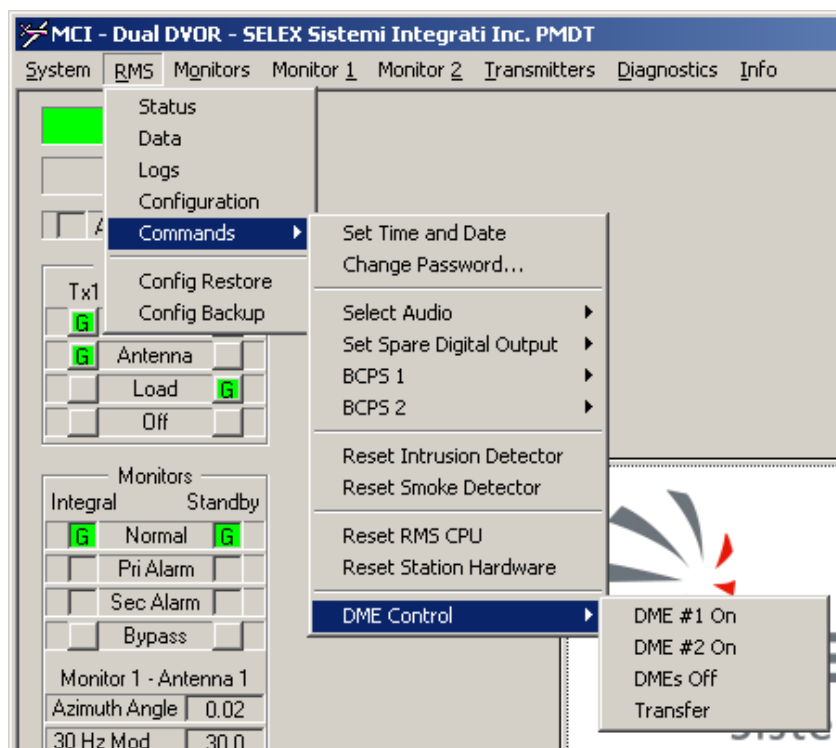


Figure 3-30 RMS Commands - DME Controls

The DME Commands sub-menu of the RMS Commands menu shown in [Figure 3-30](#) is used for basic control of a co-located Fernau DME. It is only available if the DME is configured present in the RMS >> Configuration >> General screen.

3.6.8 Monitor Screens

3.6.8.1 All Monitor Screens

The following screens provide status, data, and controls applicable to both monitors.

3.6.8.1.1 Monitors Data Screens

3.6.8.1.1.1 Integral Monitor Data Screen

The Integral Monitor screen is shown in Figure 3-31. This screen displays the current integral monitor parameters for Monitor 1 and Monitor 2. A green background for a parameter indicates that the parameter falls within the Pre-alarm and Alarm limits. A yellow background indicates that the parameter falls outside of the pre-alarm limits but is still within the integrity alarm limits. A red background indicates that the parameter falls outside of the alarm limits.

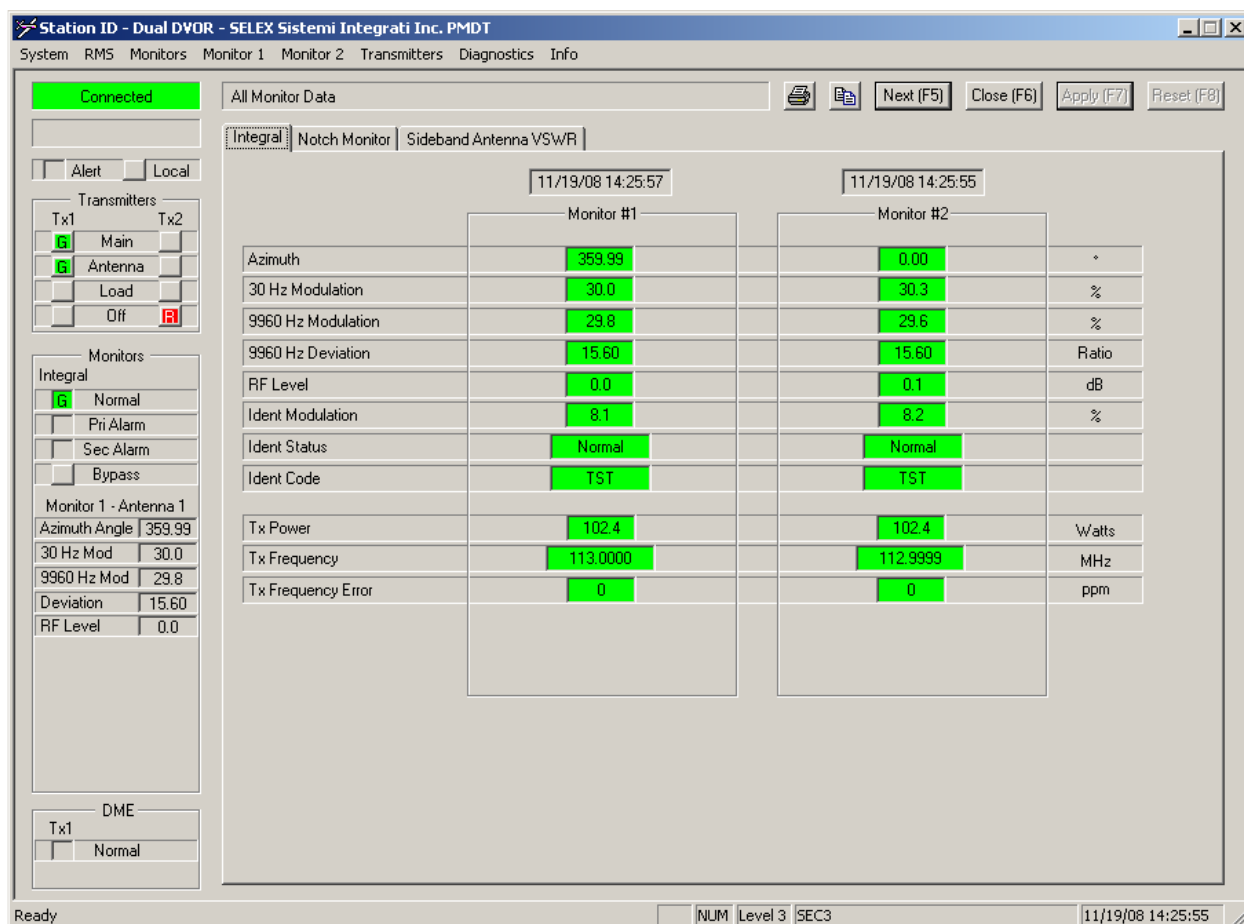


Figure 3-31 Integral Monitor 1 & 2 Data

Model 1150A DVOR

3.6.8.1.1.2 Notch Monitor Data Screen

The Notch Monitor Screen is shown in Figure 3-32. This screen displays the Notch Monitor data from the associated Monitor. The monitor measures the signal from the Field Monitor for “notches” in the detected signal. A notch indicates a fault in one or more transmitting antennas, feed cables or commutator switch channels. When a failure occurs in one of these channels there is a lack of signal and therefore a notch in the detected signal pattern. The 1150A DVOR is a double sideband configuration and therefore there are four sideband antennas on at any one time. Therefore the notch will not fall to zero but since three other antennas are contributing to the signal only a reduction in signal can be expected.

The Record baseline button is used when the technician is confident that the DVOR is operating properly, such as following a flight inspection of the facility. When the Record Baseline button is pressed, the current data is copied into memory as the “Baseline” Data and then used as the reference. If the Sideband power is varied, then a new baseline will be required. When the measured signal differs from the Baseline by more than the Notch Monitor tolerance set in the Monitor Alarm Limits screen, the alarm (red) or alert (yellow) indication is generated, depending on if the Notch Monitor is configured as a Primary or Secondary Alarm.

The tolerance for notch monitoring should be set to approximately 20% in the Monitor Alarm Limit screen, but the technician can adjust this tolerance as needed for more or less sensitivity. Note that when one antenna fails there will typically be an out-of-tolerance indication for one to four of the possible radiating antennas. When an out of tolerance condition exists, the Sideband VSWR data screen should be reviewed as well. If there is an indication of Sideband VSWR alarm, investigate the VSWR alarm indication first.

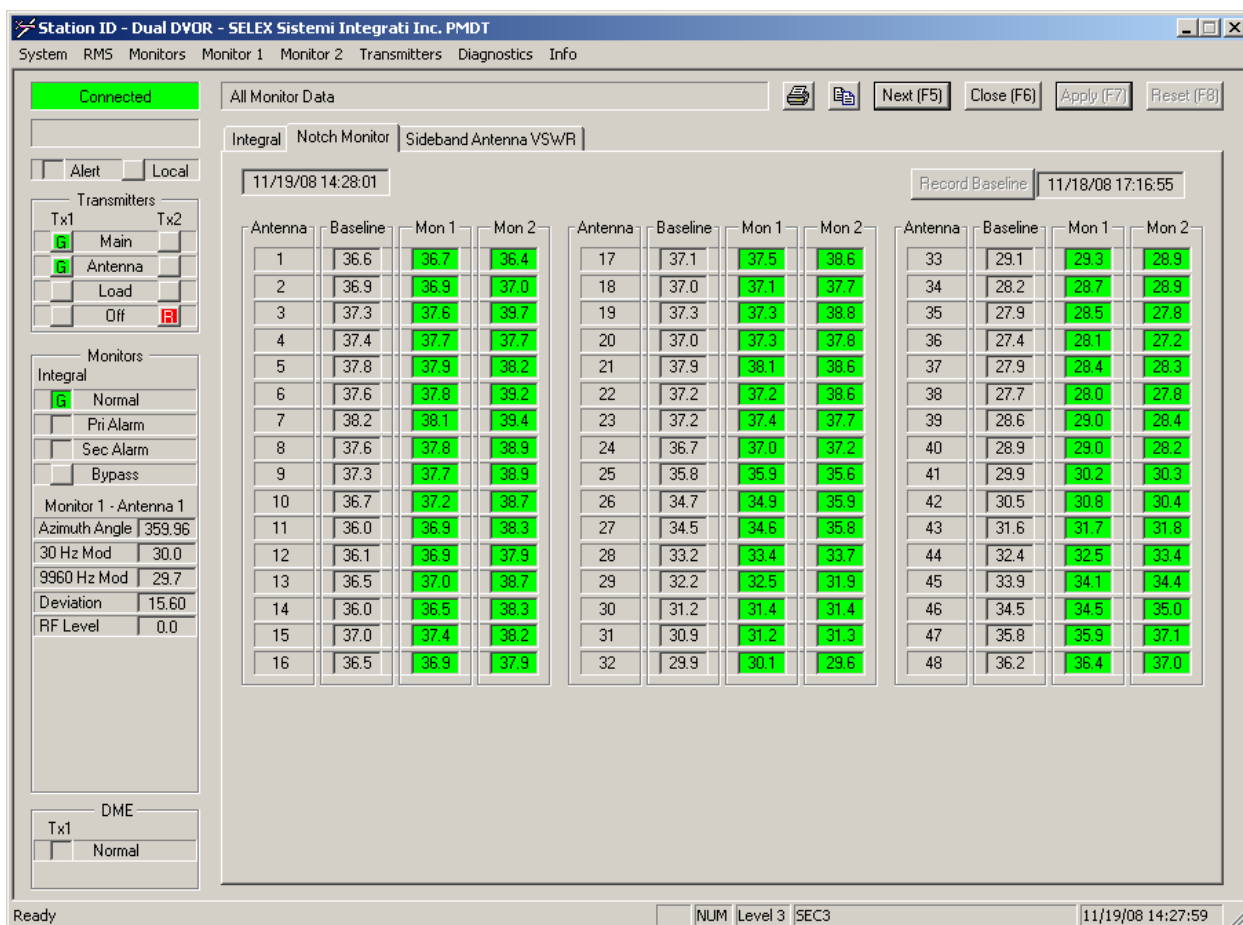


Figure 3-32 Notch Monitor 1 & 2 Data

3.6.8.1.1.3 Sideband Antenna VSWR Screen

The Sideband Antenna VSWR screen is shown in Figure 3-33. This screen displays the current Sideband Antenna VSWR data for the associated monitor. Note that Sideband VSWR Data is only displayed for the monitor associated with the on-air transmitter.

When the measured signal exceeds the Sideband Antenna VSWR tolerance set in the Monitor Alarm Limits screen, the alarm (red) or alert (yellow) indication is generated, depending on if the Sideband Antenna VSWR is configured as a Primary or Secondary Alarm. If configured as a Primary Alarm, and the number of antennas in alarm exceeds the “Number of Antennas in Alarm” then the DVOR will shut down after the alarm delay expires.

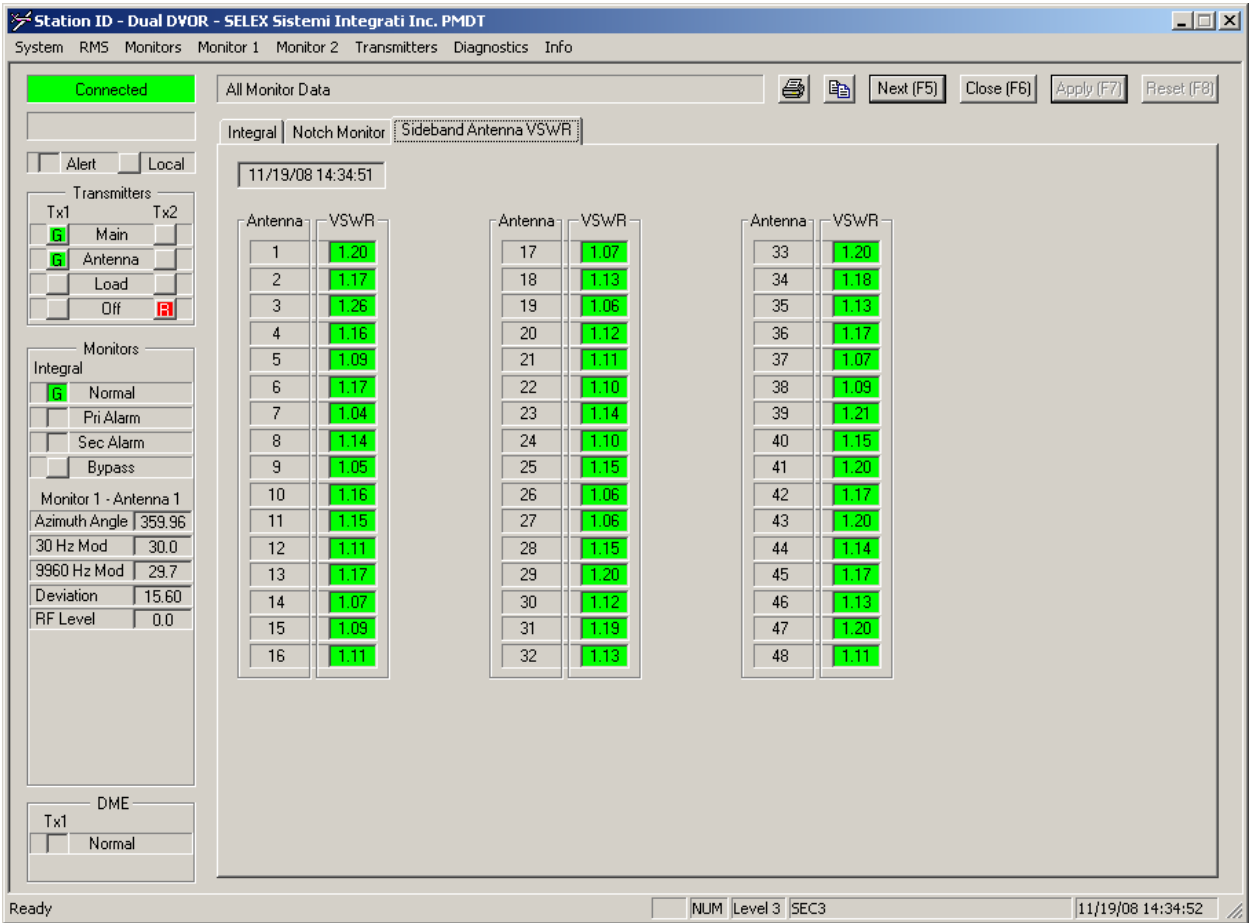


Figure 3-33 Sideband Antenna VSWR Data Screen

3.6.8.1.2 Monitor Configuration Screens

The PMDT contains the following Monitor Configuration Screens that are used to configure the VOR's Monitors. These screens and their contents are described below.

3.6.8.1.2.1 General Configuration Screen

The General Configuration screen is shown in [Figure 3-34](#). This screen is used to configure the general operation of the VOR's Monitors. It contains controls used to enable the Executive Alarm for various monitored parameters. The user can select how each of the Executive parameters is classified, either as Primary Alarm or Secondary Alarm.

When the LCU's Transfer Logic is set for Transfer on Primary/Secondary Alarm, any out of tolerance condition of a Primary or Secondary Parameter will cause the system to be shutdown. Setting the LCU's Transfer Logic to "Best Availability" allows the LCU to keep the system operating in the event of only a Secondary Alarm.

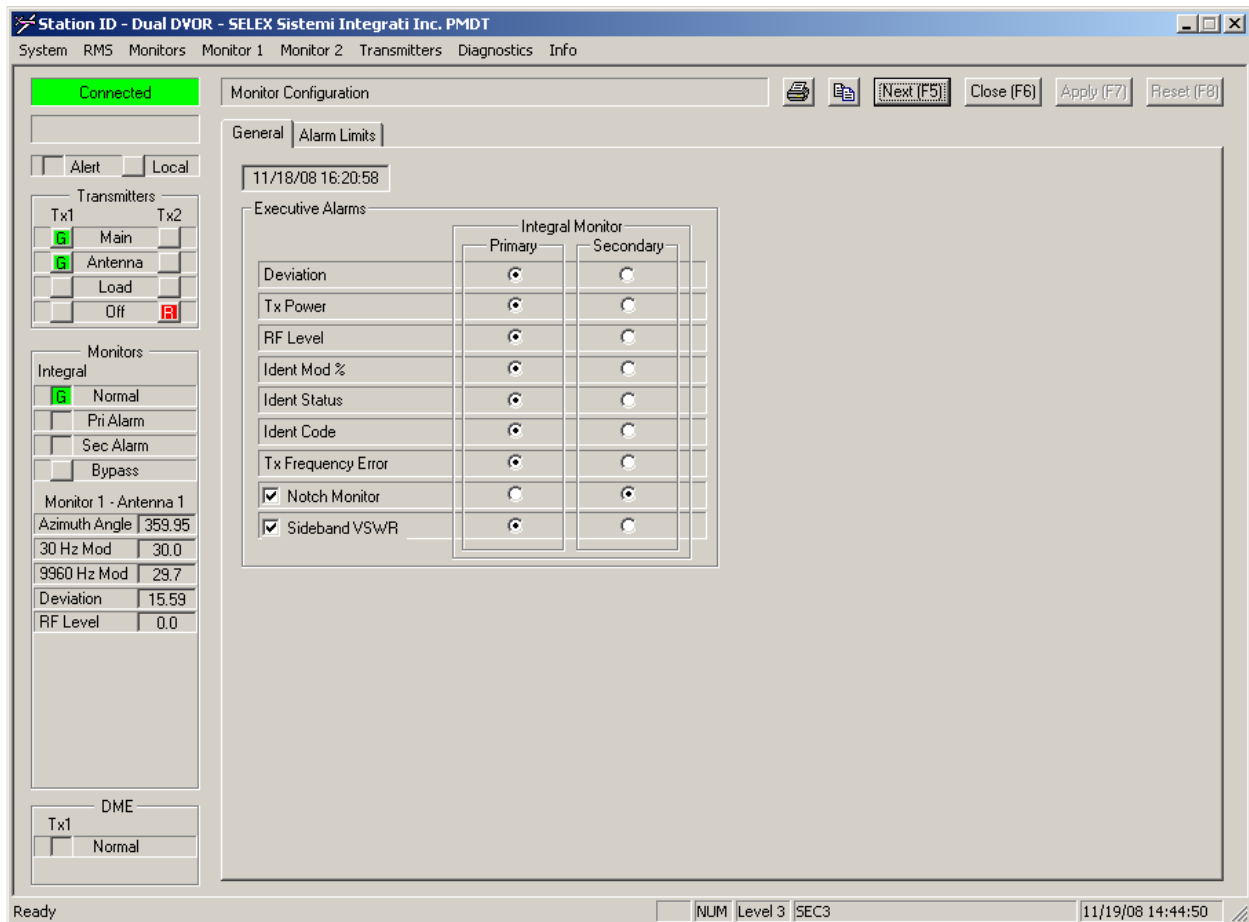


Figure 3-34 General Monitor Configuration

3.6.8.1.2.2 Monitor Alarm Limit Configuration Screen

The Monitor Alarm Limit Configuration screen is shown in Figure 3-35. This screen is used to configure the operation of the Monitors. It contains the Shutdown Delay, the Ident Delays, and the Alarm and Pre-Alarm Limits, as well as the desired Nominal values for all of the monitored parameters. The Azimuth Angle settings are separated for Monitor 1 and Monitor 2 to allow for two different field monitor positions. All other alarm parameters have common limits. The Input attenuation settings allow adjustment of the level from the field monitor antenna to compensate for line los and distance to the antenna. These attenuators are adjusted so that the RF level reading is nearly 0 dB as read on the monitors.

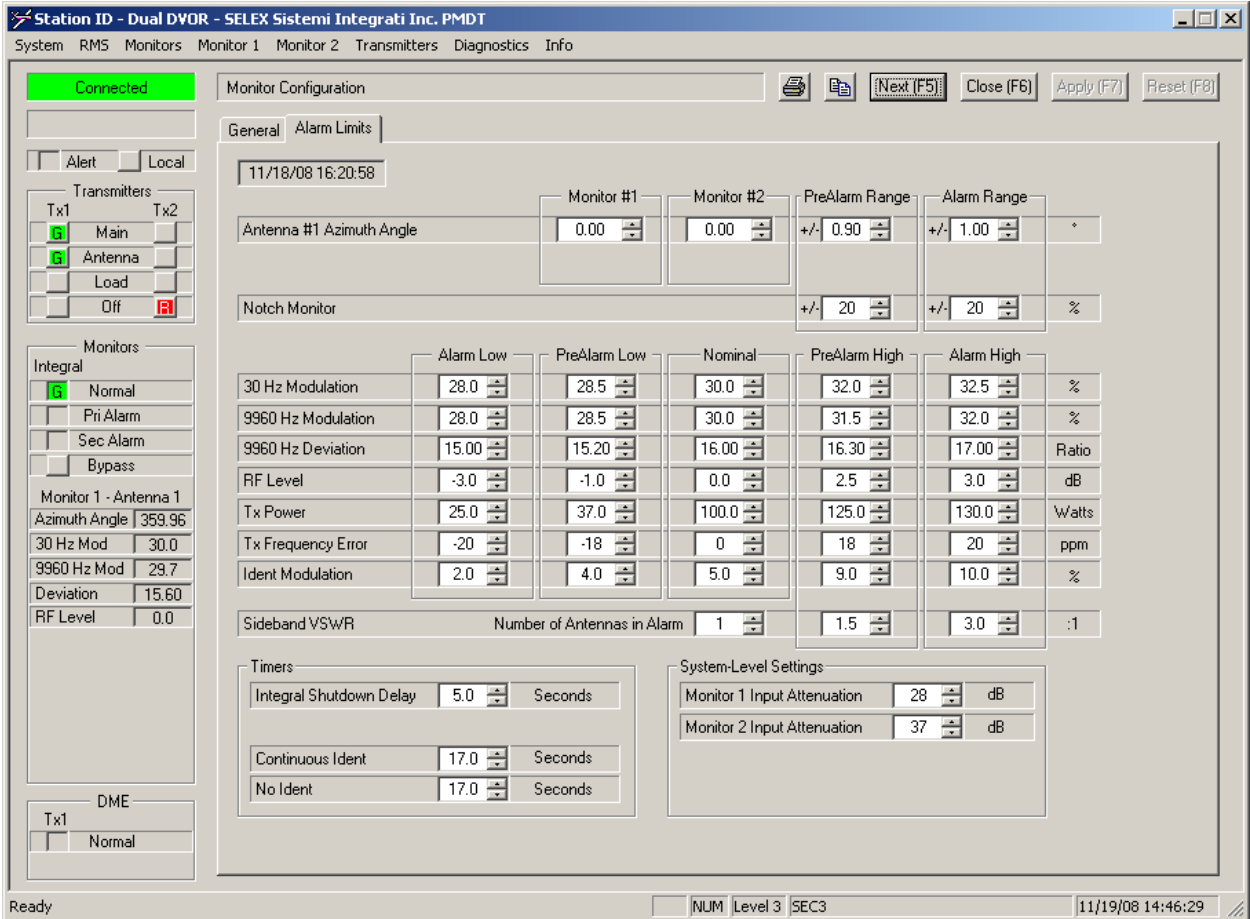


Figure 3-35 Monitor Alarm Limits

3.6.8.1.3 Monitor Commands

The Monitor Command menu is shown in Figure 3-36. The Monitors can be bypassed using the corresponding command under the Monitors >> Commands menu. Alternatively, the bypass button on the sidebar and LCU can be used.

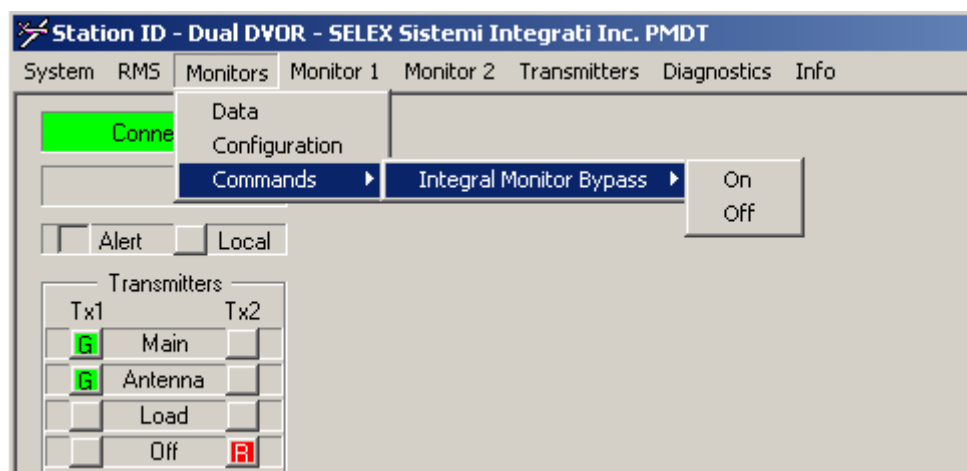


Figure 3-36 Monitor Commands

3.6.8.2 Monitor 1 & 2 Screens

The PMDT contains a set of screens for each of the two Monitor CCAs in the VOR. Only the screens for Monitor 1 are discussed in this section; those for Monitor 2 in a Dual VOR are identical.

3.6.8.2.1 Monitor Data Screens

The PMDT contains several Monitor Data Screens that are used to view the current status of the monitored parameters. The screens and their contents are described below.

3.6.8.2.1.1 Integral Monitor Data Screen

The Integral Monitor Data screen is shown in Figure 3-37. This screen displays the low and high alarm limits and pre-alarm limits with current Integral Monitor values for the selected monitor. A green background for a parameter indicates that the parameter falls within the Prealarm and Alarm limits. A yellow background indicates that the parameter falls outside of the Prealarm limits but is still within the Alarm limits. A red background indicates that the parameter falls outside of the Alarm limits.

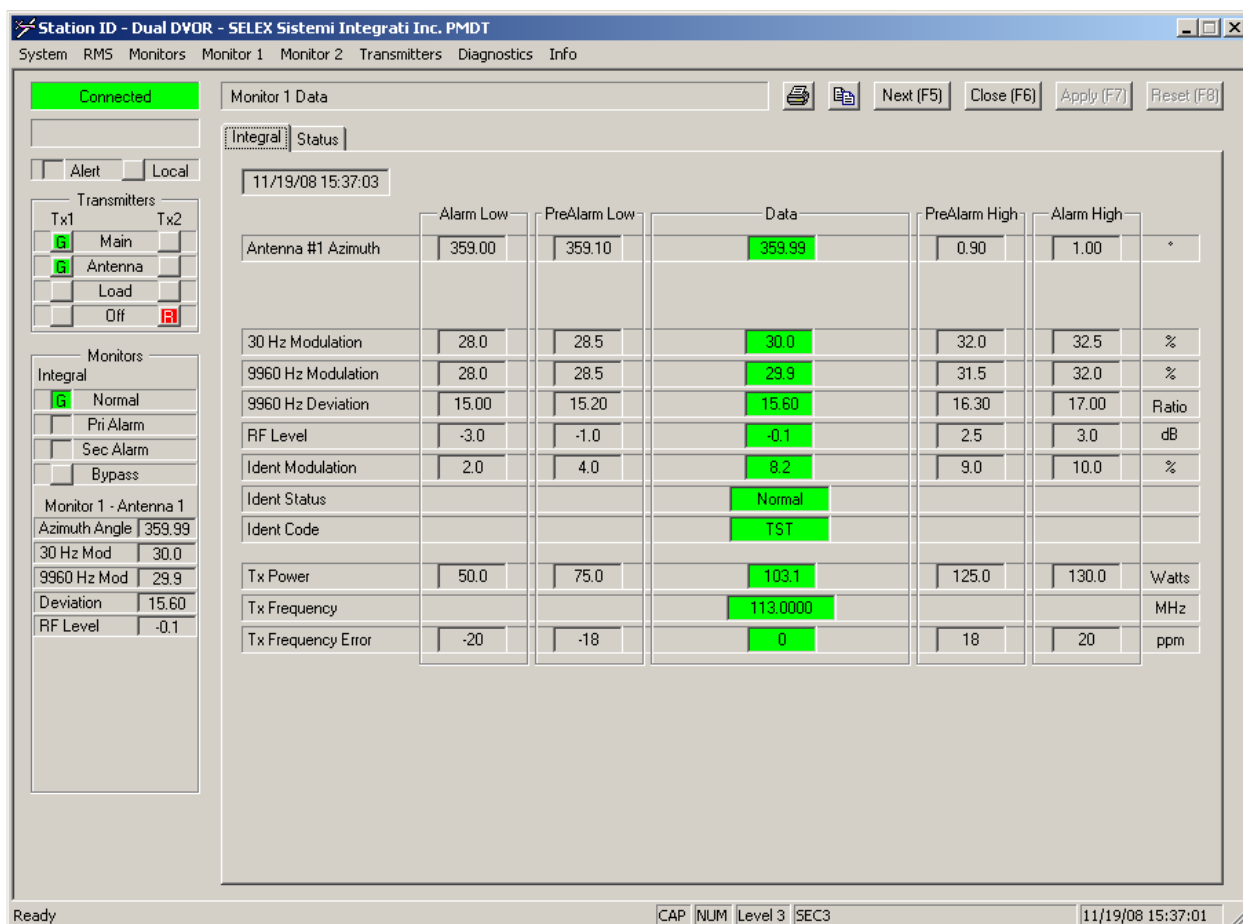


Figure 3-37 Integral Monitor Data Screen

3.6.8.2.1.2 Monitor Status Screen

The Monitor Status Screen is shown in Figure 3-38. This screen displays the general status of the associated Monitor, including any Primary/Secondary Alarms, Pre-Alarms, Maintenance Alerts, Operating Mode and Diagnostic status.

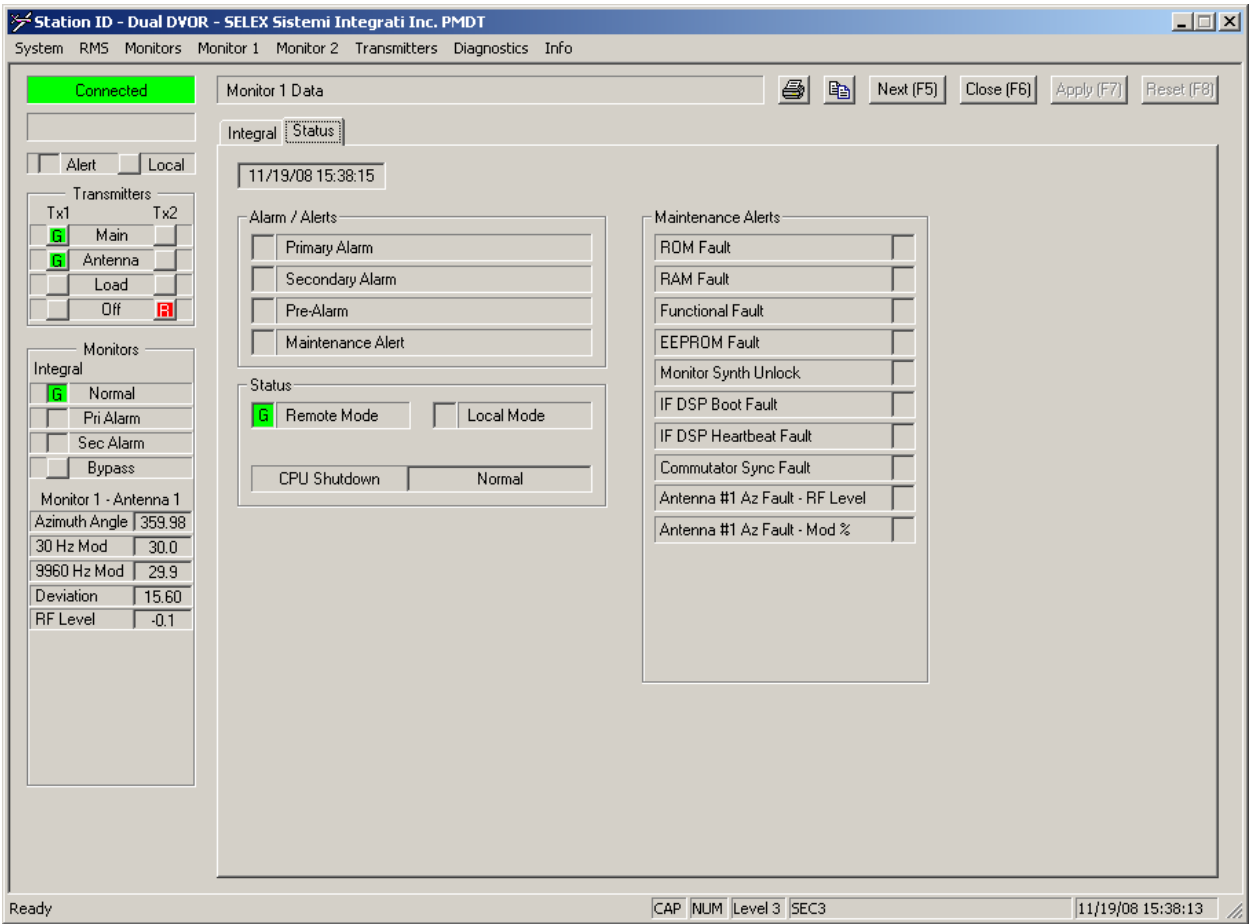


Figure 3-38 Integral Monitor Status Screen

3.6.8.2.2 Monitor Test Results Screens

The Automatic Monitor Integrity Test feature uses the RMS processor to control the Test Generator in order validate the Monitors ability to detect an out of tolerance condition. The Test Generator applies VOR composite signals to the executive monitor channels on both Monitor 1 and Monitor 2 near the alarm limits to verify the ability of the monitors to determine alarm conditions. If a monitor fails to detect an alarm for an out of tolerance parameter for three consecutive tests, it will be disabled from the monitor voting logic in the LCU and a monitor maintenance alert will be generated. The Integrity Test runs continuously, starting a new test cycle approximately every 2 minutes.

For each test case, the RMS sets the test generator to the appropriate Low Test or High Test target value then the Monitor samples the signal for display and comparison against the monitor Low and High Limits. If the monitor finds that the Low Limit Low Test or High Limit High Test does not generate the appropriate monitor alarm condition then that parameter is declared in alarm as shown with a red background. If the RMS finds that the Low Limit High Test or High Limit Low Test generates a false monitor alarm condition then that parameter is declared in alert as shown with a yellow background. The following formulas are used to determine the integrity test targets based on the monitor lower alarm, nominal, and upper alarm limits:

- Low Limit Low Test: $\text{Lower Limit} - (\text{Nominal} - \text{Lower Limit})/10$
- Low Limit High Test: $\text{Lower Limit} + (\text{Nominal} - \text{Lower Limit})/10$
- High Limit Low Test: $\text{High Limit} - (\text{High Limit} - \text{Nominal})/10$
- High Limit High Test: $\text{High Limit} + (\text{High Limit} - \text{Nominal})/10$

When the RMS finds that a monitor declared an alarm when the test condition was inside the alarm limits then the indication will be yellow (integrity alert). A disabled monitor is automatically re-enabled by the RMS following one successful Monitor Integrity cycle. Failure of the Monitor Integrity test may be caused by improper set up of the Monitor 1/2>>Offsets and Scale Factors>> Test Generator Certification settings.

When a monitor is disabled from the monitor voting logic in the LCU, a red Integrity Test Failed indicator is shown on the RMS >> Data >> Maintenance Alert/Alarms screen ([Figure 3-10](#)).

As an additional integrity check, the RMS verifies that the each monitor completes the integrity test cycle within a 10 minute period. Failure to complete all tests within this period results in disabling the monitor.

3.6.8.2.2.1 Completed Test Results

The Completed Test Results screen is shown in Figure 3-39. This screen displays the results of the last Alarm Limit Integrity Test performed by the associated Monitor. It shows the measurements made in each integrity test, as well as the high and low alarm limits for each measurement. Each test result includes the data from the test along with a pass/fail indication by color of background. If the test result background color is green then the test results were within expected limits. If the background color is red then the results exceed acceptable limits.

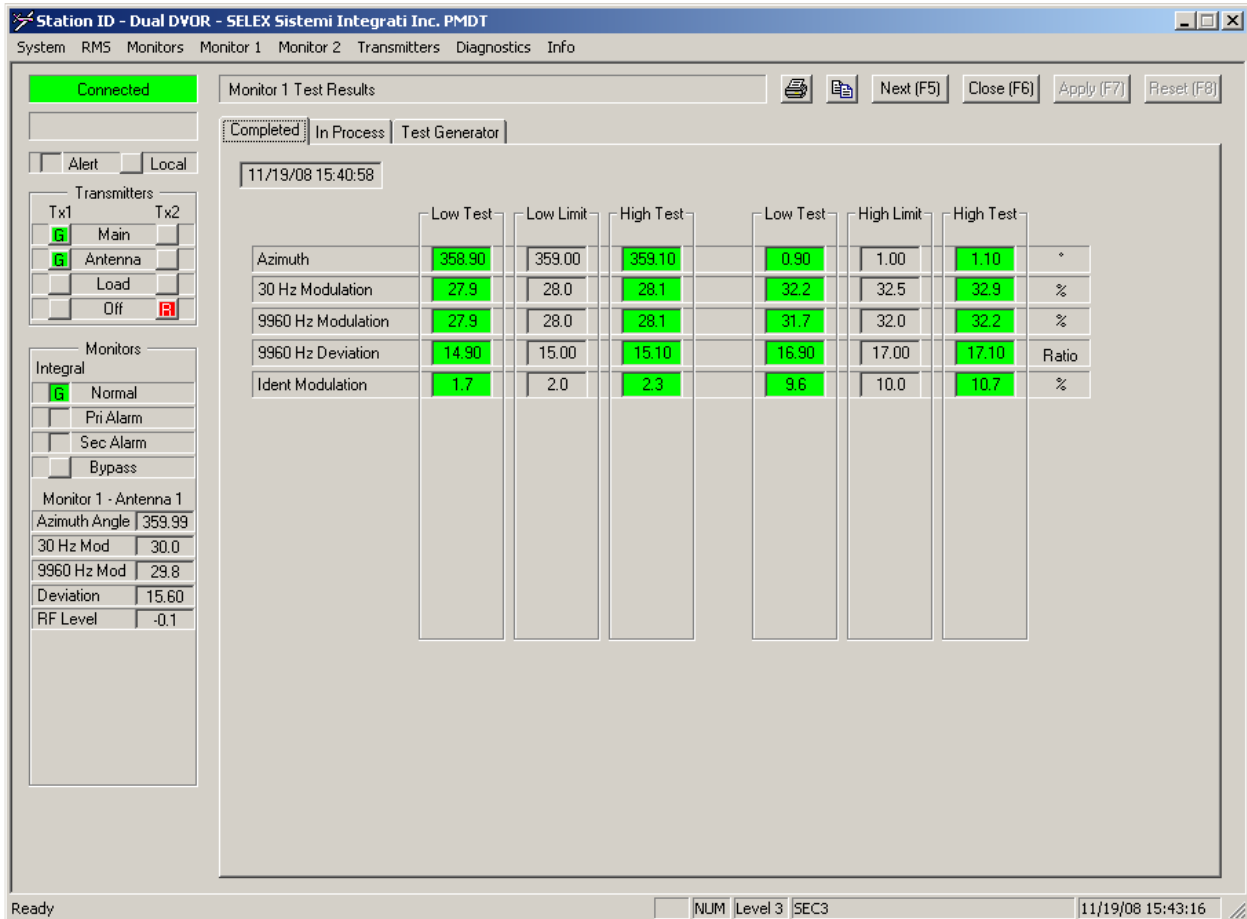


Figure 3-39 Completed Monitor Integrity Test Results Screen

3.6.8.2.2.2 In Process Test Results

The In Process Test Results screen is shown in Figure 3-40. This screen displays the results of the current Alarm Limit Integrity Test being performed by the associated Monitor. It shows the measurements being made in each integrity test, as well as the high and low alarm limits for each measurement. Each test result includes the data from the test along with a pass/fail indication by color of background. If the test result background color is green then the test results were within expected limits. If the background color is red then the results exceed acceptable limits.

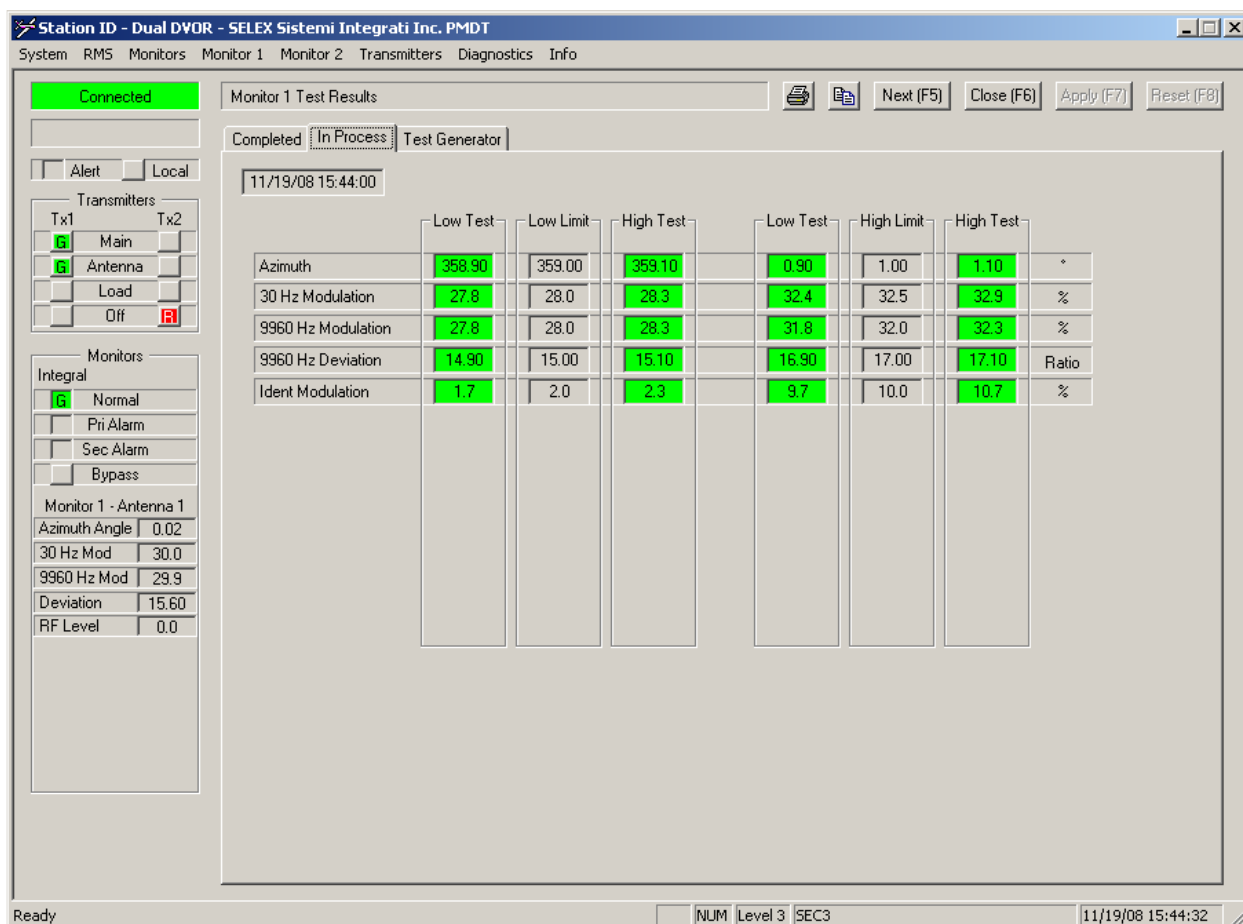


Figure 3-40 In-Process Monitor Integrity Test Results Screen

3.6.8.2.2.3 Monitor1>>Test Generator Screen

The Monitor 1 Data>>Test Generator screen is shown in Figure 3-41. This screen displays the Monitor data obtained during the last Test Generator cycle for the associated Monitor. The Test Generator runs continuously, starting a new test cycle approximately every 2 minutes. The Test Generator parameters may be changed by entering the desired values.

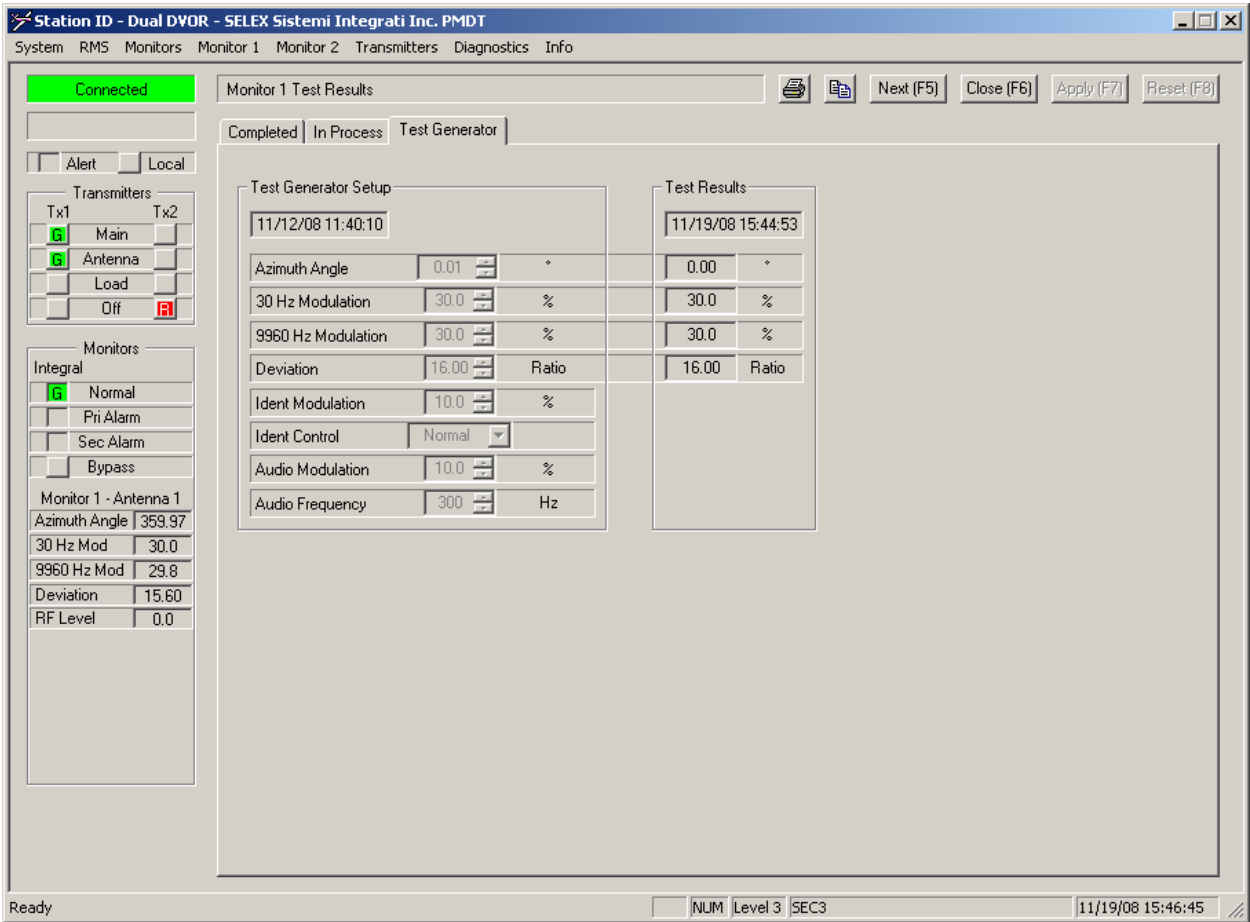


Figure 3-41 Test Generator Screen

3.6.8.2.3 Monitor Fault History Screens

The PMDT's Fault History screens display the system data that is recorded for the last three alarm condition events. This data can be used to determine the cause of the system fault.

3.6.8.2.3.1 Integral Monitor Fault History Screen

The Integral Monitor Fault History screen is shown in Figure 3-42. The Prior to Alarm #1 column contains the last good measurements made prior to the last alarm condition which shutdown the system. The Alarm column contains a snapshot of the measurements at the time that the out-of-tolerance condition occurred. Pressing the "Older" button changes the display to show the previous two alarm events and their time stamps.

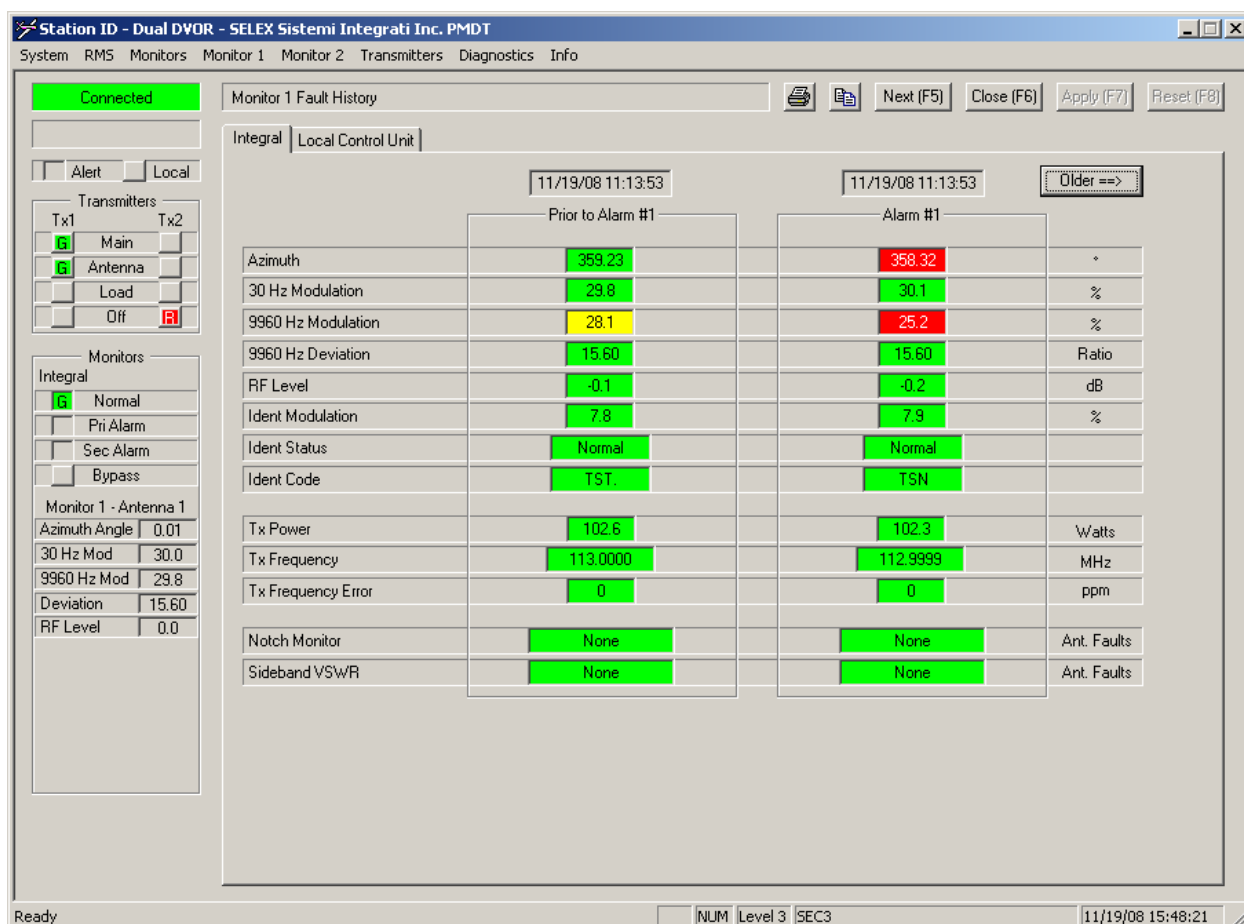


Figure 3-42 Integral Monitor Fault History Screen

3.6.8.2.3.2 Local Control Unit Fault History System Status Screen

The Fault History System Status screen is shown in Figure 3-43. This screen shows the LCU status and antenna configuration at the time of the last three fault conditions.

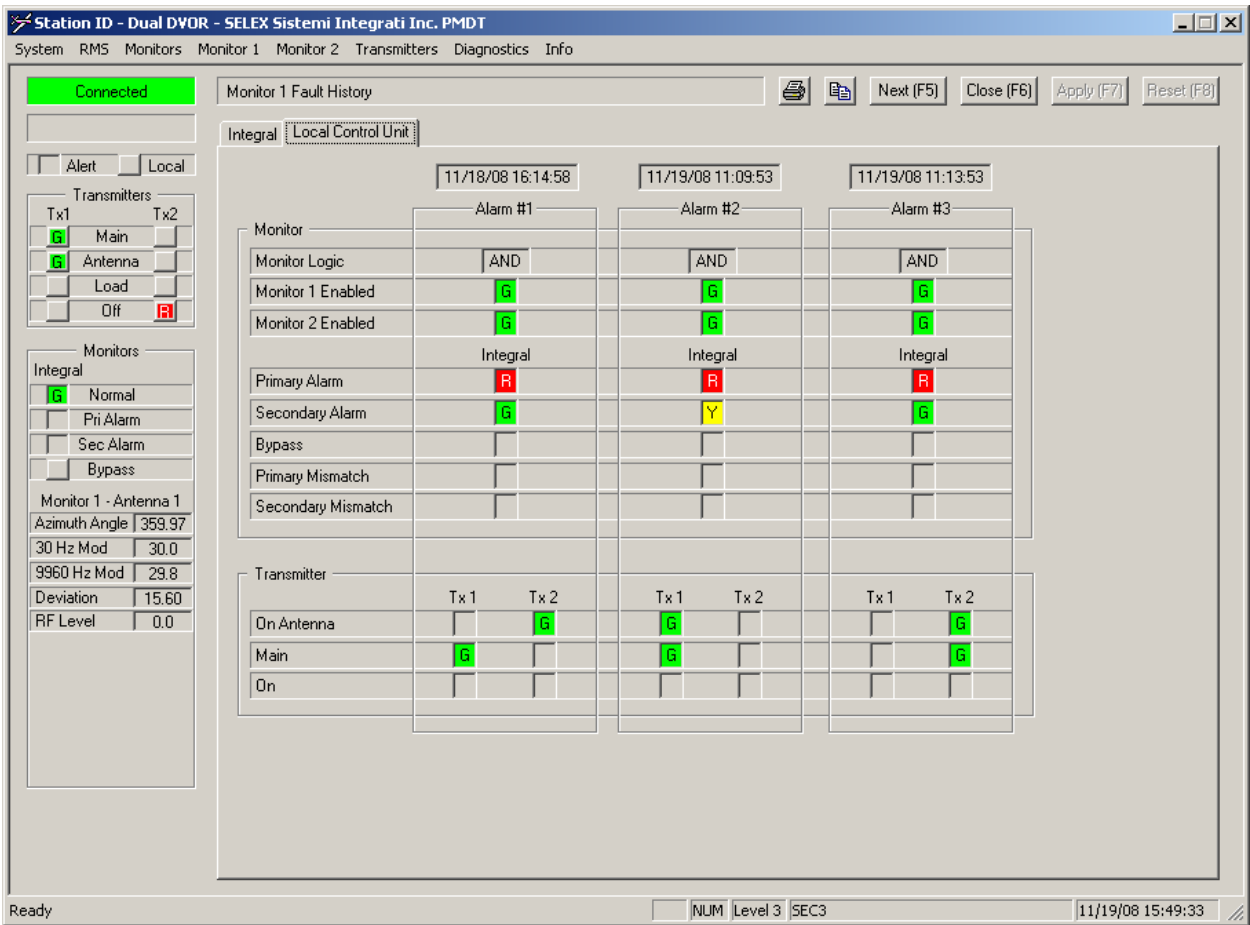


Figure 3-43 Local Control Unit Fault History System Status Screen

3.6.8.2.4 Monitor Offsets and Scale Factors

The Monitor Offsets and Scale Factors screen is shown in Figure 3-44. This screen is used to calibrate each Monitor independently of the other. Each parameter measured by the monitor may be scaled to display a corrected value. The Test Generator should be used as the initial reference for the offsets and scale factors. The values for the Test Generator/Certification Azimuth Offset should be close to 0 degrees and the other scale factors nearly 100% by design.

The Integral offsets are adjusted based on the location of the Field Monitor and flight calibration results. During flight calibration the Transmitters>>Configuration>> Offsets and scale factor are adjusted to meet the requirements the calibration. Then the Monitor 1/2>>Offset and Scale Factors>> Integral are adjusted to obtain the nominal results.

Any configuration changes intended to remain after subsequent power cycling or system resetting MUST be backed up before cycling/resetting.

Station ID - Dual DVOR - SELEX Sistemi Integrati Inc. PMDT

System RMS Monitors Monitor 1 Monitor 2 Transmitters Diagnostics Info

Connected

Monitor 1 Offsets and Scale Factors

Next (F5) Close (F6) Apply (F7) Reset (F8)

Alert Local

Transmitters

Tx1 Tx2

Main Antenna Load Off

Monitors

Integral

Normal Pri Alarm Sec Alarm Bypass

Monitor 1 - Antenna 1

Azimuth Angle 359.97

30 Hz Mod 30.0

9960 Hz Mod 29.8

Deviation 15.60

RF Level 0.0

Offsets and Scale Factors

	Integral	Standby	Test Generator/ Certification	
11/18/08 16:55:58				
Azimuth Angle Offset	0.00		0.00	°
30 Hz Modulation Scale	100.0		100.0	%
9960 Hz Modulation Scale	85.0		100.0	%
9960 Hz Deviation Scale	100.0		100.0	%
RF Level Offset	-0.5			dB
Ident Modulation Scale	100.0		100.0	%
Tx Power Scale	100.0	88.0		%
Tx Power Offset	0.0	0.0		%
Tx Frequency Error Offset	0.0	0.0		ppm
Notch Monitor Scale	100.0			

Ready NUM Level 3 SEC3 11/19/08 15:51:09

Figure 3-44 Monitor Offsets and Scale Factors

3.6.8.2.5 Monitor Test Signal Output Control

The Monitor Test Signal Output Control is shown in Figure 3-45. This screen is used to connect the desired signal to the Test BNC connector (J3) on the front of the Monitor circuit card assembly for maintenance purpose. Each of the signals are available to be connected to test equipment. The default signal connected to the Test connector is the Integral composite. Selection of these signals has no effect on the Monitoring performance.

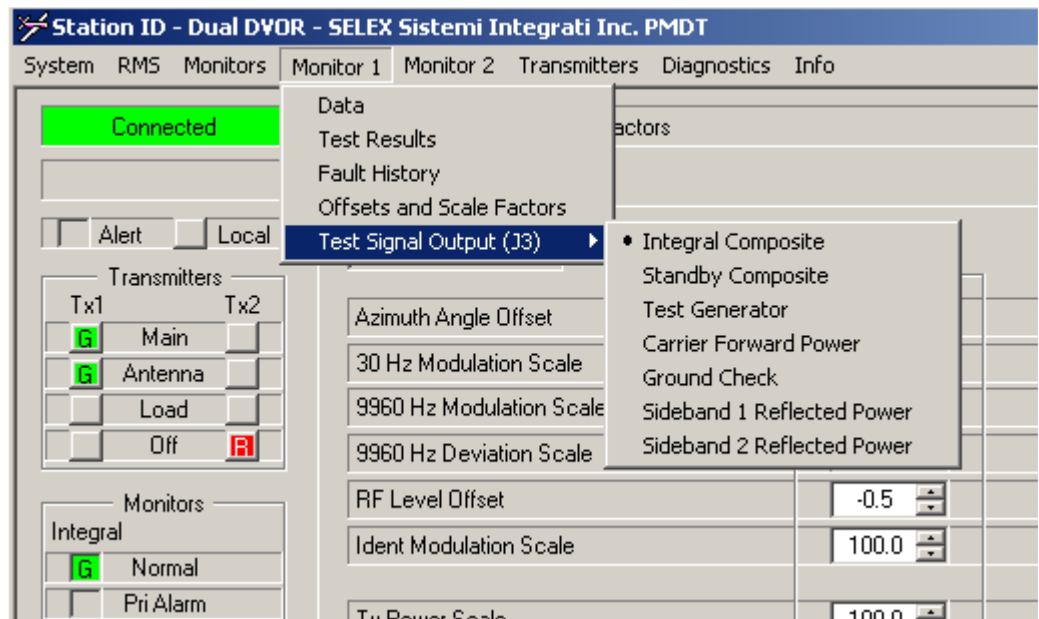


Figure 3-45 Monitor Test Signal Selection

3.6.8.3 Transmitter Data Screens

The VOR Transmitter Screens described below contain the various status and controls for the VOR transmitters.

3.6.8.3.1 Transmitter Data Screen

The Transmitter Data screen is shown in Figure 3-46. This screen displays the current transmitter data as measured by the Audio Generator and Monitor CCAs. The power level and VSWR data are measured by the associated Audio Generator CCA. The frequency data is measured by the associated Monitor.

Station ID - Dual DVOR - SELEX Sistemi Integrati Inc. PMDT

System RMS Monitors Monitor 1 Monitor 2 Transmitters Diagnostics Info

Connected

Transmitter Data

Transmitter Data | Ground Check - Tx #1 | Ground Check - Tx #2 | Status - Tx #1 | Status - Tx #2

11/19/08 15:54:16

	Tx #1	Tx #2	
Power			
Carrier	103.1	0.3	Watts
Sideband #1	2.429	0.004	Watts
Sideband #2	2.426	0.006	Watts
Sideband #3	2.429	0.013	Watts
Sideband #4	2.427	0.011	Watts
Frequency			
Carrier Frequency	113.0000	0.0000	MHz
Tx Lower Sideband	112.9900	0.0000	MHz
Tx Upper Sideband	113.0100	0.0000	MHz
30 Hz AM	30.00		Hz
30 Hz FM	30.00		Hz
Sideband Frequency	9960		Hz
VSWR			
Carrier	1.13		: 1
Sideband #1	1.14		: 1
Sideband #2	1.14		: 1
Sideband #3	1.17		: 1
Sideband #4	1.18		: 1

Transmitters

Tx1 Tx2

☒ Main ☐

☒ Antenna ☐

☐ Load ☐

☐ Off ☒

Monitors

Integral

☒ Normal

☐ Pri Alarm

☐ Sec Alarm

☐ Bypass

Monitor 1 - Antenna 1

Azimuth Angle | 353.96

30 Hz Mod | 30.0

9960 Hz Mod | 29.8

Deviation | 15.59

RF Level | 0.0

Ready

NUM Level 3 SEC3

11/19/08 15:54:14

Figure 3-46 Transmitter Data Screen

3.6.8.3.2 VOR Ground Check Data Screen

The 1150A DVOR provides the ability to perform a ground check. The Ground Check Data Screen is shown in Figure 3-47. This screen is used to initiate a VOR Ground Check and display of the data from the ground check.

SAFETY CRITICAL NOTE

The DVOR Automatic Ground Check changes the radiated signal and a NOTAM SHALL be issued to notify that the DVOR is not in service during this test. Per ICAO State letters, conducting this type of DVOR ground check is an HMI event. (HMI = Hazardously Misleading Information). When HMI is intentionally produced, ICAO requires that the NOTAM text contain information that conveys to the flight crew that the signals are not only “out of service”, but may be unsafe to use, even though they may appear normal.

The monitor controls the RS422 data to the Commutator Control CCA to rotate the position of the DVOR from the normal position in 22.5 degree increments. At each of these positions the Monitor measures the signal and computes the error for that position. When all 16 positions have been measured, a Fourier Analysis is computed and the resulting errors are displayed. The outputs of the Fourier analysis, (FFT Errors), are Duantal, Quadrantal, Octantal and Bias errors. Duantal error has one maximum and one minimum in 360 degrees around the DVOR. Similarly Quadrantal error has two peaks and two minimums around the 360 degrees. The Octantal Error has four peaks and four minimums around the DVOR. The Bias error is the average azimuth shift of the DVOR station.

By selecting one of the graph options the data appears on the graph along with the optional legend for that data set. Pressing the advanced button will display the Advanced Ground Check screen which allows viewing a larger graph, printing and copying the graph to a file.

The Station error is a plot of the errors from the data in the Station Error column of data. The FFT sum is the summation of the FFT errors components. The FFT sum plot should look like the Station error plot for a normal station.

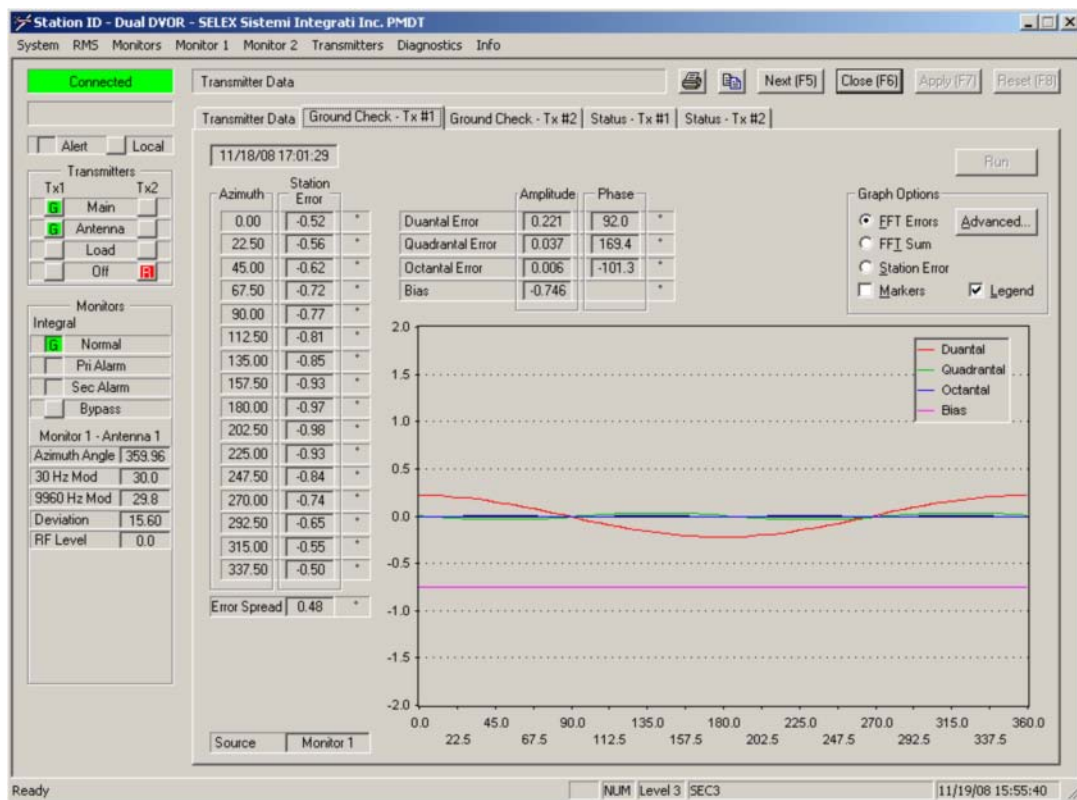


Figure 3-47 Ground Check Data Screen

3.6.8.3.3 VOR Ground Check Data Advanced Screen

The Advanced Ground Check Data Screen is shown in Figure 3-48. This screen shows VOR Ground Check Data in more detail than the previous Ground Check screen. By selecting one of the graph options the data appears on the graph along with the optional legend for that data set. The graph can be printed by pressing the Print button. The data can be stored to a file by pressing the Copy or Save As button.

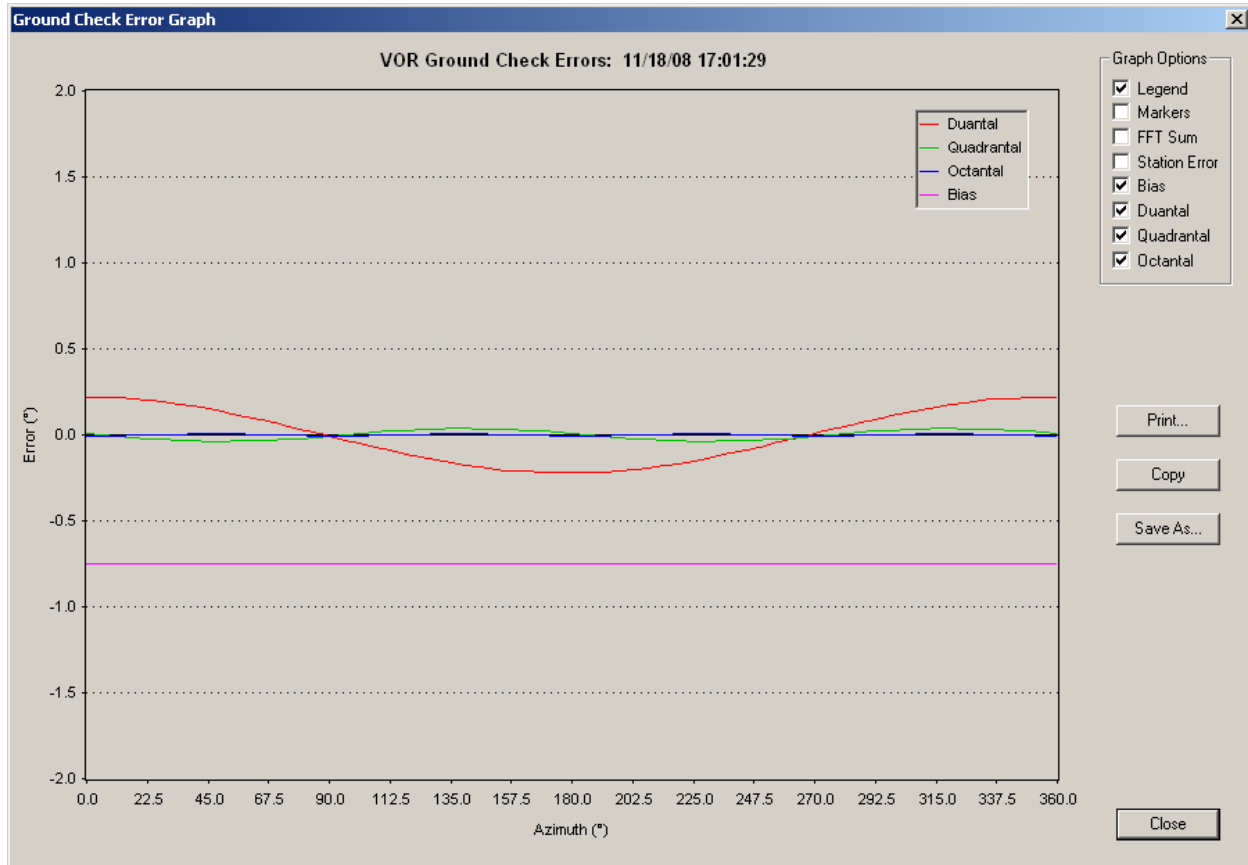


Figure 3-48 Advanced Ground Check Data Screen

3.6.8.3.4 Transmitter Status Screen

The Transmitter Status Screen is shown in Figure 3-49. This screen shows the current state of the Transmitter. A separate screen is provided for each transmitter. The ROM, RAM, Functional, EEPROM, COMM and CRC faults are background tests run on the Audio Generator. Failure of any of these items or the CPU Shutdown indicate Audio Generator CCA hardware failure. Signals from the Carrier Amplifier, Synthesizer and Sideband Amplifiers are checked for reasonable levels and status alerts generated for an aid in fault finding. The Audio Generator Disabled indication is active (yellow) when the transmitter is turned off.

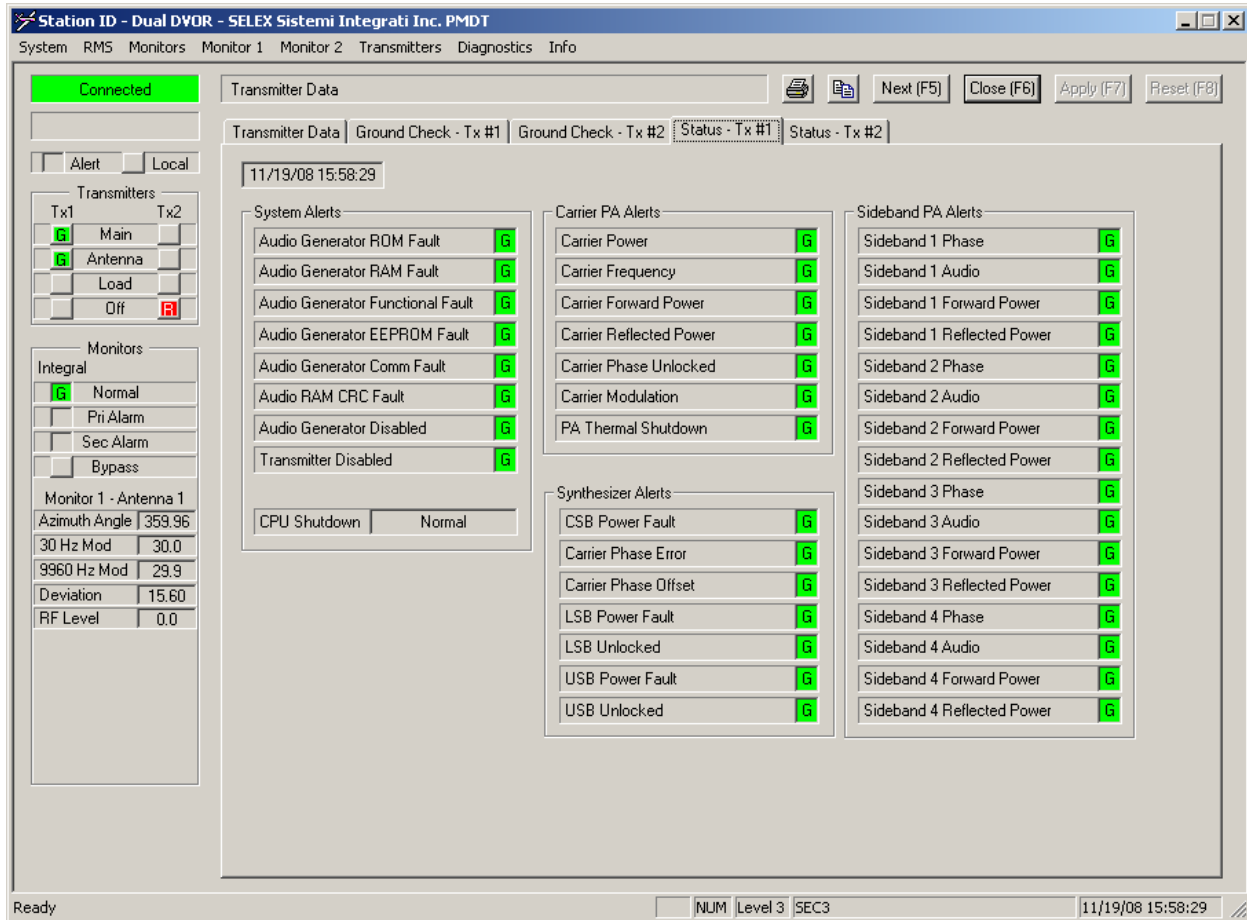


Figure 3-49 Transmitter Status Screen

3.6.8.4 Transmitter Configuration Screens

3.6.8.4.1 Nominal Configuration Screen

The Nominal Transmitter Configuration screen is shown in Figure 3-50. This screen is used to specify the transmitter waveform created by the Audio Generator.

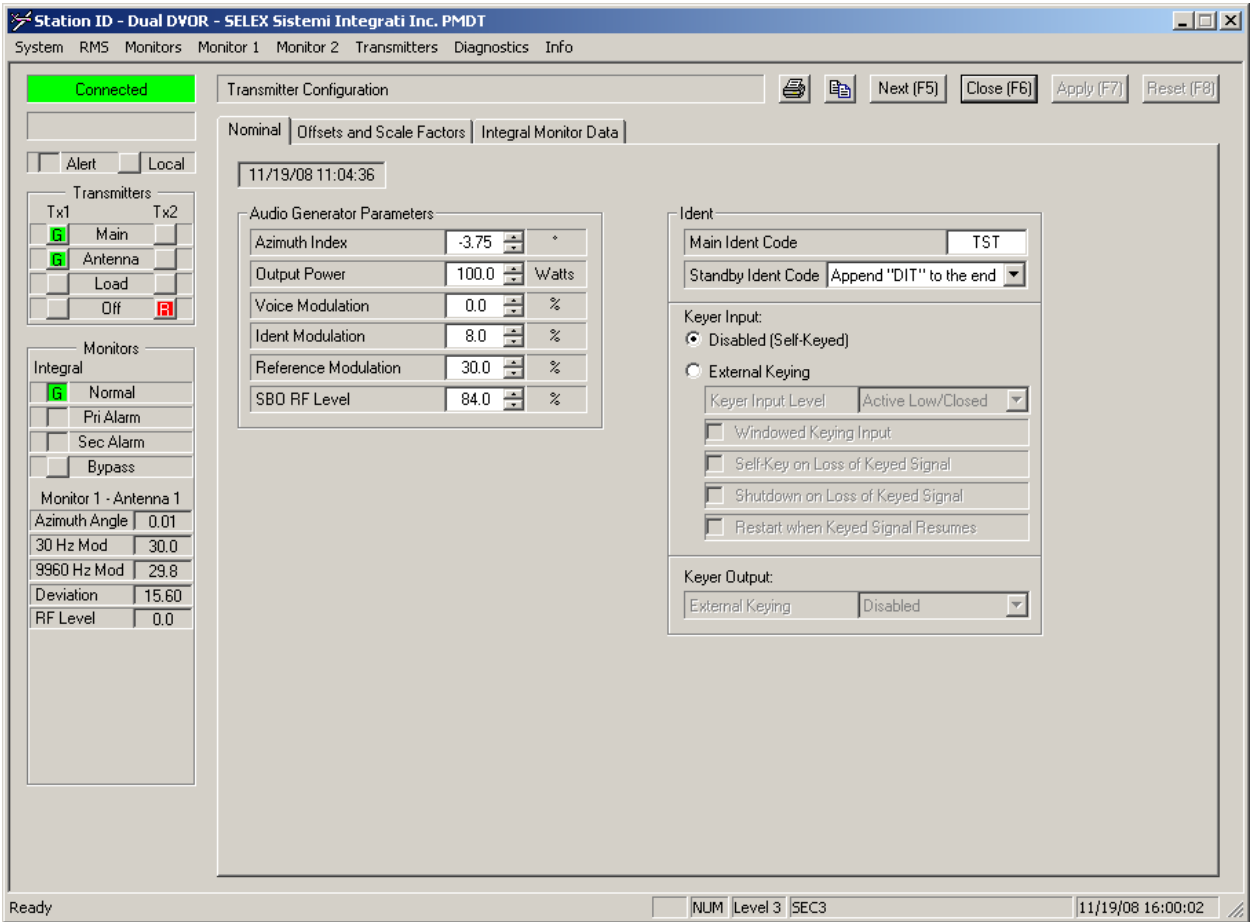


Figure 3-50 Nominal Transmitter Configuration Screen

3.6.8.4.2 Transmitter Offsets & Scale Factors

The Transmitter Offsets and Scale Factors screen is shown in Figure 3-51. This screen is used to configure the parameters of each of the two transmitters independently from the other. The Azimuth Angle Offset, Output Power scale, Voice Modulation Scale, Ident Modulation Scale and Reference Modulation Scale offsets modify the corresponding values found in the Transmitters Configuration >> Nominal screen. The TX Sideband RF Level scale modifies the SBO Level in the Transmitters Configuration >> Nominal screen for all four sidebands together. There are four Sideband RF Level Scale factors for each sideband in each transmitter to aid in matching the output power in the four sidebands.

Station ID - Dual DVOR - SELEX Sistemi Integrati Inc. PMDT

System RMS Monitors Monitor 1 Monitor 2 Transmitters Diagnostics Info

Connected

Transmitter Configuration

Nominal Offsets and Scale Factors Integral Monitor Data

11/19/08 11:57:24

	Tx #1	Tx #2	
Azimuth Angle Offset	-1.10	-1.30	*
Output Power Scale	71.0	83.0	%
Voice Modulation Scale	100.0	100.0	%
Ident Modulation Scale	107.0	100.0	%
Reference Modulation Scale	91.5	90.5	%
Carrier PLL Control	47.5	30.0	%
Carrier-Sideband Phase Offset (Coarse)	180	0	*
Carrier-Sideband Phase Offset (Fine)	37	-19	*
Sideband 1 Phase Offset	-6	-5	*
Sideband 2 Phase Offset	6	5	*
Sideband 3 Phase Offset	-6	-5	*
Sideband 4 Phase Offset	6	5	*
Tx Sideband RF Level Scale	117.0	95.0	%
Sideband 1 RF Level Scale	100.0	100.0	%
Sideband 2 RF Level Scale	100.0	100.0	%
Sideband 3 RF Level Scale	100.0	100.0	%
Sideband 4 RF Level Scale	100.0	100.0	%

Transmitters

Tx1 Main Tx2

Alert Local

Monitors

Integral

Normal

Pri Alarm

Sec Alarm

Bypass

Monitor 1 - Antenna 1

Azimuth Angle 359.98

30 Hz Mod 30.0

9960 Hz Mod 29.9

Deviation 15.59

RF Level 0.0

Ready

NUM Level 3 SEC3

11/19/08 16:05:43

Figure 3-51 Transmitter Offsets and Scale Factors Screen

3.6.8.5 Transmitter Commands

The Transmitter Commands menu is shown in Figure 3-52. These commands provide direct control of transferring between the Main and Standby transmitters, controlling the output of Transmitter 1 or 2, or setting the between Normal, Continuous, or No Ident output. Note that the Transmitter control commands can also be accessed using the corresponding buttons in the PMDT’s Sidebar. Selection of Hold Commutator brings up Figure 3-53. The Hold Commutator window allows entry of the sideband antenna which the rotation stops and radiates on only the chosen antenna position. If the antenna number is odd then Sideband 1 supplies power and all other Sidebands turned off. If the antenna number is even then Sideband 2 supplies power with all other Sidebands turned off.

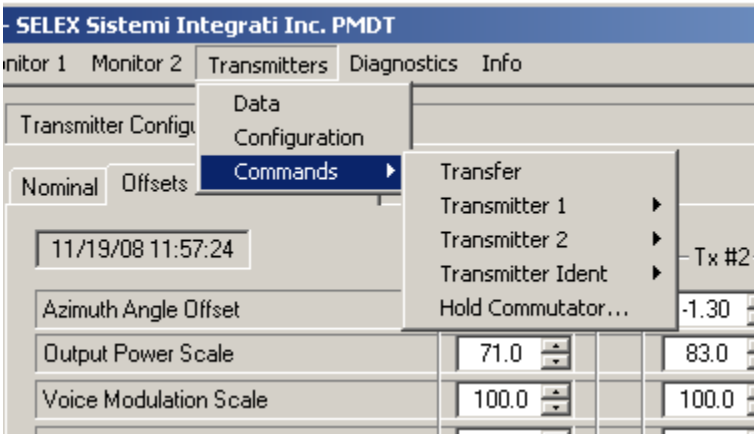


Figure 3-52 Transmitter Commands Menu

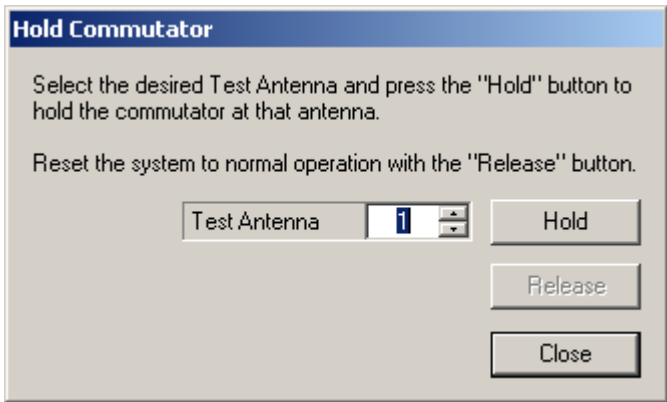


Figure 3-53 Hold Commutator Control Menu

3.6.8.6 Diagnostics Screen

3.6.8.6.1 Power-Up Diagnostics Results

The Power-up Diagnostics Results screen is shown in Figure 3-54. This screen shows the results of the most recent power-up diagnostics test. Each time any of the navaid's embedded processors is reset or powered up, it performs a series of internal diagnostic tests to verify its integrity. The results of those tests are displayed on this screen for the RMS, Monitors and Audio Generators. CPU Functional tests are instruction and data fetches, bit operations, and math operations. RAM checks are extensive tests on individual bit positions of all RAM. PROM checks are checksum calculations and comparison against checksums established at the factory. EEPROM checks are checksum validations of data held in EEPROM. Green indications are normal. If a module indicates a power-up diagnostic failure, it should be replaced.

Depending on where in the startup process the fault is detected, failure of the monitor or audio generator will either stop servicing the watch dog or enter the failsafe shutdown loop.

In the case of the audio generator, either case will result in no radiation.

In the first case for monitor, communications would never be established, and the RMS would remove it from the LCU voting logic and force the outputs into the alarm state. In the second case for the monitor, the monitor forces a hard alarm to the LCU and the RMS would remove it from LCU voting logic after the integrity tests failed.

The RMS when failed does not enable the LCU and waits for the watchdog to reset and if the fault does not clear then the reset continues until the RMS is replaced.

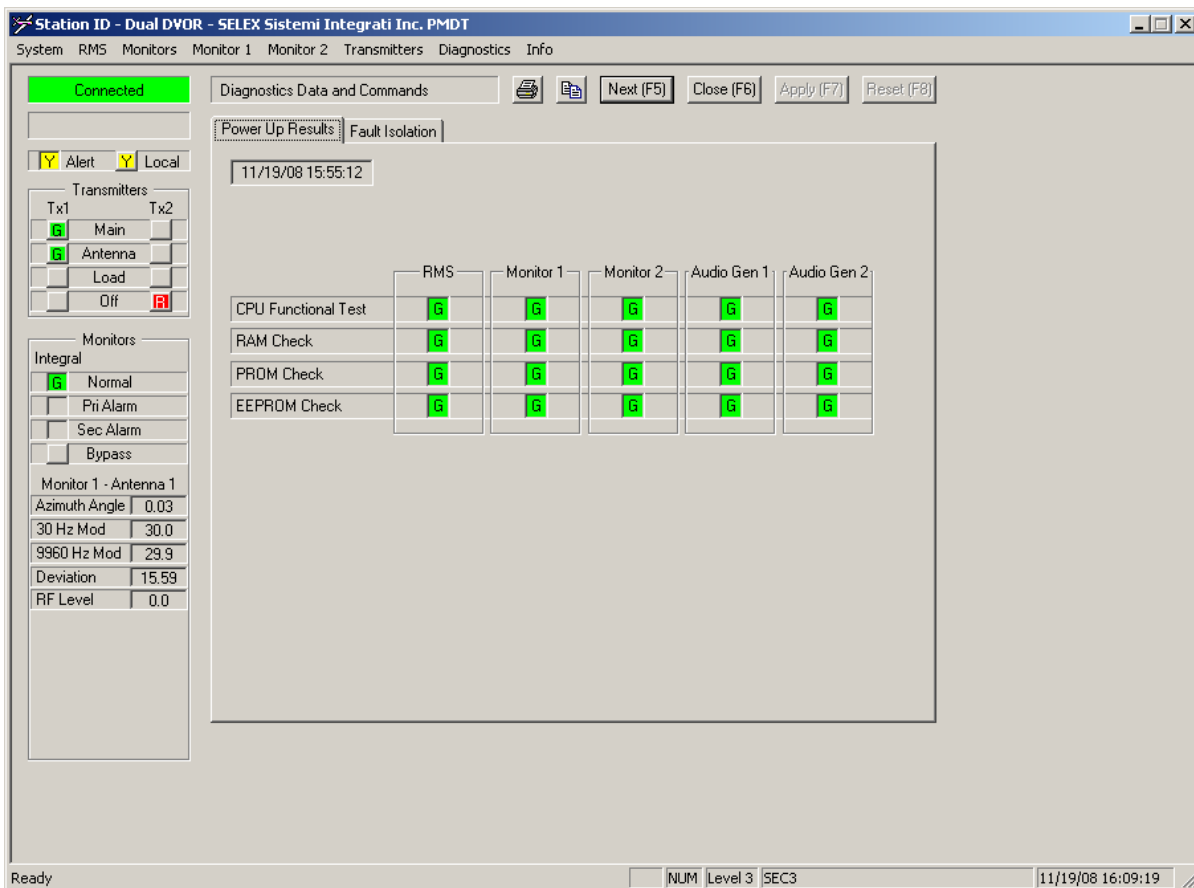


Figure 3-54 Power-Up Diagnostics Results Screen

3.6.8.6.2 Fault Isolation Test Results

The VOR Fault Isolation screen is shown in Figure 3-55. This screen shows the results of the most recent Fault Isolation Test. Pressing the “Run Full Diagnostic”, which is only available in Local Mode from Security Level 3 or higher, causes the system to execute the complete built-in diagnostics. This requires the system to be NOTAM’d off. Pressing the “Run On Air Diagnostics”, which is available either locally or remotely from Security Level 2 or higher, causes the system to execute a subset of the full diagnostics that does not require the system to be NOTAM’d off. Once started, the diagnostics can be canceled by the user with the “Cancel” button. The results are shown in the Fault Results window at the bottom of the screen.

SAFETY CRITICAL NOTE

The DVOR Run Full Diagnostics check changes the radiated signal and a NOTAM MUST be issued to notify that the DVOR is not in service during this test. Per ICAO State letters, conducting this type of DVOR test is an HMI event. (HMI = Hazardously Misleading Information). When HMI is intentionally produced, ICAO requires that the NOTAM text contain information that conveys to the flight crew that the signals are not only “out of service”, but may be unsafe to use, even though they may appear normal.

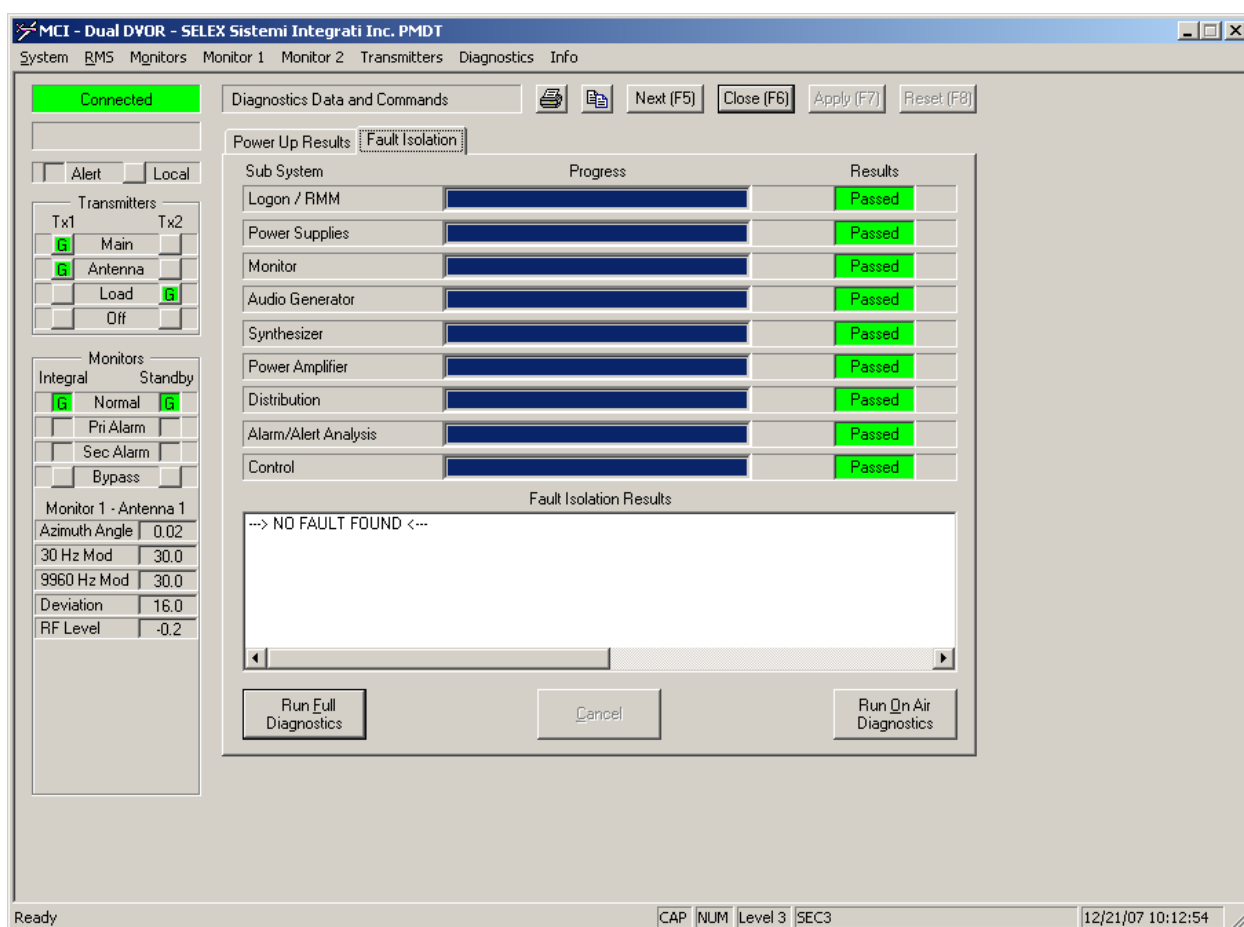


Figure 3-55 VOR Fault Isolation Screen

3.6.8.7 Controlling the Transmitter via the PMDT

Transmitter parameters are adjusted using the Nominal Screen (Figure 3-50) and the Transmitter Offsets and Scale factors Screen (Figure 3-51). Refer to these screens for the following paragraphs.

3.6.8.7.1 General Transmitter Control

With Transmitter #1 on the antenna, configure the Transmitter>>Configuration>>Nominal settings for the desired operation as measured by the Monitor. Transfer to Transmitter #2 and adjust the Transmitter>>Configuration>>Offsets And Scale Factors for Tx #2 offset to obtain the same desired operation for TX #2 as measured by the Monitor. During Flight Check adjust the Tx #1 and Tx #2 offsets and scale factors as necessary when directed by Flight Check to obtain this signal in space for each Transmitter.

3.6.8.7.2 Change the Azimuth Index

To affect both Transmitter #1 and Transmitter #2, select Transmitters >> Configuration >> Nominal. Adjust the Azimuth Index by selecting the parameter with the mouse then either enter the value or use the spin controls. Press the Apply button (or the “F7” key) to apply the change.

To affect only one transmitter, select Transmitters >> Configuration >> Offsets and Scale Factors screen. Adjust the Transmitter 1 (or 2, as desired) Az Angle Offset by selecting the parameter with the mouse, then either enter the offset value or use the spin controls. Press the Apply button (or the “F7” key) to apply the change.

3.6.8.7.3 Change the CSB Output Power

To affect both Transmitter #1 and Transmitter #2, select Transmitters >> Configuration >> Nominal. Adjust the CSB power output level by selecting the CSB Output Power parameter with the mouse then either enter the value or use the spin controls. Press the Apply button (or the “F7” key) to apply the change. The value entered is modified by the Transmitters >> Configuration >> Offsets and Scale Factors >> Output Power value. A value of 100% in the Output Power Scale along with a Nominal Setting of 125 Watts yields approximately 125 Watts. Note that the power change in the Nominal Screen also affects the Sideband RF Level proportionally so that the sideband modulation level stays nearly the same for Carrier output adjustments.

To affect only one transmitter (so that both transmitters provide the same level), select Transmitters >> Configuration >> Offsets and Scale Factors screen. Adjust the Transmitter 1 (or 2, as desired) Power Output level by selecting the Output Power Scale parameter with the mouse then either enter the percentage value or use the spin controls. Press the Apply button (or the “F7” key) to apply the change.

3.6.8.7.4 Change the Voice Depth of Modulation

To affect both Transmitter #1 and Transmitter #2, select Transmitters >> Configuration >> Nominal. Adjust the Voice Depth of Modulation by selecting the Voice Modulation parameter with the mouse then either enter the value or use the spin controls. Press the Apply button (or the “F7” key) to apply the change.

To affect only one transmitter, select Transmitters >> Configuration >> Offsets and Scale Factors screen. Adjust the Transmitter 1 (or 2, as desired) Voice Modulation Scale Percent by selecting the parameter with the mouse, then either enter the percentage value or use the spin controls. Press the Apply button (or the “F7” key) to apply the change.

3.6.8.7.5 Change the Identification Depth of Modulation

To affect both Transmitter #1 and Transmitter #2, select Transmitters >> Configuration>>Nominal. Adjust the ident depth of modulation level by selecting the Ident Mod Level parameter with the mouse then either enter the value or use the spin controls. Press the Apply button (or the “F7” key) to apply the change.

To affect only one transmitter, select Transmitters >> Configuration >> Transmitter 1 (or 2, as desired) Offsets and Scale Factors screen. Adjust the ident modulation level by selecting the Ident Level Scale parameter with the mouse then either enter the percentage value or use the spin controls. Press the Apply button (or the (“F7” key) to apply the change.

3.6.8.7.6 Change the Reference Depth of Modulation

To affect both Transmitter #1 and Transmitter #2, select Transmitters >> Configuration >> Nominal. Adjust the Reference depth of modulation by selecting the Reference Modulation parameter with the mouse then either enter the value or use the spin controls. Press the Apply button (or the “F7” key) to apply the change.

To affect only one transmitter, select Transmitters >> Configuration >> Offsets and Scale Factors screen. Adjust the Transmitter 1 (or 2, as desired) Reference Modulation Scale Percent by selecting the parameter with the mouse, then either enter the percentage value or use the spin controls. Press the Apply button (or the “F7” key) to apply the change.

3.6.8.7.7 Change the Sideband Power Level

To affect both Transmitter #1 and Transmitter #2, select Transmitters >> Configuration >> Nominal. Adjust the SBO power output level by selecting the SBO RF Level parameter with the mouse then either enter the value or use the spin controls. Press the Apply button (or the “F7” key) to apply the change. The value entered is a percentage of the maximum available for the SBO amplifier. Note that the power change of the Output Power level in the Transmitters >> Configuration >> Nominal Screen also affects the SBO RF Level.

To affect only one transmitter, select Transmitters >> Configuration >> Offsets and Scale Factors screen. Adjust the Transmitter 1 or 2 (as required) Sideband 1 RF level by selecting the Sideband 1 RF Level Scale parameter with the mouse then either enter the percentage value or use the spin controls. Press the Apply button (or the “F7” key) to apply the change. Note that a value of 100% scales the Sideband 1 power output by 1.0, and a value of 70.7% scales the Sideband 1 power output by 0.5 (since this is a Voltage Scale Factor). Sidebands 2, 3, and 4 can also be adjusted individually in this screen.

3.7 RMM

The RMM uses the same hardware and software as the PMDT but interconnects to the equipment via a modem and a telephone circuit. The software screens and operator selection of this usage of the PMDT are described above in the PMDT paragraphs

3.8 CONTROLS AND INDICATORS

The locations, descriptions and functions of the 1150A VOR Controls and indicators are described in [Figure 3-56](#) through [Figure 3-69](#) and [Table 3-4](#) through [Table 3-17](#).

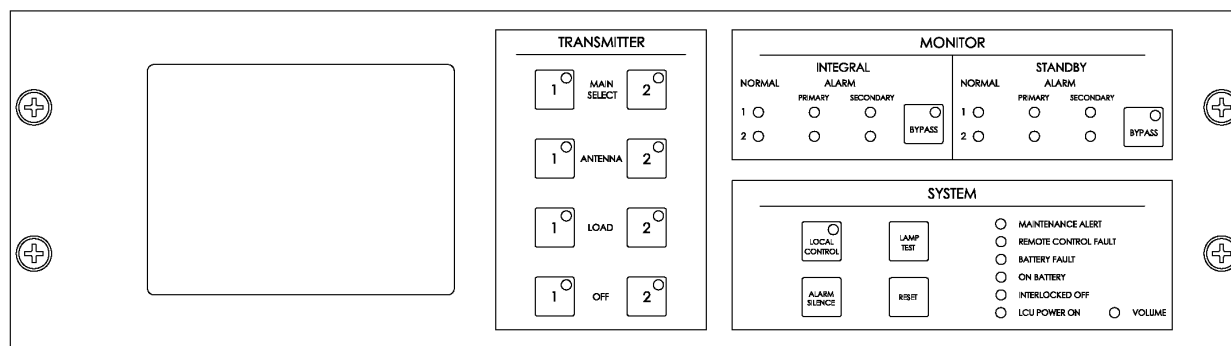
3.8.1 POWER CONTROL PANEL

The Power Control Panel mounts on the front lower section of the VOR equipment cabinet. The functions of each switch and indicator are described in [Table 3-4](#).

Table 3-4 Dual Equipment Control Panel Functions	
POWER CONTROL	
TX 1 AC	AC Circuit Breaker - In the “1” position connects AC to BCPS 1.
TX 1 BATT	DC Circuit Breaker - In the “1” position connects the BCPS1 to the battery.
TX 1 DC BUS	DC Circuit Breaker - In the “1” position connects the BCPS1 to Transmitter1. When the DVOR is set for dual power supply mode the DC BUS breaker connects both BCPS1 and BCPS2 to Transmitter1.
TX 2 AC	AC Circuit Breaker - In the “1” position powers AC and also charges the Battery Set
TX 2 BATT	DC Circuit Breaker - In the “1” position connects the BCPS to the battery.
TX 2 DC BUS	DC Circuit Breaker - In the “1” position connects the BCPS2 to Transmitter2. When the DVOR is set for dual power supply mode the DC BUS breaker connects both BCPS1 and BCPS2 to Transmitter2.

3.8.2 LOCAL CONTROL UNIT (LCU)

The Local Control Unit mounts at the top of the VOR cabinet. [Figure 3-56](#) shows the switches and indicators on the panel. The functions of each switch and indicator are described in [Table 3-5](#).



1150A-0051

Figure 3-56 Local Control Unit (LCU)

3.8.2.1 LCU Display Messages

The LCU has a touch screen to display monitored information. Navigation between the screens is achieved by pressing the Prev (Previous) and Next buttons on the display.

3.8.2.1.1 Integral Monitor

The LCD displays a subset of the readings without limits for the parameters contained in the Monitors>>>Data screen. Separate screens are provided for each Monitor. Figure 3-57 shows the Monitor Integral data display. Figure 3-58 shows the Monitor 2 Integral data display.

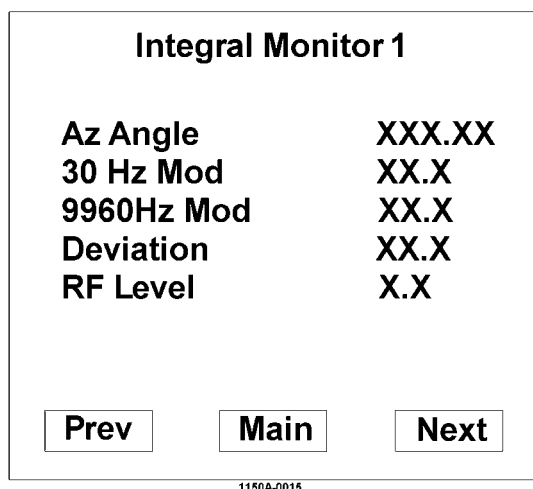


Figure 3-57 LCU Integral Monitor 1 Display

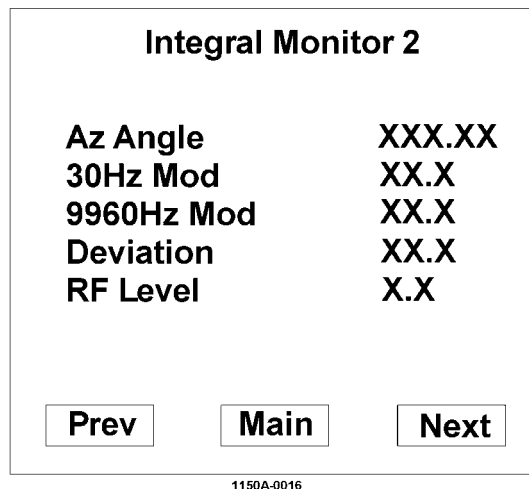


Figure 3-58 LCU Integral Monitor 2 Display

3.8.2.1.2 Transmitter Power Supply and Temperature Monitor

The DVOR Power readings are displayed on the LCU as shown in Figure 3-59. The readings are a subset of the values shown in the RMS>>>Data>>>Power Supply Data screen. Temperature data for the Interior, Exterior, RF Monitor and BCPS temperature are displayed as shown in Figure 3-60. Carrier amplifier and Sideband Amplifier are displayed as shown on Figure 3-61.

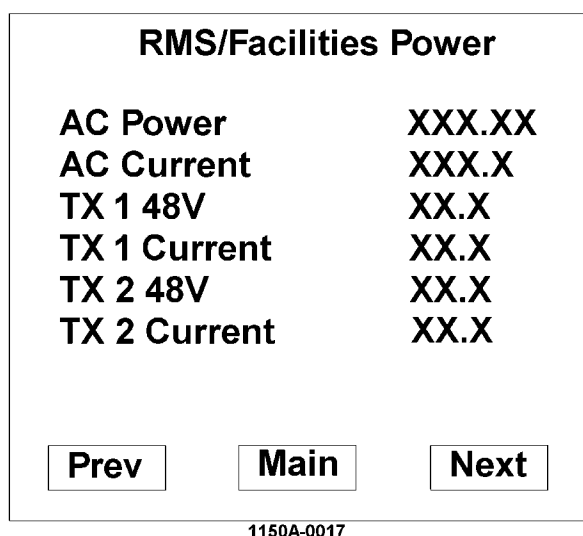


Figure 3-59 LCU Facilities Voltage and Current readings

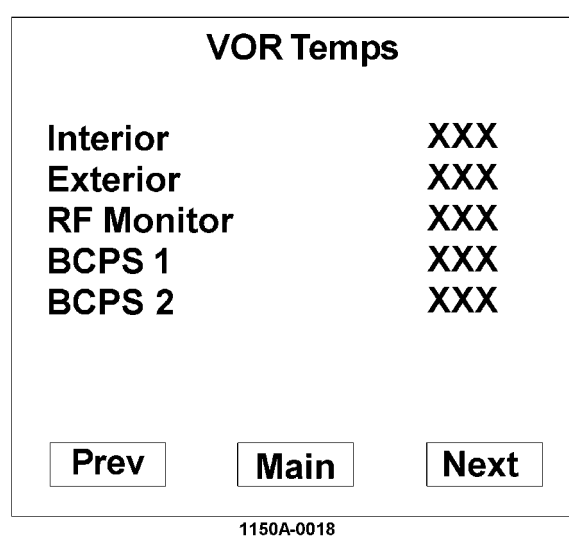
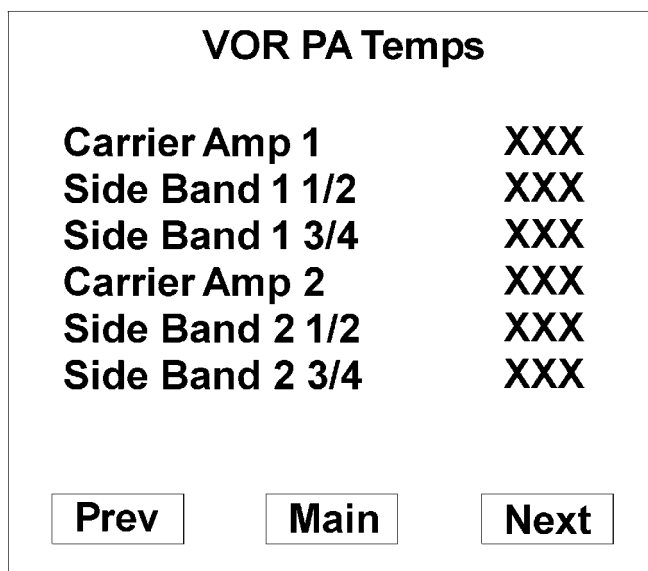


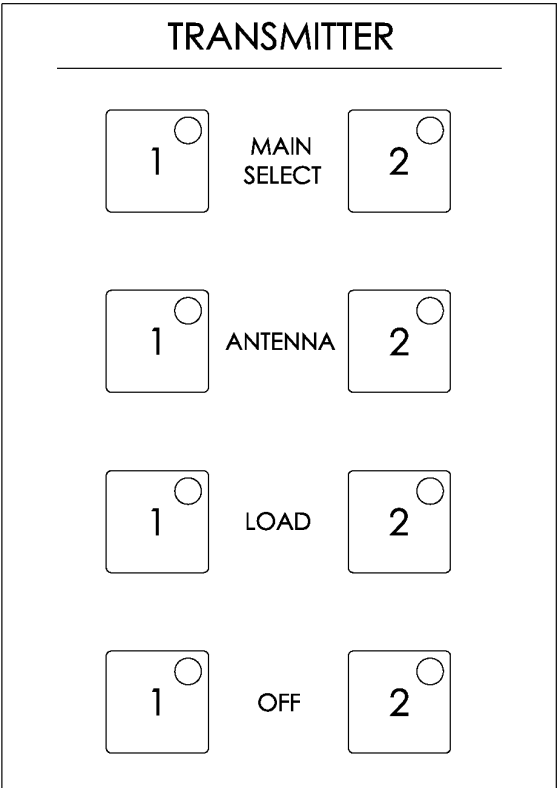
Figure 3-60 LCU Module Temperature readings



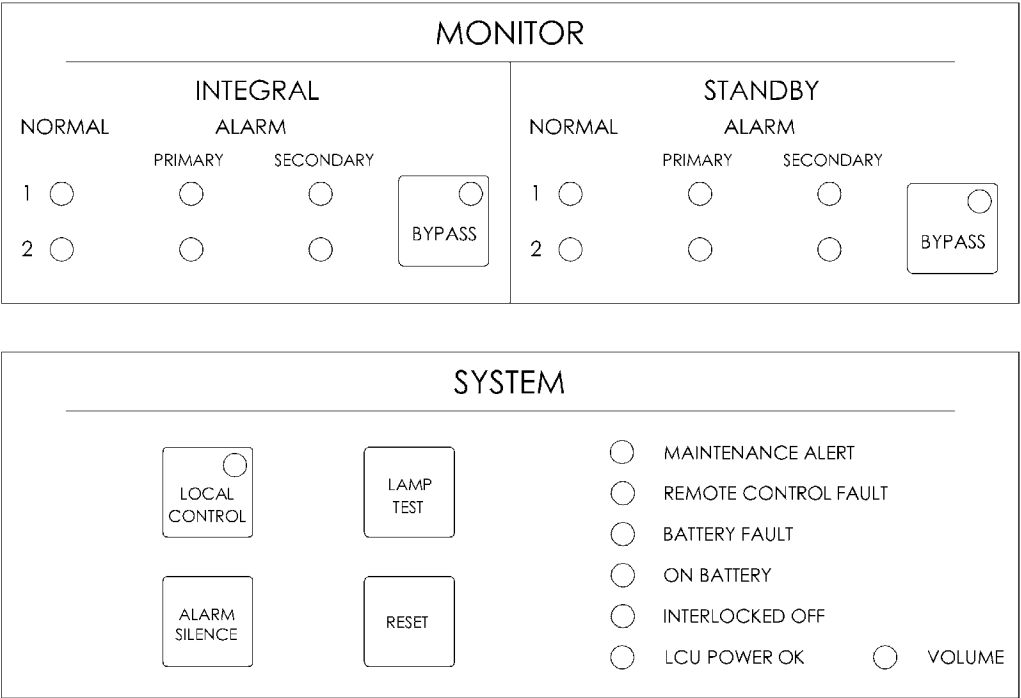
1150A-0019

Figure 3-61 LCU Transmitter Temperature Readings

Table 3-5 Equipment Control Panel Functions (Refer to Figure 3-62)	
TRANSMITTER (Refer to Figure 3-54)	Note: Switches are active in Local Mode only.
Main Select 1 and Indicator	Pressing Main Select 1 switch sets transmitter 1 as the main transmitter and places TX1 on the antenna and in the ON mode. The indicator in the switch illuminates to identify that TX 1 is selected as the Main.
Main Select 2 and Indicator	Pressing Main Select 2 switch sets transmitter 2 as the main transmitter and places TX2 on the antenna and in the ON mode. The indicator in the switch illuminates to identify that TX 2 is selected as the Main.
Antenna 1 and Indicator	Pressing Antenna 1 switch turns transmitter 1 ON and into the antenna. The indicator in the switch illuminates to identify the transmitter connected to the antenna.
Antenna 2 and Indicator	Pressing Antenna 2 switch turns transmitter 2 ON and into the antenna. The indicator in the switch illuminates to identify the transmitter connected to the antenna.
Load 1 and Indicator	Pressing Load 1 switch turns transmitter 1 ON and into the load. The indicator in the switch illuminates to identify the transmitter connected to the load.
Load 2 and Indicator	Pressing Load 2 switch turns transmitter 2 ON and into the load. The indicator in the switch illuminates to identify the transmitter connected to the load.
Off 1 and Indicator	Pressing Off 1 switch places transmitter 1 in the OFF mode without changing the relays. The indicator in the switch illuminates when the transmitter is OFF.
Off 2 and Indicator	Pressing Off 2 switch places transmitter 2 in the OFF mode without changing the relays. The indicator in the switch illuminates when the transmitter is OFF.



1150A-0052
Figure 3-62 LCU Transmitter Controls and Indicators



1150A-0049
Figure 3-63 LCU Monitor/System Controls and Indicators

Table 3-6 Equipment Control Panel Functions	
SYSTEM (Refer to Figure 3-63)	
Local Control, Switch and Indicator	Pressing the switch toggles Local Control Mode. The indicator illuminates when Local Control Mode is enabled. While in Local Control Mode, the BYPASS, MAIN SELECT, ANTENNA, LOAD and OFF switches are enabled. When in the remote mode these switches are disabled. Configuration changes via the PMDT are enabled only while in Local Control Mode. RCSU control of the VOR is disabled while in the Local Control Mode.
Alarm Silence Switch	Pressing this switch turns off the alarm tone until a new alarm condition is detected.
Lamp Test Switch	Pressing this switch causes all indicators on the panel to illuminate.
Reset Switch	Pressing this switch resets the system to the power on condition. The LCU, RMS and all Monitors are reset.
Maintenance Alert Indicator	Illuminates to indicate the presence of a maintenance alert condition.
Remote Control Fault Indicator	Illuminates to indicate a failure condition in the communications link to the RCSU.
Battery Fault Indicator	Illuminates to indicate the presence of a short, open or Battery switch in the open position.
On Battery Indicator	Illuminates to indicate that the VOR is operating on battery power.
Interlocked Off Indicator	Illuminates to indicate the VOR has been turned OFF by the communications link to the RCSU. Attempts to turn ON the VOR will be ignored.
LCU Power Ok	Indicates that the power supplies are operating normally
Volume	This is a potentiometer control to adjust the level of the aural alarm indicator.

Table 3-7 Equipment Control Panel Functions	
MONITOR (Refer to Figure 3-63)	
Integral Normal 1 Indicator	Illuminates to indicate the normal condition of monitor 1 integral channel.
Integral Alarm 1 Indicator	Illuminates to indicate the alarm condition of monitor 1 integral channel after the programmed timeout has expired
Integral Normal 2 Indicator	Illuminates to indicate the normal condition of monitor 2 integral channel.
Integral Alarm 2 Indicator	Illuminates to indicate the alarm condition of monitor 2 integral channel after the programmed timeout has expired
Integral Bypass Switch and Indicator	When in Local Mode pressing the switch toggles the bypass condition of both integral monitors. The indicator illuminates when bypass is active.
Standby Normal 1 Indicator	Not Used (OFF)
Standby Alarm 1 Indicator	Not Used (OFF)
Standby Normal 2 Indicator	Not Used (OFF)
Standby Alarm 2 Indicator	Not Used (OFF)
Standby Bypass Switch and Indicator	Not Used (OFF)

3.8.3 BCPS Asssembly Assembly (1A5A3, 1A5A4)

Refer to Table 3-8 for the indicators and on the Battery Charging Power Supply (BCPS) Assembly.

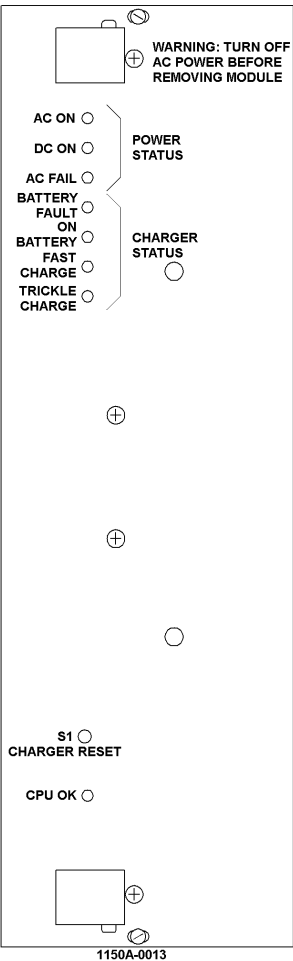


Figure 3-64 BCPS Assembly Controls and Indicators

Table 3-8 Equipment Controls & Indicators	
Battery Charger Power Supply (BCPS) (Refer to Figure 3-64)	
AC ON	This LED indicates that the AC voltage is present at the input to the VOR.
DC ON	This indicates that the DC output of the BCPS.
AC FAIL	This LED indicates that the AC voltage is not present at the input to the VOR.
BATTERY FAULT	This LED indicates that the battery voltage is very low and can be caused by a faulty or disconnected battery.
ON BATTERY	This LED indicates that the VOR is operating on batteries.
FAST CHARGE	This LED indicates that the charge current is above 2 amps.
TRICKLE CHARGE	This LED indicates that the charge current is low (trickle).
CHARGER RESET	This momentary switch is used to start operation on batteries with AC power present.
CPU OK	This LED when lit (GREEN) indicates that the BCPS processor is operating normally.

3.8.4 Carrier Amplifier Assembly (1A5A3, 1A5A4)

Refer to Table 3-9 for the indicators and connectors on the Carrier Amplifier Assembly.

Table 3-9 Carrier Amplifier (1A5A3/1A5A4)	
Carrier Amplifier (Refer to Figure 3-65)	
CSB Sample	This is a sample of the RF output signal for use by external test equipment.
Detected CSB	This is the detected video from the RF output. It allows the technician to observe output modulation and power.
Power OK LED	This LED when lit (GREEN) indicates that the amplifier DC voltages are within tolerance.

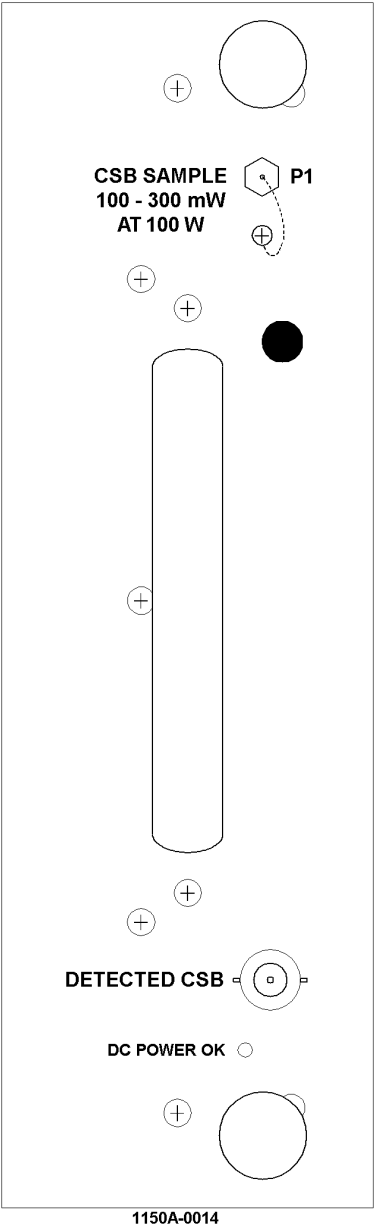


Figure 3-65 Carrier Amplifier Assembly Controls and Indicators

3.8.5 **Monitor CCA (1A3A3, 1A3A10)**

Refer to [Table 3-10](#) and [Figure 3-66](#) for the indicators and controls on the Monitor CCA.



Figure 3-66 Monitor CCA

Table 3-10 Monitor CCA (1A3A3, 1A3A10) Controls and Indicators	
Integral Primary Alarm LED	This LED when lit (RED) indicates that a primary parameter exceeds alarm limits for the transmitter on the antenna.
Integral Secondary Alarm LED	This LED when lit (RED) indicates that a secondary parameter exceeds alarm limits for the transmitter on the antenna.
Integral Pre-Alarm LED	This LED when lit (YELLOW) indicates that a primary parameter exceeds pre alarm limits for the transmitter on the antenna.
Standby Primary Alarm LED	Not Used (OFF)
Standby Secondary Alarm LED	Not Used (OFF)
Standby Pre-Alarm LED	Not Used (OFF)
Sync	This is the scope trigger for viewing the Detected Test signals.
Test	This is the detected Test signal from the Monitor.
CPU OK LED	This LED when lit (GREEN) indicates that the Monitor processor is operating normally.

3.8.6 Remote Monitoring System (RMS) CCA

Refer to [Table 3-11](#) and [Figure 3-67](#) for the RMS CCA indicators and controls).

Table 3-11 Equipment Controls and Indicators	
Auxiliary USB	This port is reserved for future expansion.
PMDT USB	This port interfaces with a portable PC computer and associated control and monitoring software (Portable Maintenance Data Terminal).
CPU OK LED	This LED when lit (GREEN) indicates that the RMS is operating normally.

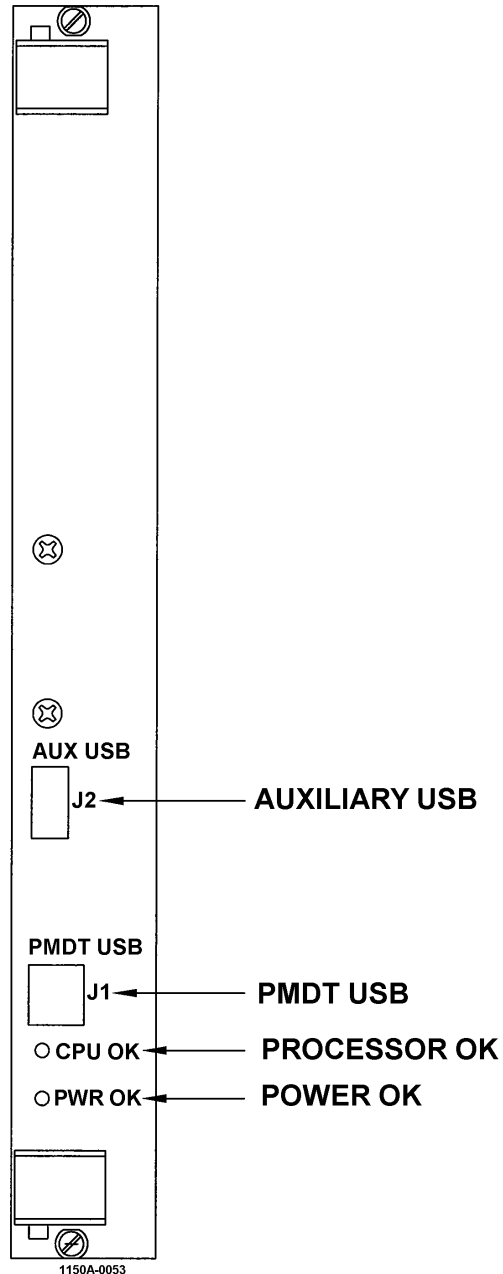


Figure 3-67 Remote Monitoring System (RMS) CCA

3.8.7 Facilities CCA (1A3A7)

Refer to Table 3-12 for the indicators and controls on the Facilities CCA.

Table 3-12 Equipment Controls and Indicators	
Facilities CCA (Refer to Figure 3-68)	
Speaker	This output device allows the technician to hear the audio output from the device selected in the RMS >> Commands >> Select Audio. The possible choices are: DME 1 Ident, DME 2 Ident
Power OK LED	This LED when lit (GREEN) indicates that the DC voltages are within tolerance.

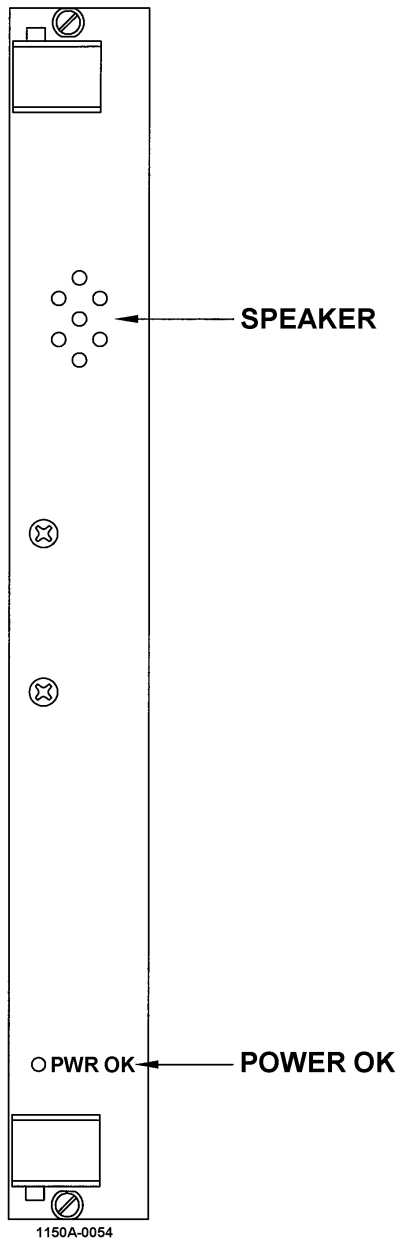


Figure 3-68 Facilities CCA

3.8.8 Synthesizer CCA (1A3A1, 1A3A11)

Refer to Figure 3-69 and Table 3-13 for the indicators and controls on the Synthesizer CCA.

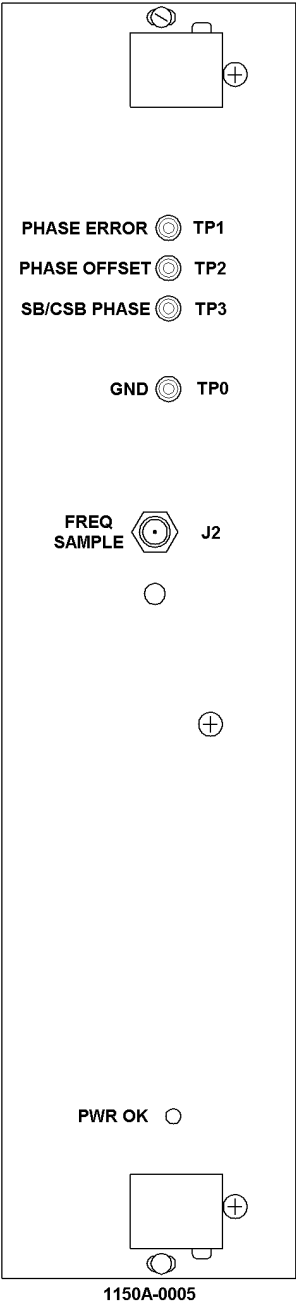


Figure 3-69 Synthesizer Controls and Indicators

Table 3-13 Synthesizer CCA (1A3A1, 1A3A11) Controls and Indicators	
TP0	This test point is available for scope or voltmeter ground.
TP1	Carrier Phase Error Voltage.
TP2	Carrier Phase Control Voltage.
TP3	DVOR Sideband to Carrier Phase Control Voltage.

3.8.9 Sideband Generator Assembly (1A4A1, 1A4A2, 1A4A5, 1A4A6)

Refer to [Figure 3-70](#) and [Table 3-14](#) for the indicators and controls on the Sideband Generator assembly. Refer to [paragraph 6.4.16](#) for alignment procedures.

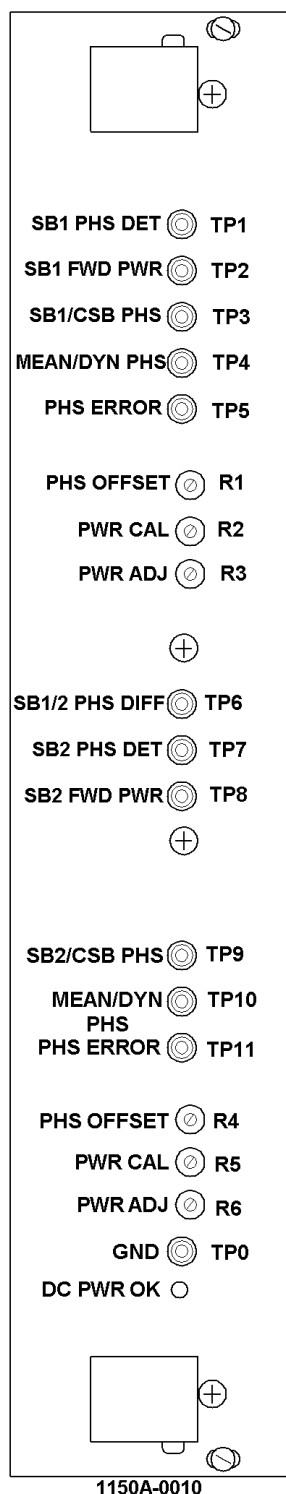


Figure 3-70 Sideband Generator Controls

Table 3-14 Sideband Generator (1A4A1, 1A4A2, 1A4A5, 1A4A6) Controls and Indicators	
TP0	Ground
TP1	Phase detector voltage. This is a DC voltage representing the detected phase difference of the input to the output of Sideband 1 (1A4A1, 1A4A5) or Sideband 3 (1A4A2, 1A4A6). If the control loop is locked this voltage should be nearly 0.9 volts.
TP2	This test point is the detected output of the Sideband 1 (1A4A1, 1A4A5) or Sideband 3 (1A4A2, 1A4A6) output. This signal is a rectified 360 Hz waveform in DVOR mode.
TP3	This test point is the Sideband 1 (1A4A1, 1A4A5) or Sideband 3 (1A4A2, 1A4A6) Manual Phase Control Voltage. This is a DC voltage representing the phaser control voltage used to align the phase between the Carrier amplifier and the sideband amplifier.
TP4	This test point is the Sideband 1 (1A4A1, 1A4A5) or Sideband 3 (1A4A2, 1A4A6) Mean Phase Control Voltage. This is a DC voltage representing the mean (slow) phaser control voltage.
TP5	This test point is the Sideband 1 (1A4A1, 1A4A5) or Sideband 3 (1A4A2, 1A4A6) Phase Error Voltage. This is a DC voltage representing the mean (slow) error control voltage. If the control loop is locked this voltage should be nearly 0.9 volts.
TP6	This test point is the Sideband to Sideband output Phase Error Voltage. This is a DC voltage represents the difference in phase in this assembly between Sideband 1 to 2 or Sideband 3 to 4. If the phase difference is 0 degrees this voltage should be nearly 0.0 volts.
TP7	Phase detector voltage. This is a DC voltage representing the detected phase difference of the input to the output of Sideband 2 (1A4A1, 1A4A5) or Sideband 4 (1A4A2, 1A4A6). If the control loop is locked this voltage should be nearly 0.9 volts.
TP8	This test point is the detected output of the Sideband 1 (1A4A1, 1A4A5) or Sideband 3 (1A4A2, 1A4A6) output. This signal is a rectified 360 Hz waveform in DVOR mode.
TP9	This test point is the Sideband 2 (1A4A1, 1A4A5) or Sideband 4 (1A4A2, 1A4A6) Manual Phase Control Voltage. This is a DC voltage representing the phaser control voltage used to align the phase between the Carrier amplifier and the sideband amplifier.
TP10	This test point is the Sideband 2 (1A4A1, 1A4A5) or Sideband 4 (1A4A2, 1A4A6) Mean Phase Control Voltage. This is a DC voltage representing the mean (slow) phaser control voltage.
TP11	This test point is the Sideband 2 (1A4A1, 1A4A5) or Sideband 4 (1A4A2, 1A4A6) Mean Phase Error Voltage. This is a DC voltage representing the mean (slow) error control voltage. If the control loop is locked this voltage should be nearly 0.9 volts.
R1	This adjustment point is the Sideband 1,3 Mean Phase Control Voltage Set Adjustment and is adjusted so that TP5 is 0.9 VDC along with TP4 between 2 and 10 VDC.
R2	This adjustment point is the Sideband 1,3 Detector Calibration Adjustment. It adjusts the power level displayed on the PMDT.
R3	This adjustment point is the Sideband 1,3 power output adjustment. Clockwise increases power. This is used for setting output power.
R4	This adjustment point is the Sideband 2,4 Mean Phase Control Voltage Set Adjustment and is adjusted so that TP7 is 0.9 VDC along with TP10 between 2 and 10 VDC.
R5	This adjustment point is the Sideband 2, 4 Detector Calibration Adjustment. It adjusts the power level displayed on the PMDT.
R6	This adjustment point is the Sideband 2, 4 power output adjustment. Clockwise increases power. This is used for setting output power.

3.8.10 Audio Generator CCA (1A3A2, 1A3A9)

Refer to Figure 3-71 and Table 3-15 for the indicators and controls on the Audio Generator CCA.

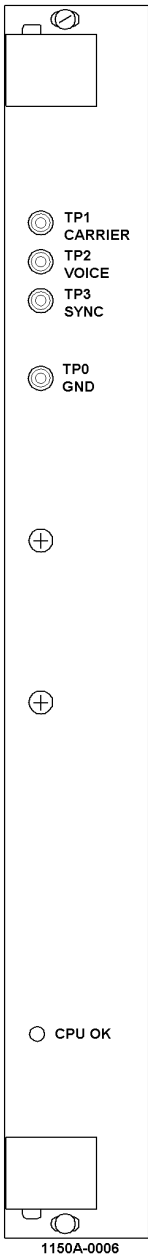


Figure 3-71 Audio Generator Controls and Indicators

Table 3-15 Audio Generator CCA (1A3A2, 1A3A9) Controls and Indicators	
TP0	Ground
TP1	Carrier Amplifier Modulation. Audio signal sent to the Carrier Amplifier to modulate the carrier
TP2	Voice modulation (with identification) audio prior to summation with the reference signal
TP3	Oscilloscope synchronization signal at 30 Hz.
CPU OK	This LED when lit (GREEN) indicates that the Audio Generator processor is operating normally

3.8.11 Low Voltage Power Supply (LVPS) CCA (1A3A4,1A3A8)

The LVPS has only a Power OK LED on the front panel to indicate when the internally generated power is within tolerance.

3.8.12 Test Generator CCA (1A3A5)

Refer to [Figure 3-72](#) and [Table 3-16](#) for the indicators and controls on the Test Generator CCA.

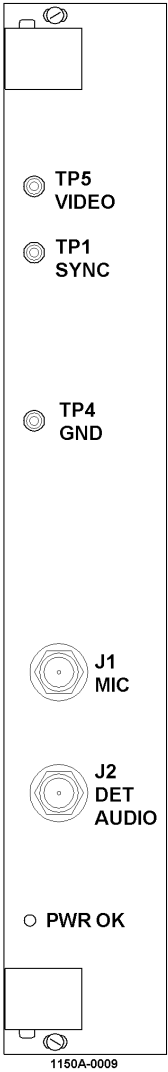


Figure 3-72 Test Generator Controls and Indicators

Table 3-16 Test Generator CCA (1A3A5) Controls and Indicators	
TP4	Ground
TP1	Scope Synchronization.
TP5	Test Generator audio signal
J1	Microphone input for voice modulation onto the carrier amplifier
J2	Detected voice/ identification modulation from the Monitor CCA
Power OK	This LED when lit (GREEN) indicates that the Test Generator internal power supplies are operating within limits.

3.8.13 RF Monitor Assembly (1A4A4)

Refer to Figure 3-73 and Table 3-17 for the indicators and controls on the RF Monitor assembly CCA.

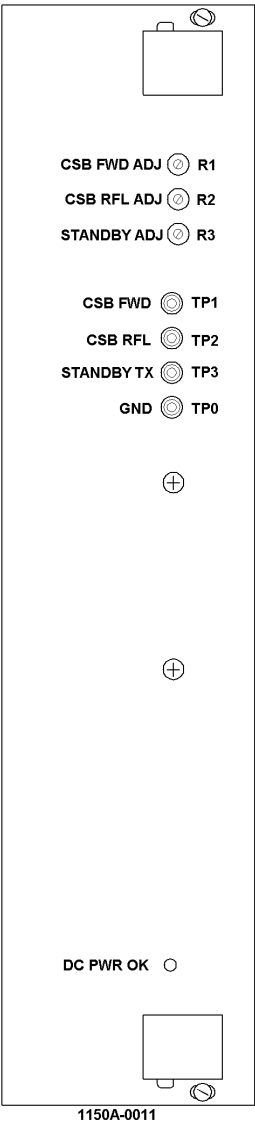


Figure 3-73 RF Monitor Controls and Indicators

Table 3-17 RF Monitor CCA (1A4A4) Controls and Indicators	
TP0	Ground
TP1	Detected Carrier Forward Power. The RF Monitor detects the forward power port of the directional coupler.
TP2	Detected Carrier Reflected Power. The RF Monitor detects the reflected power port of the directional coupler.
TP3	Detected Standby Power. The RF Monitor detects the power of the Standby Transmitter applied to the internal dummy load.
DC Power OK	This LED when lit (GREEN) indicates that the RF Monitor internal power supplies are operating within limits.

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4 STANDARDS AND TOLERANCES

4.1 INTRODUCTION

Table 4-1 is a list of equipment parameters, their standards, and their limits. In the Parameter column, each parameter measured or adjusted is listed. The paragraphs of Section 6 and Section 9 that describe the procedures used to establish the values of the parameters are listed in the Reference Paragraph column. In the Standard column are listed the optimum values of the parameters. The Initial Tolerance column is the maximum possible deviation, above or below the standard value, when the DVOR equipment is commissioned initially or subsequent to any modification. The Operating Tolerance column is the possible deviation, above or below the standard value, when the DVOR equipment is in operation after the completion of commissioning activities.

Table 4-1 Standards and Tolerances					
	Parameter	Standard	Initial Tolerance	Operating Tolerance	Reference Paragraph
a.	Antenna VSWR	1.0:1	$\leq 1.2:1$	$\leq 1.25:1$	
b.	Power Output				
	(1) Carrier	Value established by flight inspection	20% of standard (-1dB)	$\geq 50\%$ of standard (-3dB)	6.2.2 (Operating)
	(2) Sideband	For 30% AM	Value established by flight inspection	Standard, $\pm 2.0\%$ (Modulation)	6.2.4
c.	Frequencies				
	(1) Carrier	Assigned Freq.	Standard, $\pm 0.0005\%$	Nominal, $\pm 0.001\%$	6.2.3 (Initial and Operating)
	(2) 9960 Hz	9960 Hz	$\pm 0.02\%$	$\pm 0.02\%$	6.2.5 (Operating)
	(3) 30Hz Variable FM	30 Hz	$\pm 0.02\%$	$\pm 0.02\%$	6.2.5 (Operating)
	(4) 30Hz Reference AM	30 Hz	$\pm 0.02\%$	$\pm 0.02\%$	6.2.5 (Operating)
	(5) Ident	1020 Hz	± 1 Hz	± 2 Hz	6.2.11 (Initial and operating)
d.	Modulation				
	(1) 30 Hz	30%	$\pm 0.5\%$	$\pm 2\%$	6.2.4 (Operating)
	(2) 9960 Hz (AM)	30%	$\pm 0.5\%$	$\pm 2\%$	6.2.4 (Operating)
	(3) 9960Hz Deviation (FM)	16:1	± 1	± 1	6.2.4 (Operating)
	(4) Ident	8%	$\pm 1\%$	$\pm 2\%$	6.2.11 (Initial) 6.2.4 (Operating)
e.	Reflected Powers				
	(1) Reference VSWR	1.0:1	$\leq 1.25:1$	$\leq 1.25:1$	6.2.6 (Operating)
	(2) Sideband VSWR	1.0:1	$\leq 1.25:1$	$\leq 1.25:1$	6.2.6 (Operating)
f.	Monitor Alarms				
	(1) 30 Hz Modulation Low	28%	$\pm 2\%$	$\pm 1\%$	6.2.4 (Operating)
	(2) 30 Hz Modulation High	32%	$\pm 2\%$	$\pm 1\%$	6.2.4 (Operating)

Table 4-1 Standards and Tolerances					
Parameter		Standard	Initial Tolerance	Operating Tolerance	Reference Paragraph
	(3) 9960 Hz Modulation Low	28%	$\pm 0.2\%$	$\pm 1\%$	6.2.4 (Operating)
	(4) 9960 Hz Modulation High	32%	$\pm 0.2\%$	$\pm 1\%$	6.2.4 (Operating)
	(5) 9960 Hz Deviation Low	15:1	± 0.2	± 1	6.2.4 (Operating)
	(6) 9960 Hz Deviation High	17:1	± 0.2	± 1	6.2.4 (Operating)
	(7) Azimuth Shift Low	Established by flight inspection (FI) -1.0 Degree	± 0.2 degree	± 1.0 degree	6.2.4 (Operating)
	(8) Azimuth Shift High	Established by FI +1.0 Degree	± 0.2 degree	± 1.0 degree	6.2.4 (Operating)
j.	Monitor Limits				
	(1) Azimuth Angle Low	Established by FI -1.0 Degree	± 0.2 degree	Same As Initial	6.2.4 (Operating)
	(2) Azimuth Angle High	Established by FI +1.0 Degree	± 0.2 degree	Same As Initial	6.2.4 (Operating)
	(3) 30 Hz AM Modulation Low	Established by FI -1.8%	$\pm 0.2\%$	Same As Initial	6.2.4 (Operating)
	(4) 30 Hz AM Modulation High	Established by FI +1.8%	$\pm 0.2\%$	Same As Initial	6.2.4 (Operating)
	(5) 9960 Hz Modulation Low	Established by FI -1.8%	$\pm 0.2\%$	Same As Initial	6.2.4 (Operating)
	(6) 9960 Hz Modulation High	Established by FI +1.8%	$\pm 0.2\%$	Same As Initial	6.2.4 (Operating)
	(7) 9960 Hz Deviation Low	15.1	± 0.1	Same As Initial	6.2.4 (Operating)
	(8) 9960 Hz Deviation High	16.9	± 0.1	Same As Initial	6.2.4 (Operating)
	(9) Field Intensity Low	Established by FI -2.8dB	± 0.2 dB	Same As Initial	6.2.4 (Operating)
	(10) Field Intensity High	Established by FI +2.0dB	± 0.2 dB	Same As Initial	6.2.4 (Operating)
k.	Monitor Integrity Test Limits				
	(1) Azimuth Angle Low	Executive Monitor Radial -1.0°	Verified accurate to $\pm 10\%$ Limit by Test	Same As Initial	6.2.9 (Operating)
	(2) Azimuth Angle High	Executive Monitor Radial +1.0°	Verified accurate to $\pm 10\%$ Limit by Test	Same As Initial	6.2.9 (Operating)
	(3) 30 Hz AM Modulation Low	Established Modulation -2%	$\pm 0.2\%$	Same As Initial	6.2.9 (Operating)
	(4) 30 Hz AM Modulation High	Established Modulation +2%	$\pm 0.2\%$	Same As Initial	6.2.9 (Operating)
	(5) 9960 Hz Modulation Low	Established Modulation -2%	$\pm 0.2\%$	Same As Initial	6.2.9 (Operating)
	(6) 9960 Hz Modulation High	Established Modulation +2%	$\pm 0.2\%$	Same As Initial	6.2.9 (Operating)

Table 4-1 Standards and Tolerances					
Parameter		Standard	Initial Tolerance	Operating Tolerance	Reference Paragraph
k.	Monitor Integrity Test Limits				
	(7) 9960 Hz Deviation Low	Established Deviation Low	± 0.1	Same As Initial	6.2.9 (Operating)
	(8) 9960 Hz Deviation High	Established Deviation High	± 0.1	Same As Initial	6.2.9 (Operating)

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5 PERIODIC MAINTENANCE

5.1 INTRODUCTION

This section contains instructions for system level performance testing and maintenance of the VOR.

The DVOR is capable of continuous, unattended operation. Maintainability is based on a schedule consisting of a quarterly and annual performance checks. The performance checks are described in the paragraphs referenced in Section 6.

5.2 PERFORMANCE CHECK SCHEDULE

Table 5-1 is a summary of the various performance checks and their recommended intervals. Supervising personnel are responsible for scheduling these checks based on the recommended intervals. Information contained in Table 5-1 is limited to equipment specifically covered in this manual.

5.3 DOCUMENTATION AND DATA COLLECTION

The procedures and data collection tasks detailed in the maintenance procedures must be followed by detailed records of the measurements taken and the procedures performed. The regulatory agency associated with the location of the equipment is the authority on the content of data, the intervals between recordings and the format of data collected.

The 1150A provides the capability for saving and printing complete screen data sets in either text or graphical formats. Either format is suitable for historical performance records of the VOR. This data can be collected either locally or remotely through several RMM connections.

Table 5-1 Performance Check Schedule			
Performance Check Intervals can be extended in accordance with local regulations after the VOR demonstrates stability after installation.		Reference Paragraph	
		Standards and Tolerances	Maintenance Procedures
QUARTERLY	(Remote Operation)		
a.	Check Auto-Transfer	N/A	6.2.7
b.	Reassign Main/Standby Transmitters	N/A	6.4.4
c.	RCSU Operation Check	N/A	6.2.10
ANNUAL			
a.	Physical Inspections	N/A	6.3.1
b.	Check Carrier Output Power	Table 4-1.b	6.2.2
c.	Check Station Ident	Table 4-1.c	6.2.11
d.	Check Antenna VSWR	Table 4-1.a	6.2.6
e.	Check Battery Backup Transfer	N/A	6.2.1
f.	Check Carrier Frequency	Table 4-1.c	6.2.3
g.	Check Operating Frequency	Table 4-1.c	6.2.5
h.	Verify BITE Wattmeter Calibration	N/A	6.4.7
i.	Verify BITE Frequency Counter Calibration	N/A	6.4.6
j.	Verify BITE VSWR Calibration	N/A	6.4.5

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6 MAINTENANCE PROCEDURES

6.1 INTRODUCTION

This section provides the procedures required for accomplishing incidental maintenance activities. This section is divided into three parts: performance check procedures ([Paragraph 6.2](#)), other maintenance procedures ([Paragraph 6.3](#)), and special maintenance procedures ([Paragraph 6.3](#)).

6.1.1 Normal State Definition

Throughout the maintenance procedures the term NORMAL STATE refers to the following settings:

- All AC and DC circuit breakers ON
- Main Select set to Transmitter 1
- Transmitter 1 ON into antenna
- Transmitter 2 ON into dummy load (if dual equipment, hot standby)
- No monitors bypassed
- Local Control mode OFF
- Transmitter Ident Normal
- PMDT logged off

NOTE

These are the normal settings after pressing the RESET button when power is applied

6.1.2 Bypass State

The term BYPASS STATE refers to the following settings which can be accomplished by starting in the NORMAL STATE then performing the following steps:

1. Log on to the PMDT at Security Level 3 or higher. For reference the default user name is “SEC3” and password is “THREE”
2. Put the VOR in local mode by pressing the LOCAL CONTROL button on the LCU
3. Bypass the integral monitor (and standby monitor if dual equipment)

6.1.3 Turn OFF DVOR

The expression TURN OFF DVOR refers to turning OFF the Battery circuit breakers and then the AC circuit breakers.

6.1.4 Turn ON DVOR

The expression TURN ON DVOR refers to turning on the AC circuit breakers then the DC Buss circuit breakers on the BCPS assemblies and then the Battery DC circuit breakers.

6.1.5 Test Equipment

The performance checks are designed to make optimum use of the Built-in Equipment (BITE) by personnel responsible for the maintenance of the DVOR facility. The test equipment (or equivalent) listed in [Table 6-1](#) are required to perform DVOR maintenance procedures.

Table 6-1 Test Equipment	
Oscilloscope, Type TAS250 (Tektronics)	Detecting Elements Models 250B or 250C
Multimeter, Digital, Model 77 (Fluke)	Dummy Load, 5-T-N (Bird)
Frequency Counter, Model 1856D (B&K)	Type “N” Barrel (Qty. 2)
Power Meter, Model 4130A (Bird)	Type “N” Tee

6.2 PERFORMANCE CHECK PROCEDURES

Should abnormal performance occur during the performance check procedures, refer to [Section 7](#).

6.2.1 Battery Backup Transfer Performance Check

- a. Select RMS>>Status.
- b. With all cabinet circuit breakers in the ON position (AC and DC), turn off AC circuit breaker for Transmitter 1. Verify that the DVOR system continues to function and that “On Batteries” changes from No to Yes.
- c. If the VOR is a dual system, Turn off AC circuit breaker for Transmitter 2. Verify that the DVOR system continues to function and that “On Batteries” changes from No to Yes.
- d. Restore AC power for Transmitter 1 and Transmitter 2 if dual equipment. Verify that the system continues to function and that “On Batteries” changes from Yes to No for both systems if dual.

6.2.2 Carrier Output Power Performance Check

- a. Verify that transmitter 1 is operating.
- b. Select screen Transmitters>>Configuration>>Nominal. Verify Carrier Power is the same as commissioning normally 100 watts (en route) or 50 watts (terminal).
- c. Select VOR Transmitters>>Data>>Transmitter 1, observe that Carrier Power is within the operating tolerance of [Table 4-1\(b\)\(1\)](#). If not in tolerance perform alignment per [paragraph 6.4.7](#).
- d. For dual system change operating transmitter to 2 by pointing and clicking on the Sidebar Tx2 Antenna.
- e. Select screen Transmitters>>Data>>Transmitter 2, and observe that Carrier power is within the operating tolerance of [Table 4-1\(b\)\(1\)](#). If not in tolerance perform alignment per [paragraph 6.4.7](#).
- f. Change operating transmitter to 1 by pointing and clicking on the Sidebar Tx1 Antenna.

6.2.3 Carrier Frequency Performance Check

- a. Verify that transmitter 1 is operating.
- b. Connect frequency counter to “FREQ SAMPLE” jack J2 of Synthesizer Generator Assembly (1A3A1).
- c. Observe the station operating frequency on the frequency counter. Verify that the frequency is within the tolerance in [Table 4-1\(c\)\(1\)](#).
- d. For dual system connect frequency counter to “FREQ SAMPLE” jack J2 of Frequency Synthesizer assembly (1A3A11).
- e. For dual system change operating transmitter to 2 by pointing and clicking on the Sidebar Tx2 Antenna.
- f. Observe the station operating frequency on the frequency counter. Verify that the frequency is within the tolerance of [Table 4-1\(c\)\(1\)](#).
- g. Change operating transmitter to 1 by pointing and clicking on the Sidebar Tx1 Antenna.

6.2.4 Monitor 30 Hz and 9960 Hz Modulation Percentage and Deviation Ratio Performance Check

- a. Select Monitors, Data Integrity Screen on the PMDT.
- b. Observe the Monitor 1, 30 Hz modulation and verify it is within the alarm low and alarm high limits as indicated by the green background. (Red indicates out-of-tolerance)
- c. Observe Monitor 1, 9960 Hz modulation and verify it is within alarm low and alarm high limits.
- d. Observe Monitor 1, Deviation data and verify it is within alarm low and alarm high limits.
- e. Observe Monitor 1, Identification Modulation and verify it is within alarm low and alarm high limits.
- f. Observe Monitor 2, 30 Hz modulation and verify it is within the alarm low and alarm high limits.
- g. Observe Monitor 2, 9960 Hz modulation and verify it is within alarm low and alarm high limits.
- h. Observe Monitor 2, Deviation data and verify it is within alarm low and alarm high limits.
- i. Observe Monitor 2, Identification Modulation and verify it is within alarm low and alarm high limits.
- j. For dual transmitters, change operating transmitter by pointing and clicking Tx2 Antenna. Repeat steps a. through i. after Monitors have stabilized.
- k. Change operating transmitter to 1 by pointing and clicking on the Sidebar Tx1 Antenna.

6.2.5 Modulation Frequency Performance Check

- a. Verify that transmitter 1 is operating on antenna by pointing and clicking on the Sidebar Tx1 Antenna.
- b. Select Transmitters>> Data>>Transmitter 1.
- h. Verify that the 30 Hz AM frequency is within the tolerance of [Table 4-1\(c\)\(4\)](#).
- c. Verify the 30 Hz FM frequency is within the tolerance of [Table 4-1\(c\)\(3\)](#).
- d. Verify the 9960 Hz frequency is within the tolerance of [Table 4-1\(c\)\(2\)](#).

NOTE

The frequencies displayed are measured with enough precision to certify the operating tolerances of transmitter.

- e. For dual transmitters change operating transmitter to 2 by pointing and clicking Tx 2 antenna on the sidebar.
- f. Select Transmitters>> Data>> Transmitter 2 and allow the BITE data to update.
- g. Verify the 30 Hz AM frequency is within the tolerance of [Table 4-1\(c\)\(4\)](#).
- h. Verify the 30 Hz FM frequency is within the tolerance of [Table 4-1\(c\)\(3\)](#).
- i. Verify the 9960 Hz frequency is within the tolerance of [Table 4-1\(c\)\(2\)](#).
- j. Change operating transmitter to 1 by pointing and clicking on the Sidebar Tx1 Antenna.

6.2.6 Antenna VSWR Performance Check

- a. Verify that transmitter 1 is operating on antenna by pointing and clicking on the Sidebar Tx1 Antenna.
- b. Select Transmitters>> Data>>Transmitter 1. Observe Carrier VSWR and verify that this value is less than the Operating Tolerance of [Table 4-1\(e\)\(1\)](#). If out of tolerance refer to [paragraph 6.4.5](#).
- c. On the same screen, observe Sideband 1, Sideband 2, Sideband 3 and Sideband 4 VSWR. Verify that these values are less than Operating Tolerance of [Table 4-1\(e\)\(1\)](#). If out of tolerance refer to [paragraph 6.4.5](#).
- d. On screen Monitors>>Data>> Sideband Antenna VSWR observe the sideband antenna VSWR. Verify that no antennas are out of tolerance as indicated by an alert condition.

6.2.7 Automatic Transfer Performance Checks (Dual Equipment only)

- a. Log on to system. Select Local mode by pointing and clicking on the Local button. Select transmitter 1 as main by pointing and clicking the Tx1 main button.
- b. Enter the Transmitters>> Configuration>> Offsets and Scale Factors screen and record, then change the Azimuth Angle Offset for Transmitter 1 so that an out-of-tolerance condition exists for Monitor 1 and Monitor 2. Press F7 to apply.
- c. Verify that transmitter 1 turns off and approximately 20 seconds later transmitter 2 is energized on antenna
- d. Enter Transmitters>> Configuration>>Offsets and Scale Factors screen and restore the angle offsets to the original settings. Press F7 to apply.
- e. Select transmitter 2 as main by pointing and clicking on Tx 2 main button.
- f. Enter the Transmitters>>Configuration>>Offsets and Scale Factors screen and record, then change the Azimuth Angle Offset for Transmitter 2 so that an out-of-tolerance condition exists for Monitor 1 and Monitor 2. Press F7 to apply.
- g. Verify that transmitter 2 turns off and approximately 20 seconds later transmitter 1 is energized on antenna
Enter Transmitters>> Configuration>>Offsets and Scale Factors screen and restore the limits to the original settings. Press F7 to apply.
- h. Restore the appropriate Main transmitter to normal operation.

6.2.8 VOR Monitor Performance Check

- a. Select Monitor 1>>Data>>Status Screen.
- b. Verify that no maintenance alerts indications are backlit in yellow.
- c. Verify that no alarm indications are backlit in red.

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- d. Select Monitor 2>>Data>>Status Screen.
- e. Verify that no maintenance alerts are backlit in yellow.
- f. Verify that no alarm indications are backlit in red.

6.2.9 Monitor Integrity Test of VOR Monitor (Refer to Section 3.6.8.2.2)

- a. Select screen Monitor 1>>Test Results>>Completed.
- b. Verify azimuth angle, 30 Hz modulation, and 9960 Hz modulation, 9960 deviation, and Identification modulation parameters have passed the Integrity test as indicated by a green background for all parameters.
- c. Select screen Monitor 2>>Test Results>>Completed.

NOTE

All VOR Monitor Integrity tests are performed continuously in the background. The current status of the background test may be checked by selecting Monitor 1 (or 2) >> Test Results >> In Process.

6.2.10 RSCU Operation Performance Check

WARNING

This test removes the signal in space. A notice to airmen (NOTAM) must be issued prior to starting this test and planned with Air Traffic Control personnel.

6.2.10.1 Single Equipment Performance Check

- a. At the RSCU site perform a lamp test. Verify all indicators illuminate.
- b. Verify that the indicator for DVOR transmitter 1 Normal is on and the “COMM FAULT” is off.
- c. From the RSCU, turn off transmitter. Verify that the NORMAL indicator is off.
- d. Turn on the transmitter. Verify that the NORMAL indicator is on and the ALARM indicator is off.

6.2.10.2 Dual Equipment Performance Check

- a. Put the DVOR in normal configuration, with Transmitter 1 selected as main.
- b. At the RSCU site, perform a lamp test. Verify all indicators illuminate.
- c. Assure that the indicator for DVOR transmitter 1 NORMAL and antenna indicator “#1” on and the “COMM FAULT” indicator is off.
- d. Turn on the number 2 transmitter. Verify that the DVOR changes transmitters and the number 2 transmitter comes up normally. Verify the antenna indicator “#2” light is on. Press the alarm silence button.
- e. From the RSCU, turn off Transmitter 2. Turn on transmitter 1. Assure that the indicators for DVOR Transmitter 1 NORMAL and antenna indicator #1 lights are on. Press the alarm silence button.

6.2.11 Identification Frequency and Modulation Level Checks

- a. Place transmitter 1 on the air and place the monitors in bypass.
- b. Connect oscilloscope probe to Transmitter 1 Carrier Amplifier 1A5A3-P2. Select Transmitters>>Commands>>Transmitter Ident>>Continuous.
- c. Set Transmitters>>Configuration>>Reference and Voice Modulation to 0%.
- d. Adjust the oscilloscope controls to obtain a pattern showing 2 or 3 cycles of the 1020 identification modulation.
- e. Measure the high and low peak voltages and calculate the modulation by the following relation:

$$\% \text{ Ident Modulation} = \frac{E_{\text{max}} - E_{\text{min}}}{E_{\text{max}} + E_{\text{min}}}$$

- f. Verify that the modulation is within the tolerance of Table 4-1(d)(4).
- g. Measure the Ident frequency and verify it is within the tolerance of Table 4-1(c)(5).
- h. Turn on transmitter 2 by pointing and clicking the Tx 2 antenna button.
- i. Connect oscilloscope probe to Transmitter 2 Carrier Amplifier 1A5A4-P2.
- j. Measure the high and low peak voltages and calculate the modulation by the following relation:

$$\% \text{ Ident Modulation} = \frac{E_{\text{max}} - E_{\text{min}}}{E_{\text{max}} + E_{\text{min}}}$$

- k. Verify that the modulation is within the tolerance of Table 4-1(d)(4).
- l. Measure the Ident frequency and verify it is within the tolerance of Table 4-1(c)(5).
- m. Adjust Transmitters>> Configuration>> Reference and Voice Modulation to the previous settings.
- n. Select Transmitters>> Commands>> VOR Ident>> Normal.
- o. On the Monitors>> Data>> Integral screen, verify that the Ident is NORMAL.

6.3 EQUIPMENT INSPECTION PROCEDURES

6.3.1 Site Inspection

- a. Check that the site is clear of any new obstructions or materials which could affect the normal operation of the DVOR system.
- b. Check the shelter, inside and out, for any sign of water filtration, damage, or other deterioration.
- c. Check the condition of the air conditioner, shelter lighting, obstruction lights, baseboard heaters, electrical outlets, lightening arrestors, etc.
- d. Check for and remove any debris, accumulation of snow (over 4 inches, 10 cm), or ice (over 0.5 inches, 1.5 cm), on the field monitor antennas.
- e. Check for and remove any accumulation of debris or snow (over 1 foot, 30 cm) on the counterpoise surface.

6.3.2 Inspection of Transmission Antennas

- a. Insure that both DVOR transmitters are turned off.
- b. The DVOR antennas are contained within fiberglass radomes.
- c. Inspect the mating areas of the radomes where the radome interfaces with the radome base or where the radome interfaces with the antennas. Check for any signs of water leakage or deterioration. Repair or replace as necessary.
- d. If the radome shows water leakage, remove the radome and inspect the antenna for any signs of deterioration of water damage. Replace or repair the radome as necessary. Check the input cables and connectors for breaks, cracks or corrosion. Check that the connectors are securely fastened, and inspect the remaining parts of the antenna for damage or signs of vermin infestation.
- e. Inspect the counterpoise for any signs of deterioration, paying special attention to the welded joints, bolted connections, mesh, etc. Check for proper electrical connection between the counterpoise segments and grounding connections. Corrosion should be corrected by removing rust and applying paint or cold galvanizing spray.
- f. Remove any articles carried into the radome area and replace the antenna radome covers.

6.3.3 Inspection of the Field Monitor Antenna

- a. Inspect the condition of the field monitor antenna. Make sure it is solidly mounted, and that all nuts and bolts are tightened.
- b. Check the ground wire connection to earth ground, tighten connections if necessary.
- c. Inspect the condition of the field monitor antenna coaxial cables for signs of cracks or breakage. Replace if necessary.

6.3.4 Transmitter Cabinet Inspection

- a. Visually inspect interconnecting wire harnesses, coaxial cables and connectors for corrosion, cracks, breaks, and burns. Insure all RF connectors are tightened.
- b. Inspect all peripheral equipment connected to the DVOR, including the PMDT, printer, etc.
- c. Inspect the front panel indicators on the DVOR and assure that indicators are normal.

6.3.5 Battery Backup Unit Inspection

Refer to [Figure 9-4](#).

- a. Place the Battery circuit breakers on the battery boxes in the OFF position.
- b. Remove the covers from the battery boxes. Visually inspect the condition of each battery, and inspect the connectors and cables for any cracks, breaks, burns, or corrosion. Make sure that all connectors are fastened tightly to their terminals. Clean battery area if necessary.
- c. Replace the battery box covers and place the circuit breakers in the ON position.

6.4 ALIGNMENT PROCEDURES

6.4.1 Battery Charging Power Supply (BCPS) Alignment Procedures

6.4.1.1 System AC Voltage Alignment

- a. Put the VOR into the BYPASS STATE.
- b. Use a Digital Volt Meter (DVM) to measure the AC input voltage from AC Monitor (1A6) TB3 terminal 1 to 2 (TX POWER, LINE and NEUTRAL).
- c. Use the PMDT to display RMS >> RMS Data >> Power Supply Data, AC Input volts and verify the reading is within 1 VAC of DVM measurement.
- d. If not within 1 VAC adjust 1A5A1 BCPS R30 so the RMS >> RMS Data >> Power Supply Data, AC Input volts is within 1 VAC of DVM measurement.
- e. For single transmitter equipment skip to step i.
- f. Turn off Transmitter 1 AC and DC breakers.
- g. Use the PMDT to display RMS >> RMS Data >> Power Supply Data, AC Input volts and verify the reading is within 1 VAC of DVM measurement.
- h. If not within 1 VAC adjust 1A5A2 BCPS R30 so the RMS>>RMS Data>> Power Supply Data, AC Input volts is within 1 VAC of DVM measurement.
- i. Restore the VOR to the NORMAL STATE.

6.4.1.2 System AC Current Alignment

- a. Turn off AC and DC circuit breakers.
- b. At the shelter circuit breaker panel turn off AC power for the VOR station.
- c. Disconnect the wire from the AC source to AC Monitor (1A6) TB3 position 1(TX POWER, LINE).
- d. Connect a Digital Volt Meter (DVM) configured for current measurement in line with the wire from AC source to Monitor (1A6) TB3 position 1 (TX POWER, LINE). Set the DVM to measure AC current using a 10A scale.
- e. Restore AC power to the VOR at the circuit breaker panel.
- f. Turn on AC and DC circuit breakers.
- g. Put the VOR into the BYPASS STATE.
- h. Use the PMDT to display RMS >> RMS Data >> Power Supply Data, AC Input Amps and verify the reading is within 0.3 amps of DVM reading.
- i. If not within 0.3 amps adjust 1A5A1 BCPS R56 so the RMS >> RMS Data >> Power Supply Data, AC Input Amps is within 0.3 amps.
- j. For single equipment skip to step n.
- k. Turn off Transmitter 1AC and DC breakers while leaving Transmitter 2 AC and DC breakers on.

- l. Use the PMDT to display RMS >> RMS Data >> Power Supply Data, AC Input Amps and verify the reading is within 0.3 amps of DVM reading.
- m. If not within 0.3 amps adjust 1A5A2 BCPS R56 so the RMS >> RMS Data >> Power Supply Data, AC Input Amps is within 0.3 amps.
- n. Turn off TX 1 and TX 2 AC and DC circuit breakers.
- o. At the shelter circuit breaker panel turn off AC power for the VOR station.
- p. Remove the DVM and reconnect the AC line wire to the AC Monitor (1A6) TB3 position 1.
- q. Restore AC power to the VOR at the circuit breaker panel.
- r. Restore the VOR to the NORMAL STATE.

6.4.1.3 Obstruction Light AC Voltage Alignment

- a. Use a Digital Volt Meter (DVM) configured for AC voltage to measure across AC Monitor (1A6) TB1 position 1 and position 3.

NOTE

Terminal TB1-1 is normally connected to TB1-2 when a photo sensor is not used with the obstruction light. When using a photo sensor the light opening must be covered with an opaque object in order to force the obstruction light to turn on.

- b. Use the PMDT to display RMS >> RMS Data >> Power Supply Data, OB Light volts and verify the reading is within 2 VAC of DVM measurement.
- c. If not within 2 VAC adjust 1A5A1 BCPS R29 so the RMS >> RMS Data >> Power Supply Data>> OB Light volts is within 1 VAC of DVM measurement.
- d. For single transmitter equipment skip to step h.
- e. Turn off Transmitter 2 AC and DC breakers while leaving Transmitter 2 AC and DC breakers on.
- f. Use the PMDT to display RMS >> RMS Data >> Power Supply Data, OB Light volts and verify the reading is within 2 VAC of DVM measurement.
- g. If not within 2 VAC adjust 1A5A2 BCPS R29 so the RMS>>RMS Data>> Power Supply Data>> OB Light volts is within 2 VAC of DVM measurement.
- h. Restore the VOR to the NORMAL STATE.

6.4.1.4 Obstruction Light AC Current Alignment

- a. Turn off AC and DC circuit breakers.
- b. At the shelter circuit breaker panel turn off AC power for the VOR station including obstruction lights.
- c. Disconnect the wire from the AC source to AC Monitor (1A6) TB1 position 2 (LINE).
- d. Connect a Digital Volt Meter (DVM) in line with the wire from AC Monitor (1A6) TB1 position 2 (OB LITE, LINE). Set the DVM to measure AC current using a 10A scale.

NOTE

Terminal TB1-1 is normally connected to TB1-2 when a photo sensor is not used with the obstruction light. When using a photo sensor the light opening must be covered with an opaque object in order to force the obstruction light to turn on.

- e. Disconnect any equipment connected to the front panel AC convenience outlet on the 1A7 Status Panel.
- f. Connect a Digital Volt Meter (DVM) in line with the wire from AC Monitor (1A6) TB1 position 2 (OB LITE, LINE). Set the DVM to measure AC current using a 10A scale.
- g. Restore AC power to the VOR and obstruction light at the circuit breaker panel.
- h. Use the PMDT to display RMS >> RMS Data >> Power Supply Data, OB Light Amps and verify the reading is within 0.3 amps of DVM reading.
- i. If not within 0.3 amps adjust 1A5A1 BCPS R44 so the RMS >> RMS Data >> Power Supply Data, OB Light Amps is within 0.3 amps.
- j. For single equipment skip to step n.
- k. Turn off Transmitter 1 AC and DC breakers leaving Transmitter 2 circuit breakers on.

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- l. Use the PMDT to display RMS >> RMS Data >> Power Supply Data, OB Light Amps and verify the reading is within 0.3 amps of DVM reading.
- m. If not within 0.3 amps adjust 1A5A2 BCPS R44 so the RMS >> RMS Data >> Power Supply Data, OB Light Amps is within 0.3 amps.
- n. At the shelter circuit breaker panel turn off AC power for the VOR obstruction lights.
- o. Remove the DVM and reconnect the OB LITE line wire to the AC Monitor (1A6) TB1 position 2.
- p. Restore AC power to the VOR obstruction light at the circuit breaker panel.
- q. Restore the VOR to the NORMAL STATE.

6.4.2 Alarm Volume Adjustment Procedure

- a. Locate the Volume adjust pot at the bottom right of the System Controls on the 1A1 LCU.
- b. Press the lamp test switch to activate the audio alarm.
- c. Using the adjustment tool provided with the accessory kit, adjust the volume pot clockwise to increase the volume or counterclockwise to lower the volume until the desired sound level is obtained.

6.4.3 RMS Facilities Exterior and Interior Temperature Calibration

- a. If a precision thermometer is not available then skip this procedure.
- b. Put the VOR into the BYPASS STATE.
- c. Select RMS >> DATA >> A/D DATA.
- d. If an external Temperature Sensor Assembly is connected to J7 of the 1A9 Interface CCA then adjust 1A19R41 until the PMDT "Outside Temperature" display matches the temperature shown on an external thermometer as it is located near the Temperature Sensor Assembly.
- e. Adjust 1A9R42 until the "Inside Temperature" display matches the temperature shown on an internal thermometer as it is located near the 1A9 Interface CCA.
- f. Restore the VOR to the NORMAL STATE.

6.4.4 Reassign Main/Standby Transmitters (Dual Systems Only)

- a. Log on to the PMDT.
- b. Point and click on the Tx 1 Main or the Tx 2 Main Button as desired on Sidebar.

6.4.5 Verification of BITE VSWR Calibration

- a. Use the PMDT to turn both transmitters off.
- b. Disconnect the Carrier feed cable from the top of the DC1 directional coupler in the DVOR cabinet. Connect a type "N" barrel to the directional coupler. Connect a type "N" TEE to the barrel and attach a 250W load to the TEE. Attach type "N" barrel to the remaining open port of the TEE. This simulates a 1.22:1 load. If a 250 Watt load is not available a 25 Watt load may be used for less than 1 minute for this test.
- c. Turn on transmitter 1 by pointing and clicking the Tx 1 Antenna button. Place transmitter in BYPASS by pointing and clicking the Bypass button.
- d. Select screen Transmitters>>Data>> Transmitter 1 observe Carrier VSWR. The display VSWR should be between 1.20 to 1.23.
- e. If the level is not within this range, carefully adjust (on the 1A4A4 RF Monitor Assembly) the transmitter reflected power detector potentiometer 1A4A4 R2 (TX RFD). Turning the pot clockwise will increase VSWR reading and counterclockwise will decrease. Make a small adjustment and wait for display to stabilize.
- f. Point and click the OFF button for Transmitter 1 and Transmitter 2.
- g. Move the barrel, bullet, and TEE to the Sideband 1 feed cable at 1A11J25. Place a 5W termination on the TEE output. Place the Carrier Transmitter cable back to its original position.
- h. Turn on transmitter 1 by pointing and clicking the Tx 1 Antenna button. Place transmitter in BYPASS by pointing and clicking the Bypass button.

- l. Select screen Monitors>>Data>>Sideband Antenna VSWR, observe odd numbered Antenna VSWR. The displayed VSWR should be between 1.20 to 1.27 for odd numbered antennae. If not within range then the 1A4A1 Sideband amplifier (with built-in VSWR measurement circuitry) should be replaced.
- m. Turn both transmitters off. Move the load barrel, bullet, and TEE to the Sideband 2 feed cable at 1A10J25.
- n. Turn on both transmitters. Select screen Monitors>> Data>> Sideband Antenna VSWR, observe even numbered Antenna VSWR. The displayed VSWR should be between 1.20 to 1.27 for even numbered antennae. If not within range then the 1A4A1 Sideband amplifier (with built-in VSWR measurement circuitry) should be replaced.
- o. Turn off both transmitters. Remove termination, TEE and bullet. Place cables in their original positions.
- p. Turn the system on and clear the bypass condition by clicking by clicking on the bypass button.

6.4.6 Verification of BITE Frequency Counter Calibration

- a. Turn off AC/DC power.
- b. Remove Transmitter 1 Audio Generator 1A3A2 and place on an extender CCA.
- c. Turn on power. Log onto the PMDT and turn on Transmitter 1 by clicking the Tx 1 Antenna Button on the side bar.
- d. Connect a frequency counter probe to TP24 on 1A3A2.
- e. Observe the 30 Hz AM frequency on Transmitter Data >> Transmitter 1 and verify it is within $\pm 1.0\%$ of the reading from the frequency counter.
- f. Connect the external frequency counter to 1A3A1-J2 on the Transmitter 1 Synthesizer.
- g. Observe the Carrier frequency on Transmitter Data >> Transmitter 1 and assure it is within $\pm 1.0\%$ of the reading from the frequency counter.
- h. Turn off AC/DC power on VOR front panel. Remove the Audio Generator 1A3A2 CCA from extender. Put the Transmitter 2 Audio Generator CCA 1A3A9 on extender.
- i. Turn on AC/DC power on VOR front panel. Change operating transmitter to 2 by pointing to Tx 2 antenna on the sidebar..
- j. Connect a frequency counter probe to TP24 on 1A3A9.
- k. Observe the 30 Hz AM frequency on Transmitter Data >> Transmitter 2 and verify it is within $\pm 1.0\%$ of the reading from the frequency counter.
- l. Connect the frequency counter to 1A3A11-J2 on the Transmitter 2 Synthesizer.
- m. Observe the Carrier frequency on Transmitter Data >> Transmitter 2 and assure it is within $\pm 1.0\%$ of the reading from the frequency counter.
- n. Turn off the power and remove Transmitter 2 Audio Generator CCA 1A3A9 from extender and place the Audio Generator CCA back into its original position.

6.4.7 Verification of BITE Wattmeter Calibration

- a. Point and click the of f button to turn off both VOR transmitters
- b. Insert a 250 Watt plug-in element into the thru-line wattmeter body in the carrier feed cable.
- c. Point and click the Tx 1 antenna button to turn on Transmitter. Point and click the Bypass button to place the transmitter in BYPASS.
- d. Select screen Transmitters >> Data>> Tx 1, observe Carrier power output. The displayed output is to coincide with the external wattmeter indication.
- e. If the levels are not the same, carefully adjust (on the 1A4A4 RF Monitor Assembly) the CSB FWD potentiometer, 1A4A4R1 (CSB FWD ADJ). Turning the pot clockwise will decrease power reading and counterclockwise will increase.
- f. Point and click the off button to turn off both VOR transmitters.
- g. Insert a 5 Watt plug-in element into the thru-line wattmeter body in the Sideband 1 feed cable, 1A11J25.
- h. Turn on Tx 1. Select screen Transmitters>> Data>> Tx 1. Observe Sideband 1 power output. The displayed output power is to coincide with the external wattmeter indication.
- i. If the levels are not the same, carefully adjust the Sideband 1 forward power detector potentiometer 1A4A1R2 located on the Sideband Generator Assembly.
- j. Point and click on Tx 2 Antenna button to change Transmitters.
- k. Select screen Transmitters>> Data>> Tx 2. Observe Sideband 1 power output.

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- l. If the levels are not the same, carefully adjust Transmitter 2 Sideband 1 forward power detector potentiometer 1A4A6R2 located on the Sideband Generator Assembly.
- m. Point and click the off button to turn off both VOR transmitters.
- n. Move the 5 Watt plug-in element and the thru-line wattmeter body from the Sideband 1 output to the Sideband 2 output at 1A10J25.
- o. Turn on Tx 1. Select screen Transmitters>> Data>> Tx 1. Observe Sideband 2 power output.
- p. If the levels are not the same, adjust the Sideband 2 forward power detector potentiometer 1A4A1R5 located on the Sideband Generator Assembly.
- q. Point and click on Tx 2 Antenna button to change Transmitters.
- r. Select screen Transmitters>> Data>> Tx 2. Observe Sideband 2 power output.
- s. If the levels are not the same, carefully adjust Transmitter 2 Sideband 2 forward power detector potentiometer 1A4A6R5 located on the Sideband Generator Assembly.
- t. Point and click the off button to turn off both VOR transmitters.
- u. Move the 5 Watt plug-in element and the thru-line wattmeter body from the Sideband 2 output to the Sideband 3 output at 1A11J26.
- v. Turn on the Transmitter. Select screen Transmitters>> Data>> Tx 1. Observe Sideband 3 power output.
- w. If the levels are not the same, carefully adjust the Sideband 3 forward power detector potentiometer 1A4A2R2 located on the Sideband Generator Assembly.
- x. Point and click on Tx 2 Antenna button to change Transmitters.
- y. Select screen Transmitters>> Data>> Tx 2. Observe Sideband 3 power output.
- z. If the levels are not the same, carefully adjust Transmitter 2 Sideband 3 forward power detector potentiometer 1A4A6R2 located on the Sideband Generator Assembly.
- aa. Point and click the off button to turn off both VOR transmitters.
- bb. Move the 5 Watt plug-in element and the thru-line wattmeter body from the Sideband 3 output to the Sideband 4 output at 1A10J26.
- cc. Turn on the Transmitter. Select screen Transmitters>> Data>> Tx 1. Observe Sideband 4 power output.
- dd. If the levels are not the same, carefully adjust the Sideband 4 forward power detector potentiometer 1A4A2R5 located on the Sideband Generator Assembly.
- ee. Point and click on Tx 2 Antenna button to change Transmitters.
- ff. Select screen Transmitters>> Data>> Tx 2. Observe Sideband 4 power output.
- gg. If the levels are not the same, carefully adjust Transmitter 2 Sideband 4 forward power detector potentiometer 1A4A6R5 located on the Sideband Generator Assembly.
- hh. Point and click the off button to turn off both VOR transmitters.
- ii. Remove the wattmeter body from the Sideband 4 output at 1A10J26.
- jj. Take the system out of BYPASS by pointing and clicking on the bypass button.

6.4.8 RMS Lithium Battery Check Procedure

- a. Turn the VOR transmitter AC and DC breakers off.
- b. Observing ESD precautions pull out the 1A3A6 RMS CCA and place on an ESD protective surface.
- c. Verify JP1 is connected between pins 2-3 to enable battery backup.
- d. Measure the DC voltage across the lithium battery B1.
- e. Verify that the battery voltage is greater than or equal to 2.9 VDC at a room temperature of 20±5°C.
- f. Replace the battery if necessary.
- g. Place the RMS CCA into the rack and restore the VOR to the NORMAL STATE.

6.4.9 Replacing RMS CPU (1A3A6) CCA

- a. On the PMDT Select System>> Configuration Save. Select or create a distinctive filename to save the current system configuration and click save.
- b. Turn off AC/DC power on VOR front panel.
- c. Observing ESD precautions, disconnect the front connector and pull the RMS CCA (1A3A6) forward until it is clear of the transmitter cabinet
- d. Insert the new RMS CCA into the cabinet and seat securely into backplane connector. Reconnect the front card edge connector.

- e. Turn on AC/DC power on VOR front panel.
- f. Place the VOR in LOCAL mode. Select System>> Configuration Load, and select the Filename saved in Step a.
- g. Select RMS>> Config Backup.
- h. Set the current date and time by selecting RMS>> Commands>> Set Time and Date, [enter].

6.4.10 Update of DVOR Software

NOTE

During the product life cycle software updates may become available for the VOR product in service. The RMS, Monitor and Audio Generator software is updated through the PMDT port using a SELEX-SI software product called “Flash loader” Please refer to the installation instructions accompanying the software update service bulletin for detailed software upgrade procedures.

- a. On the PMDT Select System>> Configuration Save. Select or create a distinctive filename to save the current system configuration and click save.
- b. Perform the software update per the instruction provided.
- c. Place the VOR in LOCAL mode. Select System>> Configuration Load, and select the Filename saved in Step a.
- d. Select RMS>> Config Backup.
- e. Set the current date and time by selecting RMS>> Commands>> Set Time and Date, [enter].

6.4.11 Changing the Station Rotation (Azimuth)

This step may be requested during a flight inspection of the VOR station.

- a. Select Transmitters>> Configuration>> Offsets. Adjust the Azimuth angle offset for Transmitter 1 and/or Transmitter 2.
- b. Enter a more positive number for clockwise rotation or a more negative number for counterclockwise rotation. The allowable entry is ±180 degrees in 0.01 degree increments.

6.4.12 Changing the Monitoring Offsets

This procedure is required after commissioning flight check to make the monitors agree with flight inspection results.

- a. Turn on Transmitter 1 by clicking on Tx1 on the side bar
- b. Select Monitors>> Data >> Integrity and view Data.
- c. Select Monitors>> Configuration>> Offsets and Scale Factors. Enter the new azimuth offset for Monitor 1 and Monitor 2 under the Field Detector column.
- d. Select Monitors>> Data>> Integrity data. Verify that the Azimuth value displayed is correct.
- e. Compute the 30 Hz Modulation correct factors by the formula:

$$\frac{30.0}{\text{Current Reading}} \times \text{Current Offset.}$$

- f. Select Monitors>> Configuration>> Offsets and Scale factors and read the current 30 Hz modulation offset and apply the formula if step e.
- g. Enter the new offset value for Monitor 1 and Monitor 2, 30 Hz modulation under the Field Detector Column.
- h. Repeat steps e, f, and g for 9960 Hz Modulator and 9960 Hz deviation ratio.
- i. Compute the field intensity offset by reading the field intensity value in Monitors>> Data>> Integrity data and subtracting the reading from 0.0.
- j. For values that are greater than 1 dB adjust the Monitor attenuation in Monitor>> Configuration>> Alarm Limits.

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- k. Read the field intensity value in Monitors>> Data>> Integrity data and subtract the reading from 0.0. The change should be less than 1 dB.
- l. Place this offset value in Monitors>> Configuration>> Offsets and Scale Factors for Monitor 1 and for Monitor 2.

6.4.13 DME Keying Check

This procedure is used on systems where the DVOR is collocated with a DME.

- a. Place the DVOR in normal.
- b. Select (on VOR) RMS>>Commands>>Select Audio>Transmitter 1 Ident.
- c. Place DME in normal.
- d. Verify audible DME keying. Select (on SELEX-SI DME) RMS>>Commands>>Select Audio>Transmitter 1 Ident.
- e. If keying is not detected or is not in synchronization with the DVOR check terminal board wiring and connections.

6.4.14 DVOR Frequency Synthesizer Alignment

The following procedure must be used to properly align the Frequency Synthesizer Assembly for operation at a new frequency. References to the 1A3A1 Frequency Synthesizer Assembly are for Transmitter 1 and references to the 1A3A11 Frequency Synthesizer are for DVOR Transmitter No. 2.

NOTE

The RF power level at 1A3A1J2 on the front panel of the Frequency Synthesizer Assembly can be as high as +15 dBm. In the following step, use attenuators as appropriate for the frequency counter used to properly protect any counter input ports.

- a. Connect a frequency counter to 1A3A1J2, the SMA connector on the front panel of the Frequency Synthesizer Assembly.
- b. Turn on Tx 1.
- c. Measure the output frequency of the 1A3A1J2 Frequency Synthesizer Assembly. If the measured frequency is outside the Operational Tolerance of Table 4-1(c) then perform the following steps:
 - i. Remove power from the DVOR.
 - ii. Remove the Frequency Synthesizer 1A3A1 from the VOR cabinet.
 - iii. Connect the 1A3A1 Frequency Synthesizer Assembly to the DVOR with extender board.
 - iv. Apply power to the DVOR. Turn on Tx 1. Place Monitor in Bypass.
 - v. The 10.000 MHz TCXO (Y1) in the Frequency Synthesizer Assembly may be adjusted to correct the operating frequency. Small adjustments can be made to Y1 with the R27 potentiometer to achieve this. Once the TCXO is set the station frequency should be within the Initial Tolerance of [Table 4-1\(c\)](#).
 - vi. Remove power from the DVOR.
 - vii. Replace the Frequency Synthesizer Assembly in the system cabinet.
 - viii. Apply power to the DVOR.

NOTE

Placing the Frequency Synthesizer Assembly on the extender board may cause VOR Monitor to indicate an alarm condition. The alarm may be caused by carrier phase control loop unlock or phase difference of the Carrier to Sidebands. There will be no effect on the frequency counter readings taken at the test port output, J2 on the front panel of the Frequency Synthesizer Assembly.

- d. Connect a DMM to the carrier phase loop error voltage at TP1 on the 1A3A1 Frequency Synthesizer Assembly front panel.
- e. Log in to the PMDT and select Transmitters>> Configuration. Adjust Tx 1 Carrier PLL control from 0 to 100% to achieve 0.0 +/- 0.05 volts on TP1.

- f. Measure the voltage at 1A3A1TP2, carrier phase loop control voltage. This voltage must be between 2 volts and 8 volts.
- g. Adjustment of the Transmitters>> Configuration >>Carrier PLL control can result in two different settings that result in 0.0 +/- 0.05 volts on TP1. If TP2 is below 2 volts, or above 8 volts repeat steps e and f until the result 0.0 +/- 0.05 volts on TP1 with TP2 between 2 and 8 volts is achieved.
- h. Connect a frequency counter to 1A3A11J2, the SMA connector on the front panel of the Tx 2 Synthesizer Assembly.
- i. Measure the output frequency of the 1A3A11J2 Frequency Synthesizer Assembly. If the measured frequency is outside the Operational Tolerance of [Table 4-1\(c\)](#) then perform the following steps:
- j.
 - i. Remove power from the DVOR.
 - ii. Remove the Frequency Synthesizer 1A3A11 from the VOR cabinet.
 - iii. Connect the 1A3A11 Frequency Synthesizer Assembly to the DVOR with extender board.
 - iv. Apply power to the DVOR. Turn on Tx 2. Place the Monitor in Bypass.
 - v. The 10.000 MHz TCXO (Y1) in the Frequency Synthesizer Assembly may be adjusted to correct the operating frequency. Small adjustments can be made to Y1 with the R27 potentiometer to achieve this. Once the TCXO is set the station frequency should be within the Initial Tolerance of [Table 4-1\(c\)](#).
 - vi. Replace the Frequency Synthesizer Assembly in the system cabinet.
 - vii. Apply power to the DVOR.
- k. Connect a DMM to the carrier phase loop error voltage at TP1 on the 1A3A11 Frequency Synthesizer Assembly front panel.
- l. Log in to the PMDT and select Transmitters>> Configuration. Adjust Tx 2 Carrier PLL control from 0 to 100% to achieve 0.0 +/- 0.05 volts on TP1.
- m. Measure the voltage at 1A3A11 TP2, carrier phase loop control voltage. This voltage must be between 2 volts and 8 volts.
- n. Adjustment of the Transmitters>> Configuration.>> Carrier PLL control can result in two different settings that result in 0.0 +/- 0.05 volts on TP1. If TP2 is below 2 volts, or above 8 volts repeat steps e and f until the result 0.0 +/- 0.05 volts on TP1 with TP2 between 2 and 8 volts is achieved.

6.4.15 DVOR Sideband Amplifier Alignment

The following procedure is to be used to optimize the sideband generator amplifiers for operation. Instructions are provided using the 1A4A1 lower Sideband Generator Assembly; substitute 1A4A2 when performing the procedures on Tx 1 upper Sideband Generator Assembly. Substitute 1A4A5 when performing the procedures on Tx 2 lower Sideband Generator Assembly or substitute 1A4A6 when performing the procedures on transmitter Tx 2 upper Sideband Generator Assembly.

- a. Turn the DVOR power off.
- b. Pull 1A4A1 forward and move the jumper at J11 to the position shown in [Table 6-2](#) below.
- c. Place the 1A4A1 back into the rack.
- d. Turn the DVOR power on. Turn on the Transmitter and place in bypass.
- e. Refer to [Figure 3-66](#). Connect a DVM to 1A4A1 TP4. Adjust 1A4A1R1 for DVM voltage per [Table 6-2](#) for the frequency of operation as a starting point. The actual value may change due to component tolerance.
- f. Connect a DVM to 1A4A1 TP10. Adjust 1A4A1R4 for DVM voltage per [Table 6-2](#) for the frequency of operation.
- g. Connect a DVM to 1A4A1 TP1. Adjust 1A4A1R1 for 0.90 to .95 Vdc.
- h. Connect a DVM to 1A4A1 TP5. Adjust 1A4A1R1 for 0.89 to .91 Vdc.
- i. Connect DVM to 1A4A1TP4. Verify that the voltage is between 2 and 9 Vdc.
- j. If the voltage is within this range then move to step n below. If not within this range then perform steps j through m below.
- k. Turn off power.
- l. Pull 1A4A1 forward and move the jumper at J11 from the present position (connected from 1 to 2 or connected from 3 to 4) to the opposite position.
- m. Place the 1A4A1 back into the rack.

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- n. Turn on power, turn on the Transmitter and place in bypass.
- o. Connect a DVM to 1A4A1 TP5. Adjust 1A4A1R1 for 0.89 to .91 Vdc.
- p. Connect DVM to 1A4A1TP4. Verify that the voltage is between 2 and 9 Vdc.
- q. Refer to [Figure 3-66](#). Connect a DVM to 1A4A1 TP7. Adjust 1A4A1R4 for 0.9 to 0.95 Vdc.
- r. Connect a DVM to 1A4A1 TP11. Adjust 1A4A1R1 for 0.89 to .91 Vdc.
- s. Connect DVM to 1A4A1TP10. Verify that the voltage is between 2 and 9 Vdc. If not repeat steps n and o to select a different point of adjustment.
- t. Connect a DVM to 1A4A1 TP6.
- u. Adjust Transmitters>>Configuration>>Tx 1 SB1 or SB2 Phase offset to achieve 0.0 +/- 0.1 volts on TP6. Set the value so that difference is centered about 0 degrees phase shift. For example if 10 degrees difference between Sideband 1 and Sideband 2 is required then set Sideband 1 to -5 degrees and Sideband 2 to +5 degrees.
- v. Select RMS>> Data>> Maintenance Alerts/Alarms Screen. The SB1/2 Phase, SB3/4 Phase should be clear (not alert indication).
- w. Select RMS>> Data>> Maintenance Alerts/Alarms Screen. The SB1/2 Phase, SB3/4 Phase should be clear (not alert indication).

Table 6-2 Typical Mean Phaser Settings vs Frequency		
Frequency (MHz)	Mean Phase Voltage TP4/TP10 (Vdc)	Jumper Setting for J11
108	3.0	1 to 2
109	3.4	1 to 2
110	3.9	1 to 2
111	4.5	1 to 2
112	5.0	3 to 4
113	2.8	3 to 4
114	3.1	3 to 4
115	3.6	3 to 4
116	4.0	3 to 4
117	4.5	3 to 4
118	5.0	3 to 4

6.4.16 Antenna VSWR Check for New Frequency

All of the radiating antennas in the DVOR antenna system were installed with an initial VSWR that was less than 1.10:1 ([Table 4-1a](#)). DVOR antennas are narrow-band devices that are critically tuned using mechanical components (stubs, positioning pieces, and capacitors) to produce a resonant antenna that is matched to a 50 ohm impedance feed cable. Any significant change in the operating frequency of the DVOR will change the resonant point of operation of the antenna and that will affect the VSWR of the antenna and the signal in space of the DVOR system. Perform the following procedures to determine if there is a need to retune the antenna system.

- a. Remove power from the DVOR.
- b. Install a power meter (Bird model 43 or equivalent) in the carrier antenna feed cable.
- c. Install a 100 W or 250 Watt detecting element in the wattmeter to measure forward power.
- d. Turn on the DVOR and record the DVOR carrier forward power.
- e. Install a 1 W or 5 W detecting element in the wattmeter to measure reflected power.
- f. Record the DVOR reflected power.
- g. Calculate the VSWR of the Carrier Antenna using the formula:

$$VSWR = \frac{\sqrt{FWDPower} + \sqrt{REFLPower}}{\sqrt{FWDPower} - \sqrt{REFLPower}}$$

- h. A calculated VSWR exceeding 1.20:1, then is cause to suspect that the frequency change has affected the antenna tuning.
- i. With the DVOR operational select Monitors>> Data>> Sideband Antenna VSWR screen and view the sideband antenna VSWR readings.
- j. The frequency change may have affected the resonant point of the antenna. Attempts to improve their VSWR may not successful because the tuning stubs now appear to be cut too short.
- k. If the problems discussed in steps h or j exist, then perform the antenna tuning procedures in the DVOR Antenna Manual, P/N 570002-0001. If the VSWR of the antennas cannot be reduced to less than 1.20:1, it may be necessary to replace the tuning stubs or the antenna positioning pieces to insure optimum operation at the new frequency.

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7 CORRECTIVE MAINTENANCE

7.1 INTRODUCTION

This section contains instructions required for on-site corrective maintenance and offsite repair of the DVOR system. Required test equipment is defined and packing instructions are included in this section.

7.2 TEST EQUIPMENT REQUIRED

Portable Maintenance Data Terminal with current SELEX Sistemi Integrati PMDT software. In addition hand tools such as straight and Phillips screwdrivers are required for the removal and replacement of modules.

7.3 ON-SITE CORRECTIVE MAINTENANCE

The maintenance on-site is limited to identifying a faulty module and replacement with a spare module. Repair of modules on-site is not recommended due to the complex nature of the circuitry and the specialized tools necessary to remove and solder parts on to the circuit cards.

The PMDT software includes a Fault Isolation routine that is used to identify faulty modules. In addition RMM system within the DVOR provides extensive measurements and special tests to aid in any further trouble shooting so that in general the maintenance technician does not require special tools and test equipment.

7.3.1 General Troubleshooting Information

- a. Perform fault isolation test.
- b. Replace the module identified by the Fault Isolation Routine.
- c. Turn on the DVOR and verify that the equipment restores to the normal state.
- d. Make any adjustments to either Transmitters>>Configuration or Monitors>>Configuration in order to normalize DVOR performance.

7.3.2 Test Point Waveform References

NOTE

Unless otherwise indicated, Carrier output power is 100 watts and Sideband output power is 2.5 watts. Scope probe is 10:1, trigger source is Channel 1, input is DC coupled (zero ground reference point is indicated by the arrow(s) on the left side of each figure).

All oscilloscope presentations are typical; however, variations are possible due to site-specific operating requirements.

NOTE

The following waveforms vary in shape due to the difference in amplitude of the near and far antennas on the counterpoise. This creates a 60 Hz modulation which varies in phase relative to the 30 Hz modulation and is dependent upon the azimuth location of the field monitor antenna.

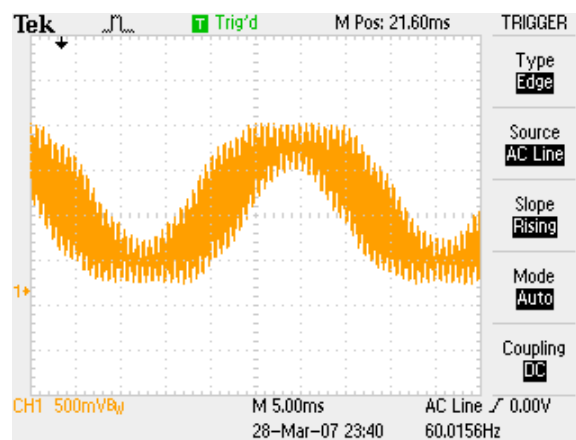


Figure 7-1 Waveform – Monitor 1A3A3/1A3A10 Composite Signal at 0 deg Azimuth

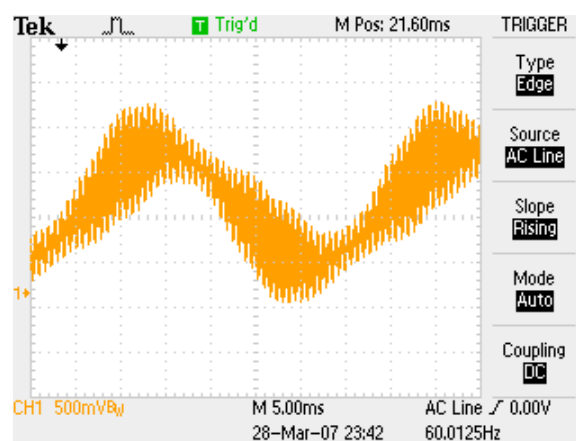


Figure 7-2 Waveform – Monitor 1A3A3/1A3A10 Composite Signal at 45 deg Azimuth

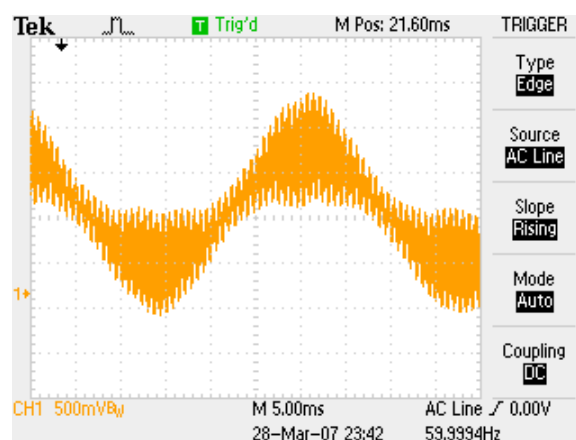


Figure 7-3 Waveform – Monitor 1A3A3/1A3A10 Composite Signal at 90 deg Azimuth

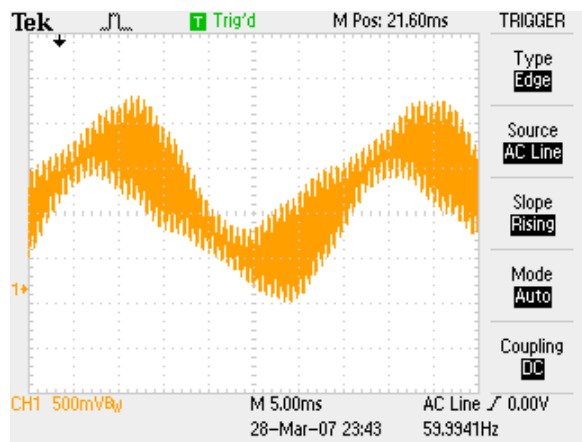


Figure 7-4 Waveform – Monitor 1A3A3/1A3A10 Composite Signal at 135 deg Azimuth

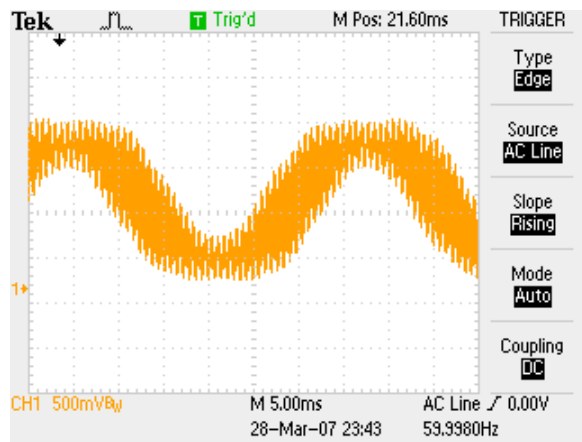


Figure 7-5 Waveform – Monitor 1A3A3/1A3A10 Composite Signal at 180 deg Azimuth

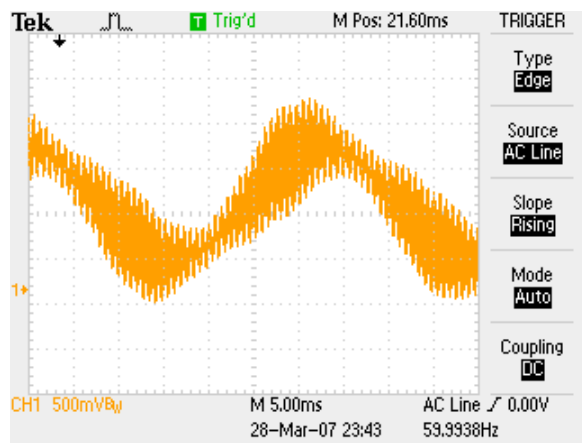


Figure 7-6 Waveform – Monitor 1A3A3/1A3A10 Composite Signal at 225 deg Azimuth

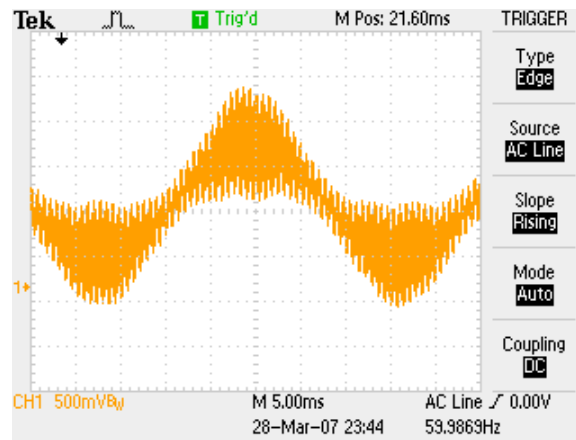


Figure 7-7 Waveform – Monitor 1A3A3/1A3A10 Composite Signal at 270 deg Azimuth

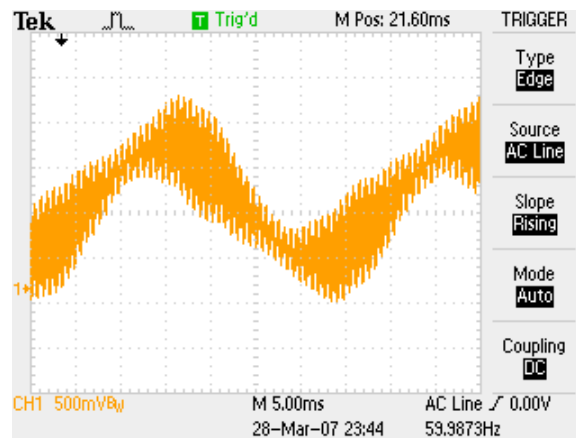


Figure 7-8 Waveform – Monitor 1A3A3/1A3A10 Composite Signal at 315 deg Azimuth

7.4 OFFSITE REPAIR

There are no assemblies that require offsite overhaul or calibration.

7.5 PACKING INSTRUCTIONS

Equipment requiring shipment from the site for repair shall be individually packaged and marked. All items sensitive to electrostatic discharge (ESD) shall be packed in ESD bags or containers.

8 PARTS LIST

8.1 INTRODUCTION

Table 8-1 contains a list of the different variations of the Model 1150A DVOR. Table 8-2 contains a list of the kits and optional equipment used in the Dual Model 1150A DVOR.

Table 8-1 Dual 1150A DVOR Parts List PN 001150A-0202		
Part Number	Description	Ref Des
030819-0002	Cabinet Assembly	Unit 1
030801-0001	Local Control Unit (LCU)	1A1
030820-0002	Control Rack Assembly	1A3
030838-0001	Synthesizer Assembly	1A3A1/1A3A11
012254-1001	Audio Generator CCA	1A3A2/1A3A9
012245-1001	Monitor CCA	1A3A3/1A3A10
012222-0001	Low Voltage Power Supply CCA	1A3A4/1A3A8
012223-1001	Test Generator CCA w/Software	1A3A5
012172-1002	RMS CCA w/Software	1A3A6
012171-0002	Facilities CCA	1A3A7
030836-0001	Sideband Rack Assembly	1A4
030824-0001	Sideband Generator Assembly	1A4A1/1A4A2/1A4A6/1A4A7
030829-0001	RF Monitor Assembly	1A4A4
012257-1001	Commutator Control CCA w/Software	1A4A5
030837-0001	Carrier Rack Assembly	1A5
030798-1001	BCPS	1A5A1/1A5A2
030825-0002	Carrier Amplifier Assembly	1A5A3/1A5A4
012186-0001	AC Monitor CCA	1A6
030813-0002	Control Panel Assembly	1A7
012167-0001	Interface CCA	1A9
012104-0001	Commutator Doppler Antenna CCA	1A10/1A11

Table 8-2 Model 1150A DVOR Kits and Optional Equipment		
Part Number	Description	
002238-0112	Remote Status/Control Unit	Model 2238/ 120 VAC
002238-0212	Remote Status/Control Unit	Model 2238/ 240 VAC
472240-0001	Remote Status/Control Unit	Model 2240
002134-0101	Monitor Receiver LOC/VOR	Status receiver, wireless
470639-0001	Battery Backup Kit	With 65 AH Batteries
470639-0003	Battery Backup Kit	With 100 AH Batteries
470639-0002	Battery Backup Kit	Without Batteries
470115-0001	Test Equipment Kit	DVOR
470159-0004	Remote Maintenance System Kit	w/Computer
470165-0003	Antenna Kit	48 Antennas
470178-0002	Field Monitor Kit	
470445-0001	Equipment Installation Kit	
470200-0001	Mast Kit	Co-Location with DME Antenna
470208-0001	Carrier Antenna Kit	Walk-In Radome, harsh environment

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Table 8-2 Model 1150A DVOR Kits and Optional Equipment		
Part Number	Description	
470209-0001	Carrier Antenna Kit	Stand Alone w/o DME Antenna
470252-0001	Civil Installation Kit	Field Monitor Tower
470360-0001	Portable Maintenance Data Terminal Kit (PMDT)	Computer Kit
480163-0003	Spares Kit	Full, Board & Modules
480163-0002	Spares Kit	Recommended
480163-0001	Spares Kit	Minimum

9 INSTALLATION, INTEGRATION, AND CHECKOUT

9.1 INTRODUCTION

This section contains installation data and initial tune-up procedures for the Model 1150A Doppler VHF Omnirange (DVOR) electronic subsystem. Refer to the appropriate equipment manuals for specific antenna installation and siting requirements. Before the equipment is installed, shelter construction must be completed. After equipment is unpacked and inspected, the installation work is divided into two major sections.

- a. Site construction work consisting of the concrete, antenna counterpoise, shelter, primary AC power installation, and DVOR system hardware is completed first. At sites where SELEX Sistemi Integrati Inc., does not supply the antenna counterpoise, shelter, or primary AC power, the customer or end user is responsible for these items and their installation.
- b. The DVOR transmitter is then powered up and aligned.

9.2 SITE INFORMATION

All structures (buildings) within 200 meters feet of the station shall be removed. No groups of trees shall be within 200 meters or subtend a vertical angle of more than 2 degrees. Farm type wire fences about 1.2 meters high are not permitted within 120 meters and chain link type fences (6 feet high) are not allowed within 500 feet. Overhead power and control lines may be installed beyond 100 meters but should be essentially radial to the station for a minimum of 100 meters. Power and control lines to the station should be buried underground within 100 meters of the station. There should be no lines or supporting structures that subtend a vertical angle of 1.5 degrees as measured from the station ground elevation.

All other conditions and considerations applicable to specific sites should follow specifications of Eurocae ED-52 Figure 18, and ICAO Annex 10, Part 1 Volume 1, Attachment C, Paragraph 3.2, VOR Siting Guidance.

9.2.1 Shelter Requirements

The DVOR requires a shelter which is located under the counterpoise. The building must not extend beyond the counterpoise edge.

9.3 UNPACKING AND REPACKING

The DVOR electronic subsystem is shipped unassembled. Only general precautions can be given because the crating and unpacking depends upon destination and which optional equipment is included. Most items are packed separately in individual containers; these are then grouped for crating. Each crate contains a packing list which details what equipment is enclosed in the crate. Unpack the equipment and visually inspect each item for accuracy and damage, but **DO NOT REMOVE** any ESD protective wrapping. Report any damage immediately. After inspection, repack each item to prevent damage. During installation, unpack items as they are needed.

9.3.1 Environmental Considerations

The environmental conditions must not exceed those listed in the Specifications of [Table 1-1](#).

9.4 INPUT POWER REQUIREMENT SUMMARY

The requirements for input power must not exceed those listed in the Specification of [Table 1-1](#).

9.5 INSTALLATION PROCEDURES

9.5.1 Tools and Test Equipment Required

Refer to [Table 9-1](#) for a list of special tools and test equipment required. Refer to [Table 9-2](#) for a list of tools needed for installation but not for normal operation of the system.

Table 9-1 Tools and Test Equipment (Equivalent tools and test equipment may be used)	
Part Number	Description
	Dummy Load, 50 ohm, 100 Watt, Load, 1kW max.
950270-0000	Dummy Loads, 50 ohm, 5 Watt (5 required)
399006-0000	ESD Wrist Strap (part of 470643-0001 Accessory Kit)
339003-0000	SMA Torque Wrench (5/16")
950552-0117	1 Watt Element
950552-0301	5 Watt Element
950552-0131	10 Watt Element
950552-0405	100 Watt Element, Bird, 100C
950552-0306 or 950552-0406	250 Watt Element, Bird, 250B or 250C or Bird 250C

Table 9-2 Tools Needed for Installation (Equivalent test equipment may be used)	
Part No.	Description
	Theodolite
950505-0000	Vector Voltmeter, HP, Model 8508A with Accessory Kit, Vector Voltmeter, Model HP11570A
950505-0001	Or Agilent Model 8712 Network Analyzer
234617-0000	NARDA Bi-directional Coupler, PN 3020A
	Soldering Iron, 30 watt
	Soldering Gun, 120 Watt
	Heat Gun, Ungar, Professional Model 6970
900065-0000	Silicon Sealant
	3/16" Drill Bit
	2-1/2" Hole Saw

9.5.2 Counterpoise and Shelter Foundation Installation

Refer to [Figure 9-1](#) and [Figure 9-2](#). The counterpoise and shelter foundation drawing is a typical installation drawing and will change per local building codes. Refer to SELEX-SI VOR Counterpoise Manual Part Number 571150-0006 for complete details about an SELEX-SI supplied VOR Counterpoise. For counterpoise and shelters not supplied by SELEX Sistemi Integrati Inc., the manufacturer of the counterpoise or shelter should supply drawings for the siting engineer.



9.5.3 Shelter Installation

Shelter installation procedures are for an 8' x 12' shelter supplied by SELEX Sistemi Integrati Inc.

- Refer to [Figure 9-1](#). Using a crane and four (4) nylon slings (20' long), position the equipment shelter on the concrete foundations. Attach shelter to the foundation anchor bolts using the 5/8" hardware and mounting plates.
- Install shelter ground rods. Refer to [Figure 9-2](#).

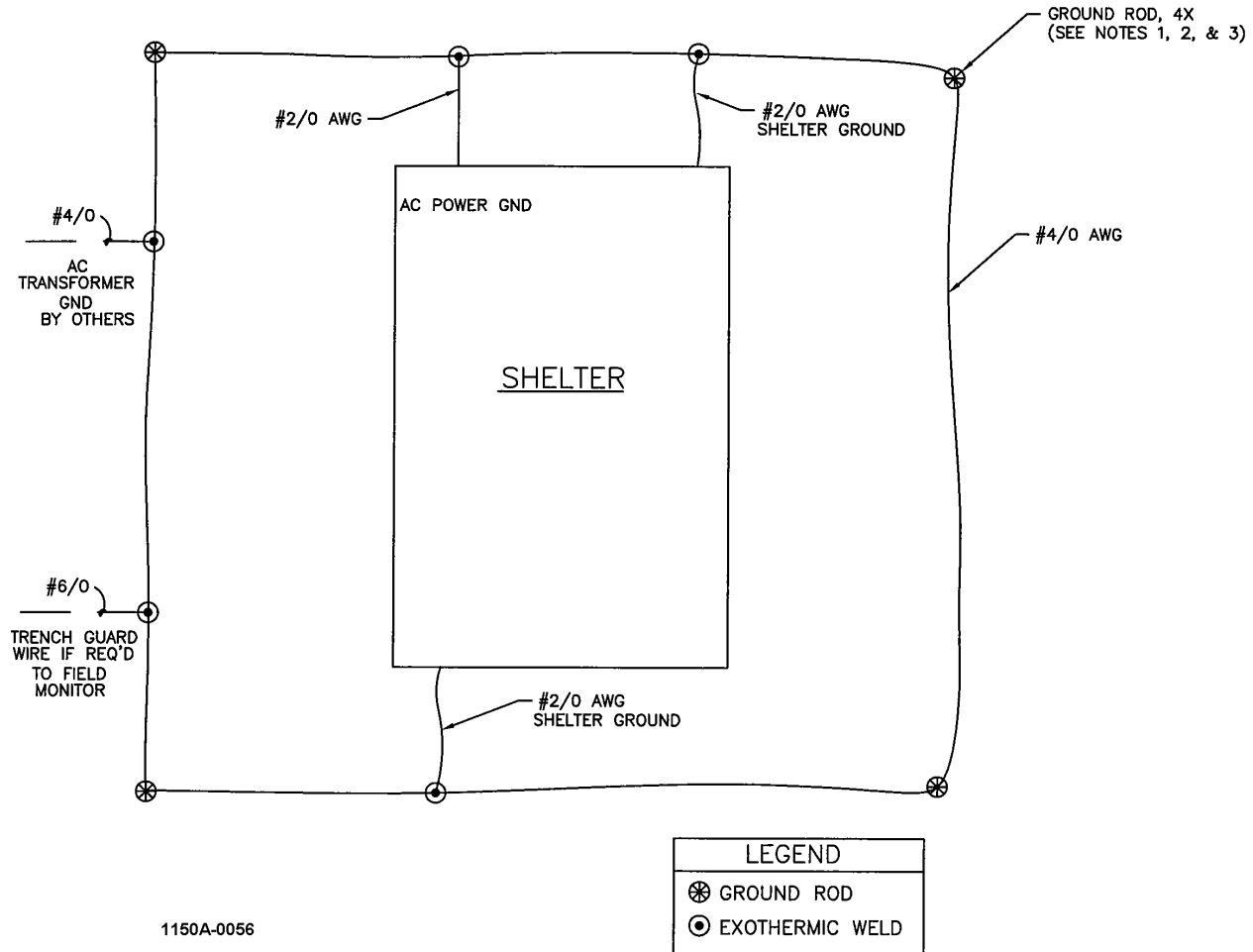


Figure 9-2 Shelter Grounding Diagram

- Notes:
- All ground rods shall be 3/4" x 10' copper clad steel, driven to 12' below grade.
 - Unless otherwise indicated, all bonds below grade shall be exothermically welded.
 - All ground rods shall be at least 24" from any foundation (6' max.).
 - Strip all bonding locations to bare, clean metal and apply anti-oxidation compound.
 - Resistance to earth of the complete earth electrode system will be 5 ohms or less.

9.5.4 Counterpoise Installation

Refer to SELEX Sistemi Integrati Inc. Manual Part Number 571150-0006 for counterpoise installations instructions. For a counterpoise not supplied by SELEX Sistemi Integrati Inc. refer to the manufacturer's installation drawings.

9.5.5 Initial Conditions

Turn off DVOR AC and DC Circuit Breakers. Do not turn on until instructions indicate to do so.

9.5.6 Sideband Antenna Installation

The sideband antennas must be mounted on a radius of 22 feet from the center of the counterpoise and evenly spaced at 7.5° intervals. They must be uniform in height and at the same height as the carrier antenna which is mounted at the center of the counterpoise. There are two methods used in locating the sideband antennas on the counterpoise mounting rail: the theodolite method and the tape measure and spirit level method. The theodolite method is the preferred method. Refer to Section 9.4 of the Model 1150A DVOR Antenna Operations and Maintenance Manual (570002-0001) provided with the 470165-0003 Antenna Kit.

9.5.7 Carrier Antenna Installation

Refer to Section 9.4.4 of the Model 1150A DVOR Antenna Operations and Maintenance Manual (570002-0001) and drawing 470200 in the 470200 Carrier Antenna kit for details. At this time install optional DME antenna and cables as shown in 470200 drawing provided with the kit.

9.5.8 Installation of Field Monitor Antenna

Refer to 1150A DVOR Antenna Operations and Maintenance Manual, part no. 570002-0001, for installation procedures.

9.5.8.1 Installation of Obstruction Lights on Field Monitor Antenna Tower

The use of obstruction lights on the DVOR field monitor antenna tower is on a site by site basis. To determine if obstruction lights are required refer to FAA Advisory Circular AC 70/7460-1F, for domestic installations. International installations are dependent upon ICAO and local regulations.

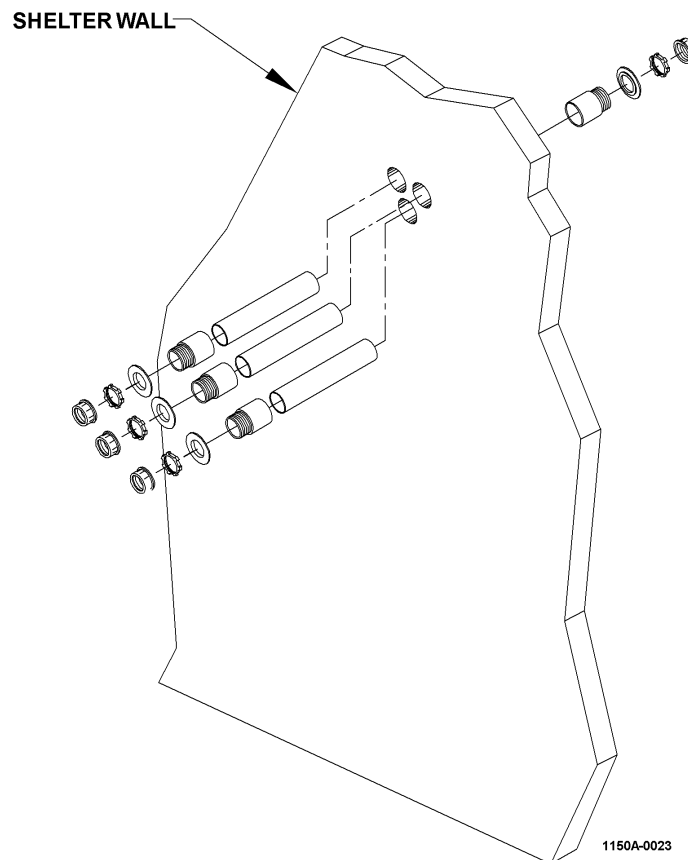


Figure 9-3 Exterior Cable Entrance Installation

9.5.9 Antenna Cable Exterior Cable Entrance Installation

Refer to [Figure 9-3](#). And [Figure 11-24](#) (additional drawings provided with kit 470445-0001).

NOTE

The following installation may be altered to match local requirements. Fewer, larger conduits may be substituted in concrete shelters. The cable entrance may be made through the shelter ceiling in which case the top entrance through the commutator can be used.

- a. Placement of the entrance holes for the Carrier and sideband cables is dependent on the location of the VOR Transmitter Cabinet in the shelter.
- b. Locate and mark three two inch conduit holes corresponding to the cable rack intersection with the wall. Drill three 3/16" pilot holes in the exterior shelter wall.
- c. Using a 3" diameter hole saw, cut a hole in the shelter wall centered on the pilot hole drilled in step b.
- d. Cut the 10 foot sections of PVC conduit into three sections so that with conduit bushing installed will be the same thickness of the wall. (only threads of the bushings exposed)
- e. Install the conduit bushing on both ends of the conduit using PVC adhesive.
- f. Place a bead of silicone sealant around the 3" inside surface of the shoulder washer on both the interior and exterior shelter walls.
- g. Tighten the 3" locknuts against the shoulder washers on both the exterior and interior walls. Do not over tighten the locknuts so that the shelter wall compresses. Only tighten to secure the conduits.
- h. Install the 3" protective bushings snugly on the conduits.
- i. Neatly organize the cables into groups and feed them through the conduits.
- j. Place the cables on to the cable tray and apply cable ties as necessary to secure.
- k. Run the cables in the cable tray over the top of the DVOR transmitter cabinet. Use the cable drop plate provided with the installation kit to route the cables into the transmitter cabinet.
- l. Use putty provided in the kit to seal the conduits from air and moisture.

9.5.10 Air Conditioner Installation

If a wall mounted air conditioner is supplied install the air conditioner in the wall opening and secure it in place using brackets supplied.

9.5.11 Transmitter Cabinet Installation

Refer to [Figure 11-24](#) (Kit 470445-0001) installation drawings.

- a. Unpack the DVOR 19" rack system and stand upright inside the equipment shelter.
- b. The rack must so that the ventilation louvers located on the sides and bottom of the cabinet are not obstructed. Clearance for the front and rear doors must be provided for ease of service.
- c. To level the rack use the adjustable feet then lock the feet positions using the jam nuts.
- d. If desired the front and rear doors can easily be removed by disconnecting the ground wires and sliding up the three hinge pins on the left inside edge of each door. If the doors are removed be sure to replace them after installation.
- e. Use #6 grounding wire provided in the AC Power Installation Kit ([Figure 11-24](#)) to connect from the VOR Ground lugs on the outside top of the cabinet to the shelter grounding plate using the shortest path possible. Local grounding ordinances may require additional grounding wires and/or larger grounding conductors.

NOTE

Do not install any modules in the rack until it is properly grounded.

9.5.12 Battery Back Up Installation

Refer to [Figure 9-4](#). The installation procedures given in the kit drawing are those required for installing optional battery back unit (part number 470639-0001/0002/0003) in supplied shelter.

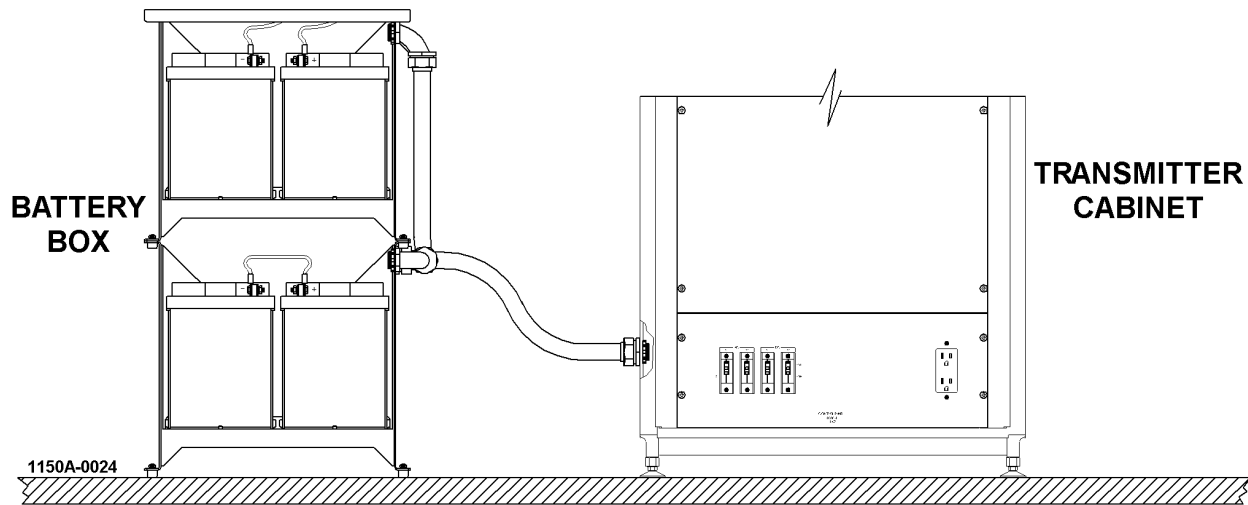


Figure 9-4 Battery Backup Kit Installation

9.5.13 DC Voltage and Battery Installation

- Insure VOR system AC and DC circuit breakers are in the OFF position.
- Construct battery backup unit as detailed in [Figure 11-25](#) or per the drawing provided with supplied battery backup kit.
- Install the four twelve-volt batteries and connect batteries in series using the short interconnect wires.
- Install battery backup wiring between the VOR transmitter cabinet and the battery backup assembly. The battery ground lead should connect to the grounding bus bar and the battery hot wire (+48V) should connect to J1-1 Battery Connector located on the 1A7 Control Panel Assembly.
- When supplied with two battery kits then connect the hot wire (+48V) from the second battery set to J1-2 Battery Connector located on the rear of the 1A7 Control Panel Assembly; otherwise connect both hot wires to the one battery sets.
- Install lid(s) on battery backup box.

CAUTION

Shorting the battery leads can cause a fire or explosion.

9.5.14 AC Voltage Installation

- Set the primary AC power circuit breakers (located in the shelter main circuit breaker box) to the OFF position.
- Refer to [Figure 1-4](#). Set DVOR SYSTEM A DC INPUT (BATTERY) and SYSTEM B DC INPUT (BATTERY) circuit breakers to the OFF position.
- Set DVOR SYSTEM A AC INPUT (LINE) and SYSTEM B AC INPUT (LINE) circuit breakers to the OFF position.
- Cut conduit and attach fittings as required to attach the conduit to the top.
- Using No. 10 AWG stranded copper wire, fabricate system power line. Route system power line through the conduit and into the DVOR transmitter cabinet to 1A7P1.

NOTE

The AC cables must not be routed in the same conduit as DC or signal wires.

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- f. Connect AC input ground (green wire) to 1A6 TB3-3.
- g. Connect AC low input (white wire) to 1A6 TB3-2.
- h. Connect AC high input (black wire) to 1A6 TB3-1.

CAUTION

Black, white and green wiring may also be used in installations outside the United States. Technicians must note that the black wire (equivalent to Blue) is the AC HIGH and the white wire (equivalent to brown) is the AC LOW. This condition may not be the same as local wiring standards, and caution must be observed when working on the AC supply wiring. The ground wire is provided as either black for dc return path or protective ground green/yellow.

9.5.15 Connecting DME Keyer Wiring

- a. Verify that the primary AC power (located in the shelter main circuit breaker box), VOR equipment and DME equipment circuit breakers are in the OFF position.
- b. Using the two-conductor electrical cable and provided in the AC Power/Installation kit (Figure 11-24), connect KEY_OUT+ and KEY_OUT- signals from the 1A9 Interface CCA located in rear of the VOR cabinet to the appropriate location as identified in Table 9-3.

Table 9-3 External Keying Connection Locations		
Signal	VOR Source	SELEX-SI Model 1118A/ 1119A DME Destination
KEY_OUT+	1A9TB2-14	KEY_IN+ (1A19TB2-16)
KEY_OUT-	1A9TB2-15	KEY_IN- (1A19TB2-17)

9.5.16 RCSU and RMM Connections

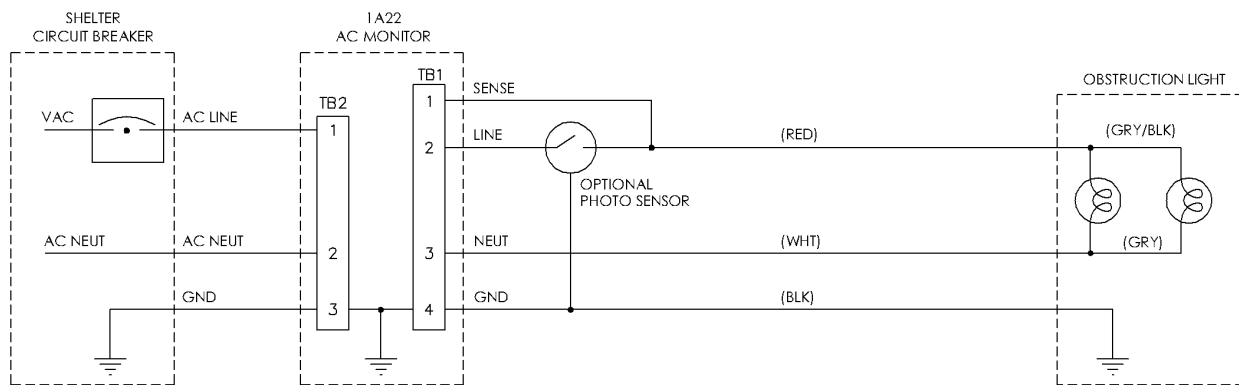
Note: Changes to the S2 Configuration DIP switch should be followed with a Reset (located on the 1A1 LCU).

- a. If the VOR is provided with a 2238 or 2240 RCSU then connect the copper wires from the RCSU to the 1A9TB2-1 and 1A9TB2-2 locations on the Interface CCA for a Dedicated Modem connection type. For a RF Modem/Fiber connection type, the RS232 connection should be made to the 1A9J5 DB9 connector. DIP switch S2-1 located on the 1A3 Control Backplane CCA should be set to match the Connection Type as well.
- b. If a telephone line is available for remote maintenance monitoring (RMM), connect the tip and ring wires from the telephone interface box to the 1A9 Interface CCA locations TB2-3 and TB2-4. Polarity is not important. DIP switch S2-2 located on the 1A3 Control Backplane CCA should be set to "DIAL-UP" when using this internal dial-up modem. Use the two-conductor electrical cable provided in the AC Power Installation kit (Figure 11-24) for this connection.
- c. If the VOR's internal dial-up modem is unable to comply with local telephone requirements then connect the telephone line to an external modem and connect the external modem serial port to the 1A9 Interface CCA J6 connector. DIP switch S2-2 located on the 1A3 Control Backplane CCA should be set to "~EXTERNAL" when using an external dial-up modem. DIP switch S1-6 located on the 1A3 Control Backplane CCA controls whether the VOR station will allow remote configuration of transmitter and monitor parameters. When set to "RMT ALLOWED" a remote user logged into Security Level 3 can put the VOR station in Local Mode from the PMDT and change all parameters as if connected directly to the cabinet in the shelter. When set to "~NOT ALLOWED" the system can not be put in Local Mode from the PMDT and remote parameter changes are blocked throughout the software.

9.5.17 Obstruction Light Installation and Wiring

The obstruction light assembly is shipped separately from the VOR antenna kits and it is necessary to attach the obstruction light to the top of the VOR Monitor or DME antenna; and the wiring that extends from the antenna must be connected to the bulb sockets. For connection of SELEX-SI DME antenna obstruction lights please refer to the DME manual.

- Remove lens and bulbs.
- Remove the hole cap at the top of the DME antenna and fish out the AC wires using stiff wire bent into a hook.
- Route the three wire AC cable from the DME antenna through the required pipe adapters and into the bulb sockets.
- Thread the obstruction light assembly into the antenna. Use thread tape on all pipe threads to insure a water tight fit.
- Connect the three AC wires from the antenna to the bulb sockets, as shown in [Figure 9-5](#) and [Figure 9-6](#).
- Install the lighting rod (if provided) to the obstruction light nipple if provided.
- Verify the obstruction light bulbs match the site AC voltage rating then install the bulbs and lens.
- After installing obstruction light, connect remaining obstruction light power wires to VOR cabinet and shelter circuit breaker box as shown in [Figure 9-5](#) and [Figure 9-6](#).

IN USA:

CONNECT GREEN WIRE TO A22TB2-3
 CONNECT BLACK WIRE (LINE) TO A22TB2-1
 CONNECT WHITE WIRE (NEUTRAL) TO A22TB2-2

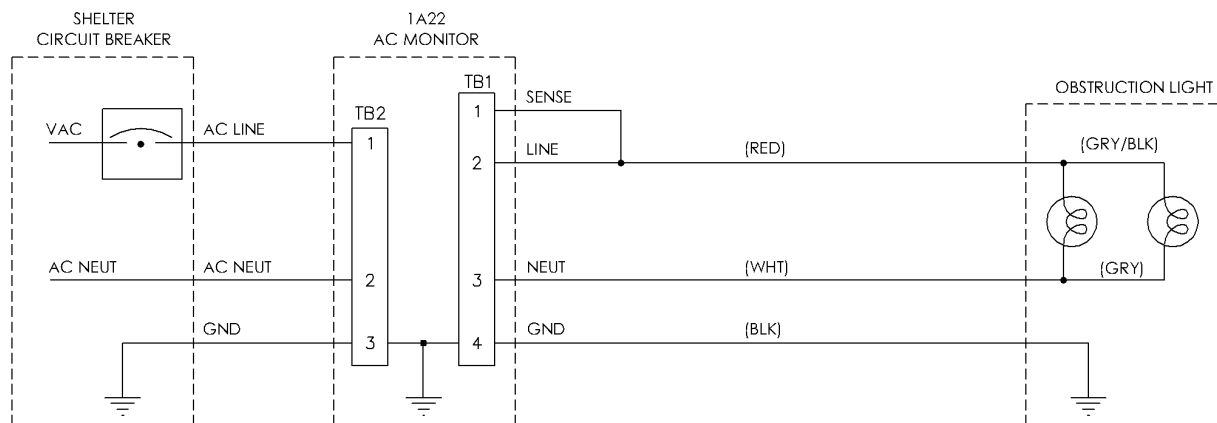
OUTSIDE USA:

CONNECT GREEN WIRE TO A22TB2-3
 CONNECT RED WIRE (LINE) TO A22TB2-1
 CONNECT BLACK WIRE (NEUTRAL) TO A22TB2-2

1150A-0021

Figure 9-5 VOR Obstruction Light Interconnect Diagram with Photo Sensor

Model 1150A DVOR



IN USA:

CONNECT GREEN WIRE TO A22TB2-3
CONNECT BLACK WIRE (LINE) TO A22TB2-1
CONNECT WHITE WIRE (NEUTRAL) TO A22TB2-2

OUTSIDE USA:

CONNECT GREEN WIRE TO A22TB2-3
CONNECT RED WIRE (LINE) TO A22TB2-1
CONNECT BLACK WIRE (NEUTRAL) TO A22TB2-2

1150A-0022

Figure 9-6 VOR Obstruction Light Interconnect Diagram without Photo Sensor

9.5.18 Cutting Antenna Cables to Proper Electrical Length

The RF cables from commutator to the antenna cables are precut and phased matched at the factory. It is recommended that the cables remain at the length set by the factory. Excess cable should be neatly stored outside the shelter. The cables must be firmly held by tie wraps (provided) to prevent damage to stress caused by wind gusts.

If the cables must be cut then a vector voltmeter or network analyzer must be used to verify that all the cables are within +/-2 degrees.

NOTE

A common mistake in cutting or measuring cable phase results in one or more cable with a phase length 180 degrees different than all other cables. To check for this mistake check cable length at 50% of the station frequency. All cables should then be the same length and any that were in error by 180 degrees at station frequency will now be in error by 90 degrees at 50% of the station frequency.

9.5.19 Tuning the Antennas

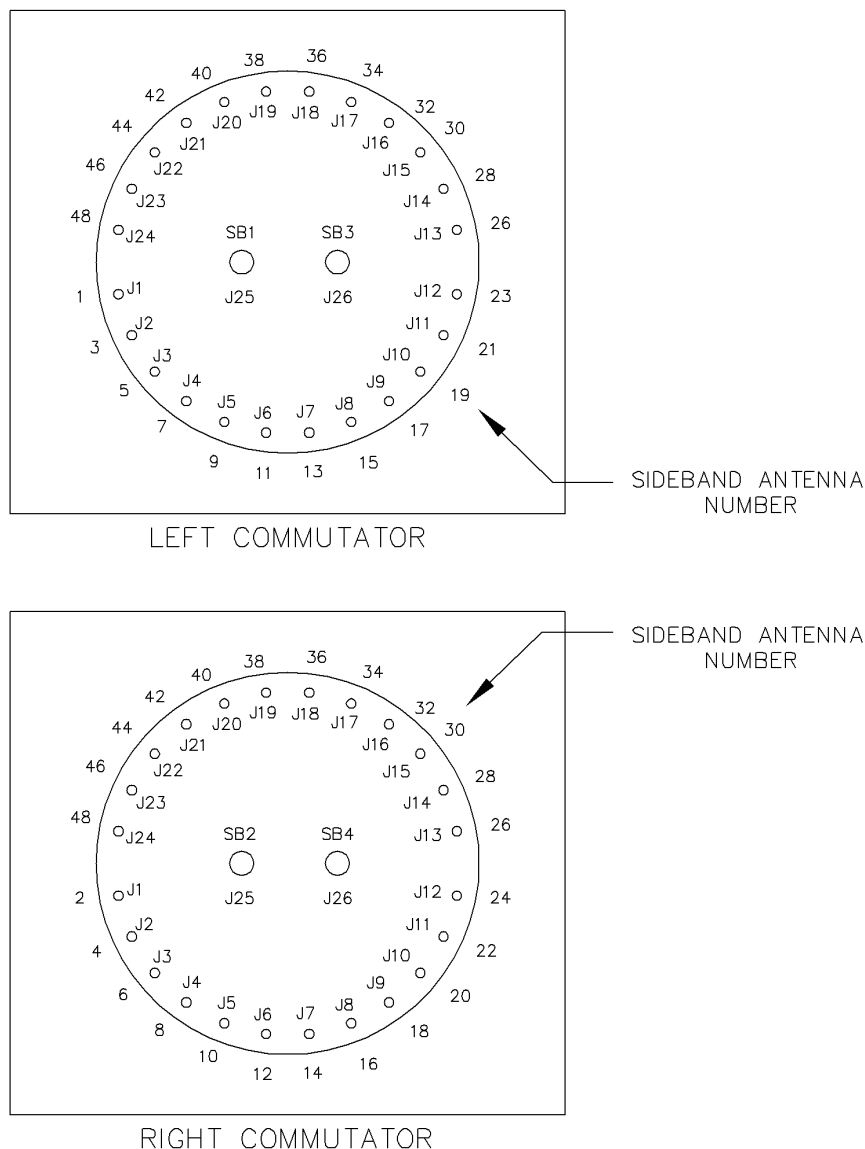
Refer to Section 9.4.6 of the DVOR Antenna Manual.

9.5.20 Sideband RF Feed Cables to Commutator Connections

Using [Figure 9-7](#) as a guide attach all sideband antenna RF feed cables to the right or left commutator CCAs as required. The odd numbered antennas are connected to the left side as viewed from the rear of the cabinet and the even numbered antennas are connected to the right side of the cabinet.

NOTE

If the DVOR is co-located with a DME, it is advisable to also run the DME RF cables and obstruction light power cable at this time.



1150A-0020

Figure 9-7 Sideband RF Feed Cable to Commutator Connections (Viewed from the rear of the Transmitter Cabinet)

9.6 INSPECTION

9.6.1 Visual Inspection

The visual inspection is made prior to operating or energizing the equipment.

- Visually inspect wire, RF coaxial cables and connectors for corrosion, loose connectors and improperly assembled connectors.
- Insure all terminal boards are free of foreign objects such as pieces of wire or other objects that could cause electrical shorts within the equipment. Remove foreign objects as necessary.
- Inspect the battery backup units to ensure that all terminals and connectors are tight and that there are no metal shavings or other objects that could cause damage to the equipment.

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9.7 INITIAL STARTUP AND PRELIMINARY TESTING

The following paragraphs detail the step-by-step procedures for initial start-up and preliminary testing of the VOR.

9.7.1 Input Voltage Checks

After the AC and DC power has been connected to the DVOR transmitter it is necessary to check the input power to ensure the proper voltage is applied to the system.

- a. Set the VOR AC and DC circuit breakers to the OFF position.
- b. Set the shelter primary AC power circuit breakers to the ON position.
- c. Using an AC voltmeter check voltage across the AC Monitor 1A22TB3-1 (LINE) to 1A22TB3-2 (NEUTRAL) terminals. Insure the voltage meets the range specified in section [Table 1-1](#).
- d. Turn on the VOR DC circuit breaker while leaving the AC circuit breakers OFF.
- e. Using a DC voltmeter check voltage across 1A5 Carrier Backplane E1 (BATT_POS) to E2 (GND). Insure the voltage is 42 to 52Vdc.
- f. For dual equipment check voltage across 1A5 Carrier Backplane E5 (BATT_POS) to E2 (GND). Insure the voltage is 42 to 52Vdc.
- g. Turn DC circuit breakers to the OFF position.

9.7.2 Installing Modules in Transmitter Cabinet

Since the VOR transmitter cabinet is shipped separately from its electronic modules, it will be necessary to install them into the transmitter equipment cabinet. Insure AC and DC circuit breakers are set to the OFF position.

CAUTION

Many of the modules used in the VOR transmitter contain Electrostatic Discharge (ESD) sensitive components. ALWAYS wear protective wrist strap when installing modules or CCAs. Before modules are installed into transmitter cabinet, check modules or CCAs for cracked or broken connectors, bent pins, and loose hardware. Report any damage immediately.

9.7.3 Turn on Procedure

- a. Verify all assemblies are properly installed and are fully seated.
- b. Turn AC and DC circuit breakers to the ON position.
- c. Verify the PWR OK LEDs are lit on card cage modules with power indication feature.
- d. Verify the CPU OK LEDs are lit on the Audio Generator, BCPS, Monitor, and RMS assemblies.

9.7.4 PMDT Hookup and Setup

- a. Unpack the PMDT laptop computer and follow the manufacturer's installation instructions to power-up the computer, create a user account, and logon to Windows™ as an administrator.
- b. Insert the 978178-XXXX PMDT CD-ROM into the laptop computer.
- c. Select Start >> Run then type D:\Setup.exe to start the PMDT installation. Note if installation does not start then use the correct drive letter associated with the CD-ROM drive.
- d. Follow the default prompts for PMDT installation.
- e. In order for the PMDT controls to be properly displayed change the DPI Setting to "Normal (96 DPI)" in Windows on the Display Properties >> Settings >> Advanced >> General tab. Note that Display Properties can be accessed by right-clicking on the Windows background then selecting Properties.
- f. At the VOR assure the AC and DC breakers are in the ON position.
- g. Plug the USB cord between the laptop computer and 1A3A6J1 (PMDT USB) located on the RMS CCA.
- h. Windows should detect the USB device and start installing a driver. If prompted for the USB driver files they are installed in the PMDT directory at C:\Program Files\SELEX-SI\PMDT\FTDI USB Driver.
- i. Start the PMDT application by double-clicking on the desktop icon named PMDT.
- j. Select System >> PMDT Setup.
- k. In the Navaid Direct COM Port control pick the COM port that contains "USB Serial Port" in the description.

- l. On the PMDT configuration screen, setup other options such as Language and Print Screen mode then select OK to save the changes.
- m. Refer to [Section 3.6.6.2](#) to connect to the VOR equipment at Security Level 3.

9.7.5 Site Adjustments and Configurations

- a. Press the LOCAL CONTROL button on the 1A1 LCU to put the VOR into Local Mode.
- b. Locate the S3 DIP switch on the 1A3 Control Rack Backplane Circuit Card Assembly and Program S3 per [Table 9-4](#).
- c. On the RMS >> Configuration >> Station screen verify the channel number and type (DVOR or CVOR) match the site requirements and frequency pairing requirements as identified in [Paragraph 3.6.7.4.2](#) and [Figure 3-20](#).
- d. At the LCU bypass the Integral monitor and put Transmitter 1 on antenna.
- e. If the VSWR reading on the Monitors >> Data >> Integral screen is in alarm then shut down the VOR and troubleshoot the RF feed cable to antenna connection before continuing.
- f. On the Monitors >> Data >> Integral screen note the ERP (Effective Radiated Power) value for each monitor.
- g. On the Monitors >> Configuration >> Alarm Limits screen change the Monitor 1 Input Attenuation setting until the Monitor 1 ERP is $0 \pm 1\text{dB}$.
- h. For dual monitor equipment change the Monitor 2 Input Attenuation setting until the Monitor 2 ERP is $0 \pm 1\text{dB}$.
- i. If the VOR is provided with a 2238 or 2240 RCSU then on the RMS >> Configuration >> General screen check the RCSU Present box and configure the Connection Type and Interlock Control to match the installation requirements.
- j. Set the Primary Ident Code to the assigned station identifier.
- k. Select RMS >> Config Backup to save changes to the VOR configuration.

Table 9-4 Frequency Selection Chart (S3 is located on the 1A3 Control Backplane) A "1" in the Table is a closed (on) position on the switch.					
S3 Switch Setting 12345678	VOR Frequency MHz	S3 Switch Setting 12345678	VOR Frequency MHz	S3 Switch Setting 12345678	VOR Frequency MHz
10000000	108.000	10001010	112.000	10000101	116.000
01000000	108.050	01001010	112.050	01000101	116.050
11000000	108.100	11001010	112.100	11000101	116.100
00100000	108.150	00101010	112.150	00100101	116.150
10100000	108.200	10101010	112.200	10100101	116.200
01100000	108.250	01101010	112.250	01100101	116.250
11100000	108.300	11101010	112.300	11100101	116.300
00010000	108.350	00011010	112.350	00010101	116.350
10010000	108.400	10011010	112.400	10010101	116.400
01010000	108.450	01011010	112.450	01010101	116.450
11010000	108.500	11011010	112.500	11010101	116.500
00110000	108.550	00111010	112.550	00110101	116.550
10110000	108.600	10111010	112.600	10110101	116.600
01110000	108.650	01111010	112.650	01110101	116.650
11110000	108.700	11111010	112.700	11110101	116.700
00001000	108.750	00000110	112.750	00001101	116.750
10001000	108.800	10000110	112.800	10001101	116.800
01001000	108.850	01000110	112.850	01001101	116.850
11001000	108.900	11000110	112.900	11001101	116.900
00101000	108.950	00100110	112.950	00101101	116.950
10101000	109.000	10100110	113.000	10101101	117.000
01101000	109.050	01100110	113.050	01101101	117.050
11101000	109.100	11100110	113.100	11101101	117.100
00011000	109.150	00010110	113.150	00011101	117.150
10011000	109.200	10010110	113.200	10011101	117.200
01011000	109.250	01010110	113.250	01011101	117.250
11011000	109.300	11010110	113.300	11011101	117.300
00111000	109.350	00110110	113.350	00111101	117.350
10111000	109.400	10110110	113.400	10111101	117.400
01111000	109.450	01110110	113.450	01111101	117.450
11111000	109.500	11110110	113.500	11111101	117.500
00000100	109.550	00000110	113.550	00000011	117.550
10000100	109.600	10000110	113.600	10000011	117.600
01000100	109.650	01000110	113.650	01000011	117.650
11000100	109.700	11000110	113.700	11000011	117.700
00100100	109.750	00100110	113.750	00100011	117.750
10100100	109.800	10100110	113.800	10100011	117.800
01100100	109.850	01100110	113.850	01100011	117.850
11100100	109.900	11100110	113.900	11100011	117.900
00010100	109.950	00010110	113.950	00010011	117.950
10010100	110.000	10010110	114.000		
01010100	110.050	01010110	114.050		
11010100	110.100	11010110	114.100		

Table 9-4 Frequency Selection Chart (S3 is located on the 1A3 Control Backplane) A “1” in the Table is a closed (on) position on the switch.					
S3 Switch Setting 12345678	VOR Frequency MHz	S3 Switch Setting 12345678	VOR Frequency MHz	S3 Switch Setting 12345678	VOR Frequency MHz
00110100	110.150	00111110	114.150		
10110100	110.200	10111110	114.200		
01110100	110.250	01111110	114.250		
11110100	110.300	11111110	114.300		
00001100	110.350	00000001	114.350		
10001100	110.400	10000001	114.400		
01001100	110.450	01000001	114.450		
11001100	110.500	11000001	114.500		
00101100	110.550	00100001	114.550		
10101100	110.600	10100001	114.600		
01101100	110.650	01100001	114.650		
11101100	110.700	11100001	114.700		
00011100	110.750	00010001	114.750		
10011100	110.800	10010001	114.800		
01011100	110.850	01010001	114.850		
11011100	110.900	11010001	114.900		
00111100	110.950	00110001	114.950		
10111100	111.000	10110001	115.000		
01111100	111.050	01110001	115.050		
11111100	111.100	11110001	115.100		
00000010	111.150	00001001	115.150		
10000010	111.200	10001001	115.200		
01000010	111.250	01001001	115.250		
11000010	111.300	11001001	115.300		
00100010	111.350	00101001	115.350		
10100010	111.400	10101001	115.400		
01100010	111.450	01101001	115.450		
11100010	111.500	11101001	115.500		
00010010	111.550	00011001	115.550		
10010010	111.600	10011001	115.600		
01010010	111.650	01011001	115.650		
11010010	111.700	11011001	115.700		
00110010	111.750	00111001	115.750		
10110010	111.800	10111001	115.800		
01110010	111.850	01111001	115.850		
11110010	111.900	11111001	115.900		
00001010	111.950	00001010	115.950		

NOTE

Shaded areas in the above table are set aside as ILS frequencies, therefore are non-valid VOR frequencies. Setting the switches to any of the shaded combinations in the table will result in the synthesizer being programmed to 108.000 MHz. Switch settings that would result in frequencies higher than 119.750 MHz will result in the synthesizer being programmed to 117.950 MHz. This will prevent the VOR transmitter system from operating on a non-valid VOR frequency.

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9.7.6 DVOR Station Power-Up

Refer to [Section 3](#) of this manual for detailed instruction on DVOR operation. The DVOR is microprocessor controlled, transmitter one will come up in the on-line mode as the normal mode of operation.

- a. Turn on the PMDT. Refer to [Section 3](#) for operating instructions.
- b. Set TX1 AC and TX 2 AC circuit breakers to the ON position.
- c. Set TX 1 Battery and TX 2 Battery circuit breakers to the ON position.
- d. Set TX 1 DC Buss and TX 2 DC Buss circuit breakers to the ON position.

9.7.7 Log-On Procedure

- a. Refer to [paragraph 3.6.6](#) for DVOR system log on procedures.
- b. Place system in bypass using the PMDT mouse to point and click the BYPASS button on the left side of the display command and shutdown transmitter by pointing and clicking the OFF button on the screen.

9.7.8 Setting Date and Time

- a. Point and click the RMS TAB pull down menu.
- b. Select set time and date and push the enter key.
- c. The RMS time will be updated to the current time on the PMDT laptop.

9.7.9 Setting Station's Descriptor

Refer to [paragraph 3.6.7.4.2](#) for this procedure. The station descriptor is an alpha or numeric descriptor that allows you to readily identify a DVOR system. This is very useful when there is more than one system that you are monitoring. This information is not broadcast by the DVOR.

9.7.10 Password Change

Refer to [paragraph 3.6.7.4.5](#) for this procedure.

9.7.11 Setting System Configuration

Refer to [paragraph 3.6.7.4.2](#) for this procedure.

9.7.12 Transmitter Tuning Procedures

9.7.12.1 Checking Output Frequency of Frequency Synthesizer

- a. Perform procedure of [paragraph 6.4.15](#) to align the Frequency synthesizers.

9.7.12.2 Amplitude Adjustment

- a. Turn off transmitter by using the mouse to point and click on the Transmitter 1 OFF button.
- b. Connect in-line wattmeter thru body in the carrier feed cable to the antenna. Install a 250 watt element into the wattmeter to measure forward power.
- c. Turn on transmitter 1 by using the mouse to point and click on the Transmitter 1 ON button.
- d. Insure that transmitter 1 is on the antenna.
- e. Place transmitter in the BYPASS mode of operation.
- f. Select Transmitters>>Configuration>>Nominal. Enter the desired Output Power from 0 to 100 Watts then F7. Select Transmitters>>Configuration>>Offsets and Scale Factors. Adjust the Output Power Scale for Transmitter 1 to obtain the desired output power.

NOTE

If the VOR is to be operated as an enroute facility, use the 250 watt element and set the station for 100 watts. If the facility is to be used as a terminal facility, use the 100 watt element and set the station for 50 watts. Other power settings between 50 and 100 watts should be at customer's request. Use the wattmeter element that provides the best display.

- g. Adjust potentiometer 1A4A4R1 (CSB FWD ADJ) on the RF Monitor until Carrier Power displayed on the Transmitters>> Data>> Transmitter 1 screen indicates the same value as the wattmeter.
- h. Turn on transmitter 2 by using the mouse to point and click on the Transmitter 2 ON button.
- i. Insure that transmitter 2 is on the antenna.
- j. Select Transmitters>>Configuration>>Offsets and Scale Factors. Adjust the Output Power Scale for Transmitter 2 to obtain the desired output power.
- k. Select Transmitters>>Configuration, and adjust the SBO RF Level to 50.0% and press F7.
- l. Turn off transmitter by using the mouse to point and click on the Transmitter 1 OFF button. Remove in-line wattmeter thru body from the carrier antenna line and install it on sideband 1 (SB1) feed line at the Commutator 1A10 input. Install a 5 watt element into wattmeter body.
- m. Click on the Transmitter 1 ON button. Adjust the potentiometer 1A4A1R3 to obtain 2.5 watts on the wattmeter.
- n. Adjust potentiometer 1A4A1R2 for a power out indication of 2.5 watts on the Transmitter>>Data>>Tx #1 Sideband 1 display.
- o. Click on the Transmitter 2 ON button. Adjust the potentiometer 1A4A6R3 to obtain 2.5 watts on the wattmeter.
- p. Adjust potentiometer 1A4A6R2 for a power out indication of 2.5 watts on the Transmitter>>Data>>Tx #1, Sideband 2 display.
- q. Turn off transmitter by clicking on the Transmitter 2 OFF button.
- r. Remove wattmeter thru body from SB1 feed cable and install it on Sideband 2 feed cable to Commutator 1A10 input. Turn on transmitter by clicking on the Transmitter 1 ON button. Adjust the potentiometer 1A4A1R6 to obtain 2.5 watts on the wattmeter.
- s. Adjust potentiometer 1A4A1R5 for a power out indication of 2.5 watts on the Transmitters>>Data screen, Tx #1, Sideband 2 display.
- t. Click on the Transmitter 2 ON button. Adjust the potentiometer 1A4A6R6 to obtain 2.5 watts on the wattmeter.
- u. Adjust potentiometer 1A4A6R5 for a power out indication of 2.5 watts on the Transmitters>>Data screen, and Tx #2, Sideband 2 display.
- v. Turn off transmitter 2 by clicking on the Transmitter 2 OFF button. Remove wattmeter thru body on Sideband 2 feed to the Commutator and install it on sideband 3 feed line to commutator 1A11.
- w. Turn on transmitter 1 by clicking on the Transmitter 1 ON button.
- x. Adjust the potentiometer 1A4A2R3 to obtain 2.5 watts on the wattmeter.
- y. Adjust potentiometer 1A4A2R2 for a power out indication of 2.5 watts on the Transmitter>>Data>>Tx #1 Sideband 3 display.
- z. Turn on transmitter 2 by clicking on the Transmitter 2 ON button.
- aa. Adjust the potentiometer 1A4A7R3 to obtain 2.5 watts on the wattmeter.
- bb. Adjust potentiometer 1A4A7R2 for a power out indication of 2.5 watts on the Transmitter>>Data>>Tx #2 Sideband 3 display.
- cc. Turn off transmitter by clicking on the Transmitter 1 OFF button. Remove wattmeter thru body on connector Sideband 3 feed cable and install it on sideband 4 (SB4) feed cable to the Commutator 1A11.
- dd. Turn on transmitter by clicking on the Transmitter 1 button. Adjust the potentiometer 1A4A2R6 to obtain 2.5 watts on the wattmeter.
- ee. Adjust potentiometer 1A4A2R5 for a power out indication of 2.5 watts on the Transmitter>>Data TX #1, Sideband 4 display.
- ff. Turn on transmitter 2 by clicking on the Transmitter 2 button. Adjust the potentiometer 1A4A7R6 to obtain 2.5 watts on the wattmeter.
- gg. Adjust potentiometer 1A4A7R5 for a power out indication of 2.5 watts on the Transmitter>>Data TX #2, Sideband 4 display.
- hh. Turn off transmitter by clicking on the Transmitter 2 OFF button. Remove wattmeter thru body on connector Sideband 4 feed cable
- ii. Perform Sideband Amplifier alignment procedure [paragraph 6.4.16](#).

9.7.12.3 Sideband Generator Phasing

This procedure is performed to align sidebands 1 and 2 to the same phase with each other. A preliminary adjustment check is made at the Sideband Generator. This adjustment is then checked using the Carrier antenna.

- a. Perform the procedure in [paragraph 6.4.16](#).
- b. Install 5 watt dummy loads to sidebands 3 and 4 at the transmitter. Install a 180° cable in-line with sideband 1 (ensure that the 180° line section is phased for the station frequency).
- c. Disconnect carrier feed to the carrier antenna and terminate with at least a 100 watt load. Connect the carrier antenna feed cable to the monitor input.
- d. Set TX1 DC INPUT (BATTERY) and TX2 INPUT (BATTERY) circuit breakers to the ON position.
- e. Set TX1 AC INPUT (LINE) and TX2 AC INPUT (LINE) circuit breakers to the ON position.
- f. Connect oscilloscope to 1A4A4. Adjust oscilloscope so that a waveform fills about 3/4 of the screen with a ground reference at the bottom of the grid. Refer to [Figure 9-8](#). In order to do this alignment adjust the time base on the oscilloscope so individual sawtooth waveforms can be viewed.
- g. Select Transmitters>>Configuration>>Offsets and Scale Factors screen. Add or subtract degrees to Tx #1 Sideband 1-2 Phase Offset until all nulls of the sawtooth are at ground or as close as possible to ground. Once this is done the waveform should look like an even band across the grid. If some of the nulls are excessively out of phase with the others (nulls are far from reaching ground); the antennas corresponding to these nulls are out of phase with the other sideband antennas with respect to the carrier antenna. Refer to 1150DVOR Antenna Operations and Maintenance Manual to check phase length of antenna feed cables.
- h. Click on the Transmitter 2 ON button.
- i. Select Transmitters>>Configuration>>Offsets and Scale Factors screen. Add or subtract degrees to Tx #2 Sideband 1-2 Phase Offset until all nulls of the sawtooth are at ground or as close as possible to ground. Once this is done the waveform should look like an even band across the grid.
- j. Click on the Transmitter 2 OFF button to shut off the transmitter. Remove 180° line section from sideband 1.
- k. Install 5 watt dummy loads to sidebands 1 and 2 at the commutator input. Reconnect sidebands 3 and 4, and install 180° line section in sideband 3. Click on the Transmitter 1 ANTENNA Button to restart Transmitter No. 1 as the on-air transmitter.
- l. Adjust oscilloscope so that a waveform fills about 3/4 of the screen with a ground reference at the bottom of the grid. Refer to [Figure 9-8](#). In order to do this alignment adjust the time base on the oscilloscope so individual sawtooth waveforms can be viewed.
- m. Select Transmitters>>Configuration>>Offsets and Scale Factors screen. Add or subtract degrees to Tx #1 Sideband 3-4 Phase Offset until all nulls of the sawtooth are at ground or as close as possible to ground. Once this is done the waveform should look like a nice even band across the grid. If some of the nulls are excessively out of phase with the others (nulls are far from reaching ground); the antennas corresponding to these nulls are out of phase with the other sideband antennas with respect to the carrier antenna.
- n. Click on the Transmitter 2 ON button.
- o. Select Transmitters>>Configuration>>Offsets and Scale Factors screen. Add or subtract degrees to Tx #2 Sideband 3-4 Phase Offset until all nulls of the sawtooth are at ground or as close as possible to ground. Once this is done the waveform should look like an even band across the grid.
- p. Click on the Transmitter 1 OFF button. Remove all loads and 180° line section. Reconnect all cables to their respective antennas.

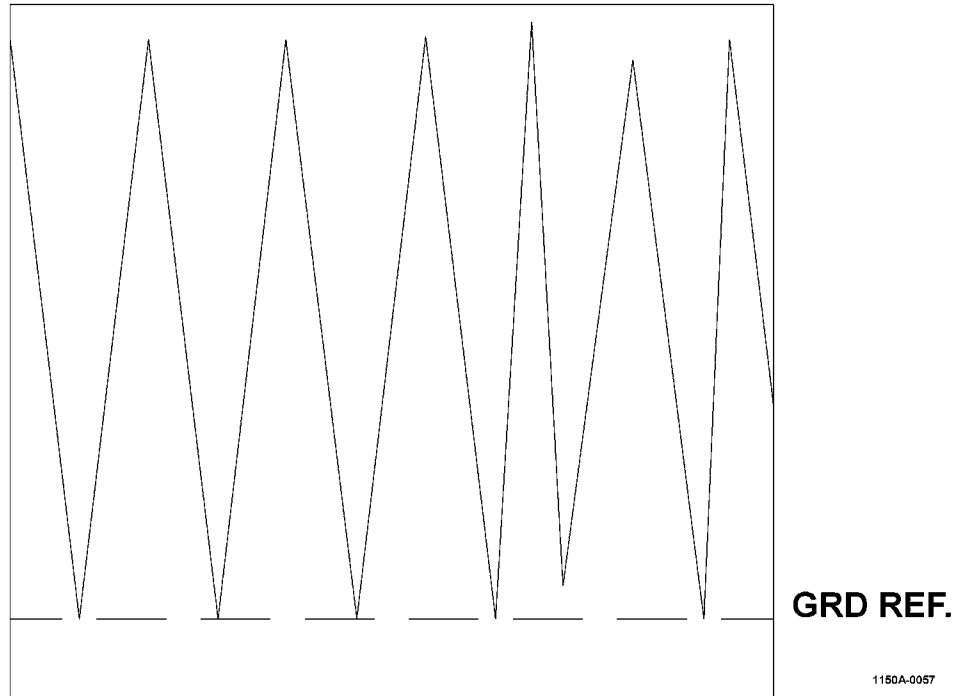


Figure 9-8 Sideband Phasing Diagram

NOTE

Bottom peaks within 5% of ground reference considered within tolerance.

9.7.13 Setting Transmitter Operating Parameters

Before the carrier forward power, carrier VSWR, SBO forward powers, and SBO VSWRs can be calibrated it will be necessary to check/set Transmitter No. 1 and No. 2's operating parameters.

9.7.13.1 Setting Transmitter Ident Code

Type RMS>>Configuration>>then enter Transmitter 1's ident, then press [enter]. Transmitter No. 1's new station's code will be entered into the station's temporary memory.

NOTE

The system will accept from 2 to 4 alpha or numeric characters for the ident code.

9.7.13.2 Setting Transmitter Voice Modulation

The Voice modulation is normally set to 0% when an external voice source is not connected. When a voice system such as automated weather data is connected then select Transmitters>>Configuration>>Nominal. Enter the voice modulation from 0% to 30%, then press [enter]. The new voice modulation will be entered into the station's temporary memory. Select Transmitters>>Configuration>>Offsets and Scale Factors. Set the Voice Modulation Scale for a value of 100% for both Tx #1 and Tx #2.

9.7.13.3 Setting Transmitter Ident Modulation

- a. Place Transmitter 1 on the antenna by pressing the Main #1 button on the LCU or PMDT.
- b. Select Transmitters>>Configuration>>Nominal. Enter the identification modulation 8%, then press [F7]. The new ident modulation will be entered into the station's temporary memory.
- c. Select Transmitters>>Configuration>>Offsets and Scale Factors. For the Tx #1 Ident Modulation Scale for Ident Modulation, enter a value from 0 to 200% to adjust the value entered into the Nominal setting to the correct value as determined by the viewing Monitors>>Data screen.
- d. Place Transmitter 2 on the antenna by pressing the Main #2 button on the LCU or PMDT.

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- e. Select Transmitters>>Configuration>>Offsets and Scale Factors. For the Tx #2 Ident Modulation Scale for Ident Modulation, enter a value from 0 to 200% to adjust the value entered into the Nominal setting to the correct value as determined by the viewing Monitors>>Data screen.

NOTE

Typical setting for ident modulation is 8.0% but may be adjusted according to local requirements.

9.7.13.4 Setting Transmitter Reference Modulation

- a. Place Transmitter 1 on the antenna by pressing the Main #1 button on the LCU or PMDT.
- b. Select Transmitters>>Configuration>>Nominal. Enter the Reference modulation to 30%, then press [F7]. The new Reference modulation will be entered into the station's temporary memory.
- c. Select Transmitters>>Configuration>>Offsets and Scale Factors. For the Tx #1 Reference Modulation Scale for Reference Modulation, enter a value from 0 to 200% to adjust the value entered into the Nominal setting to the correct value as determined by the viewing Monitors>>Data screen.
- d. Place Transmitter 2 on the antenna by pressing the Main #2 button on the LCU or PMDT.
- e. Select Transmitters>>Configuration>>Offsets and Scale Factors. For the Tx #2 Reference Modulation Scale for Reference Modulation, enter a value from 0 to 200% to adjust the value entered into the Nominal setting to the correct value as determined by the viewing Monitors>>Data screen.

NOTE

This value may be changed during the flight calibration. Use the Transmitters>>Configuration>>Offsets and Scale Factors to make the required correction

9.7.13.5 Reference to Sideband Phasing

- a. Set TX1 and TX2 circuit breakers to the ON position.
- b. Place Transmitter 1 on the antenna by pressing the Main #1 button on the LCU or PMDT.
- c. Place the monitors in bypass.
- d. Connect oscilloscope to 1A4A3 J2. Note composite signal waveform. Connect the scope sync input to 1A4A3 J3 Sync output and trigger on the falling edge.
- e. Adjust oscilloscope so that the composite signal is a full 30 Hz waveform (33 ms).
- f. On the PMDT select Transmitters>>Configuration>>Offset and Scale Factors.
- g. Adjust Tx #1 Carrier to Sideband Phase Offset (Coarse) in 90 degree increments until the waveform on the scope and the Monitors>>Data 9960 AM level displayed by the Monitor reaches a maximum amplitude.
- h. Add or subtract degrees for the Carrier Sideband Phase Offset (fine) until Monitors>>Data 9960 AM level displayed by the Monitor reaches maximum amplitude.
- i. Place Transmitter 2 on the antenna by pressing the Main #1 button on the LCU or PMDT.
- j. On the PMDT select Transmitters>>Configuration>>Offset and Scale Factors.
- k. Adjust Tx #2 Carrier to Sideband Phase Offset (Coarse) in 90 degree increments until the waveform on the scope and the Monitors>>Data 9960 AM level displayed by the Monitor reaches maximum amplitude.
- l. Add or subtract degrees for the Tx #2 Carrier Sideband Phase Offset (fine) until the Monitors>>Data 9960 AM level displayed by the Monitor reaches maximum amplitude.
- m. Once the reference to sideband phasing values have been established save the operating parameters.
- n. Switch transmitters so that Transmitter No. 1 is now operating normally.

NOTE

Further minor adjustments to the reference to sideband phasing may be made during commissioning flight check. This phase adjustment may increase the 9960 AM level as determined by the flight check panel technician. If during flight check the 9960 modulation is less than 30 percent the Reference-Sideband Phasing Parameter should be adjusted slightly to find the peak reading as determined by the panel technician. This will provide better sideband efficiency than by increasing the sideband power higher.

9.7.13.6 Setting Transmitter SBO Modulation

- a. Set TX1 and TX2 circuit breakers to the ON position.
- b. Place Transmitter 1 on the antenna by pressing the Main #1 button on the LCU or PMDT.
- c. Place the monitors in bypass.
- d. Select Monitors>>Data and view the 9960 Modulation level.
- e. Adjust Transmitters>>Configuration>>Offset and Scale Factors>> Tx Sideband RF Level Scale for Tx #1 so that Monitors>>Data 9960 Modulation level is 30%.
- f. Place Transmitter 2 on the antenna by pressing the Main #2 button on the LCU or PMDT.
- g. Adjust Transmitters>>Configuration>>Offset and Scale Factors>> Tx Sideband RF Level Scale for Tx #2 so that Monitors>>Data 9960 Modulation level is 30%.

9.7.13.7 Setting Transmitter Azimuth (Az) Index

- a. Place Transmitter 1 on the antenna by pressing the Main #1 button on the LCU or PMDT.
- b. Select Transmitters>>Configuration>>Nominal. Set the Azimuth Index to 0.00 degrees.
- c. Select Transmitters>>Configuration>>Offsets and Scale Factors. In the Tx #1 Azimuth Angle Offset enter the Az offset from -20.00 to +20.00 as needed so that the field monitor reading matches the expected result from survey information. For example if the field monitor location was surveyed to be at 30 degrees then the monitor should read 30 degrees. After a new Az offset is entered then press [F7]. Transmitter No. 1's new Az index will be entered into the station's temporary memory.
- d. Place Transmitter 2 on the antenna by pressing the Main #2 button on the LCU or PMDT.
- e. Select Transmitters>>Configuration>>Offsets and Scale Factors. In the Tx #2 Azimuth Angle Offset enter the Az offset from -20.00 to +20.00 as needed so that the field monitor reading matches the expected result from survey information. For example if the field monitor location was surveyed to be at 30 degrees then the monitor should read 30 degrees. After a new Az offset is entered then press [F7]. Transmitter No. 2's new Az index will be entered into the station's temporary memory.

NOTE

AZ index is used to rotate the RF signal pattern so that the Monitor reading for the field monitor antenna matches the surveyed location for the antenna. During commissioning flight inspection corrections will be made to each transmitter to match the position determined by the flight inspection system.

9.7.13.8 Saving No. 1 Transmitter Operating Parameters

- a. Select RMS>>Config Backup and then press [enter]. This will place the Transmitter's new operating parameters into electrically erasable memory. By means of the lithium battery, The Transmitter's operating parameters are preserved in static ram if system power is lost. The electrically erasable memory is an added precaution against the loss of setup parameters.
- b. A permanent copy should be placed onto the PMDT file system. Select System>>Configuration Save. You will be prompted for a file name. It is suggested that the configuration is saved into different files depicting progress up through the commissioning with different file names for each.

9.7.14 Setting Monitor Alarm Limits

Once Transmitter No.1's operating parameters have been set it will be necessary to check/set the Monitor alarm limits. Refer to [Section 4](#) for appropriate limits.

9.7.14.1 Setting Monitor Az Angle Low Limit

- a. Select Monitors>>Configuration>>Alarm Limits. The Alarm and Prealarm limits will be displayed for Monitor 1 and Monitor 2.
- b. Enter the Az Angle Low Alarm Limit that is needed, then press [F7]. Monitor No. 1's new Az Angle Low Limit will be entered into the station's temporary memory.

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- c. Enter the Az Angle Low PreAlarm Limit that is needed, then press [F7]. Monitor No 1 and 2's new Az Angle Low PreAlarm Limit will be entered into the station's temporary memory.

9.7.14.2 Setting Monitor Az Angle High Limit

- a. Select Monitors>>Configuration>>Alarm Limits. The Alarm and Prealarm limits will be displayed for Monitor 1 and Monitor 2.
- b. Enter the az angle high alarm limit that is needed, then press [F7].
- c. Enter the az angle high prealarm limit that is needed, then press [F7]. Monitor No. 1's new az angle low prealarm limit will be entered into the station's temporary memory.

9.7.14.3 Setting High Monitor 30 Hz Mod Low Limit

- a. Select Monitors>>Configuration>>Alarm Limits. The Alarm and Prealarm limits will be displayed for Monitor 1 and Monitor 2.
- b. Enter the 30 Hz Mod low alarm limit that is needed, then press [F7]. Monitor No. 1 and 2's 30 Hz Mod low limit will be entered into the station's temporary memory.
- c. Enter the 30 Hz Mod low prealarm limit that is needed, then press [F7]. Monitor No. 1 and 2's new 30 Hz Mod low prealarm limit will be entered into the station's temporary memory.

9.7.14.4 Setting Monitor 30 Hz Mod High Limit

- a. Select Monitors>>Configuration>>Alarm Limits. The Alarm and Prealarm limits will be displayed for Monitor 1 and Monitor 2.
- b. Enter the 30 Hz Mod high alarm limit that is needed, then press [F7]. Monitor No. 1 and 2's new 30 Hz Mod high limit will be entered into the station's temporary memory.
- c. Enter the 30 Hz Mod high prealarm limit that is needed then press [F7]. Monitor No. 1 and 2's new 30 Hz Mod high prealarm limit will be entered into the station's temporary memory.

9.7.14.5 Setting Monitor 9960 Hz Mod Low Limit

- a. Select Monitors>>Configuration>>Alarm Limits. The Alarm and Prealarm limits will be displayed for Monitor 1 and Monitor 2.
- b. Enter the 9960 Hz Mod low alarm limit that is needed, then press [F7]. Monitor No. 1 and 2's new 9960 Hz Mod low limit will be entered into the station's temporary memory.
- c. Enter the 9960 Hz Mod low prealarm limit that is needed, then press [F7]. Monitor No. 1 and 2's new 9960 Hz Mod low prealarm limit will be entered into the station's temporary memory.

9.7.14.6 Setting Monitor 9960 Hz Mod High Limit

- a. Select Monitors>>Configuration>>Alarm Limits. The Alarm and Prealarm limits will be displayed for Monitor 1 and Monitor 2.
- b. Enter the 9960 Hz Mod high alarm limit that is needed, then press [F7]. Monitor No. 1 and 2's new 9960 Hz Mod high limit will be entered into the station's temporary memory.
- c. Enter the 9960 Hz Mod high prealarm limit that is needed, then press [F7]. Monitor No. 1 and 2's new 9960 Hz Mod high prealarm limit will be entered into the station's temporary memory.

9.7.14.7 Setting Monitor 9960 Hz Dev Low Limit

- a. Select Monitors>>Configuration>>Alarm Limits. The Alarm and Prealarm limits will be displayed for Monitor 1 and Monitor 2.
- b. Enter the 9960 Hz Dev low alarm limit that is needed, then press [F7]. Monitor No. 1 and 2's new 9960 Hz Dev low limit will be entered into the station's temporary memory.
- c. Enter the 9960 Hz Dev low prealarm limit that is needed, then press [F7]. Monitor No. 1 and 2's new 9960 Hz Dev low prealarm limit will be entered into the station's temporary memory.

9.7.14.8 Setting Monitor 9960 Hz Dev High Limit

- d. Select Monitors>>Configuration>>Alarm Limits. The Alarm and Prealarm limits will be displayed for Monitor 1 and Monitor 2.
- e. Enter the 9960 Hz Dev high alarm limit that is needed, then press [F7]. Monitor No. 1 and 2's new 9960 Hz Dev high limit will be entered into the station's temporary memory.
- f. Enter the 9960 Hz Dev high prealarm limit that is needed, then press [F7]. Monitor No. 1 and 2's new 9960 Hz Dev high prealarm limit will be entered into the station's temporary memory.

9.7.14.9 Setting Monitor Field Intensity Low Limit

- a. Select Monitors>>Configuration>>Alarm Limits. The Alarm and Prealarm limits will be displayed for Monitor 1 and Monitor 2.
- b. Enter the Field Intensity Low Alarm Limit that is needed, then press [F7]. Monitor No. 1 and 2's new Field Intensity Low Alarm Limit will be entered into the station's temporary memory.
- c. Enter the Field Intensity Low PreAlarm Limit that is needed, then press [F7]. Monitor No. 1 and 2's new Field Intensity Low PreAlarm limit will be entered into the station's temporary memory.

9.7.14.10 Setting Monitor Field Intensity High Limits

- a. Select Monitors>>Configuration>>Alarm Limits. The Alarm and Prealarm limits will be displayed for Monitor 1 and Monitor 2.
- b. Enter the Field Intensity High Alarm Limit that is needed, then press [F7]. Monitor No. 1 and 2's new Field Intensity High Alarm Limit will be entered into the station's temporary memory.
- c. Enter the Field Intensity High Alarm Limit that is needed, then press [F7]. Monitor No. 1 and 2's new Field Intensity High PreAlarm Limit will be entered into the station's temporary memory.

9.7.15 Records

- a. Select RMS>>Config Backup and then press [enter]. This will place the new operating parameters into electrically erasable memory.
- b. A permanent copy should be placed onto the PMDT file system. Select System, Configuration Save. You will be prompted for a file name. It is suggested that the configuration is saved into different files depicting progress up through the commissioning with different file names for each.

9.8 INSTALLATION VERIFICATION TEST

- a. Check to make sure that all RF and power connections have been accomplished.
- b. If there are no further adjustments needed to be made to the antenna feed cables, fill the outside of the three conduits with putty to seal against water and vermin.
- c. Heat the shrink tubing on the 48 Sideband and 1 carrier antenna feed cables to provide a moisture seal on the cable connections.

9.8.1 Special Tests

Perform verification procedures of [Section 6](#).

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10 SOFTWARE

10.1 INTRODUCTION

Software documentation contains proprietary information and therefore is not included in this manual.

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11 TROUBLESHOOTING SUPPORT

11.1 INTRODUCTION

This section contains a list of drawings useful during installation and maintenance. Copies of all drawings can be found in the CDROM version of the manual. Drawings that are needed during installation are provided in paper form within the appropriate kit. Paper copies of all drawings can be purchased by contacting the SELEX Sistemi Integrati Inc. Customer Service organization.

Description	Schematic No.	Figure	CDROM	Kit
Family Tree, Dual Doppler	502082	11-1	X	
DVOR Interconnect Diagram	001150A-9101	11-2	X	
Control Backplane CCA	012215-9002	11-3	X	
Sideband Backplane CCA	012260-9001	11-4	X	
Carrier Backplane CCA	012259-9001	11-5	X	
Commutator CCA	012104-9001	11-6	X	
Local Control Unit (LCU) CCA	012179-9001	11-7	X	
Interface CCA	012167-9001	11-8	X	
AC Monitor CCA	012186-9001	11-9	X	
Synthesizer Sideband CCA	012258-0001	11-10	X	
Synthesizer Carrier CCA	012263-0001	11-11	X	
Synthesizer Interface CCA	012262-9001	11-12	X	
Audio Generator CCA	012254-9001	11-13	X	
Monitor CCA	012245-9001	11-14	X	
Low Voltage Power Supply (LVPS) CCA	012222-9001	11-15	X	
Test Generator CCA	012223-9001	11-16	X	
RMS CCA	012172-9001	11-17	X	
Facilities CCA	012171-9001	11-18	X	
Carrier Amplifier CCA	012249-9001	11-19	X	
Battery Charge / Power Supply (BCPS) CCA	012261-9001	11-20	X	

Description	Schematic No.	Figure	CDROM	Kit
Sideband Amplifier CCA	012218-9001	11-21	X	
RF Monitor CCA	012220-9001	11-22	X	
Commutator Control CCA	012257-9001	11-23	X	
Power Installation Kit	470445	11-24	X	
Battery Backup Kit	470639	11-25	X	