THEORY OF OPERATION

2.3.2 Localizer Power Amplifier (030676) (1A22/1A23/1A24/1A25) Theory of Operation -The power amplifier provides both amplification and modulation of the RF signal.

Functional operation of the power amplifiers is indicated by the block diagram Figures 2-5A and 2-5B. Figure 2-5A depicts the CSB channel of the power amplifier and 2-5B shows the SBO channel. Refer to Figure 11-13.

RF carrier at a level of +10 dBm is input to the power amplifier at connector J2. This signal is routed through a high pass filter to remove any low frequency components, amplified in MMIC amplifier C, and routed to power splitters D and E. One output from splitter D provides the carrier for the SBO channel which is described below. The other output goes to splitter E where one output provides a reference signal for the CSB phase lock loop. The other output is routed the electronic phase shifter F and after phase compensation and modulation becomes the CSB output signal which is routed to the Transfer Switch and antenna from J4.

2.3.2.1 Operation of the CSB AM Modulator and Power Amplifier.- Refer to Figure 2-5A and Figure 11-13, sheets 3, 4 and 5. RF from the electronic phase shifter is routed through the MMIC amplifier G to the PIN Diode Modulator H (CR20-CR23). This modulator consists of two diode attenuators in cascade which provide a dynamic range of over 50 dB. Power output of the modulator is controlled by the driver transistor S (Q10) which is in turn controlled by loop amplifier R. The modulator provides AM modulation as well as control of the transmitter carrier power output.

Following the modulator, the modulated signal is passed through a linear power amplifier I, J, K, L, and M. This consists of MMIC amplifier U20, the FET driver amplifier Q12, and the output stages Q13 and Q14. Following the driver amplifier, the RF power is split in power splitter K and then drives the two output power stages L in parallel. The outputs are recombined in power combiner M. After combining, a peak envelope power of over 50 Watts is obtainable. The power stages are high power FET amplifiers which are biased into class AB operation, and operate with an idle current of 200 Ma each. The amplifiers are all broad band matched and have no RF tuning adjustments. Impedance matching is accomplished by multiple step L networks and low Q, T Networks. Examples are C170, L57, C175, and L59 on the input of Q13, and the T network L52, C153, and L53 on the output of Q12.

After the power combiner M, the signal is directed to a low pass filter which removes any harmonics created in the RF power amplifier. This is an elliptic function low pass design which results in total attenuation of harmonics to more than 65 dB below the carrier.

The signal is then routed to the directional coupler O and then to the output at J4. The directional coupler provides samples of both forward and reflected power which are routed to biased, temperature compensated AM detectors Q and P.

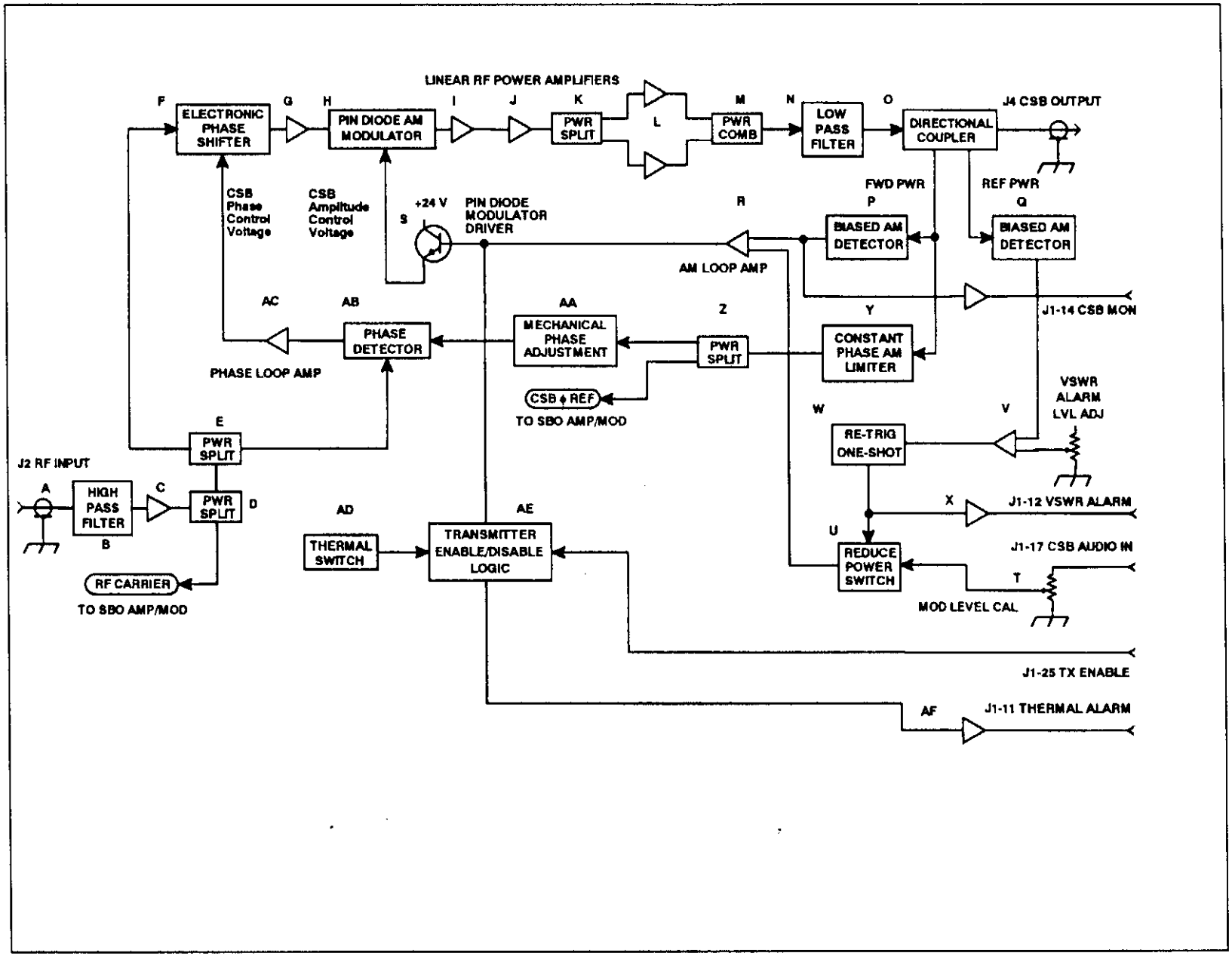

Figure 2-5A RF Power Amplifier - CSB Block Diagram

Reflected power is sensed by detector Q and routed to a comparator V which is set to trip if the reflected power exceeds approximately 5 Watts. This corresponds to a 3 to 1 VSWR at 20 Watts output power.

The comparator output fires a re-trigger able one-shot W, which has two functions, reduction of the transmitter output and sending an alarm to the monitor via the line driver X and J1-12.

2.3.2.2 Operation of the AM Modulation Feedback Loop.- The CSB section power amplifier incorporates an AM feed back loop to control the modulation, power output, and to reduce modulation distortion introduced by non-linearity in the PIN diode modulator, and the linear amplifier.

The AM loop error amplifier R is a differential amplifier which receives inputs from two sources; the audio input originating at J1-17 and the AM detector P which is sampling the transmitter modulated output from directional coupler O.

The audio input consists of the 90 and 150 Hz navigation tones, and 1024 Hz morse identification tones and a DC level. The DC level determines the carrier output level and the total peak to peak AC level of the audio tones determines the percent modulation of the transmitter. This peak level is approximately 7.2 volts relative to ground when the transmitter is running at 20 Watts output.

The audio is routed from the input connector to the modulation level calibration pot T (R113) and then to the "reduce power switch" U (U18) and finally to the loop amplifier R (U17B).

At the loop error amplifier R, the differential inputs are connected so an increased audio input results in increased power output from the modulator, while increased input from the AM detector results in decreased output. As a result, the amplifier acts to keep the waveform at the detector exactly identical to the input waveform at its inputs. Since this amplifier has a very high gain, any error in the detected waveform relative to the audio input results in a change in the output of the amplifier to the PIN diode modulator in the correct direction to correct the error.

The result is that the demodulated output from the biased AM detector P is an exact replica of the input signal with very low distortion. The detected signal is buffered and routed to the Monitor via J1-14. It is also available for test purposes on the PA test point TP4.

2.3.2.3 CSB Phase Feedback Loop Operation.- The CSB channel contains a phase lock loop which has three purposes.

a. The first is to remove undesired phase modulation sidebands from the transmitter output. This modulation occurs due to non-linearity in the PIN diode modulator and also to a lesser extent in the linear RF power amplifier.

b. The second objective is to phase lock the CSB carrier output to the RF input to prevent de-phasing of the system as the CSB power is adjusted.

c. A third function is to provide a carrier phase reference to a second phase lock loop which is used to keep the SBO phase constant and provide for adjustment relative to the CSB carrier phase.

Refer to Figure 2-5A. In addition to the forward power detector, the sample of the forward power output from the directional coupler is routed the constant phase limiter Y. The constant phase limiter consists of 4 differential pair limiter amplifiers which can be compensated such that for a 30+ dB change in input level, the output amplitude and phase do not change. Amplitude variations are held to less than 2 dB and the phase change to less than 5 degrees.

This limiter removes the AM modulation and passes through any phase variations at its input while not contributing any significant phase modulation of its own.

The limiter output is routed to power splitter Z which provides two outputs. One is the CSB phase reference for the SBO phase lock loop. The other is routed via a mechanical phase adjuster AA to the CSB phase detector AB. The mechanical phase adjuster is used to set the operating point of the CSB phase lock loop (refer to schematic sheet 3) and consists of the components associated with C106 and C109.

The phase detector receives the phase feed back from the CSB amplifier as just described. In addition a carrier phase reference is input from power splitter E. The phase detector is a balanced mixer type which produces zero error voltage output when the inputs are at an approximate 90 degree phase difference. Fixed phase shifters, not shown, in addition to the mechanical phase adjustments, provide compensation for circuit and path length phase shifts to set up the desired 90 degree phase difference.

The input of the phase loop error amplifier AC is offset about 200 mV from ground so the effective zero error voltage desired from the detector is approximately 200 mV when the loop is locked.

Total phase control range of the electronic phase shifter is more than 100 degrees for control voltage inputs of 0 to 12 volts with the center of the control range at 3 to 5 volts. The phase shifter is comprised of varactor diode CR16, 90 degree hybrid T3, (refer to schematic sheet 3).

In operation, the mechanical phase shifter is adjusted to cause the loop to lock and to position the loop control voltage output from the error amplifier AC (U10:A on the schematic) in the 3 to 5 volt range.

The loop bandwidth is sufficiently wide so that undesired Phase Modulation occurring in the PIN modulator or the linear power amplifier is processed and results in a compensating correction voltage producing an immediate and opposite phase shift by the electronic phase shifter. Phase modulation components appearing in the transmitter output spectrum are reduced to more than 30 db below the desired 90 and 150 Hz sidebands.

2.3.2.4 Transmitter Enable/Disable Logic.- Control of the transmitter On/Off status is provided by the transmitter Enable/Disable Logic AE which acts on both the CSB and SBO modulation circuits. The Tx-Enable signal is input J1-25. This is a low=True logic level which must be Low to enable

the transmitter. Also input to the logic is a signal from the Thermal Switch AD. This input will shut the transmitter down if the heat sink temperature exceeds a preset limit. In the event the thermal shut down occurs, a high=True logic level is routed to the Monitor via J1-11.

The output from the control logic is routed to the PIN diode modulator driver input transistor base terminals (transistors Q10 CSB and Q2 SBO) and essentially shunts the AM loop amplifier outputs to ground, which removes the RF drive from the linear amplifiers in both the CSB and SBO channels.

2.3.2.5 SBO Modulator and Power Amplifier Operation - Operation of the SBO AM modulator, feedback loop, and power amplifier is essentially the same as for the CSB channel, but there are some difference which will be discussed in this section. Refer to the block diagram Figure 2-5B which depicts the SBO channel.

RF carrier power is input to the SBO channel from the power splitter D on the CSB block diagram. This signal passes through an electronic phase shifter BB, a 0/180 degree Bi-Phase switch, and then to the PIN diode modulator, power amplifier, low pass filter, and to the output connector J3 via the directional coupler BH, and the output pad BI.

The linear power amplifier BF consists of Q6 and Q7 on page 2 of the schematic. A single, lower power output, device is used as only a few watts peak envelope power is required from the SBO amplifier. Again, this is wide bandwidth amplifier so no RF tuning adjustments are needed.

Operation of the AM feedback loop and modulator are identical to the CSB channel. There is one difference. A detector bias offset adjustment BT is provided to enable the SBO detector offset to be compensated so that 100 percent modulation of the SBO waveform can be obtained without clipping of the lower peaks at the base of the SBO envelope. The unit to unit modulation sensitivity is set by input pot R54 on page 1 of the schematic, and the detector offset bias control is R45.

The SBO power amplifier has a 6 dB attenuator at the output which may be selected by setting two jumpers. This attenuator is used in installations requiring very low SBO power to meet the operational requirement of the site. Provision of the attenuator enables the power stage, constant phase limiter, and detector to operate at higher levels for optimal performance.

2.3.2.6 Operation of the SBO Channel Bi-Phase Switch. - The SBO carrier is suppressed by means of a 0/180 degrees bi-phase switch BC which reverses the phase of the RF signal in synchronism with the polarity reversals of the SBO modulation wave form.

The control signal for the switch is a 0-5 Volt logic level which is input to the power amplifier from the synthesizer audio generator module. When the signal is High the SBO phase is not reversed (relative to the CSB carrier). When it is low, the phase is shifted 180 degrees.

The Bi-Phase switch drive is also applied to an error correction switch in the SBO phase lock loop which is discussed in the next section.

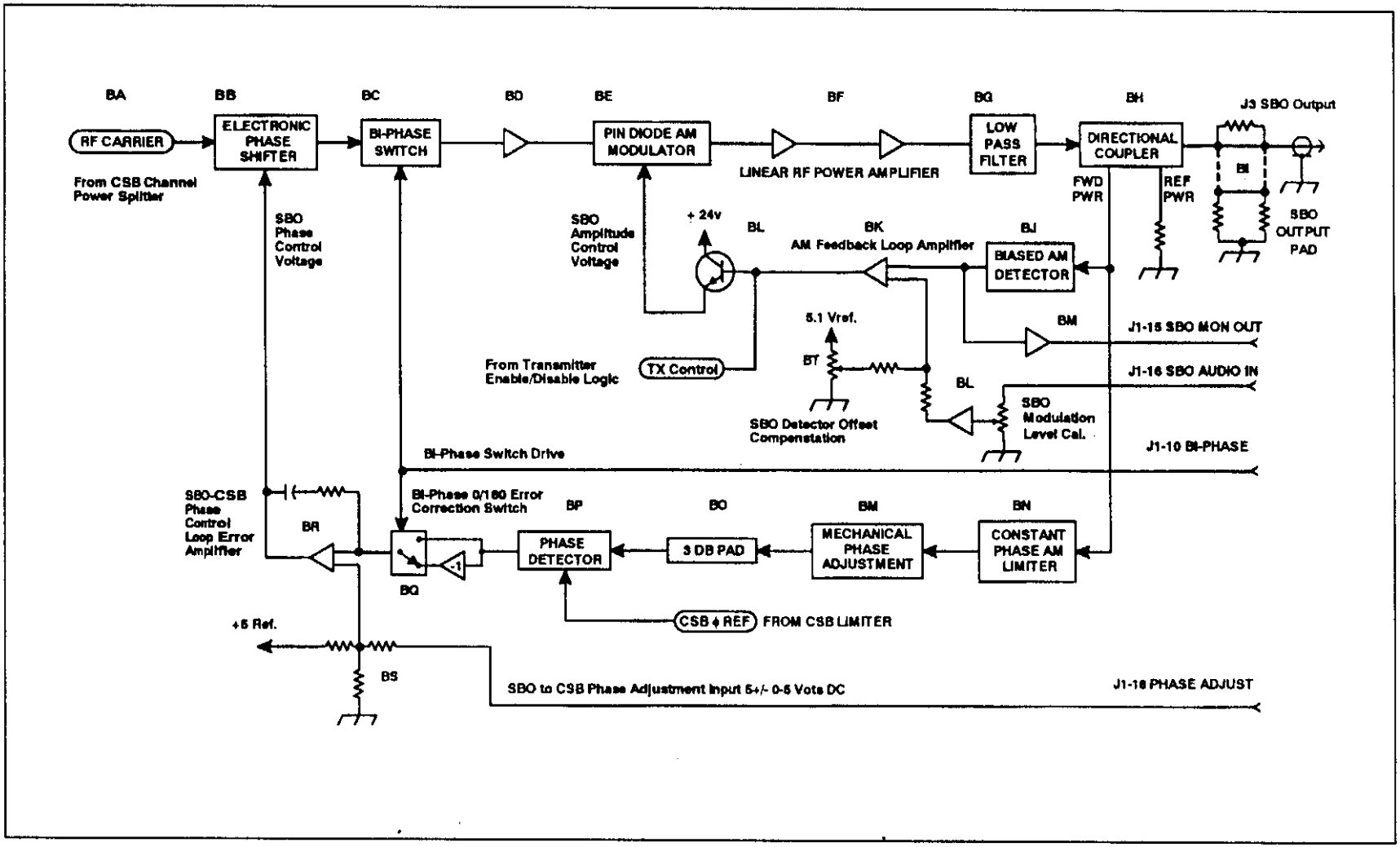

Figure 2-5B RF Power Amplifier - SBO Channel Block Diagram

2.3.2.7 Operation of the SBO Channel Phase Lock Loop. - The SBO phase lock loop is similar in operation to the CSB phase lock loop; however the functions are not the same. This PLL two main functions:

a. Maintain the phase of the SBO suppressed carrier relative to the CSB carrier as the SBO power is adjusted and over the specified service conditions.

b. Provide a convenient means to electronically adjust the SBO phase relative to the CSB to phase the system.

The phase lock loop consists of the constant phase limiter BN, a mechanical phase adjuster BM, the phase detector BP, the Bi-Phase Error Correction Switch BQ, and the loop amp and electronic phase shifter, BR and BB.

The SBO output is shifted 0/180 degrees by the Bi-phase switch. This results in a continual reversal of the error voltage from the phase detector which must be corrected before the error signal can be processed by the loop amplifier. The Bi-Phase Correction Switch synchronously selects the phase detector output or an inverted replica of the output which is created by a unity gain inverter stage. This removes the effect of the bi-phase switch from the phase error signal and permits the PLL to operate normally.

Unlike the CSB loop, the SBO loop is not a fast loop and no attempt is made to compensate for amplitude induced phase distortion. Because of the low power required of the SBO linear amplifier, dynamic phase corrections is not necessary.

It is required that the SBO suppressed carrier be nominally in phase with the CSB carrier and that the phase between the two be electronically adjustable. This is accomplished as follows.

The total phase shift through the CSB and SBO channels is well controlled such that if both electronic phase adjusters (SBO and CSB) are driven with the same control voltage the phase difference between the two channels is less than 30 degrees. The phase lock loops then act to maintain an exact phase relationship by controlling the two phase shifters.

The CSB output phase is locked to the carrier input by the CSB loop. This phase may be adjusted under closed loop conditions by adjusting the mechanical phase shifter AA in the CSB phase feed back loop. During factory alignment the SBO phase shifter is fist set to the center of the SBO electronic control range by using a fixed DC voltage. Then the CSB phase is adjusted to have the same output phase as the SBO.

The SBO loop is then closed and the SBO mechanical adjustment BM is set to make the SBO carrier phase identical to the CSB.

Because the phase reference for the SBO loop is obtained from the CSB limiter, the SBO and CSB track each other and will remain in phase if the power of either output is adjusted or if the temperature changes.

Adjustment of the SBO phase is accomplished by a DC input which ranges from 0 to 10 volts. 5.0 volts is defined as the SBO to CSB 0 degree phase difference point. Increasing voltage above 5 volts causes the SBO phase to lead the CSB, and decreasing the control voltage causes it to lag the CSB. Setting of the mechanical adjustment BM to align the SBO phase with the CSB as described above is accomplished with this phase control input voltage set to 5.0 Volts. At least +/- 20 degrees of adjustment range is provided.

The resistive summing junction at BS on Figure 2-5B (R25, R26, and R17 on sheet 1 of the schematic) is sets the phase control range. Resistor R-25 sets the slope of the phase adjustment function which is approximately linear.