CIRCUIT DESCRIPTION UHF - BAND

The paging receiver circuit is composed of 15 main sections:

1. Antenna circuit
2. RF amplifier
3. SAW filter
4. PLL IC
5. Loop filter
6. VCO
7. First mixer
8. IF IC
9. HPF
10. Squelch
11. Audio volume
12. AF PA
13. Decoder
14. D/D, Driver IC
15. EEPROM

1. Antenna Circuit
   The loop antenna (ANT 1, ANT 2) and telescoping antenna (ANT 3) are built into the pager and are designed to receive the UHF – band signals. The tuning frequency is automatically adjusted by the control voltage obtained from the PLL IC (A3). The antenna loop is adjusted by CV1 and the telescoping antenna is a pre – select tuned circuit for the designated band.

2. RF amplifier
   The RF signal couples through C6 to the input of the cascade amplifier (Q1, Q2). The amplified signal from Q2 passes through C10 to the SAW filter (FL1).

3. SAW filter
   FL1 is the wide band SAW (Surface acoustic wave) filter. The bandwidth will be 10MHz to 11MHz, which will cover one of the bands. The unwanted frequency will be attenuated fully by this SAW filter.

4. PLL IC (A3)
   The receiving frequency is determined by the data supplied from the decoder CPU (A202). The control voltage is obtained by comparing the VCO local oscillator frequency and the 12.8MHz reference oscillator frequency.

5. Loop filter
   The control voltage from A3 is supplied to the loop filter via a analog switch (A4). The loop filter consists of R21, R22, R23, C35, C36, and C37 which eliminates unwanted high frequency interference.

6. VCO
   The oscillator frequency is regulated by the control voltage and is supplied to the multiplier circuit through the buffer circuit. The oscillator frequency is set to ½ of its 1^{st} local frequency. 1^{st} local frequency = receive frequency - 21.6MHz.

7. First mixer
   The amplified RF signal and the injection signal in the VCO are fed into the 1^{st} mixer (Q3). Two signals are mixed with the resulting 21.6MHz and fed into the crystal filter (FL2).

8. IF IC (A1)
The IF IC consists of: 2nd oscillator, 2nd mixer, IF amplifier, demodulator, filter amplifier, voltage regulator, and LVA (low – voltage – alarm).

A) 2nd oscillator
The 2nd oscillator circuit consists of a series resonate quartz crystal (21.145MHz) and IC (A1).

B) 2nd mixer
The output signal (21.6MHz) from FL2 and the output signal (21.145MHz) from the 2nd oscillator are mixed for a resulting signal of 455KHz.

C) IF amplifier / demodulator
The output of the 2nd mixer is routed through a ceramic filter (FL3), internal IF amplifier, and demodulator stages

D) Filter amplifier
After demodulation, the audio signal is fed into the HPF (for tone and voice) and the BPF (for noise amp.). The output signal of the HPF is fed into the LPF consisting of R50, R51, R52, C65, C66, C67, and the internal filter amplifier of A1. The LPF attenuates and filters frequencies over 3KHz.

E) Comparator
The filtered signal is then converted to a digital signal, the output is on A1 pin 15.

F) Voltage regulator
The battery voltage is regulated by A1 and Q7. The voltage regulator supplies 1.0V to the receiver circuit.

G) LVA
The LVA circuit produces a low battery signal to the decoder CPU (A202) when the battery voltage drops below 1.1 volts

9. HPF
The high pass filter (HPF) consists of A2, C62, C63, C64, R42, R43, and R44 which eliminate the CTCSS tones from being amplified by the audio circuitry.

10. Squelch
The squelch circuit consists of the BPF (A2 – D / A, C51 thru C56 and R27 thru R30), noise amplifier (Q8, Q9), and detector (Q10 thru Q13). The squelch sensitivity is controlled by variable resistor RV1.

11. Audio volume
The audio signal is controlled by R105 and R106 thru R108 in 4 audio volume levels. The output of audio signal is supplied by the AF PA through the buffer amplifier (Q106).

12. AF PA
The audio IC (A102) and associated components form a complementary amplifier circuit for the alert tone and voice message. Transistors Q108 and Q109 provide additional current handling for driving the speaker SP1.

13. Decoder
The decoder consists of two clock oscillators (A104, A105), tone detector module (A201), and CPU (A202).

A) Clock oscillator
The pager operates with two clock oscillator circuits. The main clock circuit frequency is 1.2288MHz and is controlled by A202 pin 16. When the pager is operating with the battery save function, the main clock oscillator is stopped for a period of time and the pager is in the "SAVE" mode. The SUB clock circuit oscillates continuously and provides a means for the internal timer operation.

B) Tone detector (A201)
The tone detect module (A201) consists of a alert generator circuit and tone detector circuit.

C) CPU (A202)
The CPU will control various functions based on the EEPROM such as, tone parameter setting to detector IC (A201), frequency parameter setting to the PLL IC (A3), various switching operations, and the CPU output of the detector IC and timing of ESGA and ESGB.

14. D/D, Driver IC
The regulated 3.0V is developed through L101 and the associated voltage multiplier circuitry in the A103. The voltage multiplier drives a switching circuit which sends pulses to L101. D102 rectifies the pulses and C109 filters them generating a regulated 3.0V. This is distributed to the decoder IC (A201, A202), EEPROM (A101), clock oscillator (A104, A105), and PLL IC (A3). A103 provides the functions for the LED (D101) and vibrator (MR101) option.

15. EEPROM
The EEPROM (A101) will retain all programmed information such as: channel frequencies, tone frequencies, tone combinations, alert cycles, scan, timing, and etc… When the paged is turned "ON", A202 will detect the required information from the EEPROM.