FACSIMILE COVER PAGE

To :	**MR. SCOTT**	**From :**	ANTONY
Sent :	3/24/99 at 3:40:16 PM	**Pages :**	4 (including Cover)
Subject :			

Scott,

I only have the information attached and below.

Bit 0 = 1
Bit 1 = 2
Bit 2 = 3
Bit 3 = 4

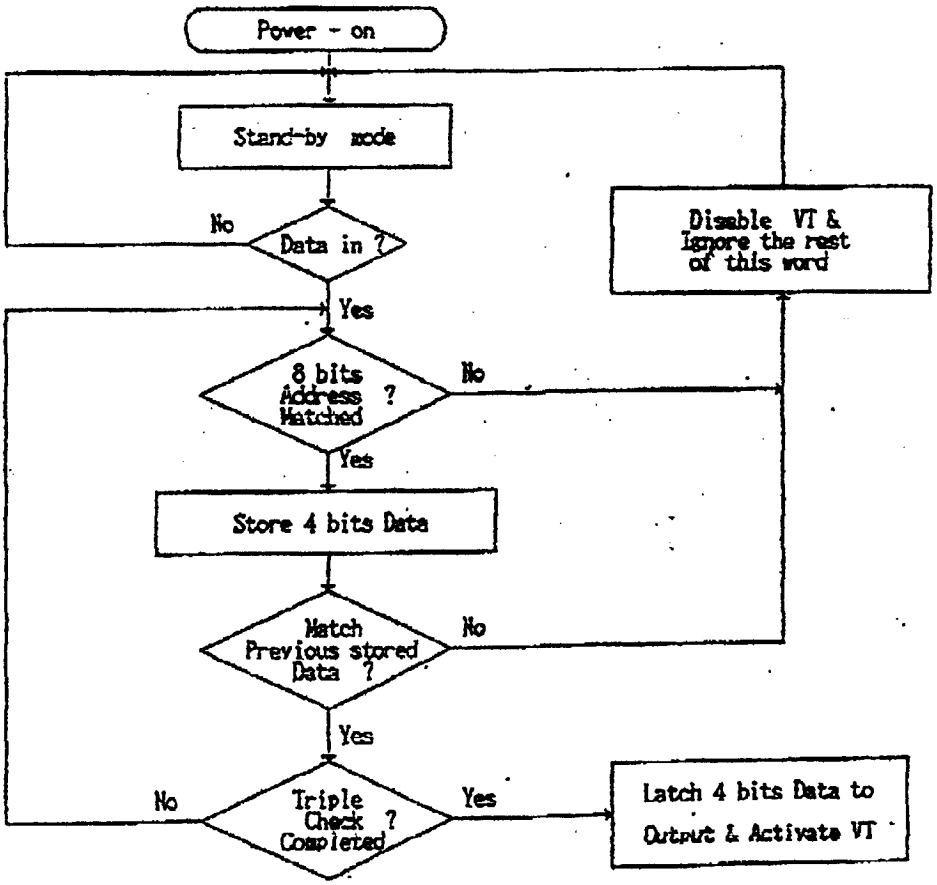
Bit 0 is LSB.

The 1,2,3,4 are the ID selection at the back of the receiver & transmitter. Moreover, the engineer used 4 bits only of 8 bits for the ID selection. } THE ENGINEER USED 4 OF THE 8 BITS FOR THE TX,

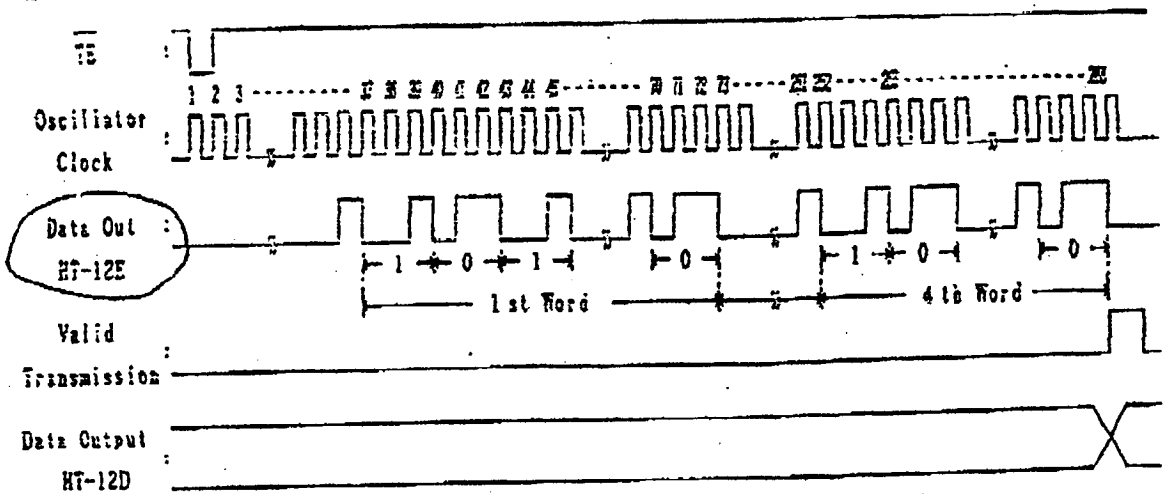
If you have any problems, please feel free to contact me. Thanks!!!

Regards,
Antony Chung
P.S. : We still waiting for your quotation of 2.4 GHz A/V Tx system.

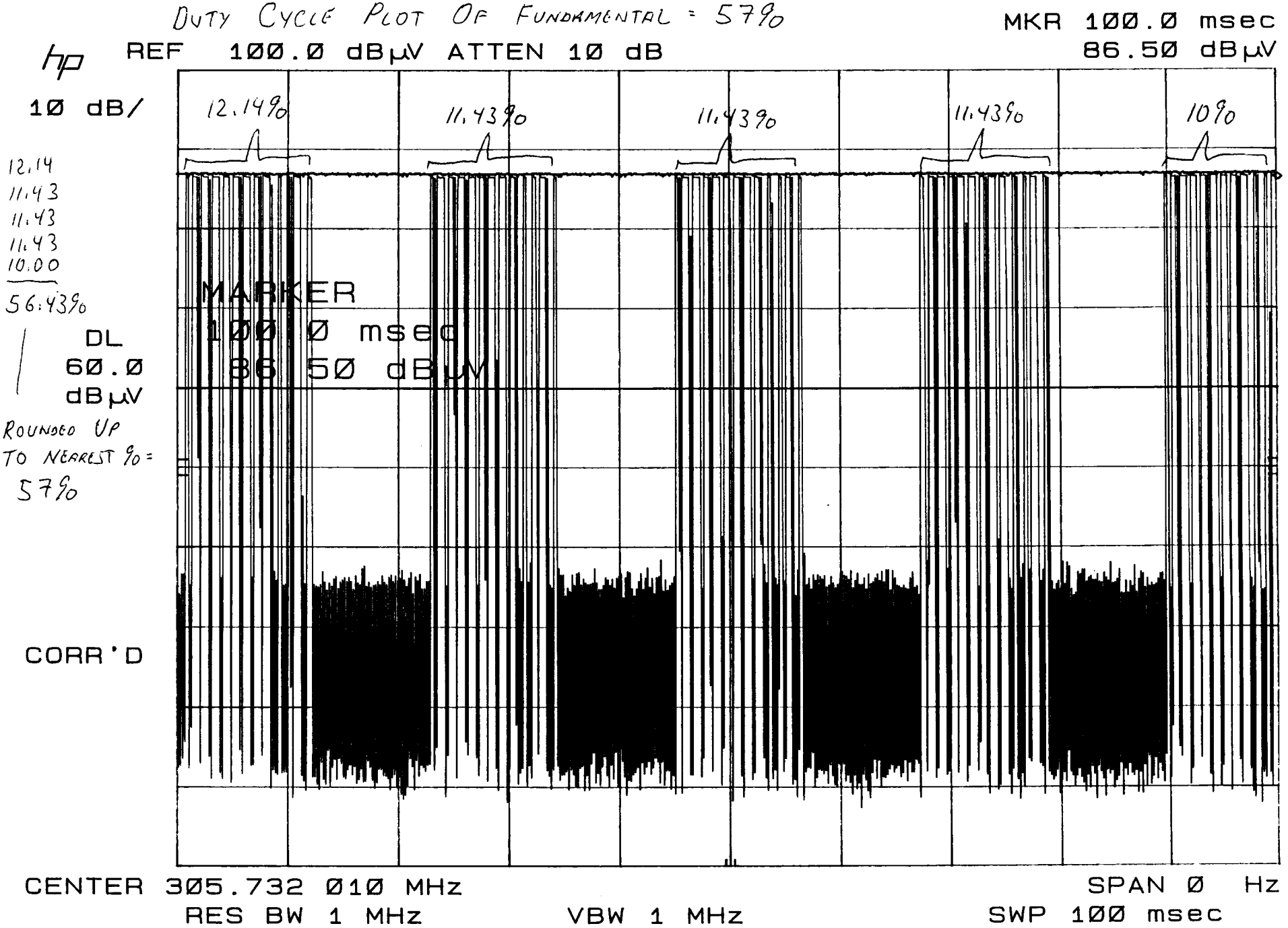
K. HT-12D Decoder Flowchart -



. Encoder / Decoder Timing Diagram -



DUTY CYCLE PLOT OF FUNDAMENTAL = 57%



12.14
11.43
11.43
11.43
10.00

56.43%

ROUNDED UP TO NEAREST % =
57%