CIRCUIT DESCRIPTION

4.1 GENERAL

4.1.1 INTRODUCTION

The DM-3473 consists of a low dropout regulator power supply, frequency synthesizer and VCO (voltage controlled oscillator), 2 watt RF power amplifier, and dual down conversion FM receiver. A block diagram of the transceiver is located in Figure 4-1 and shows the four major sections of the unit.

The VCO is enclosed by a metal shield and soldered directly to the printed circuit board (PCB). The VCO unit is not field serviceable. The transmitter is also covered by a metal shield to prevent radiation of RF power causing interference. The 3473 comes standard with a reference oscillator stability of + 1.5 PPM over the entire operating temperature range.

4.2 POWER SUPPLY CIRCUIT DESCRIPTION

Main DC power is delivered to the transceiver on pin 5 of the user interface connector (J201). This pin requires a regulated power supply voltage between 6 and 9 VDC. The voltage on this pin powers the on board low drop out regulator U130. The regulator provides constant 5.5 VDC to all of the relevant sections of the transceiver such as the VCO/Synthesizer, Receiver, and Regulator sections of the transmitter. Pins 1 and 2 provide the ground connection of the transceiver.

Pins 3 and 4 of J201 are the main power supply to the RF power amplifier. This voltage is set between 6 and 9 VDC with 7.2 VDC being the nominal voltage to guarantee 2 watts +\-0.4 watts of RF power at the antenna connector. All three pins (3,4,and 5) can be tied together on a customer interface board if the maximum voltage limits are always between 6-9 VDC.

The transmit and receive enable pins (pins 6 and 7) of J201 are a logic voltage input to turn on the transmitter or receiver. The necessary voltage is between 4.5 and 13 VDC for the enable mode. Refer to the programming section 3 for the implementation of the transmit and receive enable pins.

The DM-3473 is equipped with a sleep mode pin for implementing current saving features by the customer when a transceiver requires a standby mode. Pin 8 requires a logic level >2.0 VDC to enable the transceiver, this voltage must always be high when the transceiver is in operation. Pin 8 can be grounded to put the radio to sleep. The transceiver will draw less than one milliampere in sleep mode.

4.3 SYNTHESIZER/VCO/TX MODULATION

The VCO is an oscillator which can be controlled by an input voltage to oscillate at a desired frequency. The VCO in the 3473 serves either the receiver or the transmitter dependent on the desired operation. The frequency of the VCO for receive mode is 86.85 MHz above the desired receive frequency. For the transmitter the VCO produces the signal corresponding to the desired transmit frequency.

The DC voltage controlling the oscillator frequency is generated by synthesizer IC U811. The VCO control voltage can be measured at test point TP831 on the PCB. When the VCO is locked (>3.5 Vdc on pin 11 of J201) TP831 will measure between 0.5 and 5.00 VDC, dependent on the frequency of operation. An unlocked condition (indicated on pin 11 of J201) is less than 1.5 VDC. The synthesizer determines the lock state of the radio by comparing the scaled VCO frequency to the scaled reference oscillator TCXO of 14.4 MHz.

The VCO is a Colpitts oscillator formed by Q962 along with several capacitors, varactor diodes, and a ceramic resonator. The DC bias to the VCO is provided by transistor Q901 and forms a capacitance multiplier which delivers filtered, noise free supply voltage to the oscillator circuitry. The VCO is followed by gain stages which amplify the signal to approximately 0 dBm and then divide the signal using a splitter and sending it to the receiver or transmitter.

The VCO is capable of oscillating between 403-434 MHz or 450-480 MHz in transmit and 489.85-520.85 MHz or 536.85-566.85 MHz in receive. The course frequency shift in the VCO between receive and transmit is accomplished by shifting in a capacitor to the tank of the oscillator. Pin 7 of J201 (receive enable) performs this function. When transmitting, the receive enable is forced low and a pin diode is turned on by a digital transistor connected to pin 7 which switches capacitance into the oscillator circuit. The reverse happens when returning to receive mode. Refer to section 3 for receive to transmit and transmit to receive load sequences.

There are two parts to the transceiver modulation circuitry. With the placement of the VCO control line voltage low pass filter at approximately 400 Hz, it is necessary to modulate both the VCO and the TCXO. A loop response of 400 Hz is necessary to accomplish the fast lock times of the 3473. If only the VCO were modulated to transmit data, any baseband frequency component below 400 Hz would not be modulated onto the transmit carrier. To accomplish this the transceiver was designed to modulate both the VCO and TCXO, thus creating two parts to the modulation circuit and modulation capability from below 50 Hz up to 5000 Hz.
It is important to note that modulation sensitivity adjustment and modulation deviation limiting are to be supplied in the customer interface equipment, and are required by most regulatory agencies, such as the Federal Communications Commission (FCC) in the United States.
The modulation flatness adjustment (R825) balances the sensitivity of the VCO vs. the TCXO. The radio is set to best modulation flatness in the center of the RF band (418.5 MHz or 465 MHz) when the unit leaves the Dataradio factory. The modulation flatness becomes uneven when nearing the band edges due to changing sensitivity of the TCXO and VCO across a wide range of RF frequencies.

If optimal modulation flatness is desired across the whole RF band of 450-480 or 403-434 MHz, the unit is equipped with an external flatness adjust. Pin 9 of J201 allows the implementation of an analog voltage between 0 and 5 VDC to obtain flat modulation. Linear interpolation of this voltage between the RF band edges will insure flat modulation everywhere in the band. If flat modulation is desired only in a single or small range of grouped frequencies, R825 of the 3473 module can be tuned for flat modulation and pin 9 of the user connector left open.
The frequency stability of the VCO in receive and transmit mode is established by the stability of the reference oscillator. The reference oscillator for the 3473 is 14.4 MHz and is designed to be stable between + 1.5 PPM over the entire operating temperature range of -30 ° ° to +60 ° ° C. Pin 10 of the user interface connector is the modulation input to the VCO and TCXO as described above, however this pin also serves another purpose. A precision 2.5 VDC reference is essential for the TCXO to compensate + 1.5 ppm for changes in ambient temperature. Pin 10, in addition to modulating the data, requires a DC component of 2.5 VDC + 0.05 VDC.
Channels are selected by programming counters in U811. Section 3 of this manual shows how to program the Phillips SA7025A Frequency Synthesizer for the DM-3473. This programming is performed over a 3-wire serial bus formed by pins 14, 15, and 16 of user interface J201. These pins are labeled Synth Enable, Synth Data, and Synth Clock. This programming is supplied by customer hardware and software interface equipment. A block diagram of the synthesizer/VCO is shown in Figure 4-1 along with a block diagram of the Phillips synthesizer IC SA7025A in Figure 4-2.

4.4 RF POWER AMPLIFIER CIRCUIT DESCRIPTION

The 3473 transmitter produces a nominal RF power output of 2 Watts (+33 dBm) at a supply voltage on pins 3 and 4 of 7.2 VDC. Frequency modulation (FM) of the transmit data input stream occurs in the VCO (see previous section).
The transmitter line-up on the 3473 is a class C conduction type amplifier. A class C amplifier requires that the RF voltage being applied to the amplification device is sufficient as to cause the transistor to “turn-on”. This type of design was incorporated to improve efficiency over a class A type amplifier.
There are two major sections to the power amplifier in the 3473. A driver integrated circuit is the first device in the amplification line-up. The VCO is applied through a splitter and matching network to this device for intermediate amplification to +26 dBm (400 mW). The input voltage for this device is approximately 2.7 VDC. This low dropout regulated supply is produced by a dual op amp and a high current series pass PNP transistor Q611.
The power delivered from the driver stage is matched into a high power MOSFET transistor Q541. This device has about 8 dB of gain and amplifies the signal to +34.5 dBm. The RF voltage created from the driver stage is sufficient to turn on the MOSFET. The final is biased on to a quiescent current of Idss=200 mA which is set by R521. C552 is adjusted for balanced output power across the RF band. Present on the output of the final transistor is a low-pass transmitter harmonic filter. To insure the 3473 meets stringent regulatory guidelines a 5 pole filter rejects the harmonics created in the power amplifier.

Three PIN diodes and several matching components are used to implement the antenna switch. In transmit mode, the diodes are all forward biased. A finely tuned coil and capacitor create a quarter wave open which reflects the transmitter power and protects the receiver front end from the transmitter. In receive mode the diodes are off thus creating a 50 ohm impedance path to the front end of the 3473 receiver. Due to passive device losses in the low pass filter and the antenna switch, the output power is reduced to 2 watts. The transmit signal is then fed to the female MCX antenna connector J501.

The 3473 implements a logic level at the user interface connector to enable the transmitter. By applying a logic high to pin 6 the transmitter will enable, assuming the synthesizer and VCO are locked and ready to transmit. Refer to section 3 for the exact receive to transmit load sequence. When the logic level is applied the RF is brought up relatively slow so that spectral spreading of the transmitter does not occur. An RC time constant 'ramps' up the RF power to the final which takes no longer than 2 ms. The ramping is incorporated so that the power of the transmitter does not splatter into channels adjacent to the frequency of operation.

4.5 RECEIVER CIRCUIT DESCRIPTION

The receiver on the 3473 is a FM dual down conversion superheterodyne topology. Dual down conversion means that the receiver has two intermediate frequencies (IF) of 86.85 MHz and 450 kHz. The first local oscillator (LO) is high side injected 86.85 MHz above the desired receive frequency. This is the function of the VCO in receive mode. The design also incorporates two discrete bandpass filters to reject image and other wideband frequencies. A surface acoustic wave (SAW) filter is implemented in the first IF to enhance receiver selectivity. 10 poles of filtering are used in the second IF to further improve selectivity and to set the IF bandwidth of either 12.5 kHz or 25 kHz. Figure 4-1 shows the receiver block diagram for the 3473 radio module.

From the antenna connector the signal is fed to a two pole bandpass filter. This filter sets the initial RF bandwidth of approximately 30 MHz for the receiver. A low noise amplifier (LNA) is matched from the bandpass filter. The LNA transistor Q210 produces about 14 dB of gain and sets the overall sensitivity of the radio. The LNA is followed by a three pole bandpass filter to help reject unwanted out of band RF signals. Both bandpass filters are discrete filter designs comprising of several air wound inductor coils and many surface mount capacitors.

The front end of the receiver is finely tuned into the mixer of the receiver. The mixer is an active design using a dual gate gallium arsenide MESFET labeled Q240. One gate of the FET is fed the RF signal from the front end network, and the other gate is fed the first LO injection from the VCO. To buffer the VCO from the receiver a transistor (Q302) with unity gain is in between the mixer and the VCO. The mixer, for example, converts the RF signal of 450 MHz and the first LO signal of 536.85 MHz to the first IF frequency 86.85 MHz.

From the mixer, the receive signal is delivered to a SAW filter which has a bandwidth of 40 kHz and provides the first narrow band filtering in the receiver. SAW filter technology features low group delay performance for data applications, low distortion at high RF input levels, and fixed tuning. The output of the SAW filter travels to a Phillips SA676 IF IC for down conversion to the second IF frequency, FM limiting, and demodulation to baseband of the data signal. The block diagram of U261 is shown in Figure 4-3.