

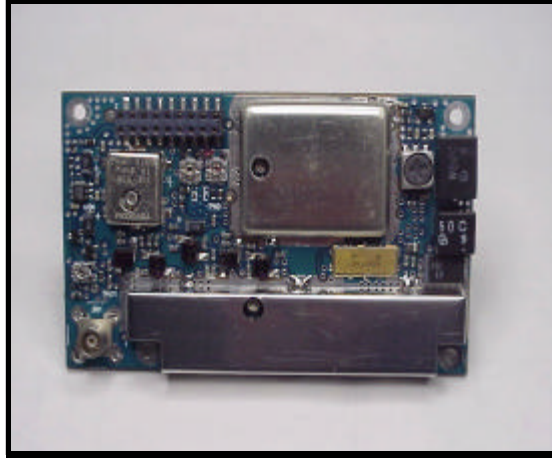
**DM-3473 Synthesized  
UHF Data Module  
Technical Manual**

Part Number: 242-3473-XXX

***DATARADIO***®

# **DM-3473**

## **Synthesized UHF Data Module**



001-3473-202  
Revision 1  
February 2000

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Dataradio COR Ltd. designs and manufactures radios and radio modems to serve a wide variety of data communication needs. The Dataradio Corporation produces equipment for the fixed data market including SCADA systems for utilities, petrochemical, waste and fresh water management markets and RF boards for OEM applications in the Radio Frequency Data Capture market.

### **PRODUCT WARRANTY**

The manufacturer's warranty statement for this product is available from Dataradio COR Ltd., 299 Johnson Avenue, Box 1733, Waseca, MN 56093-0833. Phone (507) 835-8819.

The information in this document is subject to change without notice.

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# TABLE OF CONTENTS

## 1 GENERAL INFORMATION

1.1	SCOPE OF MANUAL	1-1
1.2	EQUIPMENT DESCRIPTION	1-1
	GENERAL	1-1
	DM-3473 SYNTHESIZER PROGRAMMING	1-1
1.3	TRANSCEIVER IDENTIFICATION	1-1
1.4	PART NUMBER BREAKDOWN	1-2
1.5	CUSTOMER SERVICE/TECHNICAL SUPPORT	1-2
1.6	PRODUCT WARRANTY	1-3
1.7	REPLACEMENT PARTS	1-3
1.8	IF A PROBLEM ARISES	1-3
	FACTORY REPAIR	1-3
	GENERAL SPECIFICATIONS	1-4

## 2 INSTALLATION

2.1	PRE-INSTALLATION CHECKS	2-1
2.2	INTERFACING WITH DATA EQUIPMENT	2-1
	CONNECTOR PIN ASSIGNMENTS	2-1

## 3 PROGRAMMING

3.1	INTRODUCTION	3-1
3.2	DM-3473 SERIAL INTERFACE SPECIFICATION	3-1
3.3	FRACTIONAL-N SYNTHESIZER	3-1
	INTRODUCTION	3-1
	SYNTHESIZER DATA PROTOCOL	3-2
	SYNTHESIZER DATA	3-2
3.4	SYNTHESIZER BIT DEFINITIONS	3-3
	INTRODUCTION	3-3
	D-WORD	3-3
	C-WORD	3-4
	B-WORD	3-4
	A0-WORD	3-4
3.5	SYNTHESIZER LOAD PARAMETER EXAMPLE	3-4
3.6	RECOMMENDED SYNTHESIZER LOAD SEQUENCE	3-11
	RECEIVE TO TRANSMIT SEQUENCE	3-11
	TRANSMIT TO RECEIVE SEQUENCE	3-12
3.7	A0 WORD ALGORITHM	3-13

## 4 CIRCUIT DESCRIPTION

4.1	GENERAL	4-1
	INTRODUCTION	4-1
4.2	POWER SUPPLY CIRCUIT DESCRIPTION	4-1
4.3	SYNTHESIZER/VCO/TX MODULATION	4-4
4.4	RF POWER AMPLIFIER CIRCUIT DESCRIPTION	4-5
4.5	RECEIVER CIRCUIT DESCRIPTION	4-10

# TABLE OF CONTENTS

## 5 SERVICING

<b>5.1</b>	<b>GENERAL</b> .....	5-1
	PERIODIC CHECKS .....	5-1
	SURFACE-MOUNTED COMPONENTS .....	5-1
	COMPONENT LAYOUTS AND SCHEMATIC DIAGRAM .....	5-1
	REPLACEMENT PARTS LIST .....	5-1
	TCXO MODULE NOT SERVICEABLE .....	5-1
<b>5.2</b>	<b>SYNTHESIZER SERVICING</b> .....	5-1
	INTRODUCTION .....	5-1
	REFERENCE OSCILLATOR .....	5-2
	VCO .....	5-2
	SYNTHESIZER (U811) .....	5-2
<b>5.3</b>	<b>RECEIVER SERVICING</b> .....	5-2
	SUPPLY VOLTAGES AND CURRENT .....	5-3
	IF/LIMITER/DETECTOR/2ND LO (U261) .....	5-3
	RF AMPLIFIER (Q210) AND FIRST MIXER (Q240) .....	5-4
<b>5.4</b>	<b>TRANSMITTER SERVICING</b> .....	5-5
	SUPPLY VOLTAGES AND CURRENT .....	5-4
	TRANSMIT DRIVER STAGE .....	5-5
	POWER AMPLIFIER FINAL STAGE .....	5-5
	LOW PASS FILTER AND ANTENNA SWITCH .....	5-5

## 6 ALIGNMENT PROCEDURE AND PERFORMANCE TESTS

<b>6.1</b>	<b>GENERAL</b> .....	6-1
<b>6.2</b>	<b>ALIGNMENT PROCEDURE</b> .....	6-1
	VCTCXO SETUP (Y801) .....	6-1
	FREQUENCY AND CONTROL LINE VOLTAGE CHECK .....	6-1
	2W TRANSMITTER POWER ALIGNMENT .....	6-1
	MODULATION FLATNESS ALIGNMENT .....	6-2
	FRACTIONAL CHANNEL SPUR ADJUSTMENT .....	6-3
	RECEIVER ALIGNMENT .....	6-4

## 7 PARTS LIST

## 8 COMPONENT LAYOUTS

TRANSCIEVER COMPONENT LAYOUT-COMPONENT SIDE VIEW .....	8-1
TRANSCIEVER COMPONENT LAYOUT-OPPOSITE SIDE VIEW .....	8-2
DM-3473 MECHANICAL DIMENSIONS .....	8-3

## 9 SCHEMATIC

TRANSCIEVER SCHEMATIC .....	9-1
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# TABLE OF CONTENTS

## LIST OF FIGURES

3-1	SYNTHESIZER SERIAL DATA STREAM.....	3-2
3-2	BIT DEFINITIONS .....	3-3
4-1	DATA TRANSCEIVER BLOCK DIAGRAM .....	4-2
4-2	U811 SYNTHESIZER BLOCK DIAGRAM.....	4-3
4-3	U261 BLOCK DIAGRAM.....	4-7
5-1	RECEIVER SERVICING FLOWCHART .....	5-4
5-2	TRANSMITTER SERVICING FLOWCHART .....	5-6
6-1	TRANSMITTER TEST SETUP .....	6-2
6-2	RECEIVER TEST SETUP.....	6-4
6-3	ALIGNMENT POINTS DIAGRAM.....	6-5
8-1	3473 COMPONENT LAYOUT (TOP SIDE VIEW) .....	8-1
8-3	3473 COMPONENT LAYOUT (BOTTOM SIDE VIEW).....	8-2
9-1	TRANSCEIVER SCHEMATIC .....	9-1

## LIST OF TABLES

2-1	PIN ASSIGNMENTS.....	2-1
3-1	UHF SERIAL INTERFACE SPECIFICATION .....	3-1

## GENERAL INFORMATION

## 1.1 SCOPE OF MANUAL

This service manual contains alignment and service information for Dataradio COR Ltd.'s DM-3473 Synthesized UHF Data Module.

## 1.2 EQUIPMENT DESCRIPTION

## 1.2.1 GENERAL

The Dataradio DM-3473 is a synthesized data module transceiver (transmitter and receiver) which operates in the 403-480 MHz UHF frequency range. Transmitter power output is 2 watts nominal, and operation is simplex or half duplex. The 3473 has a frequency stability of  $\pm 1.5$  PPM. The 3473 OEM Data Module supplies the RF transceiver. It must be interfaced to a customer supplied logic board for synthesizer loading and all data conditioning. The number of channels that can be selected with the DM-3473 model is determined by customer supplied synthesizer loading circuitry.

Versions of the 3473 covered in this manual are indicated in Section 1.4.

## 1.2.2 DM-3473 SYNTHESIZER PROGRAMMING

The DM-3473 requires customer supplied circuitry to load the synthesizer with channel information. The protocol that this circuitry must follow is described in Section 3.

## 1.3 TRANSCEIVER IDENTIFICATION

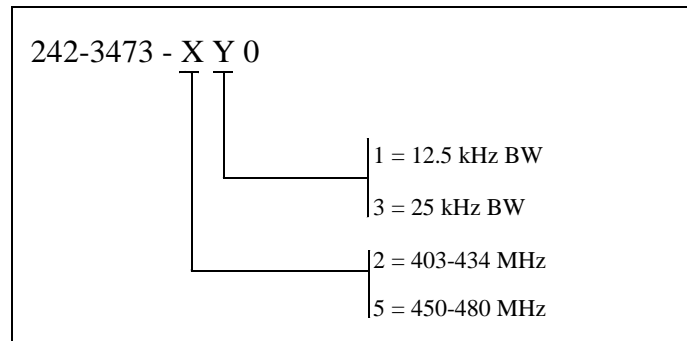
The transceiver identification number is printed on a label that is affixed to the PC board. The following information is contained in that number:

Model	Revision Letter		Manufacture Date		Plant	Warranty Number
3473	2	A	1	4 3	A	12345
Range <input type="checkbox"/>		Week No. <input type="checkbox"/>		Year <input type="checkbox"/>		
Eighth Digit of PN						

## GENERAL INFORMATION

### 1.4 PART NUMBER BREAKDOWN

The following is a breakdown of the part number used to identify this transceiver:



For sales information in the United States phone 1-800-992-7774. For international sales, phone 1-612-882-5529 or 1-305-829-4030.

### 1.5 TECHNICAL SUPPORT

The Technical Service Department at Dataradio COR Ltd. provides customer assistance on technical problems and serve as an interface with factory repair facilities. They can be reached by mail, phone, and E-mail at:

Dataradio COR Ltd.  
Technical Service Department  
299 Johnson Avenue, P.O. Box 1733  
Waseca, MN 56093-0833

Phone: 800-992-7774  
Fax: 507-835-6501

E-mail address: [support@dataradio-cor.com](mailto:support@dataradio-cor.com)

Technical Service hours: Monday through Friday 7:30 A.M. to 4:30 P.M. Central Time

### 1.6 PRODUCT WARRANTY

The warranty statement for the DM-3473 is available by contacting your sales representative.

### 1.7 REPLACEMENT PARTS

Replacement parts are available through Technical Service. Contact the Technical Service Department at 1-800-992-7774, extension 6290. Section 7 contains a parts list for this transceiver.

### 1.8 IF A PROBLEM ARISES...

#### 1.8.1 FACTORY REPAIR

Dataradio products are designed for long life and failure-free operation. If a problem arises, factory service is available. Contact the Technical Service Department before returning equipment. A service representative may suggest a solution eliminating the need to return equipment.

A Return Material Authorization (RMA) is required when returning equipment to Dataradio for repair. Contact the Technical Service Department at 800-992-7774, extension 6290 to request an RMA number. Be prepared to give the equipment model and serial number, your account number (if known), and billing and shipping addresses.

Include the RMA number, a complete description of the problem, and the name and phone number of a contact person with the returned units. This information is important. The technician may have questions that need to be answered to identify the problem and repair the equipment. The RMA number helps locate your equipment in the repair lab if there is a need to contact Dataradio concerning the equipment. Units sent in for repair will be returned to the customer re-tuned to the current Dataradio Test and Tune Procedure and will conform to all specifications noted in this section

Customers are responsible for shipping charges (to Dataradio) for returned units in warranty. Units in warranty are repaired free of charge unless there is evidence of abuse or damage beyond the terms of the warranty. Dataradio covers return shipping costs for equipment repaired while under warranty.

Units out of warranty are subject to repair service charges. Customers are responsible for shipping charges (to and from Dataradio) on units out of warranty. Return shipping instructions are the responsibility of the customer.



# GENERAL INFORMATION

## DM-3473 SYNTHESIZED UHF DATA MODULE GENERAL SPECIFICATIONS

*The following general specifications are subject to change without notice.*

### GENERAL

Frequency Range	403-434 MHz, 450-480 MHz
Frequency Control	Synthesized
Channel Spacing	12.5/25 kHz
Channel Steps	6.25 kHz or 10 kHz
Mode of Operation	Simplex or Half Duplex
Operating Voltage	+7.2V DC Nominal 6-9 VDC Max. Range
RF Input/Output	MCX Jack Female
Power and Data Interface	18 position dual row socket, 2mm (.0787 in.) pitch
Operating Temperature	-30° to +60° C (-22° to +140° F)
Max Dimensions	2.84" L (7.22 cm), 1.76" (4.47 cm) W, 0.45" (1.14 cm) H
Weight	≤ 40 grams
FCC Compliance	DM-3473 customer must apply
Rx to Tx, Tx to Rx Turnaround Time	≤ 10ms from Rx Enable (pin 7) / Tx Enable (pin 6) to Fc ± 500 Hz (See Section 3 for Tx to Rx, Rx to Tx protocol)

### RECEIVER

Bandwidth	30 MHz 450-480 MHz, 31 MHz 403-434 MHz without retuning
Frequency Stability	±1.5 PPM (-30° to +60° C)
Sensitivity - 12 dB SINAD	-116 dBm (Psophometrically weighted) 60% Max deviation, 1 kHz tone
RF Input Impedance	50 ohms
Spurious and Image Rejection	≥60 dB
Selectivity	≥50 dB (12.5 kHz), 60 dB (25 kHz)
Half IF	≥ 60 dB ≥ 55 dB 403-408 MHz and 450-455 MHz
Intermodulation	≥60 dB
Conducted Spurious	≤-57 dBm
Receive Current Drain	≤ 60 mA
Receive Lock Time	< 7 ms from last synth enable pulse to lock detect
Rx Data/Audio	
Distortion	≤ 3% (psophometrically weighted)
Bias	2.5 VDC ± 0.5 VDC
Output Level	150 mV rms ± 50 mVrms 1 kHz tone with 60% max. deviation
Response	+1/-3 dB @2.5 kHz, +1/-3 dB @5 kHz
Load Impedance	≥10k ohms
Conducted Spurious Emissions	≤ -57 dBm

## GENERAL INFORMATION

### TRANSMITTER

Bandwidth	30 MHz 450-480 MHz, 31 MHz 403-434 without retuning
Frequency Stability	$\pm 1.5$ PPM ( $-30\times$ to $+60\times$ C)
TCXO Coupling	DC 2.5 VDC $\pm .05$ VDC (customer supplied on Pin 10 in both Rx & Tx)
RF Power Output	2W @ 7.2 VDC nominal
RF Output Impedance	50 ohms
Duty Cycle	50%, 5 sec. max transmit
Transmitter Lock Time	$\leq 7$ ms from last synth enable pulse to lock detect
Tx Attach Time	$\leq 3$ ms from Tx Enable (pin 6) to 50% power out
Spurious and Harmonic FM	$\leq -20$ dBm
Audio Response	$+1/-3$ dB from DC to 5 kHz (reference to 1 kHz)
Modulation Distortion	$< 3\%$ (psophometrically weighted)
Data Input Impedance	$\geq 100$ k ohm
Modulation Response Flatness	$\pm 3$ dB from DC to 5 kHz (reference to 1 kHz -Programmable to $\pm 1$ dB via J201, pin 9) across full RF band
Current Drain	1500 mA maximum, 1200 mA nominal @ 2 watts output (Refer to Section 2 for pin by pin current drain)
Transmitter Stability	No failure or instability at up to 10:1 VSWR
External Modulation Adjust	
Source Impedance	$\leq 1$ k ohms (pin 9)
External Modulation Adjust	0.5 Vdc - 5.0 Vdc to obtain $\pm 1.0$ dB modulation flatness across RF band (pin 9)
Modulation Capability	200 mVrms (Band 2) to produce 1.5 kHz deviation 180 mVrms (Band 5) to produce 1.5 kHz deviation

# INSTALLATION

## 2.1 PRE-INSTALLATION CHECKS

Field alignment should not be required before the 3473 is installed. However, it is a good practice to check the performance to ensure that no damage occurred during shipment. Performance tests are located in Section 6.

## 2.2 INTERFACING WITH DATA EQUIPMENT

The DM-3473 User Interface (J201) is a Samtec 18-pin dual-row connector socket with a 2 mm pitch, vertical mount. It is made of a black liquid crystal polymer. The contact material is phosphor bronze. The current capacity per pin is 1 Amp maximum at 80° C. The insertion depth is .084 to .170 inches with .015 inch wipe. For pin orientation, see Section 8.

### 2.2.1 CONNECTOR PIN ASSIGNMENTS

**Table 2-1 PIN ASSIGNMENTS**

PIN	ASSIGNMENT	DESCRIPTION
1	Ground	
2	Ground	
3	7.2 VDC Switched Battery	
4	7.2 VDC Switched Battery	Pins 3 & 4 are identical and must be doubled up on customer supplied interface for supply current restrictions. Voltage supply is 6-9 VDC with 7.2VDC nominal for 2 Watt output power. Maximum current is 1.5 Amps or 750 mA per pin.
5	7.2 VDC Regulated	This pin must always be regulated between 6-9 VDC for onboard regulation. If 2 Watts is the desired output power, then pins 3,4, & 5 can be tied together on a customer supplied interface board and regulated to 7.2 VDC. Maximum current is 750 mA.
6	Tx_Enable	Transmit enable pin. This is a logic level to enable the transmitter and is logic high (4.5 - 13VDC)
7	Rx_Enable	Receive enable pin. This is a logic level to enable the receiver and is logic high (4.5 - 13VDC). This pin also performs the VCO Tx to Rx course frequency shift. <i>continued</i>

## INSTALLATION

**Table 2-1 PIN ASSIGNMENTS**

PIN	ASSIGNMENT	DESCRIPTION
8	Sleep Mode	This pin puts the transceiver into a sleep mode drawing <1mA. This pin is a logic level to enable/disable the transceiver. Enable high is 2.0V to pin 5 voltage. Disable low or sleep mode is <.60 VDC. Note: The synthesizer channel load information must be re-loaded when coming out of sleep mode.
9	Tx_MOD_ADJ	This pin can be used to adjust the modulation balance of the transmitter across the RF band (403-434 MHz or 450-480 MHz). A voltage is applied to the pin from 0-5VDC at the desired RF frequency of operation and is tied directly to a VCO varactor to tune the modulation flatness. Internally, the transceiver is tuned flat for the center of the RF band (418.5 MHz and 465 MHz) with this pin open. <i>The use of an op-amp is recommended to interface to this pin or a source with the resistance <math>\leq 1\text{ k ohms}</math>.</i>
10	Tx_MOD_IN	Transmit modulation input. This pin must have a DC coupled, regulated $2.5 \pm 0.05$ VDC supply to bias the TCXO in transmit and receive and also be temperature compensated. This pin is tied directly to the VCO for modulating the radio in transmit mode. <i>See Section 1: General Specifications for modulation capability.</i>
11	Lock Detect	The synthesizer lock detect pin indication: $\geq 4\text{VDC}$ = lock $\leq 1.5\text{ VDC}$ = unlock
12	Rx_DATA_OUT	This output is the DC coupled wideband output of the receiver baseband detected data. The nominal output is 2.5VDC bias with 150mVrms audio out with 60% rated deviation and a 1 kHz tone. <i>NOTE: The nature of the receiver will output inverted audio.</i>
13	RSSI Output	Receiver Signal Strength Indicator. The receiver's detector outputs a DC voltage logarithmically related to the strength of the received signal. With -60 to -120 dBm at the RF input the voltage will be $V(\text{high}) - V(\text{low}) \geq 0.7$ VDC and $V(\text{low}) \leq 1.1$ Vdc. This output can be used to implement a data detect circuit (DCD) on the customer supplied interface board.
14	SYNTH_ENABLE	This is part of the 3 pin serial interface to load the synthesizer. See Section 3 to implement pins 14, 15, & 16.
15	SYN_DATA	3 pin serial interface which carries the raw data of A, B, and D Words to the synthesizer following the Phillips SA7025 loading protocol. (The C-Word is not necessary on the DM-3473.) See Section 3.
16	SYN_CLOCK	3 pin serial interface pin which requires the synthesizer clock. The synthesizer maximum clock frequency is 1 MHz. See Section 3.
17	NO CONNECT	
18	NO CONNECT	

## PROGRAMMING

## 3.1 INTRODUCTION

The information in Section 3 describes synthesizer programming protocol of the Philips SA7025A IC used on the DM-3473. This information can be used as a basis for designing the synthesizer programming hardware and software.

## 3.2 DM-3473 SERIAL INTERFACE SPECIFICATION

## 3.2.1 SUMMARY

Table 3-1 contains a summary of the serial interface specifications for the DM-3473. These parameters are used to calculate the synthesizer load data. See Section 3.5 for example calculations.

Table 3-1 UHF Serial Interface Specification

Specification	Requirement
Receive Bandwidth	403-434 & 450-480 MHz
Transmit Bandwidth	403-434 & 450-480 MHz
First IF	86.85 MHz
Second IF	450.0 kHz
First LO Injection	489.85 to 520.85 & 536.85 to 566.85 MHz (high side injection)
Second LO Injection	86.40 MHz (Low side injection)
TCXO Frequency	14.4 MHz
Frequency Resolution	6.25 or 10 kHz (FMOD dependent)
Loop Comparison Frequency	50 kHz (optimum)
Synthesizer IC	Philips SA7025A

## 3.3 FRACTIONAL-N SYNTHESIZER

## 3.3.1 INTRODUCTION

The DM-3473 UHF transceiver uses a high performance Fractional-N Synthesizer and Voltage Controlled Oscillator (VCO). The Fractional-N Synthesizer offers high frequency resolution, fast lock times, and improved noise performance over conventional synthesis techniques. A conventional synthesizer's detector comparison frequency must be equal to the channel spacing because the main divider changes in integer steps. The channel spacing (resolution) of a Fractional-N Synthesizer is a fraction of the comparison (reference) frequency. The SA7025 Fractional-N Synthesizer's comparison frequency is increased to 5 or 8 times the channel step frequency resolution. The higher comparison frequency's loop division is reduced which improves phase noise. Improved lock times are possible because the loop bandwidth can be wider.

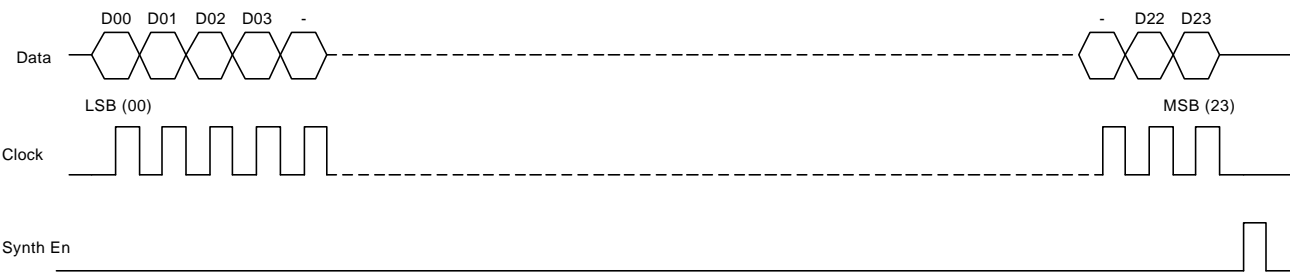
PROGRAMMING

3.3.2 SYNTHESIZER DATA PROTOCOL

Programming the SA-7025 synthesizer IC is accomplished via the 3-wire bus (Data, Clock, and Synthesizer Enable) located on the 18 pin radio interface connector. Three words are required to load the synthesizer (in their order-D, B, and A0 Words). The D and B words contain four address bits each, the A0 Word has a one bit address. Synthesizer frequency acquisition is initiated when the final word (A0 Word) is loaded by the Synth Enable. *Note: The C Word is not required in the DM-3473 load sequence.*

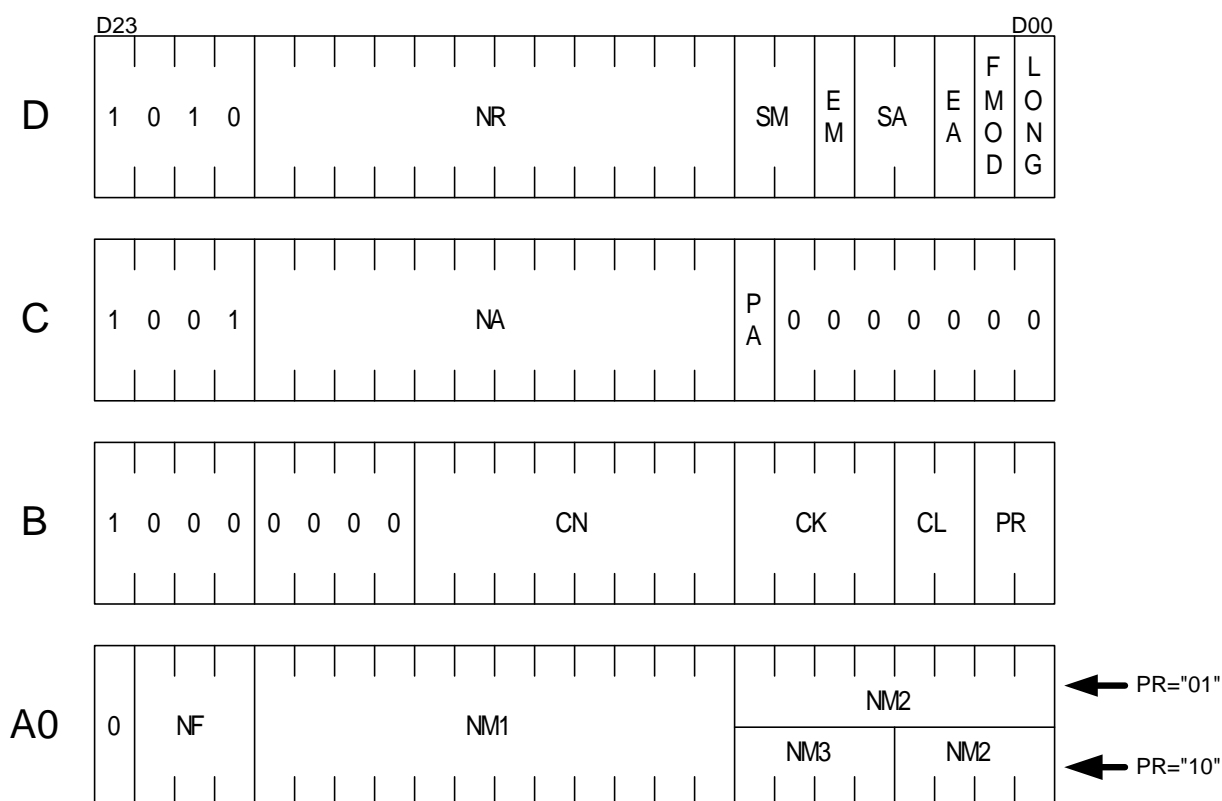
3.3.3 SYNTHESIZER DATA

A modulus 3 is recommended to send the D, B, and A0 words for each synthesizer load. Figure 3-1 shows the Synthesizer Serial Data Stream. Bit definitions are shown in Figure 3-2 (the figure is 24 Bits long).



- Clock (max) = 1MHz
- Synth Enable (min) = 250 nS (for D and B and A0 Words)
- D00 - D23 = D, B, and A0 Words (Least Significant Bit of Least Significant Byte first)

Figure 3-1 Synthesizer Serial Data Stream



**Figure 3-1 Bit Definitions**

## 3.4 SYNTHESIZER BIT DEFINITIONS

### 3.4.1 INTRODUCTION

Sections 3.4.2, 3.4.3, 3.4.4, and 3.4.5 are the decimal values of the recommended synthesizer load implementation of the DM-3473 for the D, C, B, and A0 Words.

### 3.4.2 D WORD

NR	= 288 (0 X 120)(14.40 / 0.0500) (for 6.25 kHz channels) (50.0 kHz reference)
NR	= 288 (0 x 120) (14.40 / 0.0500) (for 10.0 kHz channels) (50.0 kHz reference)
SM	= 00 Reference select for main phase detector
EM	= 1 Main divider enable flag (enabled)
SA	= 00 Reference select for aux. phase detector
EA	= 0 Aux. divider enable flag (disabled)
FMOD	= 0 (modulo 5 for 10.0 kHz channels)
FMOD	= 1 (modulo 8 for 6.25 kHz channels)
LONG	= 0 (send all 3 words with A0)

# PROGRAMMING

## 3.4.3 C WORD

The DM-3473 transceiver derives its' Second Local Oscillator directly from the TCXO. The C Word is not required in the load sequence. Other Dataradio OEM products do use the C Word. For code implementations, the C Word may be sent with the address 1001 and all other bits set to 0 on the DM-3473 for compatibility with other Dataradio products.

## 3.4.4 B WORD

CN	= See Note	Charge Number (frequency dependent)
CK	= 0000	Binary acceleration factor for integral charge pump
CL	= 00	Binary acceleration factor for proportional charge pump
PR	= 10	Prescaler (Modulus 3)

Note: The value of CN should be interpolated for frequencies between the band edges (shown below) from low frequency to high frequency. The recommended range of CN provides the necessary spurious rejection required to meet the adjacent channel rejection specifications across the band.

### 5Y0

Rx:	450 MHz - 108	465 MHz - 114	480 MHz - 115
Tx:	450 MHz - 92	465 MHz - 97	480 MHz - 97

### 2Y0

Rx:	403 MHz - 82	418.5 MHz - 85	434 MHz - 86
Tx:	403 MHz - 67	418.5 MHz - 72	434 MHz - 73

## 3.4.5 A0 WORD: (Refer to Section 3.7 for the C+ Code implementation of the A0 Word.)

NF	= ____	Fractional increment for modulus (3 bits, frequency, and FMOD dependent)
NM1	= ____	Number of main divide cycles when prescaler modulus = 64 (12 bits)
NM2	= ____	Number of main divide cycles when prescaler modulus = 65 (4 bits, PR = 10)
NM3	= ____	Number of main divide cycles when modulus = 72 (4 bits, PR = 10)

## 3.5 Synthesizer Load Parameter Example

This section works through two examples to calculate the synthesizer load parameters for the DM-3473. The table in section 3.2 has the radio specific information to follow the Philips SA7025A synthesizer programming protocol.



## Example #1

### Transmit at 470.79375 MHz

#### D Word Calculation

Address = 0xA This is the address for the synthesizer to recognize the D-Word. (4 bits)

NR = TCXO Freq. / Reference Freq. = 14.4 MHz / 0.05 MHz = 288 = 0x120

For all applications of the DM-3473 this should be set to 288 (12 bits)

SM = b'00 (For all DM-3473 applications this number is zero) (2 bits)

EM = b'1 (This is the main synthesizer enable flag. It is always one) (1 bit)

SA = b'00 (For all DM-3473 applications this number is zero) (2 bits)

EA = b'0 (This is the auxiliary synthesizer enable flag. The auxiliary loop is not used in the DM-3473 and is always zero) (1 bit)

FMOD = b'1 FMOD sets the resolution of the synthesizer. When FMOD is set to zero, the reference frequency (50 kHz) is divided by 5 giving 10 kHz steps. When set to one, the reference is divided by 8 giving 6.25 kHz steps. For this example we will use FMOD = 1 or divide by 8. To determine which FMOD to use, simply divide your frequency of operation by 10.0 kHz and 6.25 kHz. Whichever result is an integer, use that FMOD. If both are an integer, you may choose which to use. (1 bit)

LONG = b'0 It is recommended to always set this to zero and send all the serial 'words' to the synthesizer whenever changing channels. Setting this to zero requires the A word to be the short version or 24 bits. It has been our experience with this synthesizer IC that if only the A1 word is sent to change from receive to transmit that after several thousand times the B, C, and D words can be corrupted in the synthesizer IC. On power down, all memory is lost. (1 bit)

For our example (in fact for all implementations of the DM-3473 load except possibly FMOD) the D word should look like this.

D-Word	0xA1	0x20	0x22
	1010 0001	0010 0000	0010 0010

# PROGRAMMING

## C Word Calculation

The C word contains the address bits as well as the NA variable and PA variable which are only used to set the auxiliary loop of the synthesizer. This loop is not used in the DM-3473 even though the receiver is a dual conversion process requiring two local oscillators. The second local oscillator is derived from the sixth harmonic of the VCTCXO reference frequency of 14.4 MHz and does not need to be phase locked. Thus 14.4 times 6 equals 86.4 MHz. See section 3.2 for radio parameters.

The C word can be handled in one of two ways. The first way would be to not send it at all. In this configuration only the D, B, and A words would be sent, and this works fine. The other way is to send the word but set both of the variables (NA and PA) to all zeros. One possible advantage to sending the C word would be that some other Dataradio-COR products do use the C word. The code would be somewhat backward compatible with a dummy C word sent to the DM-3473.

For our example, and all other implementations of the DM-3473, the C word would look like this. Don't forget to send the C word address of 0x9 so the synthesizer recognizes what it is receiving

C-Word	0x90	0x00	0x00
	1001 0000	0000 0000	0000 0000

## B Word Calculation

Address = 0x8      This is the address for the synthesizer to recognize the B-Word. (4 bits)

The first four bits after the address are set to zero. (4 bits)

CN = 0x61      \* See table in section 3.4.4 (8 bits)

The CN or Charge Number sets the charge current in the main phase detector of the synthesizer and is very important for proper noise free operation of the radio. The CN value is dependant on the frequency of operation of the unit and is set between 0 and 255 decimal. The best way to implement this is to do a linear interpolation of the values in the table of section 3.4.4 across the band. Each band is split into two smaller bands approximately 15 MHz wide for both receive and transmit.

For our example the value is easily interpolated. From 465 MHz to 480 MHz the CN is 97 and is a straight line with no slope. See the second example to calculate CN between two values with a non zero slope.

CK = b'0000      CK is the binary acceleration factor of the integral speed up charge pump, which is not used in the DM-3473. (4 bits)

CL = b'00      CL is the binary acceleration factor of the proportional speed up charge pump, which is not used on the DM-3473. (2 bits)

**PR = b'10** PR sets the prescaler modulus. There are two ways to set the prescaler modulus, either dual or triple. For all examples given in this manual, we use triple modulus or PR = 10 binary. What PR is set to determines how the A word will be calculated. If set to dual modulus, the main dividers are 64/65, and use NM1 and NM2 for calculating the A word. If set to triple modulus, the main dividers are 64/65/72, and use NM1, NM2, and NM3 for calculating the A word. Depending on which is used, different equations apply to calculate the main dividers. (2 bits)

<b>B-Word</b>	0x80	0x61	0x02
	1000 0000	0110 0001	0000 0010

## A0 Word Calculation

**Address = b'1** This is the address for the synthesizer to recognize the A-Word. (1 bit)

**NF = 0x7** NF is the fractional increment of the synthesizer and is calculated as follows. (3 bits)

To calculate NF, the total N must be calculated first.

$$N = \text{INT} (\text{Frequency} / \text{Reference Frequency})$$

$$= \text{INT} (470,793,750 / 50,000) = 9415$$

$$NF = (\text{Frequency} \% \text{Reference Frequency}) / \text{Frequency Resolution}$$

$$\text{Frequency Resolution} = \text{Reference Frequency} / \text{FMOD}$$

$$= 50,000 / 8 = 6,250 \quad (\text{Table 3-1})$$

$$NF = (470,793,750 \% 50,000) / 6,250$$

$$NF = 43,750 / 6,250 = 0x7$$

Note: % is the operator modulus. Modulus is the fractional remainder of the division of two numbers. In our example  $470,793,750 / 50,000 = 9415.875$  To get the modulus, take the remainder  $(0.875 * 50,000 = 43,750)$

**NM3 = 0x7** This is the main divider for prescaler modulus 72. (4 bits)

NM3 is calculated as follows.

$$NM3 = (\text{INT} ((N \% 64) / 8)) - 1 \text{ AND } 0x7$$

$$NM3 = (\text{INT} ((9415 \% 64) / 8)) - 1 \text{ AND } 0x7$$

## PROGRAMMING

$$NM3 = (\text{INT} ( 7 / 8) - 1) \text{ AND } 0x7$$

$$NM3 = (0 - 1) \text{ AND } 0x7$$

$$NM3 = -1 \text{ AND } 0x7 = 0x7$$

NM2 = 0x7 This is the main divider for prescaler modulus 65. (4 bits)

NM2 is calculated as follows.

$$NM2 = N \% 8$$

$$NM2 = 9415 \% 8 = 0x7$$

NM1 = 0x081 This is the main divider for prescaler modulus 64. (12 bits)

NM1 is calculated as follows.

$$\text{IF } (NM3 = 0x7) \text{ THEN } NM1 = (\text{INT} (N / 64) - 4 - NM2 - NM3)$$

$$\text{ELSE } NM1 = (\text{INT} (N / 64) - 3 - NM2 - NM3)$$

Therefore since NM3 = 0x7:

$$NM1 = (\text{INT} (9415 / 64) - 4 - 7 - 7)$$

$$NM1 = 147 - 4 - 7 - 7$$

$$NM1 = 129 = 0x081$$

A0-Word	0x70	0x81	0x77
	0111 0000	1000 0001	0111 0111

## Example # 2

### Receive at 411.1375 MHz

In transmit mode, the synthesizer is programmed to the frequency of operation. In receive mode, the synthesizer must be programmed with the first intermediate frequency (IF) shift. To receive at 411.1375 MHz, the synthesizer actually is programmed using the following equation:

$$\text{Synth Program} = \text{Rx Freq.} + \text{IF Freq.}$$

$$\text{Synth Program} = 411,137,5000 \text{ Hz} + 86,850,000 \text{ Hz} = 497,987,500 \text{ Hz}$$

For the DM-3473, the first LO is high side injected so the frequency of operation of the synthesizer is 86.85 MHz above the receive frequency. The above equation would subtract 86.85 MHz if the first LO was low side injected. See Table 3-1 for the DM-3473 radio parameters.

Below, all of the synthesizer parameters are calculated and then given in the form of the D, C, B, and A0 words as they should be loaded into the synthesizer. The CN value works through the linear interpolation below as well.

#### D Word

$$\text{NR} = 14,4000 / 50,000 = 288 = 0\text{x}120$$

$$\text{SM} = \text{b}'00$$

$$\text{EM} = \text{b}'1$$

$$\text{SA} = \text{b}'00$$

$$\text{EA} = \text{b}'0$$

$$\text{FMOD} = \text{b}'1 \text{ (Modulo 8) Remember to use } 411,137,500 + 86,850,000 \text{ to calculate FMOD. At this frequency, only modulo 8 works.}$$

$$\text{LONG} = \text{b}'0$$

#### C Word

Address and all zeros.

# PROGRAMMING

## B Word

$$CN = 0x54$$

CN was calculated as follows. From the table in section 3.4.4, in receive between 403 MHz and 418.5 MHz, the CN should be interpolated between 82 and 85 for a receive frequency of 411,137,500 Hz.

It is important to note that the CN value should be rounded to the nearest integer for optimum operation of the DM-3473. The following equation was used.

$$CN = \frac{(CN1 - CN0) * (Fop - F0) + ((F1 - F0) >> 1)}{F1 - F0} + CN0$$

Where:

$$CN1 = 85 \quad CN0 = 82 \quad Fop = 411,137,500$$

$$F0 = 403,000,000 \quad F1 = 418,500,000$$

The term  $(F1 - F0) >> 1$  means the binary equivalent of  $(F1 - F0)/2$ . This allows the user to round to the nearest integer without doing a floating point operation in the code. This equation can be used in conjunction with the CN values given in section 3.4.4 for the appropriate range and transmit or receive frequency.

$$CK = b'0000$$

$$CL = b'00$$

$$PR = b'10 \text{ (Modulus 3)}$$

## A0 Word

$$NF = 0x6$$

$$N = \text{INT} (497,987,500 / 50,000) = 9959$$

\* Remember 411,137,500 + 86,850,000

$$NF = (497,987,500 \% 50,000) / 6,250 = 6 = 0x6$$

$$NM3 = 0x3$$

$$NM3 = (\text{INT} ((9959 \% 64) / 8) - 1) \text{ AND } 0x7 = 3 = 0x3$$

$$NM2 = 0x7$$

$$NM2 = 9959 \% 8 = 7 = 0x7$$

NM1 = 0x08E

NM3 does not = 0x7 therefore

$NM1 = (INT(9959 / 64) - 3 - 7 - 3) = 142$

NM1 = 142 = 0x08E

The synthesizer load parameters should look like this to program a range 2 403-434 MHz DM-3473 to 411.1375 MHz receive mode.

D - Word	0xA1	0x20	0x22
	1010 0001	0010 0000	0010 0010
C - Word	0x90	0x00	0x00
	1001 0000	0000 0000	0000 0000
B - Word	0x80	0x54	0x02
	1000 0000	0101 0100	0000 0010
A0 - Word	0x60	0x8E	0x37
	0110 0000	1000 1110	0011 0111

Remember that the bits are loaded with the first bit of the address as the most significant bit. The bits would be loaded from right to left in the chart above, and the A0 word is always the last word sent.

## 3.6 RECOMMENDED SYNTHESIZER LOAD SEQUENCE

Sections 3.6.1 and 3.6.2 contain the recommended Receive to Transmit and Transmit to Receive synthesizer load sequence for the DM-3473. The 3473 was designed to follow this protocol to achieve fast lock and turnaround times. This protocol is the standard for DM-3473 testing for all specifications regarding lock, turnaround, and switching times and will insure the unit complies with FCC guidelines Part 90.214 for Transient Frequency Behavior radiated emissions.

### 3.6.1 RECEIVE TO TRANSMIT SEQUENCE

1. Load the Synthesizer Transmit Frequency ('D', 'B', and 'A0' Words).
2. The Rx Enable (Pin-7 of the Radio Interface Connector) is changed from a logic high to a logic low simultaneously as the A0 Word is latched.

## PROGRAMMING

3. Before enabling the transmitter, the Lock Detect (Pin 11) should be monitored and in a lock state (logic high) before and throughout the duration of the transmission. After the lock detect has been high for 1 ms, apply a logic high to the Tx\_Enable (Pin 6). *FCC regulations requires user monitoring of the lock detect* state. If an unlock condition occurs, the transmitter must be disabled.
4. A “Ramp-Up” circuit has been employed on the transceiver to minimize adjacent channel interference caused by the spectral spreading that occurs when a transmitter is suddenly switched on or off. The ramp-up time is  $\leq 2$  ms after Tx\_Enable is applied. The total turn-around time from receive to transmit is guaranteed to be  $\leq 10$  ms from Rx\_Enable low to  $F_c \pm 500$  Hz of the transmit frequency and  $\geq 90\%$  power out by implementing the load sequence described in Steps 1-3.

### 3.6.2 TRANSMIT TO RECEIVE SEQUENCE

1. A logic low is applied to the Tx Enable (Pin-6 of the Radio Interface Connector).
2. Allow 2 ms for transmitter power to “ramp-down” after the Tx Enable is brought low to minimize adjacent channel interference caused by spectral spreading.
3. The receive load parameters D and B Words can be clocked and latched as well as the A0 Word clocked into the synthesizer during the 2 ms “ramp down”. At 2 ms, simultaneously latch the A0 Word and apply a logic high to the Rx\_Enable (Pin 7).
4. After the A0-Word is latched in and Rx\_Enable sent high, the synthesizer will initiate frequency acquisition and achieve a locked state (Logic high) on Pin-11. The total turn-around time from transmit to receive is guaranteed to be  $\leq 10$  ms from Tx\_Enable low to  $F_c \pm 500$  Hz of the receive frequency by implementing the load sequence described in Steps 1-3.



## 3.7 A0 WORD ALGORITHM

```

#define REF_FREQ          50000      /* for 6.25 kHz Channels */
#define REF_FREQ          50000      /* for 10.0 kHz Channels */

#define CHAN_SPACE_FREQ   6250       /* for 6.25 kHz Channels */
#define CHAN_SPACE_FREQ   10000      /* for 10.0 kHz Channels */

void A_Word_Calculation(unsigned long freq)
{
    unsigned char    nf, buf[3];
    unsigned int     n, nm1, nm2, nm3;

    n = (unsigned int)(freq / REF_FREQ);
    nf = (unsigned char)((freq % REF_FREQ) / CHAN_SPACE_FREQ);

    /*
    **      Use Modulus 3 Calculations
    */
    nm3 = (((n % 64) / 8) - 1) & 0x0007;
    nm2 = n % 8;
    nm1 = ((n / 64) - 3 - nm2 - nm3) & 0x0FFF;
    if (nm3 == 0x0007)
        nm1--;

    buf[0] = (unsigned char)((nf & 0x07) << 4);
    buf[0] |= (unsigned char)(nm1 >> 8);
    buf[1] = (unsigned char)(nm1);
    buf[2] = (unsigned char)(nm2);
    buf[2] |= (unsigned char)(nm3 << 4);
}

```

**CIRCUIT DESCRIPTION****4.1 GENERAL****4.1.1 INTRODUCTION**

The DM-3473 consists of a low dropout regulator power supply, frequency synthesizer and VCO (voltage controlled oscillator), 2 watt RF power amplifier, and dual down conversion FM receiver. A block diagram of the transceiver is located in Figure 4-1 and shows the four major sections of the unit.

The VCO is enclosed by a metal shield and soldered directly to the printed circuit board (PCB). The VCO unit is not field serviceable. The transmitter is also covered by a metal shield to prevent radiation of RF power causing interference. The 3473 comes standard with a reference oscillator stability of + 1.5 PPM over the entire operating temperature range.

**4.2 POWER SUPPLY CIRCUIT DESCRIPTION**

Main DC power is delivered to the transceiver on pin 5 of the user interface connector (J201). This pin requires a regulated power supply voltage between 6 and 9 VDC. The voltage on this pin powers the on board low drop out regulator U130. The regulator provides constant 5.5 VDC to all of the relevant sections of the transceiver such as the VCO/Synthesizer, Receiver, and Regulator sections of the transmitter. Pins 1 and 2 provide the ground connection of the transceiver.

Pins 3 and 4 of J201 are the main power supply to the RF power amplifier. This voltage is set between 6 and 9 VDC with 7.2 VDC being the nominal voltage to guarantee 2 watts  $\pm$  0.4 watts of RF power at the antenna connector. All three pins (3,4,and 5) can be tied together on a customer interface board if the maximum voltage limits are always between 6-9 VDC.

The transmit and receive enable pins (pins 6 and 7) of J201 are a logic voltage input to turn on the transmitter or receiver. The necessary voltage is between 4.5 and 13 VDC for the enable mode. Refer to the programming section 3 for the implementation of the transmit and receive enable pins.

The DM-3473 is equipped with a sleep mode pin for implementing current saving features by the customer when a transceiver requires a standby mode. Pin 8 requires a logic level  $>2.0$  VDC to enable the transceiver, this voltage must always be high when the transceiver is in operation. Pin 8 can be grounded to put the radio to sleep. The transceiver will draw less than one milliampere in sleep mode.

CIRCUIT DESCRIPTION

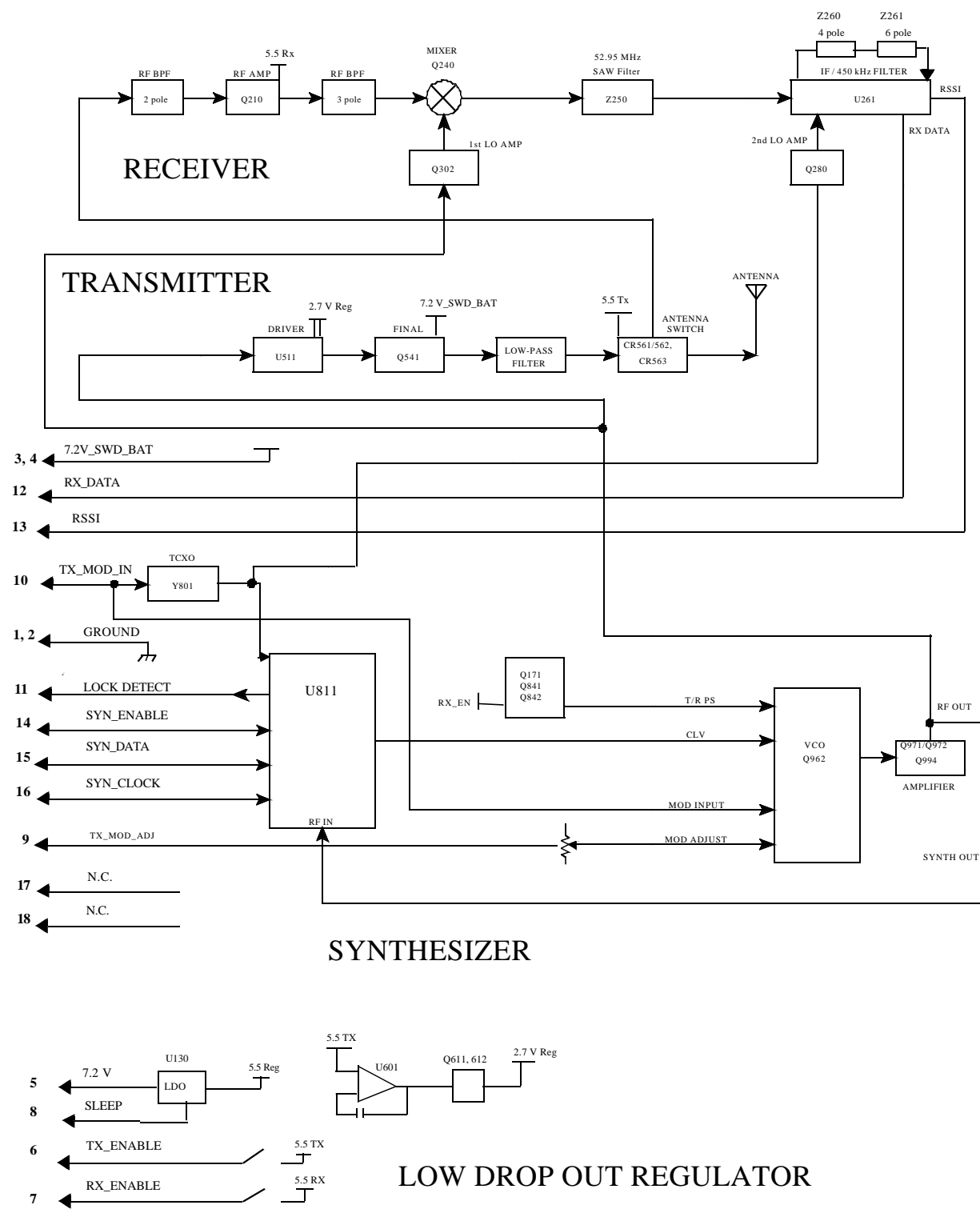
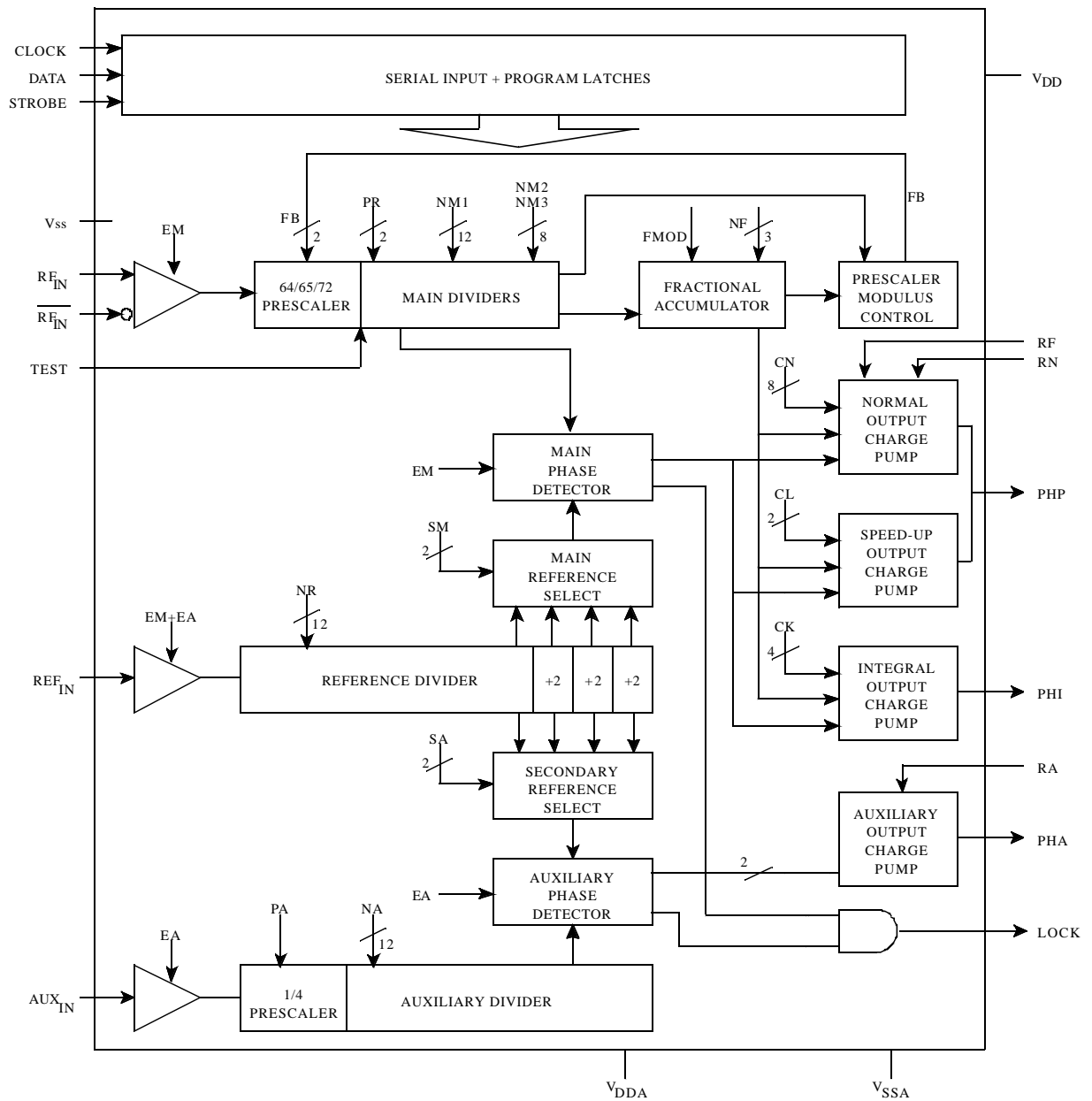


Figure 4-1 DATA TRANSCEIVER BLOCK DIAGRAM

# CIRCUIT DESCRIPTION



**Figure 4-2 U811 SYNTHESIZER BLOCK DIAGRAM**

## CIRCUIT DESCRIPTION

### 4.3 SYNTHESIZER/VCO/TX MODULATION

The VCO is an oscillator which can be controlled by an input voltage to oscillate at a desired frequency. The VCO in the 3473 serves either the receiver or the transmitter dependent on the desired operation. The frequency of the VCO for receive mode is 86.85 MHz above the desired receive frequency. For the transmitter the VCO produces the signal corresponding to the desired transmit frequency.

The DC voltage controlling the oscillator frequency is generated by synthesizer IC U811. The VCO control voltage can be measured at test point TP831 on the PCB. When the VCO is locked ( $>3.5$  Vdc on pin 11 of J201) TP831 will measure between 0.5 and 5.00 VDC, dependent on the frequency of operation. An unlocked condition (indicated on pin 11 of J201) is less than 1.5 VDC. The synthesizer determines the lock state of the radio by comparing the scaled VCO frequency to the scaled reference oscillator TCXO of 14.4 MHz.

The VCO is a Colpitts oscillator formed by Q962 along with several capacitors, varactor diodes, and a ceramic resonator. The DC bias to the VCO is provided by transistor Q901 and forms a capacitance multiplier which delivers filtered, noise free supply voltage to the oscillator circuitry. The VCO is followed by gain stages which amplify the signal to approximately 0 dBm and then divide the signal using a splitter and sending it to the receiver or transmitter.

The VCO is capable of oscillating between 403-434 MHz or 450-480 MHz in transmit and 489.85-520.85 MHz or 536.85-566.85 MHz in receive. The course frequency shift in the VCO between receive and transmit is accomplished by shifting in a capacitor to the tank of the oscillator. Pin 7 of J201 (receive enable) performs this function. When transmitting, the receive enable is forced low and a pin diode is turned on by a digital transistor connected to pin 7 which switches capacitance into the oscillator circuit. The reverse happens when returning to receive mode. Refer to section 3 for receive to transmit and transmit to receive load sequences.

There are two parts to the transceiver modulation circuitry. With the placement of the VCO control line voltage low pass filter at approximately 400 Hz, it is necessary to modulate both the VCO and the TCXO. A loop response of 400 Hz is necessary to accomplish the fast lock times of the 3473. If only the VCO were modulated to transmit data, any baseband frequency component below 400 Hz would not be modulated onto the transmit carrier. To accomplish this the transceiver was designed to modulate both the VCO and TCXO, thus creating two parts to the modulation circuit and modulation capability from below 50 Hz up to 5000 Hz.

It is important to note that modulation sensitivity adjustment and modulation deviation limiting are to be supplied in the customer interface equipment, and are required by most regulatory agencies, such as the Federal Communications Commission (FCC) in the United States.

The modulation flatness adjustment (R825) balances the sensitivity of the VCO vs. the TCXO. The radio is set to best modulation flatness in the center of the RF band (418.5 MHz or 465 MHz) when the unit leaves the Dataradio factory. The modulation flatness becomes uneven when nearing the band edges due to changing sensitivity of the TCXO and VCO across a wide range of RF frequencies.

## CIRCUIT DESCRIPTION

If optimal modulation flatness is desired across the whole RF band of 450-480 or 403-434 MHz, the unit is equipped with an external flatness adjust. Pin 9 of J201 allows the implementation of an analog voltage between 0 and 5 VDC to obtain flat modulation. Linear interpolation of this voltage between the RF band edges will insure flat modulation everywhere in the band. If flat modulation is desired only in a single or small range of grouped frequencies, R825 of the 3473 module can be tuned for flat modulation and pin 9 of the user connector left open.

The frequency stability of the VCO in receive and transmit mode is established by the stability of the reference oscillator. The reference oscillator for the 3473 is 14.4 MHz and is designed to be stable between  $\pm 1.5$  PPM over the entire operating temperature range of  $-30^{\circ}$  to  $+60^{\circ}$  C. Pin 10 of the user interface connector is the modulation input to the VCO and TCXO as described above, however this pin also serves another purpose. A precision 2.5 VDC reference is essential for the TCXO to compensate  $\pm 1.5$  ppm for changes in ambient temperature. Pin 10, in addition to modulating the data, requires a DC component of 2.5 VDC  $\pm 0.05$  VDC.

Channels are selected by programming counters in U811. Section 3 of this manual shows how to program the Phillips SA7025A Frequency Synthesizer for the DM-3473. This programming is performed over a 3-wire serial bus formed by pins 14, 15, and 16 of user interface J201. These pins are labeled Synth Enable, Synth Data, and Synth Clock. This programming is supplied by customer hardware and software interface equipment. A block diagram of the synthesizer/VCO is shown in Figure 4-1 along with a block diagram of the Phillips synthesizer IC SA7025A in Figure 4-2.

### 4.4 RF POWER AMPLIFIER CIRCUIT DESCRIPTION

The 3473 transmitter produces a nominal RF power output of 2 Watts (+33 dBm) at a supply voltage on pins 3 and 4 of 7.2 VDC. Frequency modulation (FM) of the transmit data input stream occurs in the VCO (see previous section).

The transmitter line-up on the 3473 is a class C conduction type amplifier. A class C amplifier requires that the RF voltage being applied to the amplification device is sufficient as to cause the transistor to “turn-on”. This type of design was incorporated to improve efficiency over a class A type amplifier.

There are two major sections to the power amplifier in the 3473. A driver integrated circuit is the first device in the amplification line-up. The VCO is applied through a splitter and matching network to this device for intermediate amplification to +26 dBm (400 mW). The input voltage for this device is approximately 2.7 VDC. This low dropout regulated supply is produced by a dual op amp and a high current series pass PNP transistor Q611.

The power delivered from the driver stage is matched into a high power MOSFET transistor Q541. This device has about 8 dB of gain and amplifies the signal to +34.5 dBm. The RF voltage created from the driver stage is sufficient to turn on the MOSFET. The final is biased on to a quiescent current of  $I_{dss}=200$  mA which is set by R521. C552 is adjusted for balanced output power across the RF band. Present on the output of the final transistor is a low-pass transmitter harmonic filter. To insure the 3473 meets stringent regulatory guidelines a 5 pole filter rejects the harmonics created in the power amplifier.

## CIRCUIT DESCRIPTION

Three PIN diodes and several matching components are used to implement the antenna switch. In transmit mode, the diodes are all forward biased. A finely tuned coil and capacitor create a quarter wave open which reflects the transmitter power and protects the receiver front end from the transmitter. In receive mode the diodes are off thus creating a 50 ohm impedance path to the front end of the 3473 receiver. Due to passive device losses in the low pass filter and the antenna switch, the output power is reduced to 2 watts. The transmit signal is then fed to the female MCX antenna connector J501.

The 3473 implements a logic level at the user interface connector to enable the transmitter. By applying a logic high to pin 6 the transmitter will enable, assuming the synthesizer and VCO are locked and ready to transmit. Refer to section 3 for the exact receive to transmit load sequence. When the logic level is applied the RF is brought up relatively slow so that spectral spreading of the transmitter does not occur. An RC time constant 'ramps' up the RF power to the final which takes no longer than 2 ms. The ramping is incorporated so that the power of the transmitter does not splatter into channels adjacent to the frequency of operation.

## 4.5 RECEIVER CIRCUIT DESCRIPTION

The receiver on the 3473 is a FM dual down conversion superheterodyne topology. Dual down conversion means that the receiver has two intermediate frequencies (IF) of 86.85 MHz and 450 kHz. The first local oscillator (LO) is high side injected 86.85 MHz above the desired receive frequency. This is the function of the VCO in receive mode. The design also incorporates two discrete bandpass filters to reject image and other wideband frequencies. A surface acoustic wave (SAW) filter is implemented in the first IF to enhance receiver selectivity. 10 poles of filtering are used in the second IF to further improve selectivity and to set the IF bandwidth of either 12.5 kHz or 25 kHz. Figure 4-1 shows the receiver block diagram for the 3473 radio module.

From the antenna connector the signal is fed to a two pole bandpass filter. This filter sets the initial RF bandwidth of approximately 30 MHz for the receiver. A low noise amplifier (LNA) is matched from the bandpass filter. The LNA transistor Q210 produces about 14 dB of gain and sets the overall sensitivity of the radio. The LNA is followed by a three pole bandpass filter to help reject unwanted out of band RF signals. Both bandpass filters are discrete filter designs comprising of several air wound inductor coils and many surface mount capacitors.

The front end of the receiver is finely tuned into the mixer of the receiver. The mixer is an active design using a dual gate gallium arsenide MESFET labeled Q240. One gate of the FET is fed the RF signal from the front end network, and the other gate is fed the first LO injection from the VCO. To buffer the VCO from the receiver a transistor (Q302) with unity gain is in between the mixer and the VCO. The mixer, for example, converts the RF signal of 450 MHz and the first LO signal of 536.85 MHz to the first IF frequency 86.85 MHz.

From the mixer, the receive signal is delivered to a SAW filter which has a bandwidth of 40 kHz and provides the first narrow band filtering in the receiver. SAW filter technology features low group delay performance for data applications, low distortion at high RF input levels, and fixed tuning. The output of the SAW filter travels to a Phillips SA676 IF IC for down conversion to the second IF frequency, FM limiting, and demodulation to baseband of the data signal. The block diagram of U261 is shown in Figure 4-3.

## **5.1 GENERAL**

### **5.1.1 PERIODIC CHECKS**

This transceiver should be put on a regular maintenance schedule and an accurate performance record maintained. Important checks are receiver sensitivity and transmitter frequency, modulation, and power output. A procedure for these and other tests is located in Section 6. It is recommended that transceiver performance be checked annually even though periodic checks are not required by the FCC. During the first year, make an additional check or two to ensure no TCXO frequency drifting has occurred.

### **5.1.2 SURFACE-MOUNTED COMPONENTS**

A large number of the components used on the transceiver board are the surface-mounted type. Since these components are relatively small in size and are soldered directly to the PC board, care must be used when they are replaced to prevent damage to the component or PC board. Surface-mounted components should not be re-used because they may be damaged by the unsoldering process.

### **5.1.3 COMPONENT LAYOUTS AND SCHEMATIC DIAGRAM**

The component layouts of the PC boards used in this transceiver are located in Section 8. The schematic diagram is located in Section 9.

### **5.1.4 REPLACEMENT PARTS LIST**

A replacement parts list with all the parts used in this transceiver is located in Section 7. Parts are listed alpha-numerically according to designator. For information on ordering parts, refer to Section 1.7.

### **5.1.5 TCXO MODULE NOT SERVICEABLE**

The  $\pm 1.5$  PPM TCXO module is not field serviceable. Part changes require a factory recalibration to ensure that the oscillator stays within its  $\pm 1.5$  PPM tolerance.

## **5.2 SYNTHESIZER SERVICING**

### **5.2.1 INTRODUCTION**

When there is a synthesizer malfunction, the VCO is not locked on frequency. When an unlocked VCO is detected by the lock detector circuit, U811, pin 18 goes low.

*NOTE: The user-supplied circuitry must disable the transmitter and receiver when an out-of-lock condition is indicated.*



## SERVICING

When the VCO is unlocked, the fr and fv inputs to the phase detector are not in phase (see Section 4.3). The phase detector in U811 then causes the VCO control voltage to go to the high or low end of its operating range. This in turn causes the VCO to oscillate at the high or low end of its frequency range.

A loop is formed by VCO Q962, amplifier Q971/Q972, Q994 and the RF IN of U811 (see Figure 4-1). If any of these components begin to malfunction, improper signals appear throughout the loop. Correct operation of the counters can still be verified by measuring the input and output frequencies to check the divide number.

Proceed as follows to check the synthesizer I/O signals to determine if it is operating properly.

### 5.2.2 REFERENCE OSCILLATOR

Check the signal at U811, pin 8. It should be 14.4 MHz at 1.0 Vp-p. If the TCXO module is defective, it is not serviceable and must be replaced with a new module at the Dataradio factory.

### 5.2.3 VCO

The output level of Q994 can be measured with an RF voltmeter or some other type of high impedance meter. The minimum level after a power splitter at R893 or R894 should be -10 dBm.

Check the DC control voltage at TP831 (Test Point) with a channel near the center of the band. If the VCO is locked on frequency, this should be a steady DC voltage near 3V. Check the VCO frequency at R893 or R894. If the VCO is locked on frequency, it should be stable on the transmit or receive channel frequency. If it is not locked on frequency, The control line voltage will be near the lower or upper end of its range (0V or 5.5V).

### 5.2.4 SYNTHESIZER (U811)

When the VCO is locked on frequency, the lock detect output on J201, pin 11 should be high (>4.0 VDC).

## 5.3 RECEIVER SERVICING

To isolate a receiver problem to a specific section, refer to the troubleshooting flowchart in Figure 5-1. Tests referenced in the flowchart are described in the following information. *NOTE: Supply voltages are provided by the user.*

### 5.3.1 SUPPLY VOLTAGES AND CURRENT

Measure the supply voltages on the following pins at interface connector J201:

Pins 3, 4, 5 - 7.2V DC nominal

Pin 6 - 0.0 VDC in Tx Mode

Pin 7 - > 4.5 VDC Receive

Pin 8 - 5.0V DC

Pin 10 - 2.5 VDC Receive (no modulation)

Place a DC ammeter in the supply line to the transceiver and the following maximum currents should be measured:

Pins 3, 4, 5 - combined should be < 60 mA

### 5.3.2 IF/LIMITER/DETECTOR/2ND LO (U261)

#### Data Output

Using a coupling capacitor, inject at U261, pin 1, a 86.85 MHz, 1 mV signal, modulated with 1 kHz at  $\pm 3$  kHz deviation. The audio output level at J201, pin 12 should be approximately 150 mV RMS (25 kHz BW) or  $\pm 1.5$  kHz deviation (12.5 kHz BW).

#### RSSI Output

The RSSI output on J201, pin 13 should be greater than 100 mV and less than 1.2 VDC with no RF signal present. If either of the preceding measurements is not correct, there may be a problem with U261.

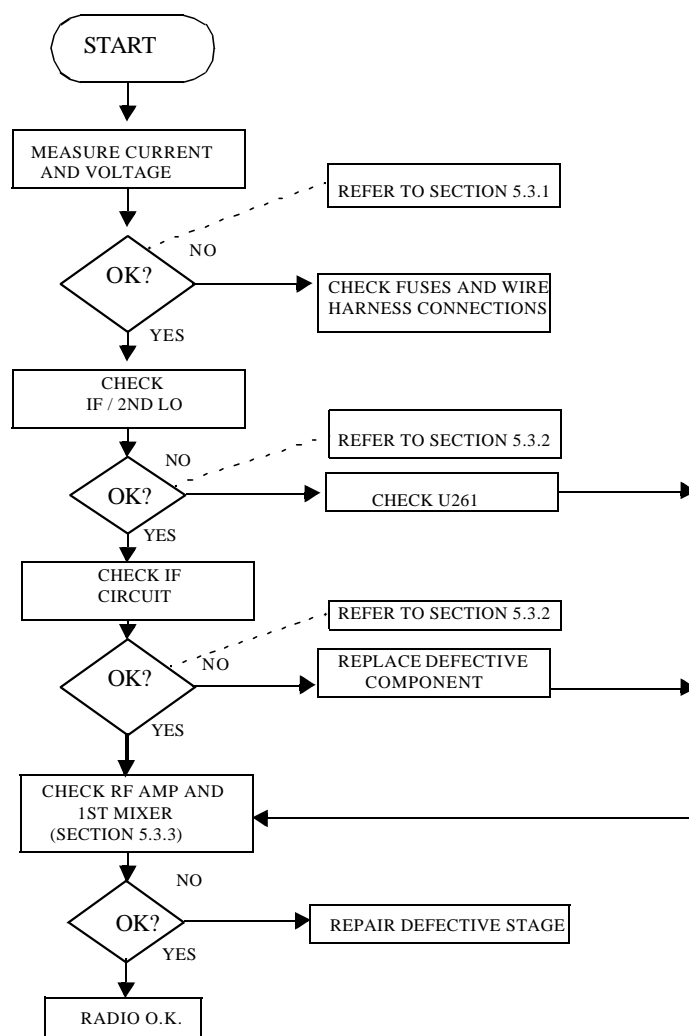
#### 2nd Local Oscillator Injection

The 86.4 MHz 2nd LO injection into pin 4 of U261 should be > 200 m Vp-p.

#### Quadrature Detector (L263)

The data detector must be peaked for maximum audio. Adjust L263 for peak AC audio. Check the DC output (2.5 VDC nominal).

## SERVICING



**Figure 5-1 RECEIVER SERVICING FLOWCHART**

### 5.3.3 RF AMPLIFIER (Q210) AND FIRST MIXER (Q240)

Check Q210 and Q240 for proper DC voltage operation. The voltage across R210 should be approximately 0.7 VDC. The voltage across R212 should be such that Q210 draws about 5 mA in receive mode. Q240 should have a voltage across R241 such that the Dual Gate MESFET draws between 2 - 4 mA. Q302 buffers the VCO from the mixer. The voltage at R306 should be between .20 - .40V for 2 - 4 mA of current.

## **5.4 TRANSMITTER SERVICING**

### **5.4.1 SUPPLY VOLTAGES AND CURRENT**

Measure the supply voltages on the following pins of interface connector J201:

Pins 3, 4, 5 - 7.2V DC nominal

Pin 6 - >4.5V DC

Pin 7 - 0.0V DC (while transmitting)

Pin 8 - >5.0 VDC  $\leq$  Pin 5 Vdc

Pin 10 - 2.5V  $\pm$  0.05 Vdc DC Transmit

Place a DC ammeter in the supply line to the transceiver and the following nominal currents should be measured:

Pins 3, 4 - 800 mA

Pin 5 - 400 mA

### **5.4.2 TRANSMIT DRIVER STAGE**

In transmit, measure pin 1 and pin 4 of U511. This is the supply voltage for the power amplifier driver stage. This voltage should measure 2.70 VDC. The voltage on pin 8 should be between 2.5 and 3.0V. Measure the RF input power to pin 5 of U511 by capacitive coupling an RF power meter. The RF power should be > -10 dBm. If the input power is not adequate, refer to Section 5.2.3 for more information about the VCO functionality. Measure the RF output at the junction of L522 and C524. The power should be > +25 dBm. If the power supply is correct and output power and current are low, replace U511.

### **5.4.3 POWER AMPLIFIER FINAL STAGE**

Q541 is a power RF MOSFET. Measure the voltage on the gate of the final (R533). This voltage should be between 4 - 5 VDC for 2 watt operation. To verify the IDSS is properly adjusted, short to ground TP601 while in transmit mode. The transceiver should be drawing ~ 350 mA of current. See Section 6.2.2 if the current is not > 300 mA and < 380 mA. Verify supply voltage on the drain of the RF MOSFET (Q541) is 7.2 Vdc nominal for 2 watt power output. Measure the output power of the transistor at the junction of C554. The power should be  $\geq$  2.5 watts. If not, replace Q541.

### **5.4.4 LOW PASS FILTER AND ANTENNA SWITCH**

There should be approximately 1.0 dB of loss through the Low Pass Filter (LPF) and Antenna Switch to J501. The voltage drop across R561 should be approximately 3.0 V for 36 mA of current.

## SERVICING

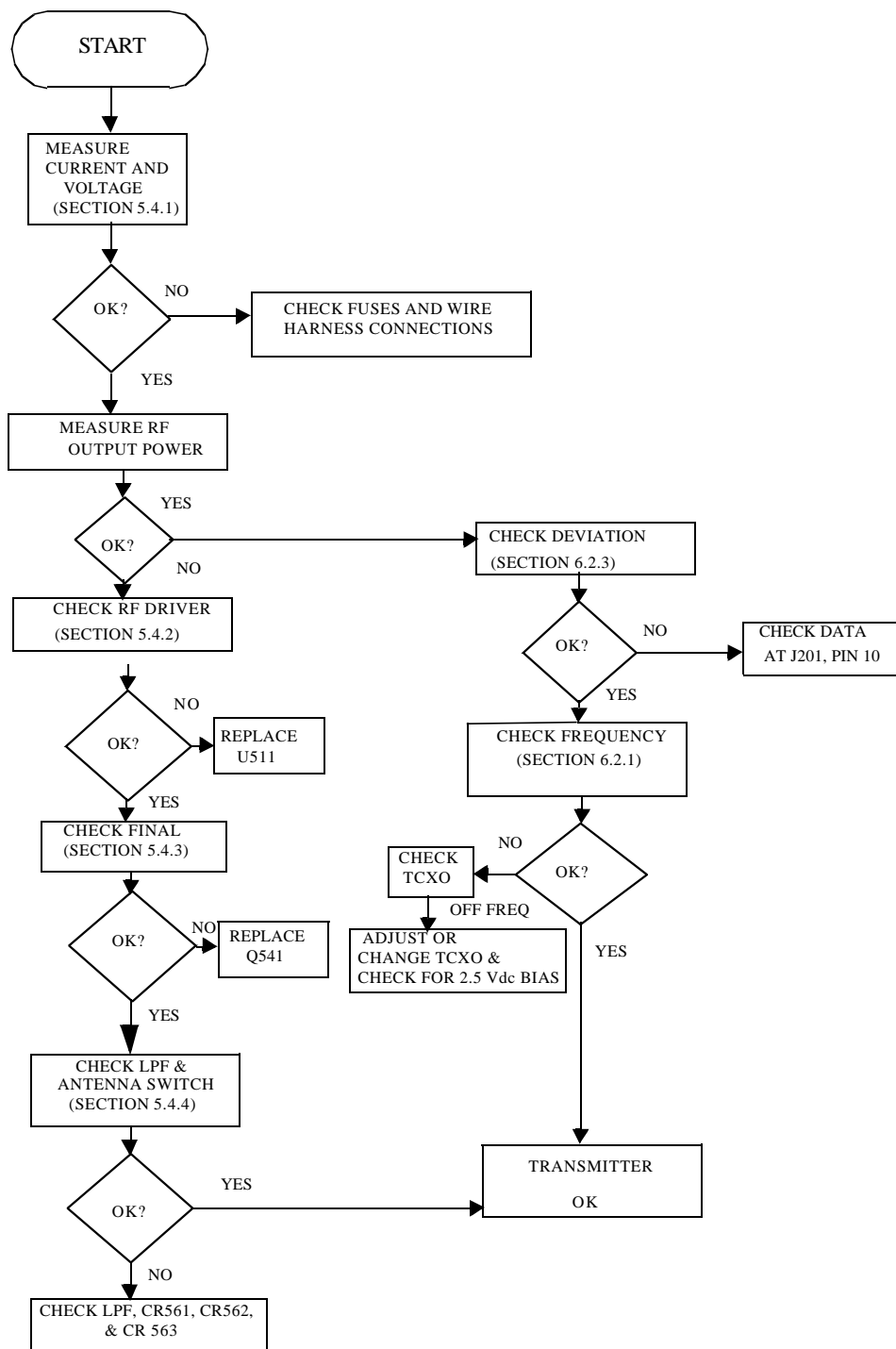


Figure 5-2 TRANSMITTER SERVICING FLOWCHART

## ALIGNMENT PROCEDURE AND PERFORMANCE TESTS

### 6.1 GENERAL

Receiver or transmitter alignment may be necessary if repairs are made that could affect tuning. Alignment points diagrams are located in Figure 6-3 or component layouts are located in Section 8.

Fabricate test cables by referring to Section 2.2 Interfacing with Data Equipment. This cable should include power and ground, a transmit keying switch that applies 5.5 VDC to the Rx and Tx Enable, data input and data output. The test setup must apply the various supply voltages and load the synthesizer with channel information.

### 6.2 ALIGNMENT PROCEDURE

#### 6.2.1 VCTCXO SETUP (Y801)

1. Apply 7.2 Vdc  $\pm$  0.1 Vdc to pins 3, 4, and 5.
2. Verify 2.5 Vdc  $\pm$  0.05 Vdc is on pin 10.
3. Set Y801 (the VCTCXO) to 14.400000 MHz  $\pm$  6.0 Hz ( $\pm$  0.4PPM)

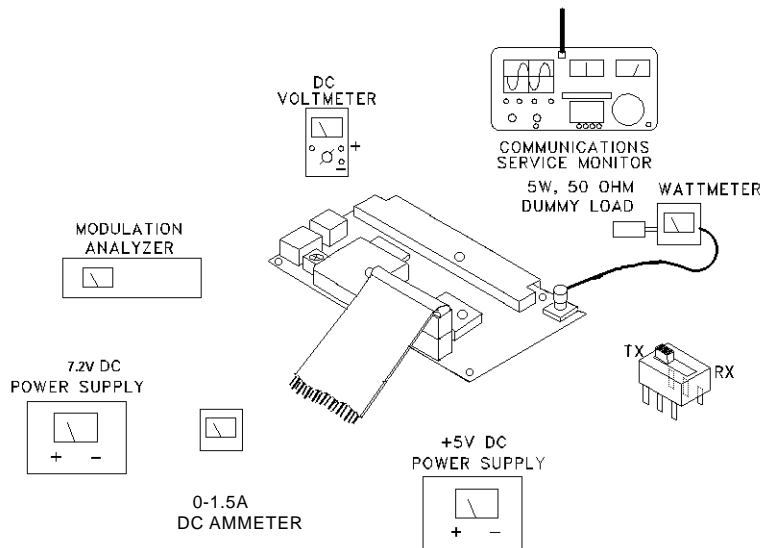
#### 6.2.2 FREQUENCY AND CONTROL LINE VOLTAGE CHECK

1. Connect the test setup shown in Figure 6-1. Set the power supply for +7.2V DC.
2. Load the synthesizer with the channel frequency.
3. Connect a DC voltmeter at TP831 to measure the VCO control line voltage for a meter reading of  $\geq 0.50$  -  $\leq 5.0$ VDC for all desired frequencies of operation in both transmit and receive.

#### 6.2.3 2W TRANSMITTER POWER ALIGNMENT

1. Connect the test setup shown in Figure 6-1. A DC ammeter capable of measuring up to 2.0 A should be installed in the supply line.
2. Load the synthesizer with the desired channel frequency.
3. Set the IDSS of the final by shorting TP601. To Ground R521, turn counter-clockwise for minimum transmit current. Note the current and adjust R521 for 200 mA more current.
4. Key the transmitter and make sure that pins 3, 4, and 5 on the RF board are 7.2V.  
**(Do not transmit for extended periods.)**
5. Adjust C552 for 2 watts output power.

# ALIGNMENT PROCEDURE AND PERFORMANCE TESTS



**Figure 6-1 TRANSMITTER TEST SETUP**

## 6.2.4 MODULATION FLATNESS ALIGNMENT

1. Transmit into the modulation analyzer at the desired frequency and observe modulation output on the oscilloscope. Set the modulation analyzer high pass filtering off and no less than a 15 kHz low pass filter.
2. Inject a 100 Hz sine-wave on J201, pin 10, biased at 2.5V DC, at the level below according to the bandwidth:

200 m Vrms for 12.5 kHz BW (-210 Radios)  
400 m Vrms for 25.0 kHz BW (-230 Radios)  
180 m Vrms for 12.5 kHz BW (-510 Radios)  
360 m Vrms for 25.0 kHz BW (-530 Radios)

3. Switch on TX Modulation. Set the modulation analyzer for 15 kHz low pass filtering.
4. Note the transmit deviation \_\_\_\_\_ kHz. The deviation should be between:

$\pm 1.2/\pm 1.8$  kHz for 12.5 kHz BW (-X10 Radios)  
 $\pm 2.4/\pm 3.6$  kHz for 25.0 kHz BW (-X30 Radios)

5. Input a 1.0 kHz sine-wave at the same voltage. The transmit deviation should be the same as that noted in Step 4. If not, adjust R826 until the deviation level matches that of Step 4.
6. Remove transmit modulation and unkey the transmitter.

*Note: The modulation flatness can also be set flat by adjusting the voltage on pin 9 of J201 between 0-5 VDC.*

# ALIGNMENT PROCEDURE AND PERFORMANCE TESTS

## 6.2.5 FRACTIONAL CHANNEL SPUR ADJUSTMENT

1. Refer to Section 3.4.4 for the default CN values for the appropriate band radio (-2Y0 or -5Y0) to load into the synthesizer.
2. To determine if your desired frequency is a fractional channel, divide the frequency by 6.25 kHz. The number will be a whole integer. Divide the channel frequency by 12.5 kHz. If the number is not a whole integer, the frequency is a fraction channel frequency.
3. To optimize the performance of the receiver on a fractional channel, input an unmodulated (desired) frequency. Monitor the output of J201, pin 12 with an oscilloscope. Adjust R823 for a minimum level of 6.25 kHz recovered audio.
4. To optimize the performance of the transmitter on a fractional channel, monitor the de-modulated transmit signal of a modulation analyzer and adjust R823 for minimum level of 6.25 kHz recovered audio.
5. Receive and transmit performance can be further optimized by adjusting the CN value up or down for minimum recovered 6.25 kHz audio signal.

## 6.2.6 RECEIVER ALIGNMENT

**CAUTION:** *Do not key the transmitter with the generator connected! Severe generator damage may result.*

1. Connect the test setup shown in Figure 6-2. Adjust the power supply for +7.2V DC.
2. Measure the receive current drain. (current should be <60 mA.)
3. Load the synthesizer with the channel frequency.
4. Set the RF signal generator for this frequency with a 1 kHz tone (modulated output shown below) at a level of -47 dBm (1000  $\mu$ V) and inject into J501.

1.5 kHz deviation (-X10 12.5 kHz BW Radio)

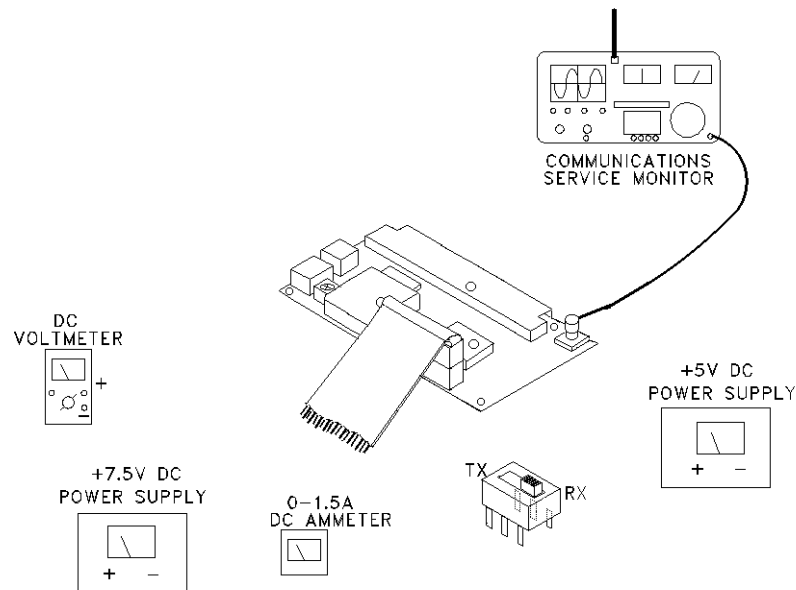
3.0 kHz deviation (-X30 25.0 kHz BW Radio)

*NOTE: Maintain these deviation levels throughout the test when measuring AC levels, SINAD and % distortion.*

5. Adjust L263 for maximum  $V_{rms}$  at the receive audio output.



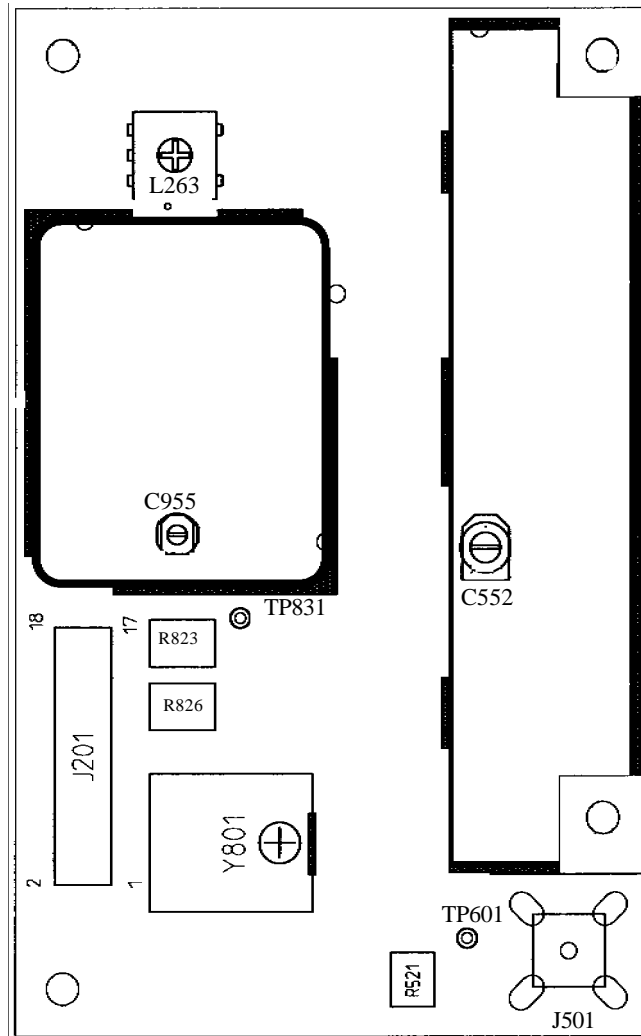
## ALIGNMENT PROCEDURE AND PERFORMANCE TESTS



**Figure 6-2 RECEIVER TEST SETUP**

6. Record the RMS audio voltage level \_\_\_\_ RMS. (Typically 150 mV  $\pm$  50 mV.) Record the DC Bias level of the audio out \_\_\_\_ Vdc. (Typically 2.5 Vdc  $\pm$  0.5 Vdc)
7. Record the percent distortion \_\_\_\_%. (Typically <3%.) (psophometrically weighted)
8. Adjust the RF input level until 12 dB SINAD is measured. (Typically < -116 dBm).
9. Adjust the generator RF level to -120 dBm and measure DC (RSSI) voltage on J201, pin 12 \_\_\_\_ Vdc at -120 dBm.
10. Adjust the generator RF level to -60 dBm and measure DC (RSSI) voltage on J201, pin 12 \_\_\_\_ Vdc at -60 dBm.
11. The RSSI voltage at -60 dBm minus the (RSSI) voltage -120 dBm should be >0.7 VDC and the RSSI voltage at -120 dBm  $\leq$  1.1 Vdc.

# ALIGNMENT PROCEDURE AND PERFORMANCE TESTS



**Figure 6-3 ALIGNMENT POINTS DIAGRAM**

## SECTION 7

### PARTS LIST

This parts list applies to 242-3473-510 transceivers. Part numbers for other bands of this transceiver are available from Technical Service representatives.

<b>SYMBOL NUMBER</b>	<b>DESCRIPTION</b>	<b>PART NUMBER</b>
A 515	AUTO 450-480 MHZ 3473	0233473515
C 130	1uf 16V 1206 CHIP CAP	6103606105
C 131	68pF 5% NPO 0603	6103674680
C 133	.01MF X7R K 0603 CHPR	6103675103
C 135	68pF 5% NPO 0603	6103674680
C 136	.01MF X7R K 0603 CHPR	6103675103
C 137	1uf 16V 1206 CHIP CAP	6103606105
C 151	68pF 5% NPO 0603	6103674680
C 152	68pF 5% NPO 0603	6103674680
C 153	68pF 5% NPO 0603	6103674680
C 154	68pF 5% NPO 0603	6103674680
C 155	68pF 5% NPO 0603	6103674680
C 156	68pF 5% NPO 0603	6103674680
C 157	100pF 5% NPO 0603	6103674101
C 158	68pF 5% NPO 0603	6103674680
C 159	68pF 5% NPO 0603	6103674680
C 160	68pF 5% NPO 0603	6103674680
C 161	68pF 5% NPO 0603	6103674680
C 162	68pF 5% NPO 0603	6103674680
C 163	68pF 5% NPO 0603	6103674680
C 171	68pF 5% NPO 0603	6103674680
C 172	1uf 16V 1206 CHIP CAP	6103606105
C 173	68pF 5% NPO 0603	6103674680
C 200	68pF 5% NPO 0603	6103674680
C 201	18pF 5% NPO 0603	6103674180
C 202	6.2pf +/- .1pF NPO 0603	6103673629
C 203	10pF +/- .1pF NPO 0603	6103673100
C 204	6.2pf +/- .1pF NPO 0603	6103673629
C 205	10pF +/- .1pF NPO 0603	6103673100
C 206	6.2pf +/- .1pF NPO 0603	6103673629
C 207	18pF 5% NPO 0603	6103674180
C 208	10pF +/- .1pF NPO 0603	6103673100
C 211	68pF 5% NPO 0603	6103674680

## PARTS LIST

SYMBOL NUMBER	DESCRIPTION	PART NUMBER
C 212	6.8pF +/- .1pF NPO 0603	6103673689
C 213	68pF 5% NPO 0603	6103674680
C 214	.01MF X7R K 0603 CHPR	6103675103
C 215	68pF 5% NPO 0603	6103674680
C 220	22pF 5% NPO 0603	6103674220
C 221	12pF 5% NPO 0603	6103674120
C 222	4.7pF +/- .1pF NPO 0603	6103673479
C 223	10pF +/- .1pF NPO 0603	6103673100
C 224	7.5pF +/- .1pF NPO 0603	6103673759
C 225	10pF +/- .1pF NPO 0603	6103673100
C 226	7.5pF +/- .1pF NPO 0603	6103673759
C 227	5.6pF +/- .1pF NPO 0603	6103673569
C 228	12pF 5% NPO 0603	6103674120
C 229	18pF 5% NPO 0603	6103674180
C 235	3.0pf +/- .1pF NPO 0603	6103673309
C 240	2.2pF +/- .1pF NPO 0603	6103673229
C 241	.01MF X7R K 0603 CHPR	6103675103
C 242	.01MF X7R K 0603 CHPR	6103675103
C 243	7.5pF +/- .1pF NPO 0603	6103673759
C 244	68pF 5% NPO 0603	6103674680
C 245	.01MF X7R K 0603 CHPR	6103675103
C 250	12pF 5% NPO 0603	6103674120
C 251	6.2pf +/- .1pF NPO 0603	6103673629
C 252	5.1pf +/- .1pF NPO 0603	6103673519
C 253	.01MF X7R K 0603 CHPR	6103675103
C 260	.01MF X7R K 0603 CHPR	6103675103
C 261	.01MF X7R K 0603 CHPR	6103675103
C 262	.01MF X7R K 0603 CHPR	6103675103
C 263	.01MF X7R K 0603 CHPR	6103675103
C 264	.01MF X7R K 0603 CHPR	6103675103
C 265	10pF +/- .1pF NPO 0603	6103673100
C 270	47UFD 10V SMD TANT RL	6102624470
C 271	.01MF X7R K 0603 CHPR	6103675103
C 272	68pF 5% NPO 0603	6103674680
C 273	.01MF X7R K 0603 CHPR	6103675103
C 274	.01MF X7R K 0603 CHPR	6103675103
C 277	.01MF X7R K 0603 CHPR	6103675103
C 278	.1UFD X7R J 1206 RL	6103609104
C 280	39pF 5% NPO 0603	6103674390
C 281	4.3pF +/- .1pF NPO 0603	6103673439
C 282	39pF 5% NPO 0603	6103674390
C 283	.01MF X7R K 0603 CHPR	6103675103
C 284	.01MF X7R K 0603 CHPR	6103675103
C 285	.01MF X7R K 0603 CHPR	6103675103
C 290	.01MF X7R K 0603 CHPR	6103675103

## PARTS LIST

SYMBOL NUMBER	DESCRIPTION	PART NUMBER
C 291	.01MF X7R K 0603 CHPR	6103675103
C 301	68pF 5% NPO 0603	6103674680
C 303	68pF 5% NPO 0603	6103674680
C 304	10pF +/- .1pF NPO 0603	6103673100
C 305	68pF 5% NPO 0603	6103674680
C 306	68pF 5% NPO 0603	6103674680
C 307	68pF 5% NPO 0603	6103674680
C 511	1uf 16V 1206 CHIP CAP	6103606105
C 512	.01MF X7R K 0603 CHPR	6103675103
C 513	68pF 5% NPO 0603	6103674680
C 514	.01MF X7R K 0603 CHPR	6103675103
C 515	68pF 5% NPO 0603	6103674680
C 516	68pF 5% NPO 0603	6103674680
C 517	6.8pF +/- .1pF NPO 0603	6103673689
C 518	68pF 5% NPO 0603	6103674680
C 521	68pF 5% NPO 0603	6103674680
C 522	.01MF X7R K 0603 CHPR	6103675103
C 523	12pF 5% NPO 0603	6103674120
C 524	12pF 5% NPO 0603	6103674120
C 525	68pF 5% NPO 0603	6103674680
C 531	.01MF X7R K 0603 CHPR	6103675103
C 532	68pF 5% NPO 0603	6103674680
C 533	27pF 5% NPO 0603	6103674270
C 546	68pF 5% NPO 0603	6103674680
C 547	68pF 5% NPO 0603	6103674680
C 548	1uf 16V 1206 CHIP CAP	6103606105
C 549	.01MF X7R K 0603 CHPR	6103675103
C 551	20PF NPO J 0805 CHP RL	6103601200
C 552	2.5-10PF SMD CERAMIC	6121602002
C 554	68pF 5% NPO 0603	6103674680
C 561	15PF NPO J 0805CHP RL	6103601150
C 562	33PF NPO J 0805 CHP RL	6103601330
C 564	13PF NPO J 0805 CHIP/R	6103601130
C 565	10pF +/- .1pF NPO 0603	6103673100
C 566	22pF 5% NPO 0603	6103674220
C 567	.01MF X7R K 0603 CHPR	6103675103
C 568	68pF 5% NPO 0603	6103674680
C 569	1.2PF NPO J0805 CHP RL	6103601129
C 570	2.2PF NPO J0805 CHP RL	6103601229
C 571	68pF 5% NPO 0603	6103674680
C 572	.01MF X7R K 0603 CHPR	6103675103
C 573	68pF 5% NPO 0603	6103674680
C 601	.001uF 10% X7R 0603	6103675102
C 602	1uf 16V 1206 CHIP CAP	6103606105
C 603	.1UFD X7R J 1206 RL	6103609104

## PARTS LIST

SYMBOL NUMBER	DESCRIPTION	PART NUMBER
C 604	.01MF X7R K 0603 CHPR	6103675103
C 605	.0082UF X7R K 0805 CHIP	6103605822
C 606	.01MF X7R K 0603 CHPR	6103675103
C 607	68pF 5% NPO 0603	6103674680
C 611	1uf 16V 1206 CHIP CAP	6103606105
C 612	68pF 5% NPO 0603	6103674680
C 613	.01MF X7R K 0603 CHPR	6103675103
C 621	.1UFD X7R J 1206 RL	6103609104
C 622	.01MF X7R K 0603 CHPR	6103675103
C 623	68pF 5% NPO 0603	6103674680
C 624	.0082UF X7R K 0805 CHIP	6103605822
C 803	.01MF X7R K 0603 CHPR	6103675103
C 804	.01MF X7R K 0603 CHPR	6103675103
C 805	68pF 5% NPO 0603	6103674680
C 806	.01MF X7R K 0603 CHPR	6103675103
C 807	68pF 5% NPO 0603	6103674680
C 811	.001uF 10% X7R 0603	6103675102
C 812	.01MF X7R K 0603 CHPR	6103675103
C 813	.001uF 10% X7R 0603	6103675102
C 815	3.3pF +/- .1pF NPO 0603	6103673339
C 816	3.9pF +/- .1pF NPO 0603	6103673399
C 821	1uf 16V 1206 CHIP CAP	6103606105
C 822	.001uF 10% X7R 0603	6103675102
C 824	12pF 5% NPO 0603	6103674120
C 825	.001uF 10% X7R 0603	6103675102
C 826	1uf 16V 1206 CHIP CAP	6103606105
C 827	68pF 5% NPO 0603	6103674680
C 831	100pF 5% NPO 0603	6103674101
C 832	.039UF X7R K CHIP RL	6103606393
C 833	.0039UF X7R K0805 C/RL	6103605392
C 836	3900PF NPO G 1206 RL	6103616392
C 842	68pF 5% NPO 0603	6103674680
C 844	68pF 5% NPO 0603	6103674680
C 845	.01MF X7R K 0603 CHPR	6103675103
C 846	68pF 5% NPO 0603	6103674680
C 847	68pF 5% NPO 0603	6103674680
C 901	4.7UF,16V,SMDA,20%,TANT	6109224011
C 902	.001uF 10% X7R 0603	6103675102
C 903	68pF 5% NPO 0603	6103674680
C 904	.01MF X7R K 0603 CHPR	6103675103
C 910	68pF 5% NPO 0603	6103674680
C 913	1pF +/- .1pF NPO 0603	6103673109
C 914	1.5pF +/- .1pF NPO 0603	6103673159
C 945	68pF 5% NPO 0603	6103674680
C 946	68pF 5% NPO 0603	6103674680

# PARTS LIST

SYMBOL NUMBER	DESCRIPTION	PART NUMBER
C 948	68pF 5% NPO 0603	6103674680
C 949	12pF 5% NPO 0603	6103674120
C 950	33pF 5% NPO 0603	6103674330
C 951	18pF 5% NPO 0603	6103674180
C 952	9.1pF +/- .1pF NPO 0603	6103673919
C 953	10pF +/- .1pF NPO 0603	6103673100
C 954	1.5pF +/- .1pF NPO 0603	6103673159
C 955	CER CHIP TRIM CAP,3.0PF	6121700006
C 960	15pF 5% NPO 0603	6103674150
C 962	10pF +/- .1pF NPO 0603	6103673100
C 963	6.8pF +/- .1pF NPO 0603	6103673689
C 964	6.8pF +/- .1pF NPO 0603	6103673689
C 965	68pF 5% NPO 0603	6103674680
C 971	100pF 5% NPO 0603	6103674101
C 972	100pF 5% NPO 0603	6103674101
C 973	10pF +/- .1pF NPO 0603	6103673100
C 974	68pF 5% NPO 0603	6103674680
C 982	5.6pF +/- .1pF NPO 0603	6103673569
C 983	68pF 5% NPO 0603	6103674680
C 990	68pF 5% NPO 0603	6103674680
C 991	68pF 5% NPO 0603	6103674680
C 992	.01MF X7R K 0603 CHPR	6103675103
C 993	5.6pF +/- .1pF NPO 0603	6103673569
C 994	68pF 5% NPO 0603	6103674680
CR 210	SWITCHING DIODE SOT-23	6231504002
CR 561	SOT23 LOW DIST. PIN DI	6231504042
CR 562	SOT23 LOW DIST. PIN DI	6231504042
CR 563	SOT23 LOW DIST. PIN DI	6231504042
CR 801	DUAL SWITCH-COM CATH	6231504022
CR 901	BB535 SOD 323 VARACTOR	6235005022
CR 911	LO SER RESIS ABRPTVARAC	6235005028
CR 945	BB535 SOD 323 VARACTOR	6235005022
CR 948	BAND SWITCH DIODESOT23	6231504035
EP 511	FERRITE BEAD, SMD, 3AMP	6172503003
EP 541	FERRITE BEAD, SMD, 3AMP	6172503003
J 201	SOCKET,2MM,DBLROW,VERT	6157102410
J 501	STR TERM PCB(MCX CON)	6153013030
J 501	STR TERM PCB(MCX CON)	6153013030
L 200	8.0NH SM AIR CORE IND	6420030003
L 206	8.0NH SM AIR CORE IND	6420030003
L 210	INDUCTLL2012F12N0805	6429003127
L 211	INDUCTLL2012F15N0805	6429003157
L 220	8.0NH SM AIR CORE IND	6420030003
L 224	8.0NH SM AIR CORE IND	6420030003
L 229	8.0NH SM AIR CORE IND	6420030003

## PARTS LIST

SYMBOL NUMBER	DESCRIPTION	PART NUMBER
L 235	SMD INDUCTOR REELED	6429003277
L 240	SMD INDUCTOR REELED	6429003277
L 241	270 NYH0805SMD5%INDUC	6429003278
L 251	330 NHY0805SMD10%INDUC	6429003338
L 263	QUADCOIL68OUH/180PF	6425102001
L 277	1.0 UHY SMD INDUCTOR	6429001109
L 280	.082 UHY SMD INDUCTOR	6429001827
L 282	.082 UHY SMD INDUCTOR	6429001827
L 301	INDUCTLL2012F6N80805	6429003686
L 302	SMD INDUCTOR REELED	6429003277
L 511	INDUCT LL2012F6N80805	6429003686
L 512	INDUCT LL2012F12N 0805	6429003127
L 521	2TURN 24AWG .080ID	6420030002
L 522	4.7 NHY0805SMD10%INDUC	6429003476
L 531	5.6NH IND REELCER10%	6429003566
L 541	5T 18.5nh SMD AIR CORE	6420030005
L 551	1T 2.5nh SMD AIR CORED	6420030001
L 552	2TURN 24AWG .080ID	6420030002
L 561	2TURN 24AWG .080ID	6420030002
L 563	8.0NH SM AIR CORE IND	6420030003
L 565	1.0 UHY SMD INDUCTOR	6429001109
L 566	5T 18.5nhAIR CORE IND	6420030005
L 815	39 NHY0805SMD10%INDUC	6429003397
L 945	100 MHY0805 5% INDUC	6429003108
L 949	100 MHY0805 5% INDUC	6429003108
L 962	100 MHY0805 5% INDUC	6429003108
L 981	INDUCTLL2012F18N 0805	6429003187
L 995	INDUCTLL2012F18N 0805	6429003187
MP 801	3473 VCO CAN	0172225040
MP 801	3473 VCO CAN	0172225040
MP 802	3473 TX SHIELD	0172225042
MP 802	3473 TX SHIELD	0172225042
PC 001	3473 UHFTRANS PCB	0353473030
Q 132	DIG TRANS PNP10K/47K	6760013032
Q 133	DIG TRANS NPN 47K/47K	6760013046
Q 171	DIG TRANS NPN 47K/47K	6760013046
Q 172	DIG TRANS PNP 10K/47K	6760013032
Q 173	DIG TRANS NPN 47K/47K	6760013046
Q 210	NPN TRANS NE85619 SC9	6760003651
Q 240	DUAL GATE GAAS MESFET	6760006407
Q 280	IV (NPN) 85633 SOT23R25	6760003636
Q 302	NPN TRANS NE85619 SC90	6760003651
Q 541	7.5W12.5VUHFN-CHDMOSFET	6760006054
Q 601	DIG TRANS NPN 47K/47K	6760013046
Q 602	DIG TRANS NPN 47K/47K	6760013046



## PARTS LIST

SYMBOL NUMBER	DESCRIPTION	PART NUMBER
Q 603	DIG TRANS PNP 10K/47K	6760013032
Q 611	MJD42C PNP SMD 6 AMP	6760002603
Q 612	XSTR, SI,NPN SOT-23	6760003658
Q 841	DIG TRANS NPN 47K/47K	6760013046
Q 842	DIG TRANS PNP 10K/47K	6760013032
Q 901	NPN SC70MSD1819GEN PURP	6760013701
Q 962	IV (NPN) 85633 SOT23R25	6760003636
Q 971	NPN TRANS NE85619 SC90	6760003651
Q 972	NPN TRANS NE85619 SC90	6760003651
Q 994	NPN TRANS NE85619 SC90	6760003651
R 132	10 OHMS J 063W 0603CHIP	6690155100
R 171	10K OHMS J063W 0603CHIP	6690155103
R 210	3.9K OHM J063W0603 CHIP	6690155392
R 211	18k OHMS J063W0603 CHIP	6690155183
R 212	100 OHMS J063W0603 CHIP	6690155101
R 213	2.2K OHMS J063W0603CHIP	6690155222
R 214	820 OHMS J 063W0603CHIP	6690155821
R 240	1K OHM J 063W 0603 CHIP	6690155102
R 241	270 OHMS J 063W0603CHIP	6690155271
R 242	10 OHMS J 063W 0603CHIP	6690155100
R 243	4.7K OHM J 063W0603CHIP	6690155472
R 251	8.2k OHMS J063W0603CHIP	6690155822
R 261	2.4K OHMS J063W0603CHIP	6690155242
R 262	3.3K OHM J 063W0603CHIP	6690155332
R 265	39K OHMS J063W 0603CHIP	6690155393
R 271	100 OHMS J 063W0603CHIP	6690155101
R 273	75K OHM J 0603W0603CHIP	6690155753
R 275	33K OHMS J 063W0603CHIP	6690155333
R 276	15k OHMS J 063W0603CHIP	6690155153
R 278	18K OHM J 0805 CHIP/RL	6690105183
R 282	10 OHMS J 063W 0603CHIP	6690155100
R 283	470 OHMS J 063W0603CHIP	6690155471
R 284	33K OHMS J 063W0603CHIP	6690155333
R 285	4.7K OHM J 063W0603CHIP	6690155472
R 286	470 OHMS J 063W0603CHIP	6690155471
R 290	330 OHMS J 063W0603CHIP	6690155331
R 291	10K OHMS J 063W0603CHIP	6690155103
R 301	10 OHMS J 063W 0603CHIP	6690155100
R 302	10K OHMS J 063W0603CHIP	6690155103
R 303	1K OHM J 063W 0603 CHIP	6690155102
R 304	2K OHMS J 063W0603 CHIP	6690155202
R 305	1K OHM J 063W 0603 CHIP	6690155102
R 306	100 OHMS J063W0603 CHIP	6690155101
R 502	1 OHM J 063W 0603 CHIP	6690155109
R 521	100K OHM SMDTRIMMER3MM	6620132104

## PARTS LIST

SYMBOL NUMBER	DESCRIPTION	PART NUMBER
R 523	1K OHM J 063W 0603 CHIP	6690155102
R 531	1K OHM J 063W 0603 CHIP	6690155102
R 533	100k OHMS J063W0603CHIP	6690155104
R 561	82 OHM J 1206 SMD REEL	6690115820
R 564	47K OHMSJ063W 0603 CHIP	6690155473
R 601	56K OHMSJ063W 0603 CHIP	6690155563
R 602	1K OHM J 063W 0603 CHIP	6690155102
R 603	1K OHM J 063W 0603 CHIP	6690155102
R 604	22K OHMSJ063W 0603 CHIP	6690155223
R 605	10K OHMSJ063W 0603 CHIP	6690155103
R 606	43K OHMSJ063W 0603 CHIP	6690155433
R 607	10K OHMSJ063W 0603 CHIP	6690155103
R 608	10K OHMSJ063W 0603 CHIP	6690155103
R 609	150K OHMSJ063W0603 CHIP	6690155154
R 610	150K OHMS J063W0603CHIP	6690155154
R 611	470 OHMS J063W0603 CHIP	6690155471
R 612	10K OHMSJ063W 0603 CHIP	6690155103
R 613	10K OHMSJ063W 0603 CHIP	6690155103
R 614	470 OHMSJ063W 0603 CHIP	6690155471
R 615	100 OHMSJ063W 0603 CHIP	6690155101
R 616	2.7K OHMJ063W 0603 CHIP	6690155272
R 621	27K OHMSJ063W 0603 CHIP	6690155273
R 622	10K OHMSJ063W 0603 CHIP	6690155103
R 623	10K OHMSJ063W 0603 CHIP	6690155103
R 624	12K OHMSJ063W 0603 CHIP	6690155123
R 625	10K OHMSJ063W 0603 CHIP	6690155103
R 626	150K OHMSJ063W0603 CHIP	6690155154
R 627	150K OHMSJ063W0603 CHIP	6690155154
R 801	10K OHMSJ063W0603 CHIP	6690155103
R 802	20 OHM J063W0603 CHIP	6690155200
R 803	20 OHM J 063W0603 CHIP	6690155200
R 817	4.7K OHM J063W0603 CHIP	6690155472
R 821	100k OHMSJ063W0603 CHIP	6690155104
R 822	4.7K OHMJ063W 0603 CHIP	6690155472
R 823	100K SMDTRIMMER	6620130104
R 824	33K OHMS J 063W0603CHIP	6690155333
R 825	1K OHM J 063W 0603 CHIP	6690155102
R 826	10K OHM SMD TRIMMER	6620130103
R 828	1K OHM J 063W 0603 CHIP	6690155102
R 829	27K OHMS J 063W0603CHIP	6690155273
R 832	15k OHMS J 063W0603CHIP	6690155153
R 838	10K OHMS J 063W0603CHIP	6690155103
R 841	10K OHMS J 063W0603CHIP	6690155103
R 842	100 OHMS J 063W0603CHIP	6690155101
R 843	1K OHM J 063W 0603CHIP	6690155102

# PARTS LIST

SYMBOL NUMBER	DESCRIPTION	PART NUMBER
R 892	18 OHMS J 063W0603 CHIP	6690155180
R 893	18 OHMS J 063W0603 CHIP	6690155180
R 894	18 OHMS J 063W0603 CHIP	6690155180
R 901	4.7K OHM J063W0603 CHIP	6690155472
R 902	100 OHMSJ063W 0603 CHIP	6690155101
R 903	100 OHMS J063W0603 CHIP	6690155101
R 911	47K OHMS J063W0603 CHIP	6690155473
R 946	10K OHMS J063W0603 CHIP	6690155103
R 947	1K OHM J 063W 0603 CHIP	6690155102
R 948	1K OHM J 063W 0603 CHIP	6690155102
R 960	6.8K OHM J063W0603 CHIP	6690155682
R 961	10K OHMS J063W0603 CHIP	6690155103
R 962	150 OHMS J063W0603 CHIP	6690155151
R 963	10 OHMS J 063W0603 CHIP	6690155100
R 964	10 OHMS J 063W0603 CHIP	6690155100
R 971	470 OHMS J063W0603 CHIP	6690155471
R 972	2.7K OHM J063W0603 CHIP	6690155272
R 973	47 OHMS J 063W0603 CHIP	6690155470
R 974	3.3K OHMJ063W 0603 CHIP	6690155332
R 975	100 OHMSJ063W 0603 CHIP	6690155101
R 982	1K OHM J063W 0603 CHIP	6690155102
R 991	27 OHM J 063W 0603 CHIP	6690155270
R 992	47 OHMSJ 063W 0603 CHIP	6690155470
R 993	27 OHM J 063W 0603 CHIP	6690155270
R 994	10 OHMSJ 063W 0603 CHIP	6690155100
R 995	3.3K OHMJ063W 0603 CHIP	6690155332
R 996	1K OHM J 063W 0603 CHIP	6690155102
R 997	1K OHM J 063W 0603 CHIP	6690155102
U 130	5.5VLDOREGULATOR SOT-23	6442603060
U 261	SA676DK LV FM IF SSOP20	6442002037
U 511	500 MW UHF AMP, SOP-16	6444001016
U 601	QUAD OPAMP SO-14 33174	6442020017
U 811	FRACTIONAL-N SYNTH	6443954027
Y 801	TCVCXO,14.4MHZ,1.5,5VDC	6187009527
Y 801	TCVCXO,14.4MHZ,1.5,5VDC	6187009527
Z 250	86.85 MHZSAWFILT30 KHZ	6327000100
Z 260	450 KHZ4POLE12KHZCERFIL	6322004024
Z 260	450 KHZ4POLE25KHZCERFIL	6322004021
Z 261	450 KHZ6POLE12KHZCERFIL	6322004044
Z 261	450 KHZ6POLE25KHZCERFIL	6322004041
Z 954	0.5"LG RESONATOR1155MHZ	6429004008



## COMPONENT LAYOUTS

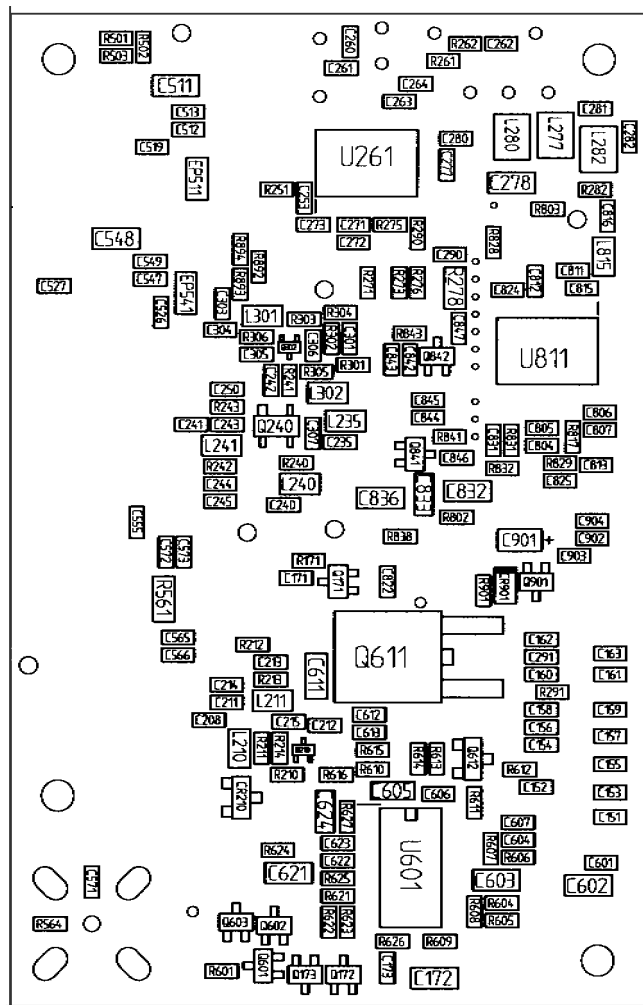
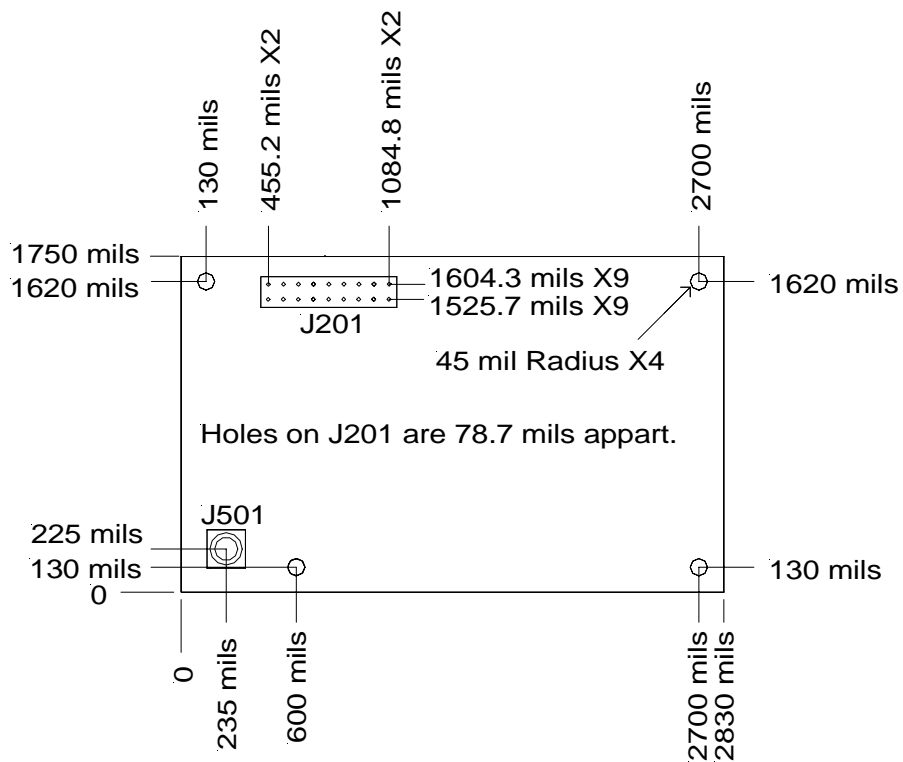
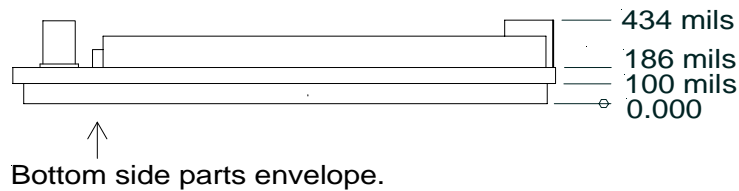


FIGURE 8-2 3473 COMPONENT LAYOUT (BOTTOM SIDE)

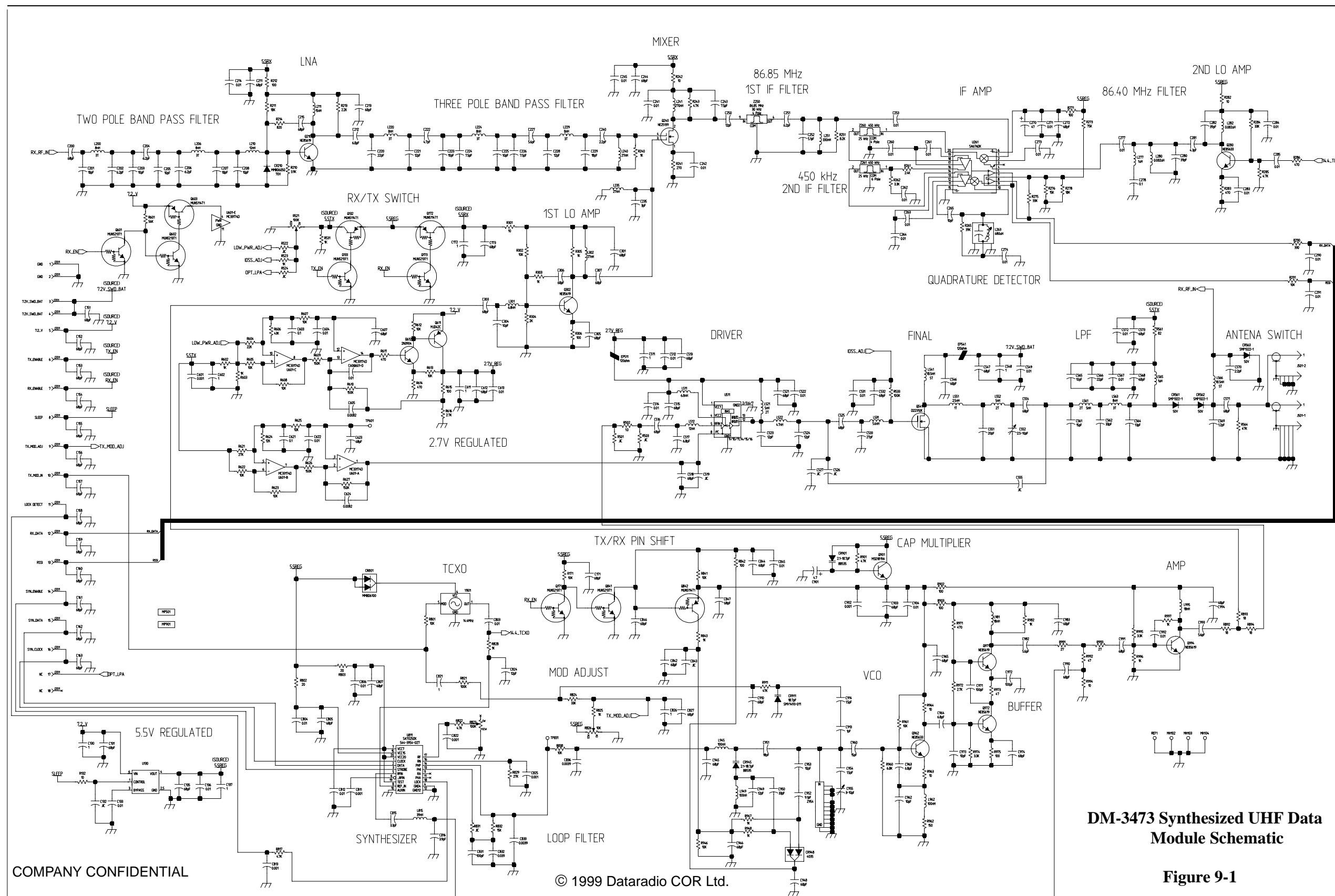
# COMPONENT LAYOUTS



Maximum height is .450 inches.



**FIGURE 8-3 DM-3473 MECHANICAL DIMENSIONS**



### Figure 9-1