

D670
Block Diagram
Theory of Operation

Project Name: D670

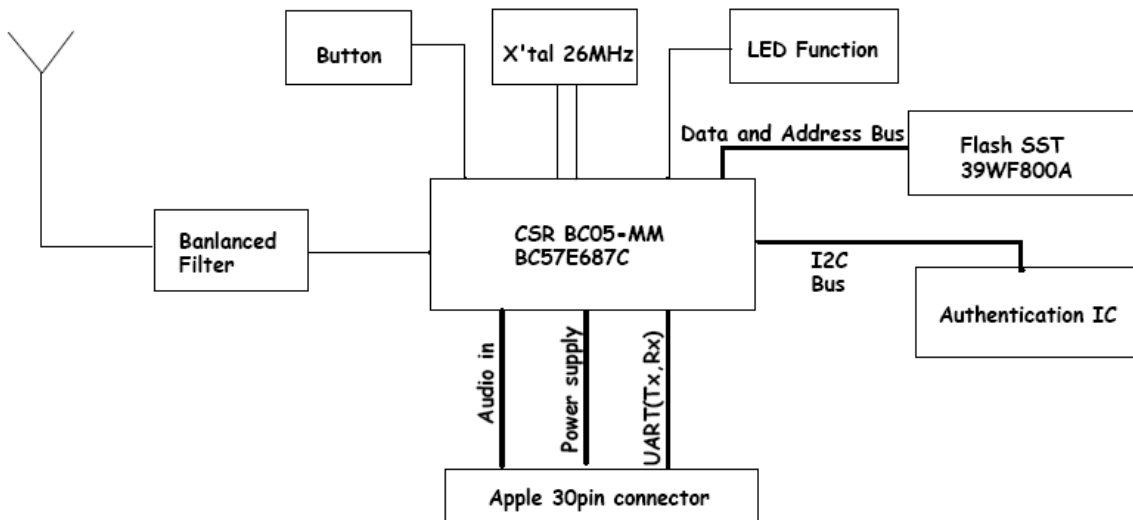
Date: Dec 22, 2008

Edited by: Allan Wang

1. Block Diagram

Block Diagram

Fusca 2.4G BT Antenna



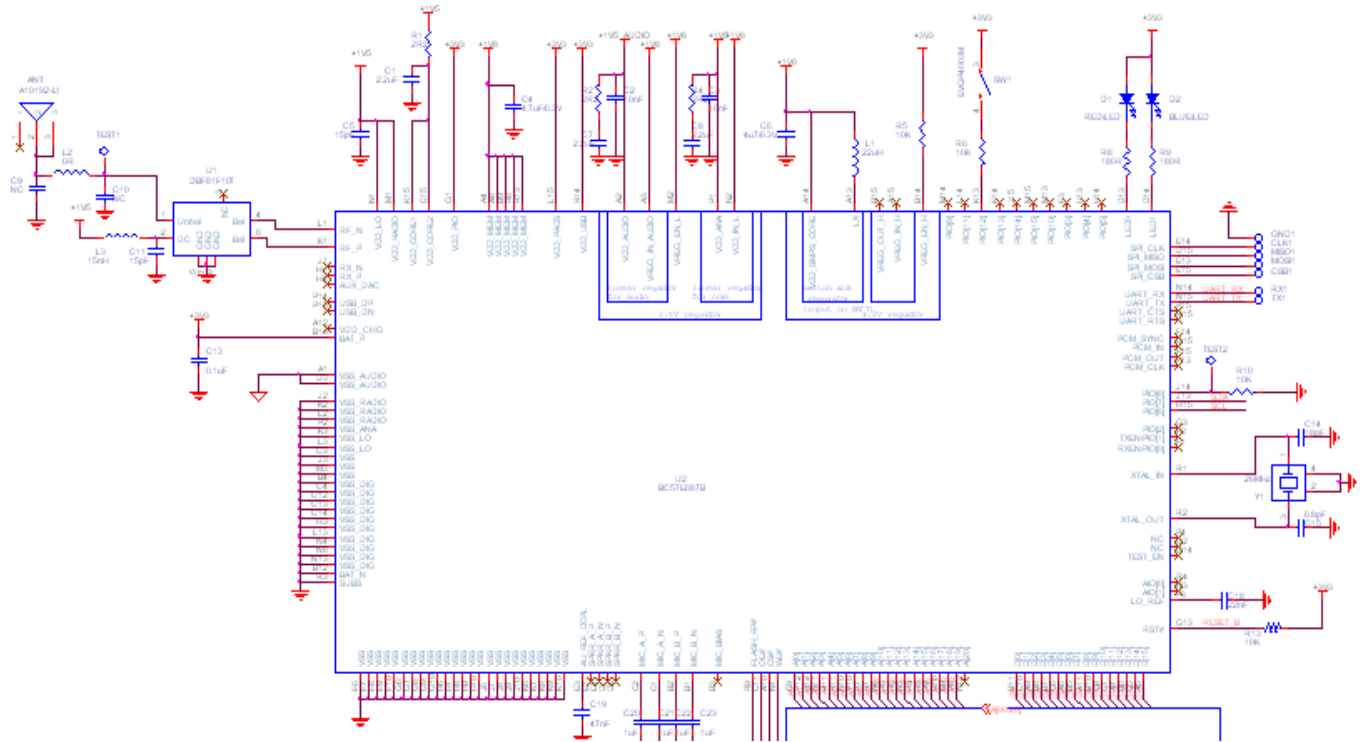
Microlink		
D670 iPod BT adapter		
Size A4	Document Number Block Diagram	Rev V2R1
Date Thursday, December 18, 2008	Sheet 1	of 2

Key parts:

- 1, CSR Chip: BC05-MM BC57E687C
- 2, Apple Authentication IC
- 3, Flash Memory: SST 39WF800A
- 4, Connector: 30pin Apple Connector
- 5, Antenna: Antenova 2.4G Chip Antenna

2. Detailed Descriptions

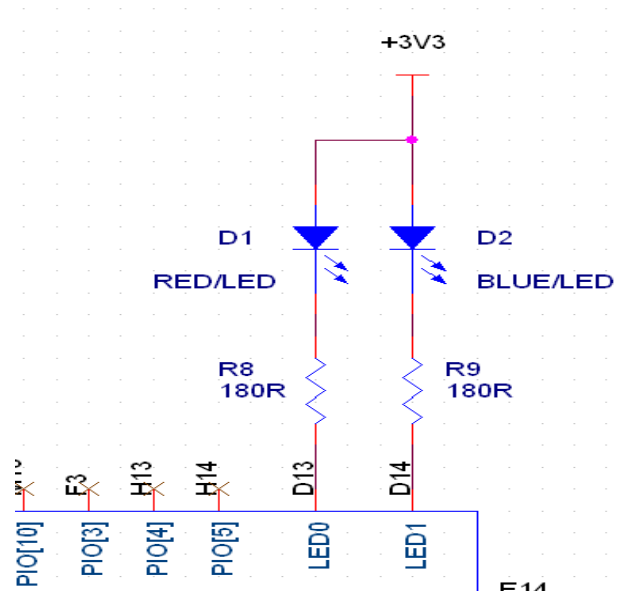
2.1 Bluetooth Circuit



Function Explanations:

1. Bluetooth chip: CSR BC57E687C.
2. Class 1.5 Bluetooth design with a balance filter.
3. Antenna: Antenova 2.4GHz chip antenna.
4. Crystal: 26MHz, 9pF, ± 10 ppm.
5. Flash memory: 8Mbit.
6. The firmware of Bluetooth is updated by SPI interface.

2.2 LED Control

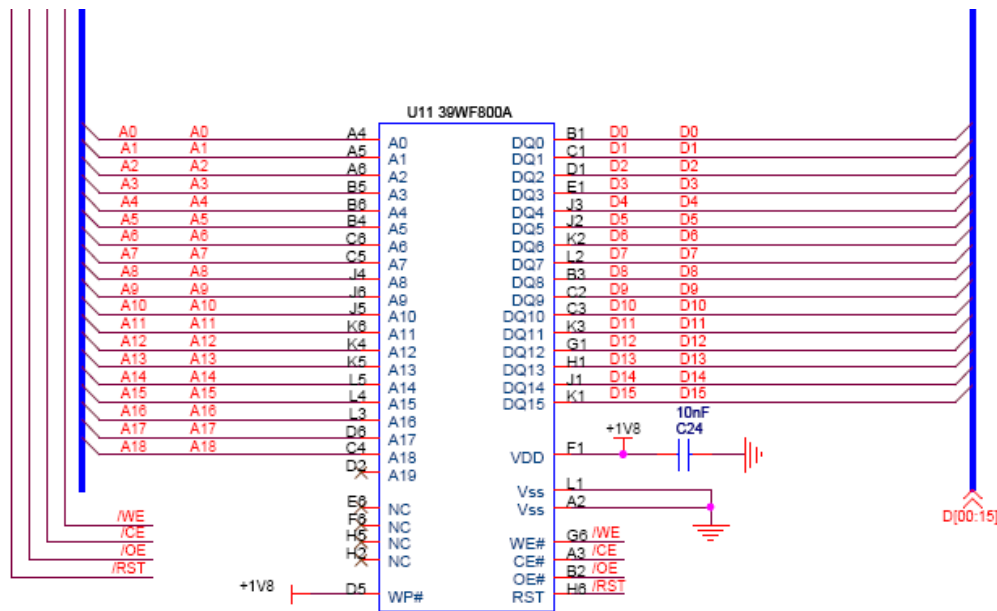


D1 (LED with Red) & D2 (LED with Blue) are controlled by LED0 and LED1.

BC05 includes two pads dedicated to driving LED indicators. Both terminals can be controlled by firmware to enable Red and Blue lighting.

The terminals are low output impedance pull downs, so the LED must be connected from a positive supply rail to the pad in series with a current limiting resistor.

2.3 External Flash Memory



The flash device used with BlueCore5-Multimedia External must meet the following criteria:

Either standard or extended form of the JEDEC (AMD/Fujitsu/SST) or Intel command set.

Access time must be $\leq 90\text{ns}$ @125°C 50pF load or $\leq 110\text{ns}$ @85°C 10pF load (typically $\leq 70\text{ns}$).

Write strobe of 100ns.

Accessible in word mode, i.e., via a 19-bit data bus.

Support changing different bits within each word from 1 to 0 in at least two separate programming operations.

Programming and erase times must have fixed upper limits.

It must be bottom boot or uniform sector.

It must have independently erasable sectors with at least the following

boundaries.

SST39WF800A-90-4C-C2KE Nor Flash

P/N code explanation:

39=Multi-Purpose Flash

W=1.65-1.95V

800=8M bit

90=90ns

4=10,000 cycles

C=Commercial=0°C to +70°C

C2=XFLGA (0.5 mm pitch, 5mm X 6mm)

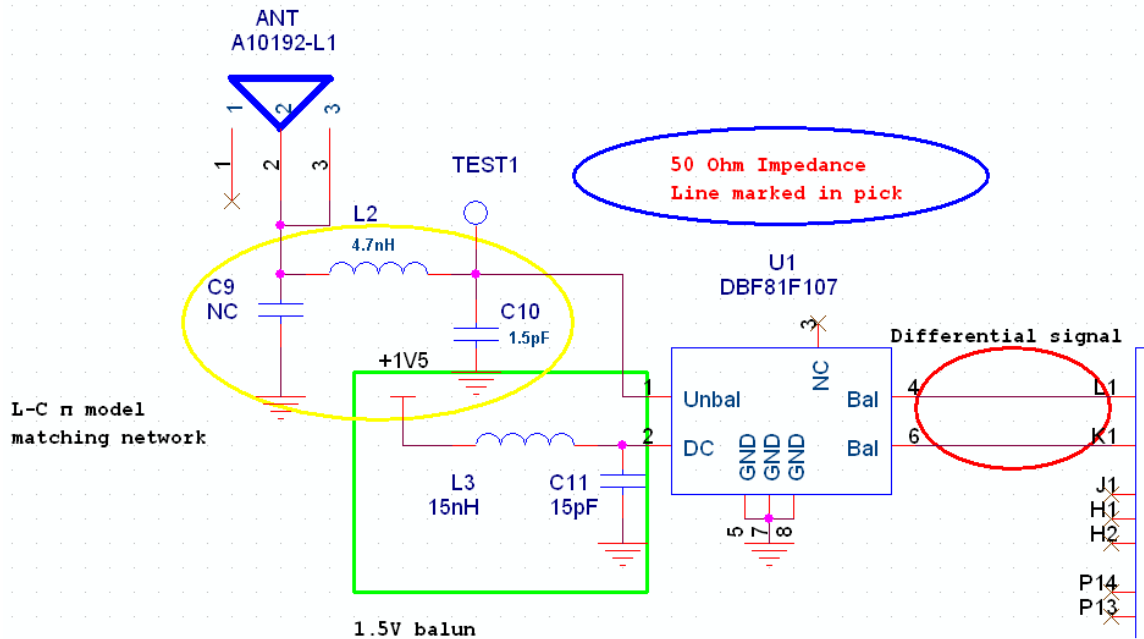
K=48 balls

E=non-Pd

Suitable reason:

1. JEDEC Standard-Flash EEPROM Pin outs and command set.
2. Contain the CFI information to describe the characteristics of the device.
3. Access time 90nS.
4. Bottom boot.
5. Uniform Sector.

2.4 Antenna & RF Circuit



Antenna:

The antenna is Antenova 2.4GHz Chip Antenna.

L-C π model matching network:

We reserved π model matching that's 3 0402 components to fine to antenna matching.

Balun filter:

The balun converts the differential signal into a single –ended signal, which includes a band pass filter then into matching network and antenna.

The balun must provides enough cancellation of common mode distortion products to prevent these components from degrading signal modulation quality and spurious and harmonic filtering for the transit signal and

interferer suppression in the receive path.

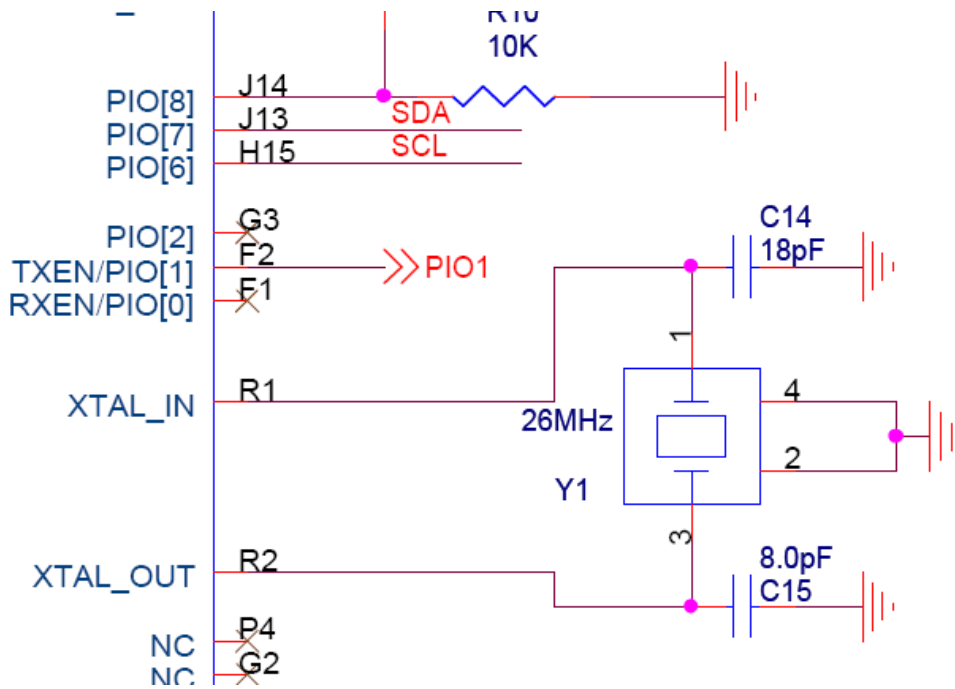
Differential signal RF-P and RF-N:

Make sure these 2 traces identical length and parallel on the board.

1.5V balun supply:

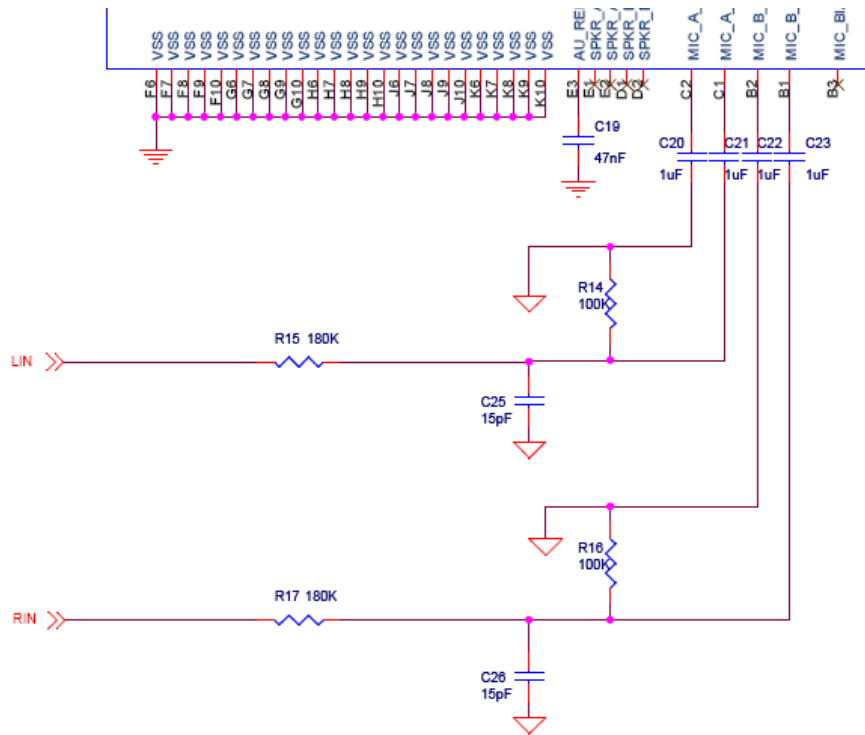
There is a L-C low pass filter, and its components and trace should be away from RF trace on the PCB board.

2.5 Crystal 26MHz



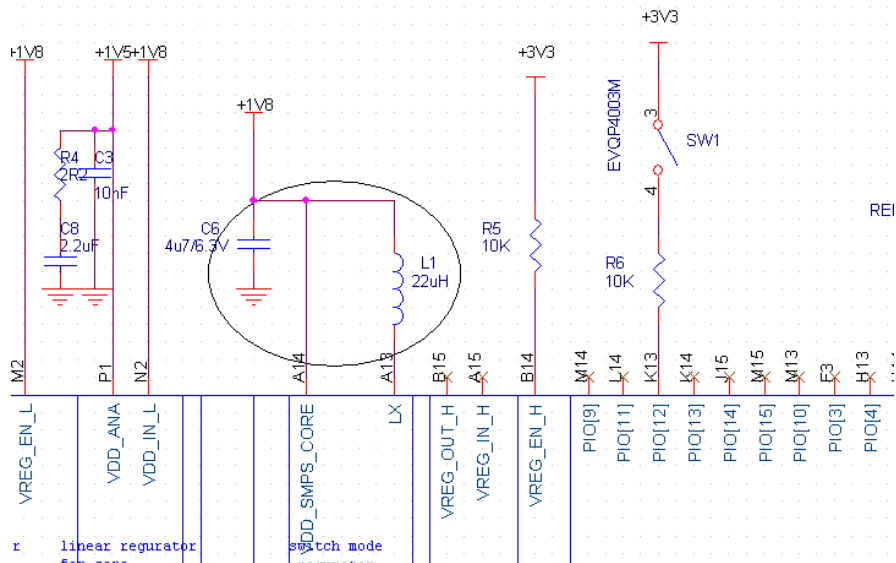
Crystal: 26MHz, 3225 package, frequency tolerance is $\pm 10\text{ppm}$, and tune C14 & C15 for frequency accuracy.

2.6 Audio input:



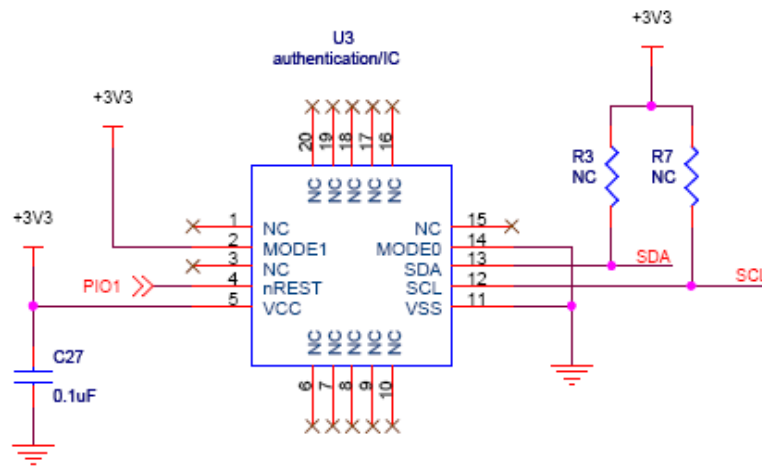
Analog audio input from the iPod, and the audio output of iPod is fixed, it can be changed the value of the audio output by change impedance of resistors. We can match the ratio of R15 and R14 (the other channel can match R17 and R16), and also work with SW to change gain of internal audio amplifier, so we can do the audio level as the standard of D650.

2.7 Inductor



This inductor need 22uH, rated current more than 185mA, this inductor and the near capacitor must be clear to the BGA pads when layout.

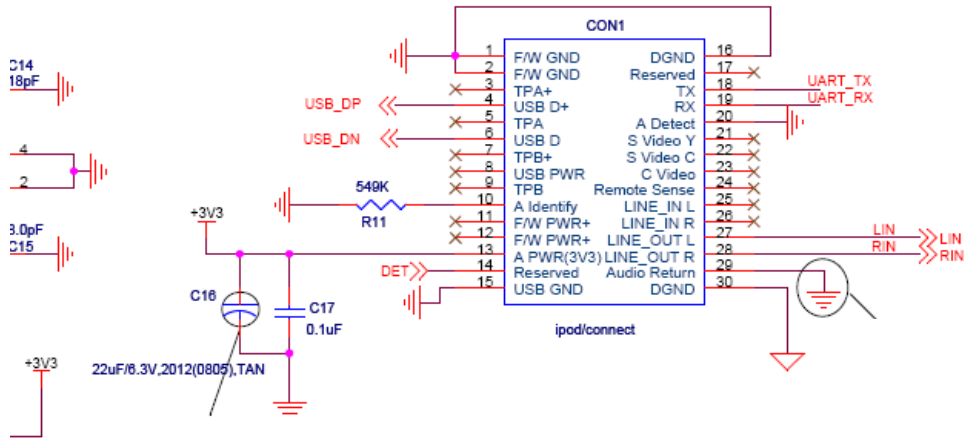
2.8 Authentication IC



Authentication IC communicate with BC05 by I2C bus.

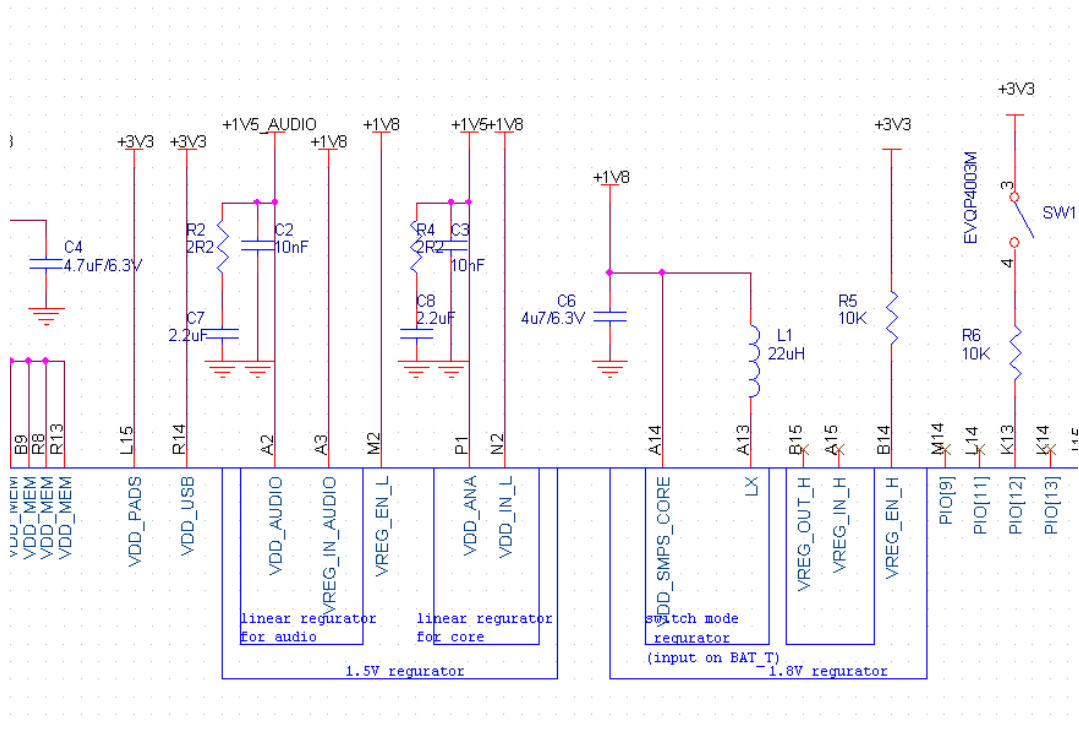
First, Authentication IC send certified information to iPod, then iPod return information to Authentication IC, communicate with each other and then the certified is will be ok.

2.9 UATR port



Adapter communicate with iPod by UART port, iPod can be control by headset, the music volume, music up and down are controlled by headset, so the AVRCP will be ok.

3.1 The 1.8V and 1.5V regulator



The 1.8V and the 1.5V is the main power of adapter.

When the pin VREG_EN_H is high, 1.8V will be output from the pin VDD_SMPS_CORE, the 1.8V regulator is active now.

When the pin VEE_IN_L and the pin VREG_IN_AUDIO input 1.8V, and the pin VREG_EN_L is high, the two 1.5V regulator is active, and output 1.5V.