

Permanent Confidentiality Requested**Exhibit 5. Schematic Diagrams of the Transmitter Block – 47 CFR 2.1003(c)(10), and RSP100, Section 5.**

The transmitter schematics below illustrate the circuitry for frequency generation, determination, and stabilization, as well as modulation limiting, power control, and suppression of spurious emissions. To view text and component values zoom.

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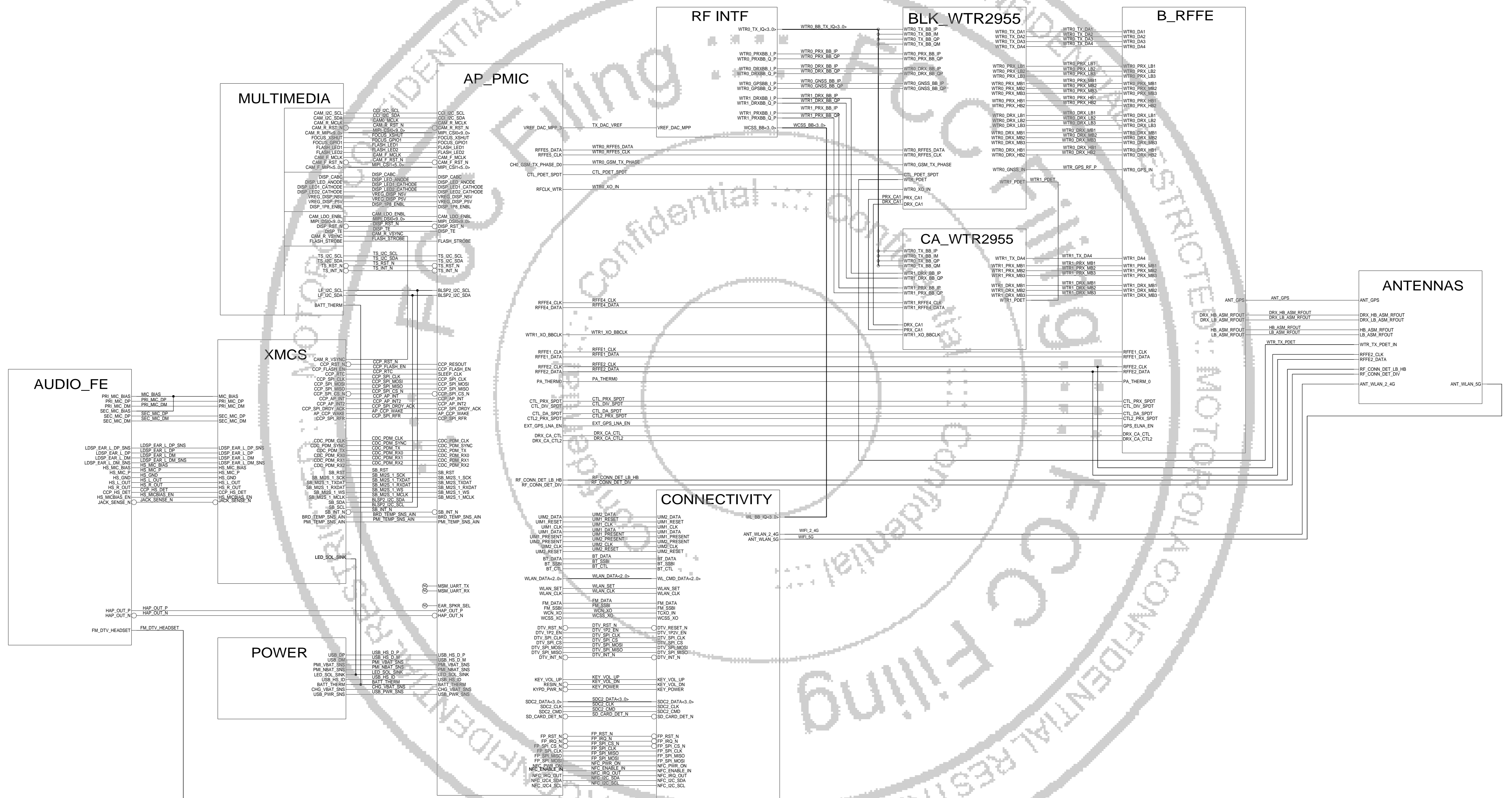
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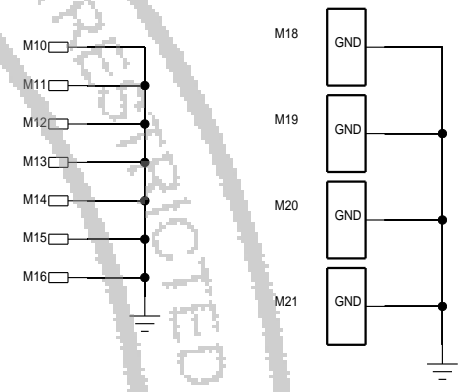
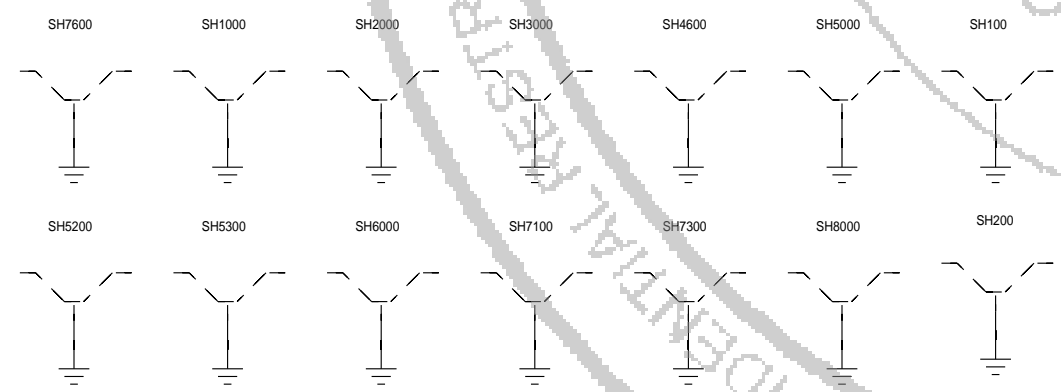
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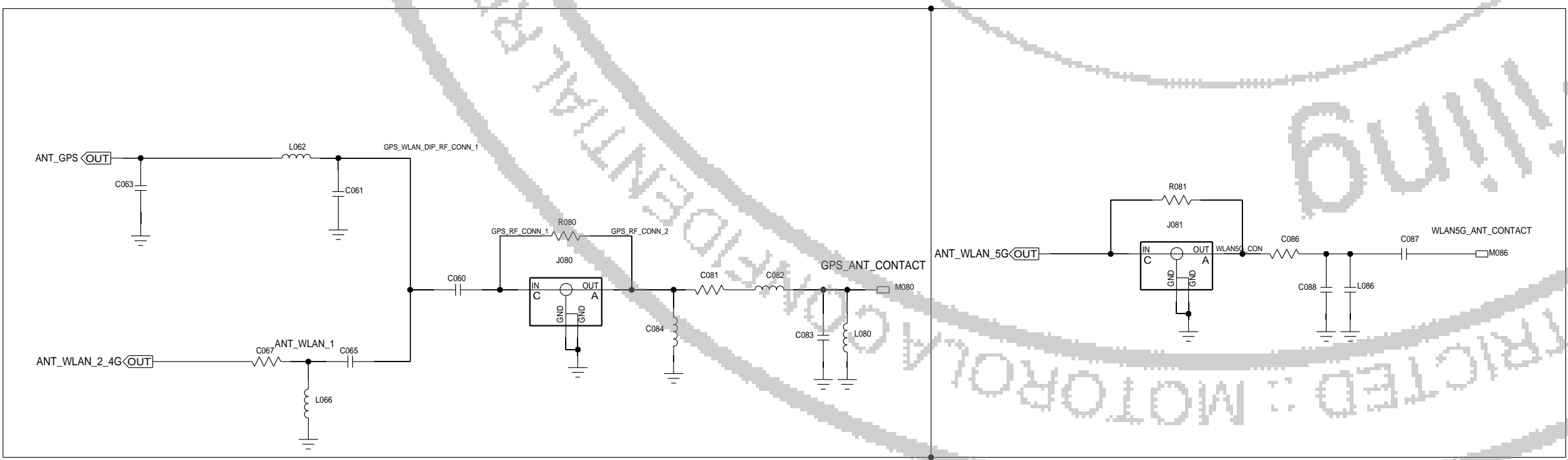
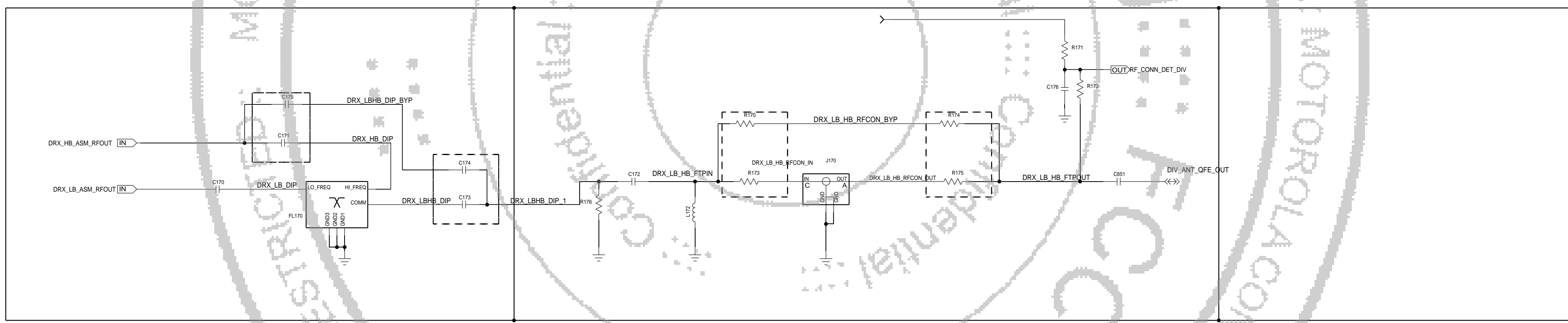
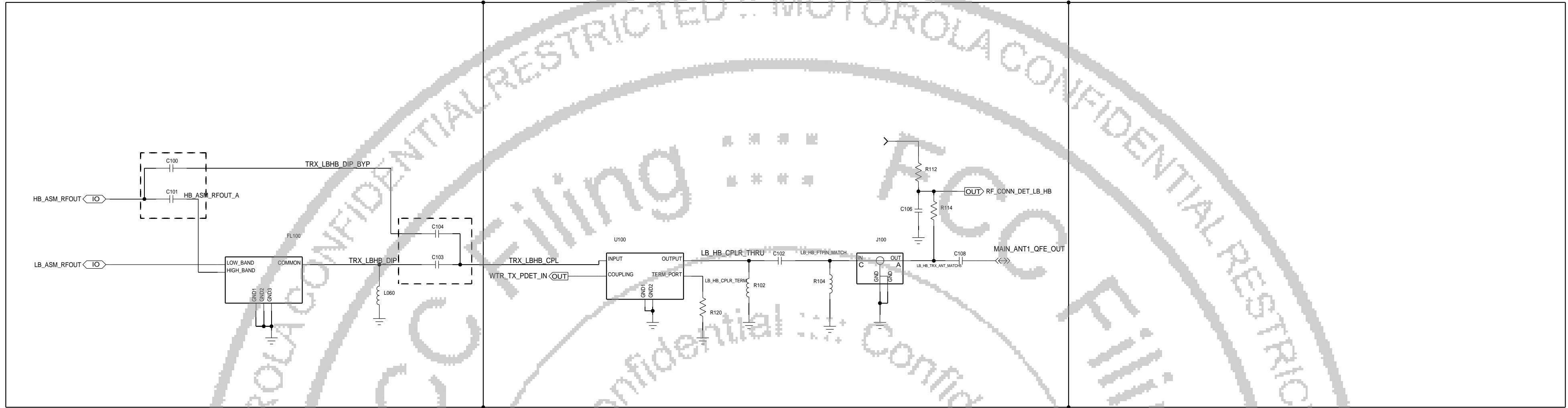


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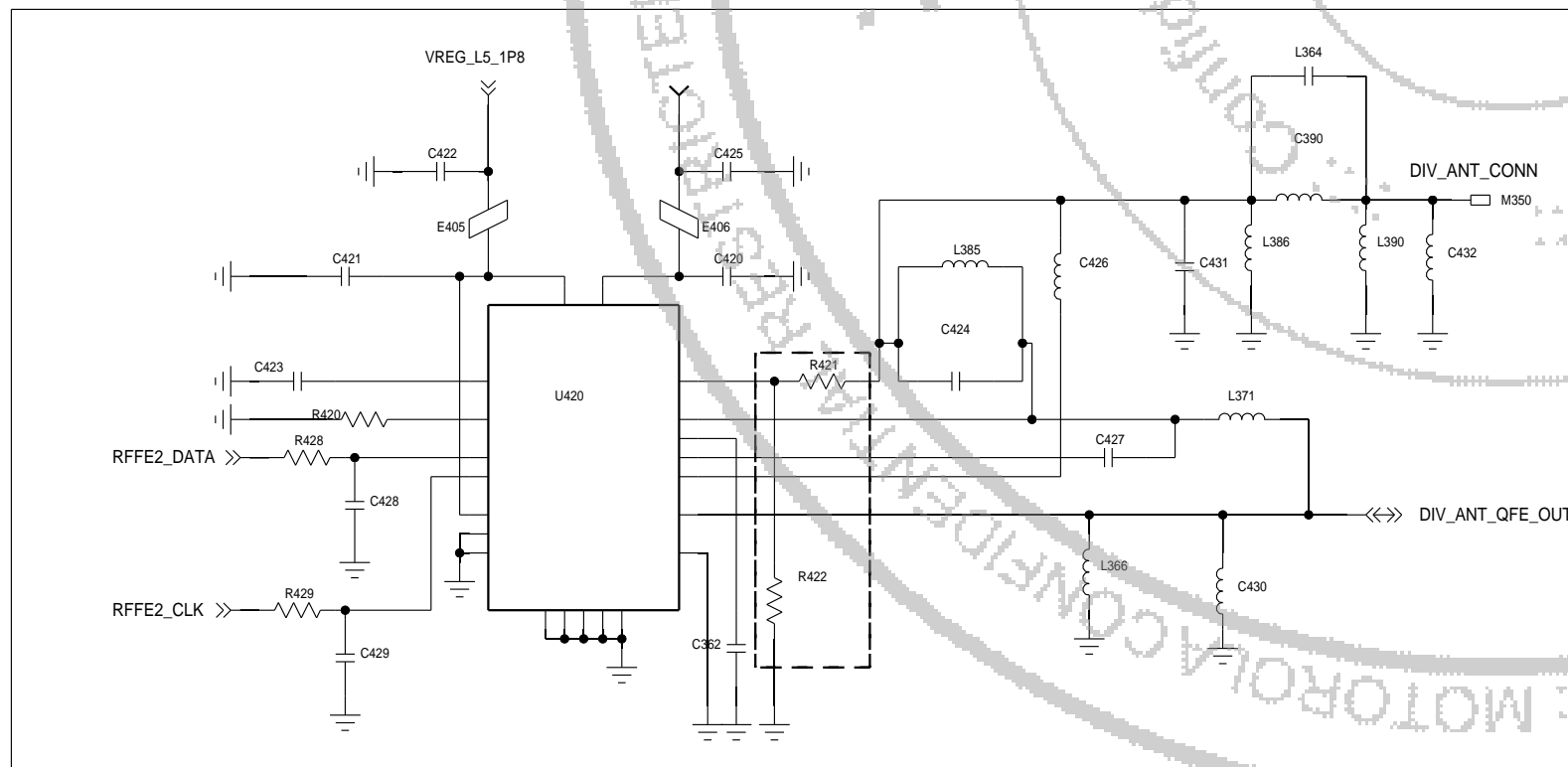
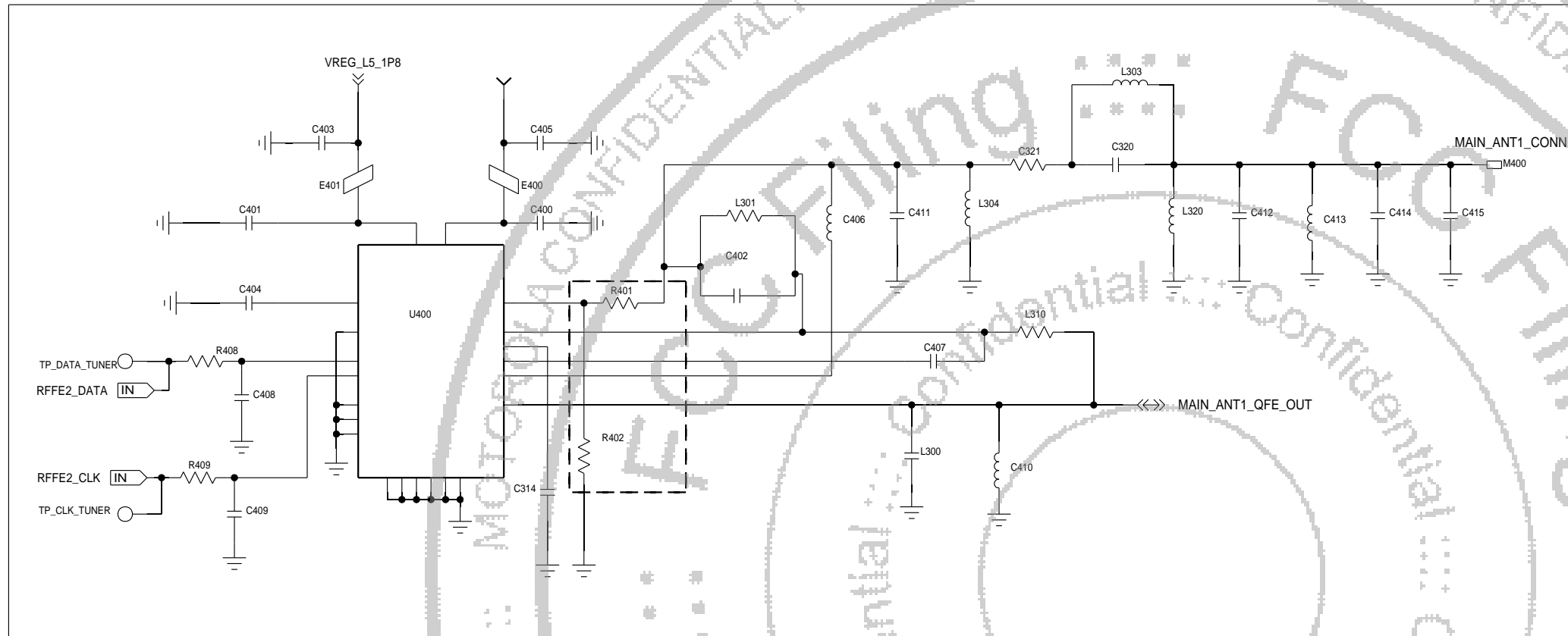
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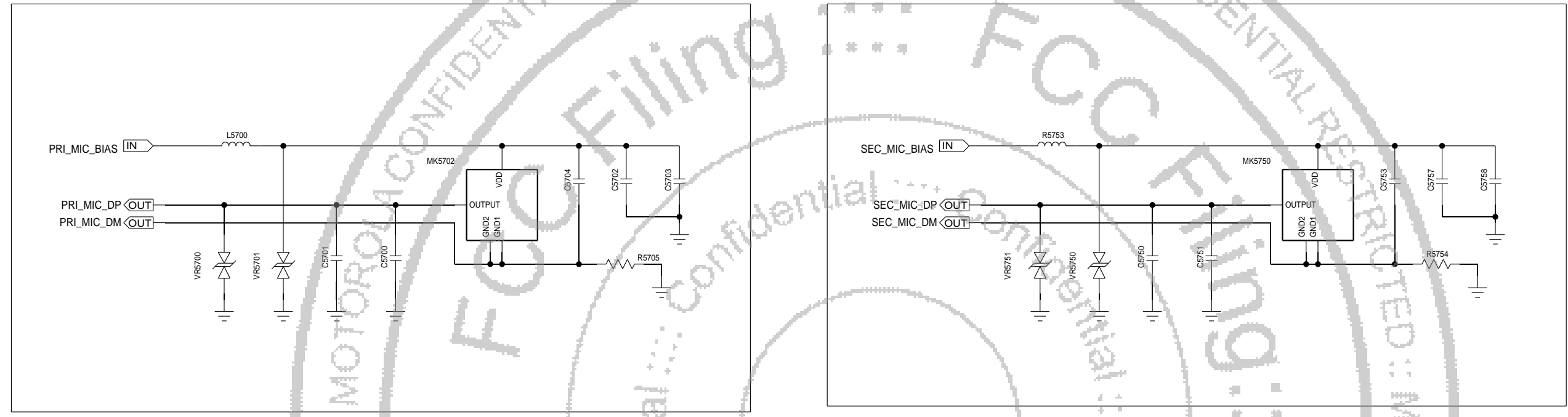
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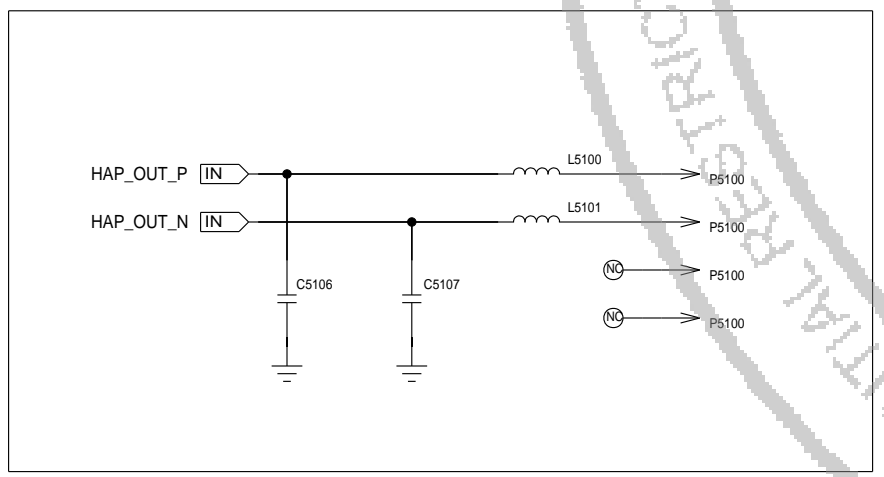
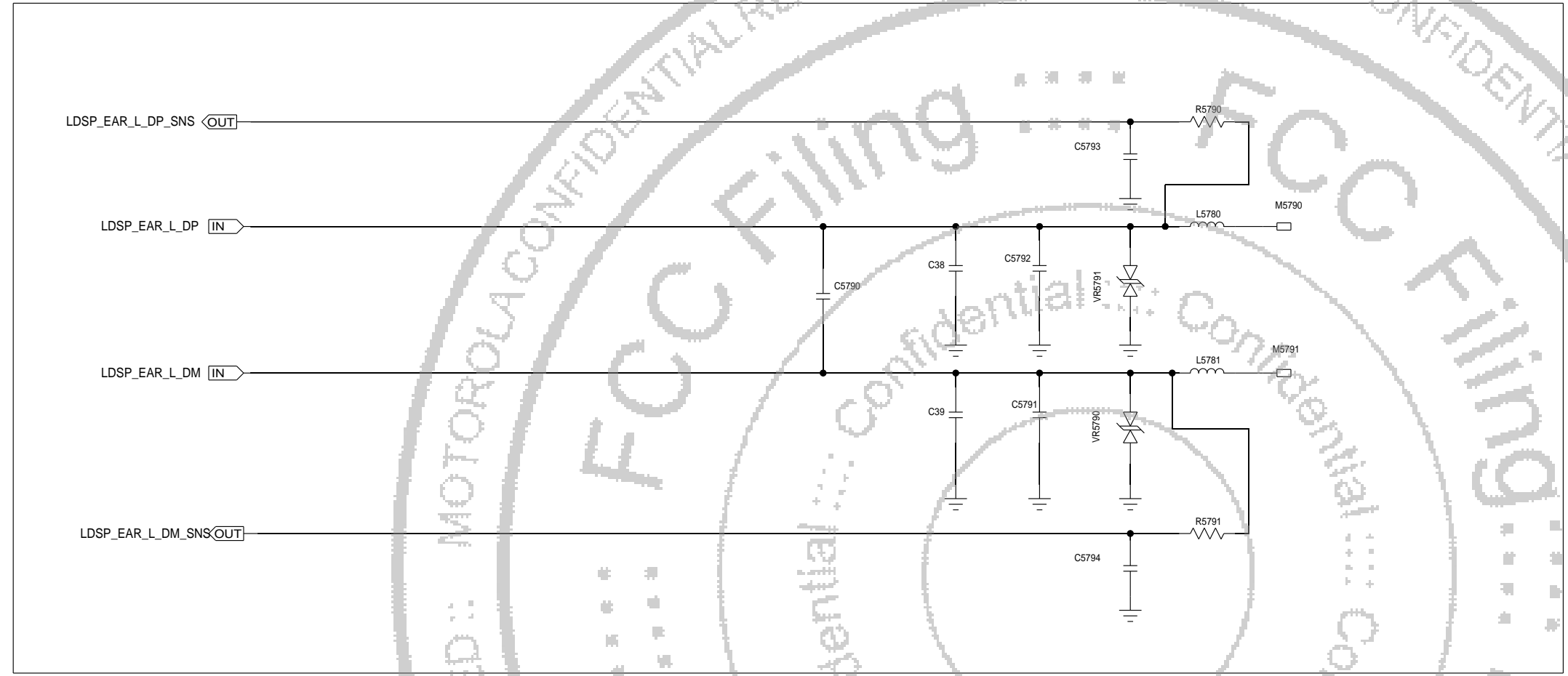
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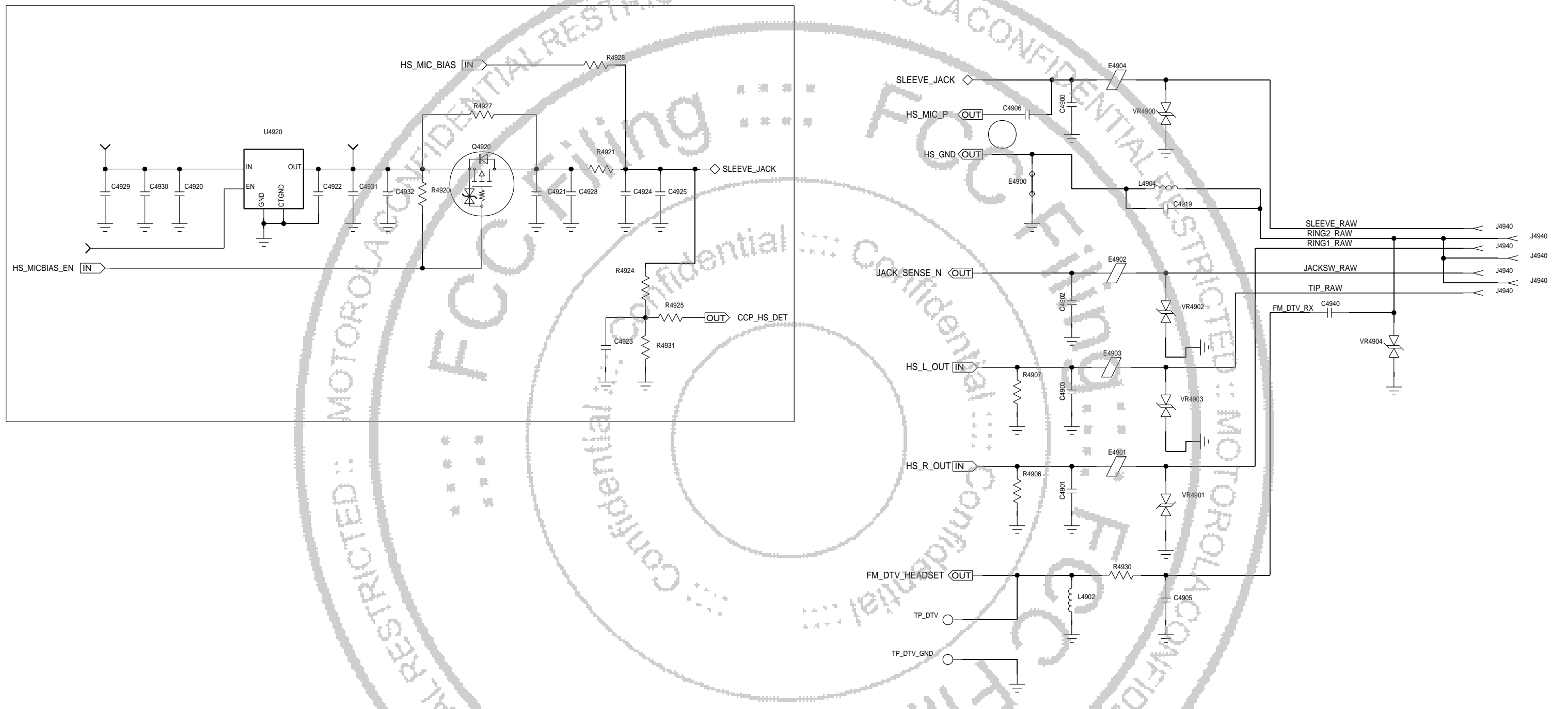


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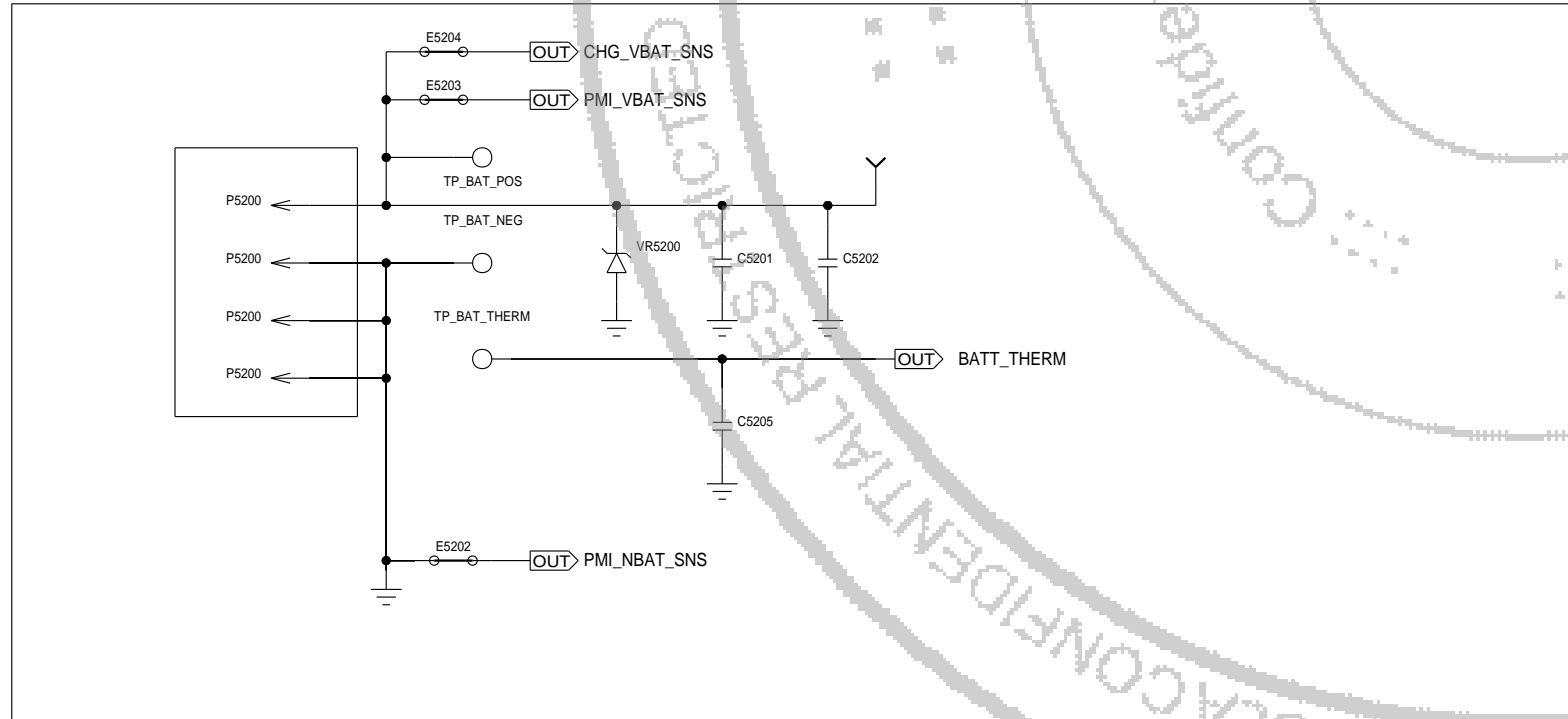
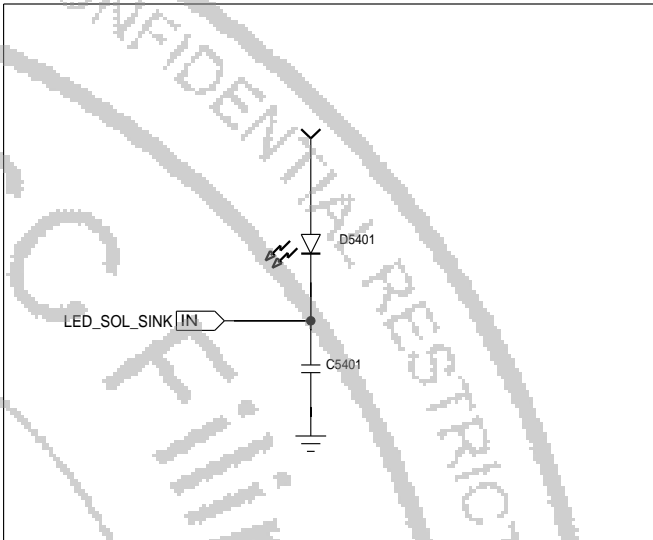
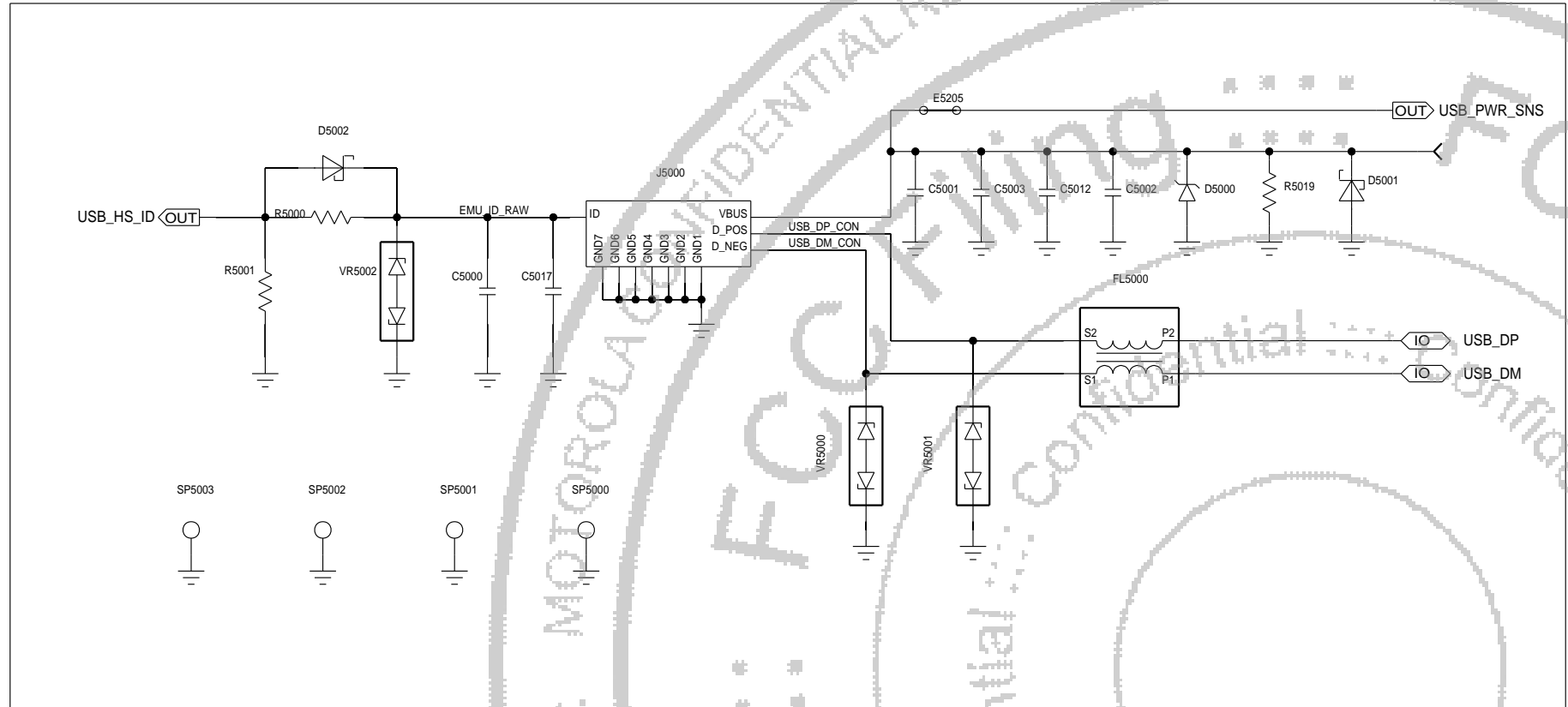
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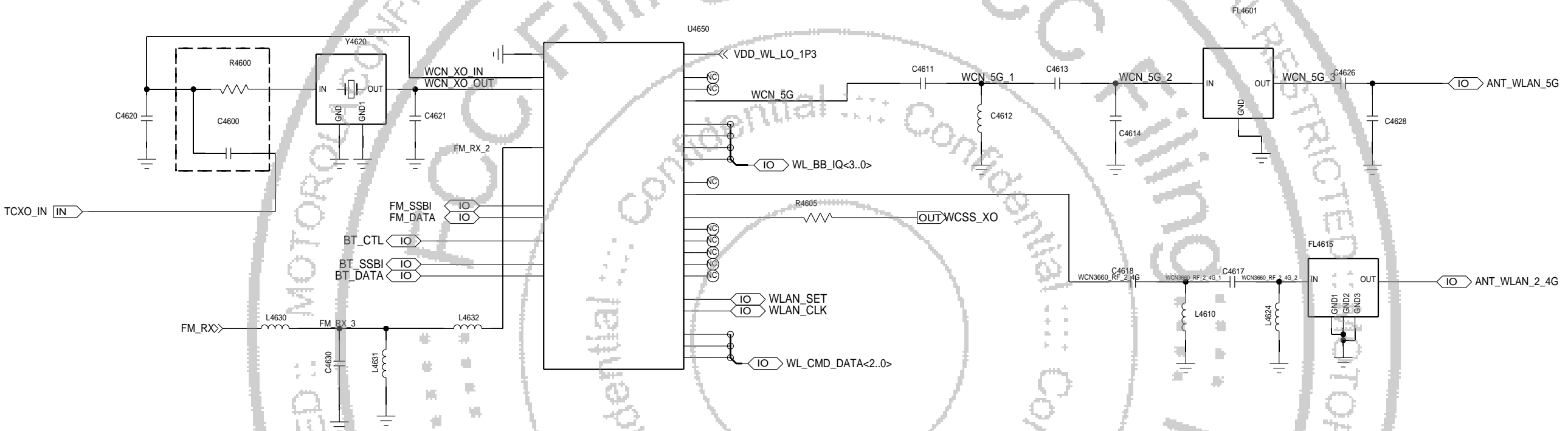
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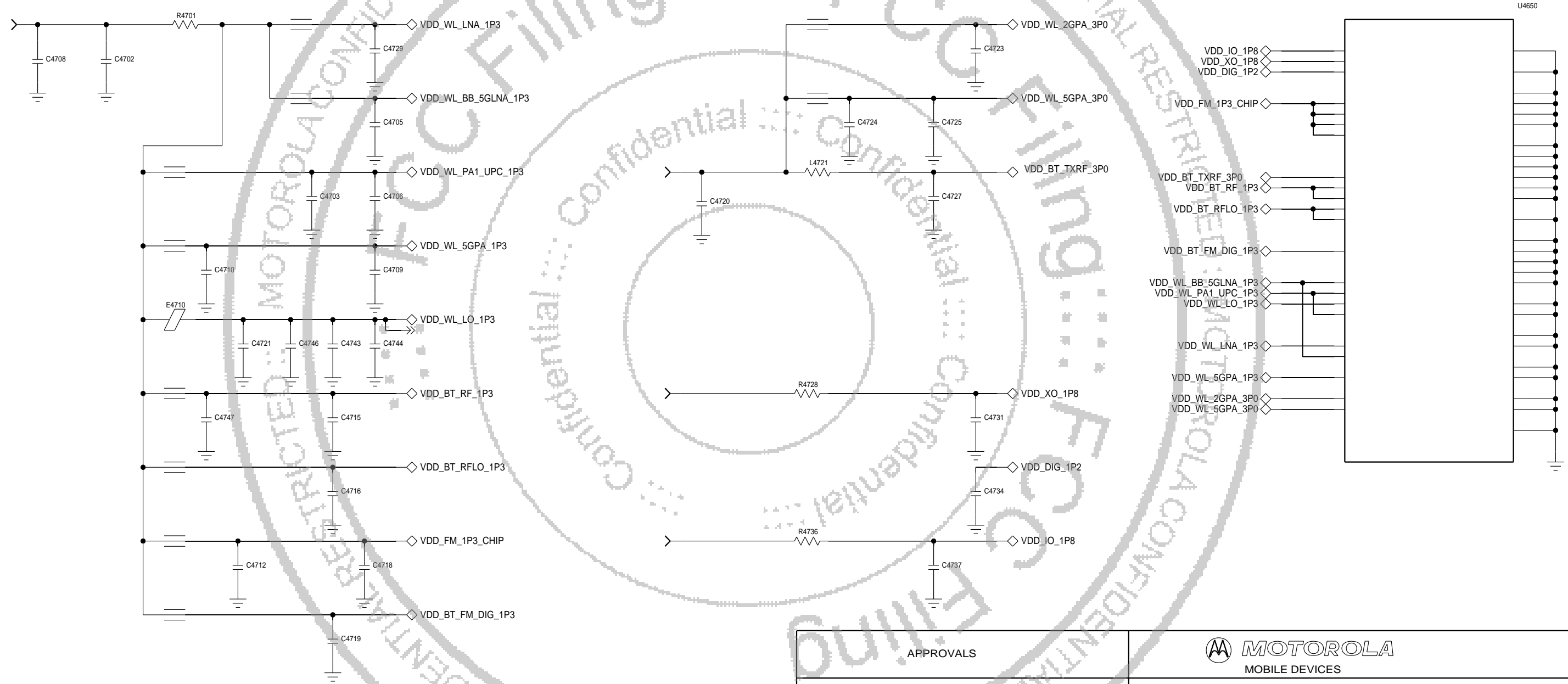
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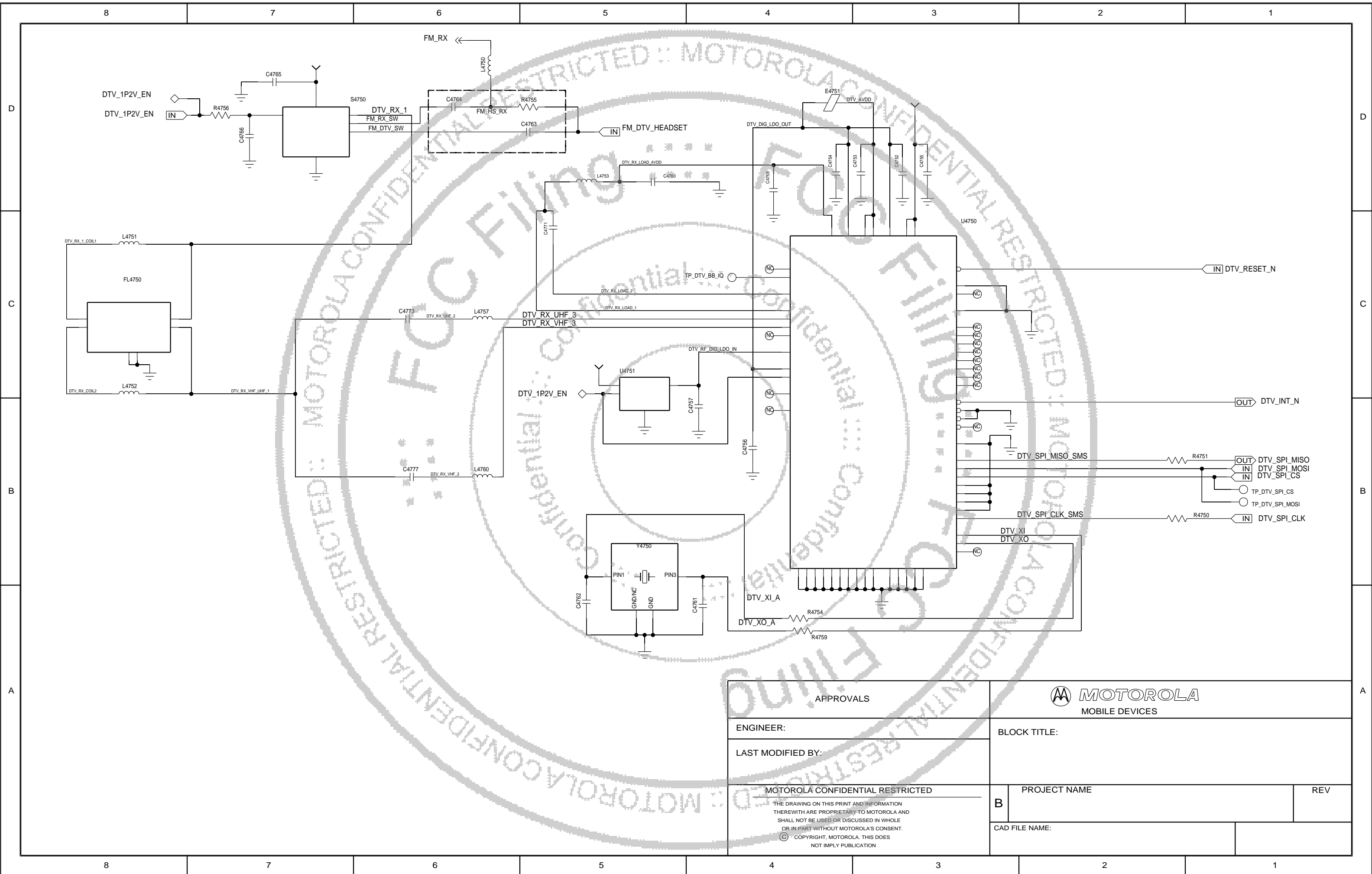
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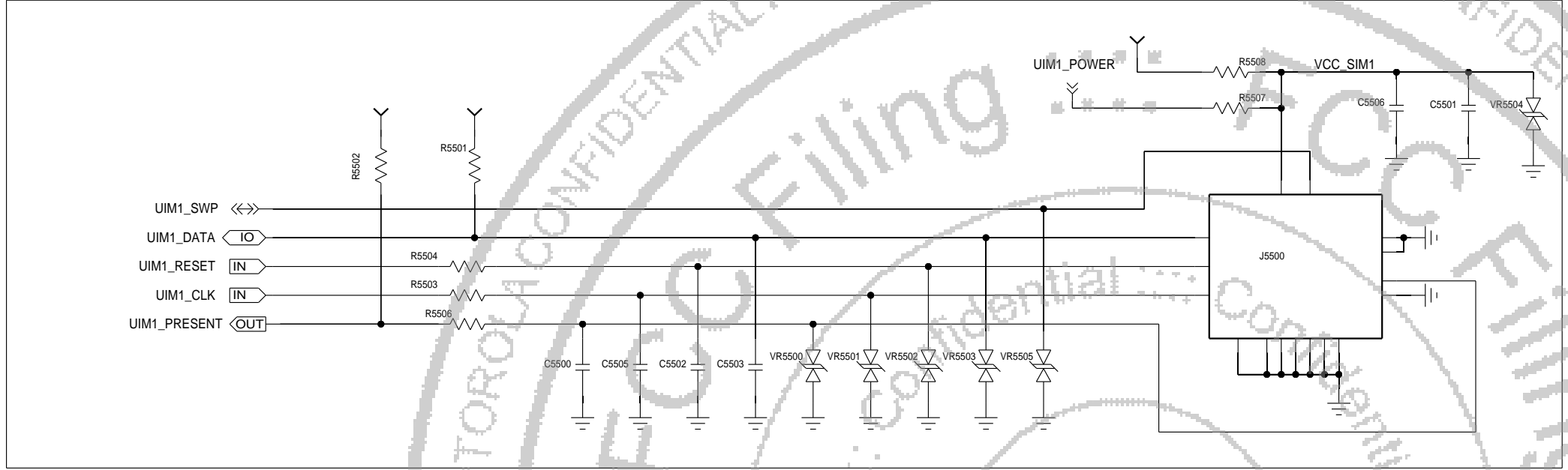
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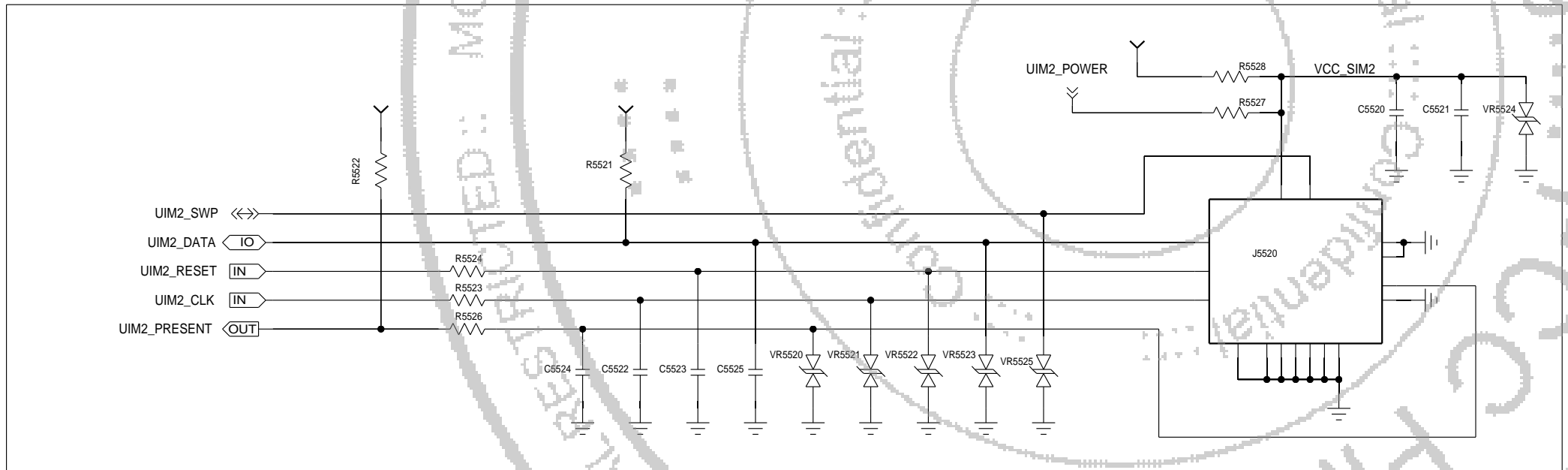


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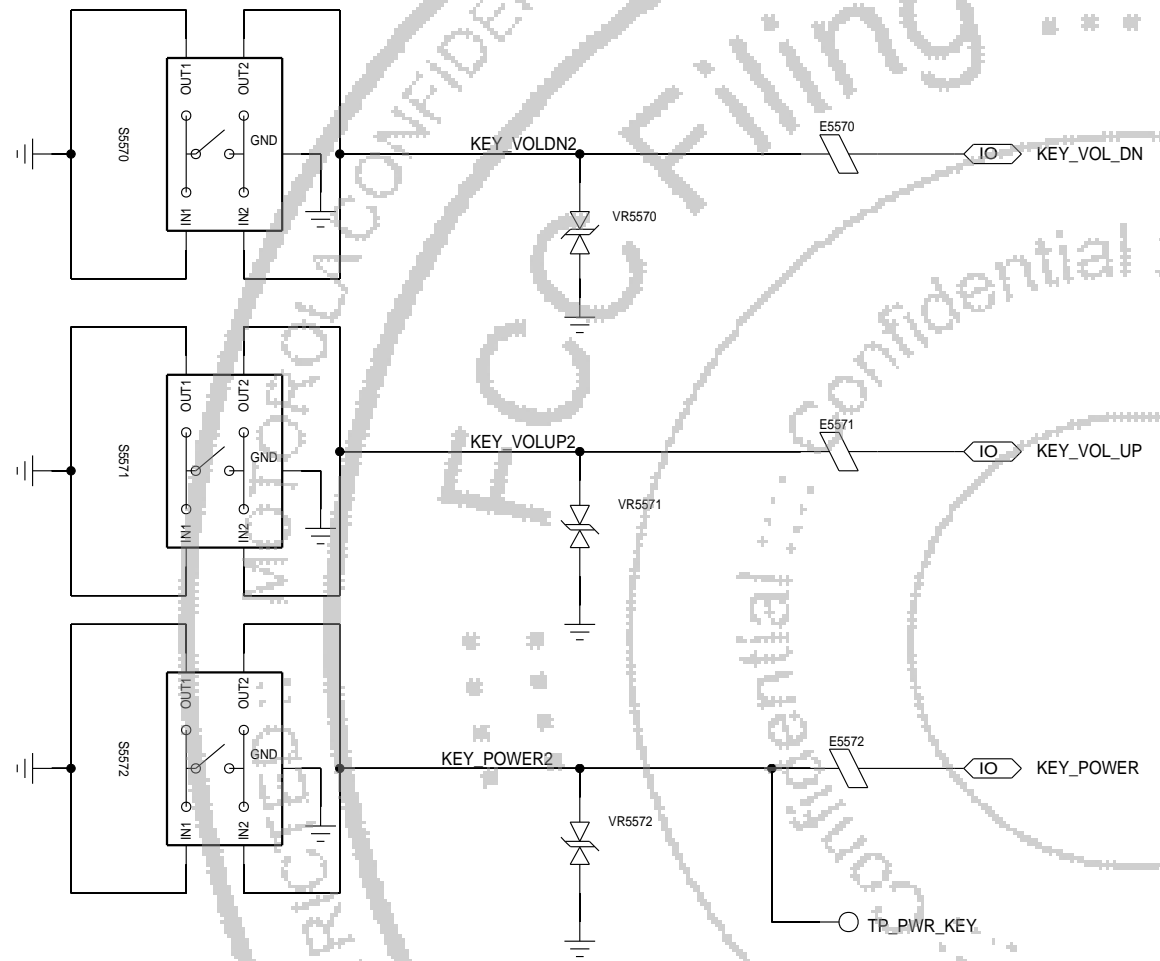
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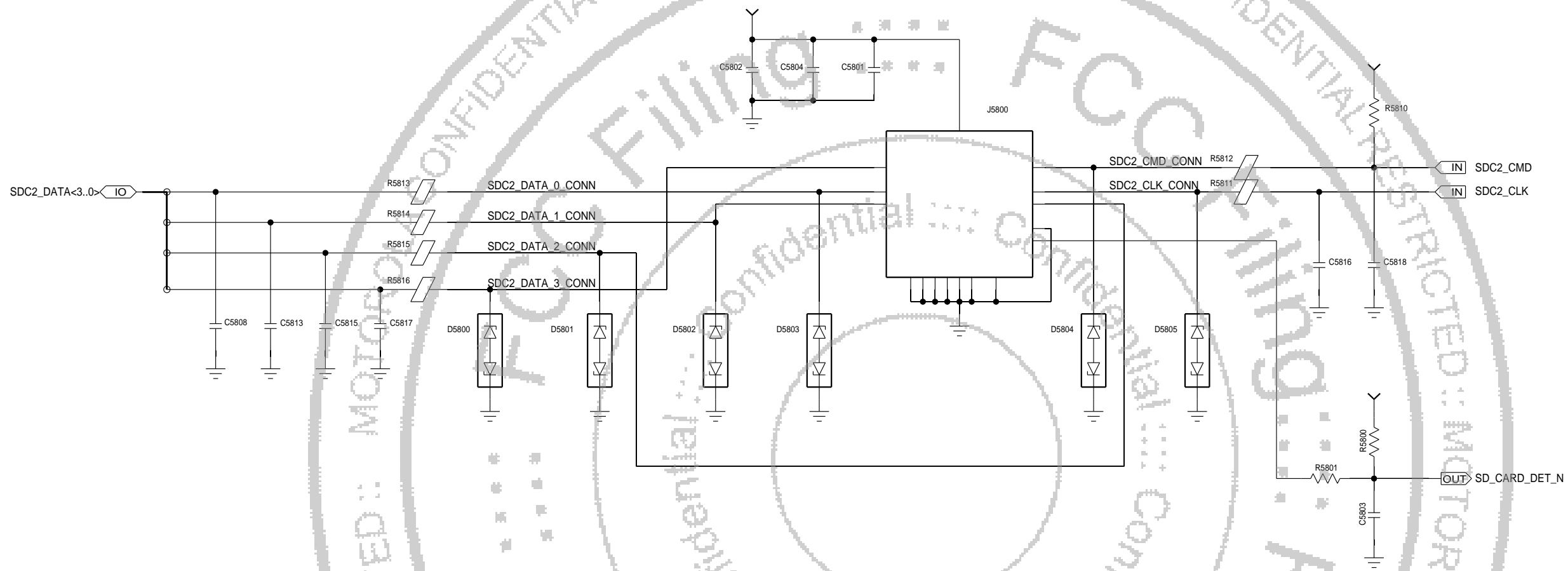
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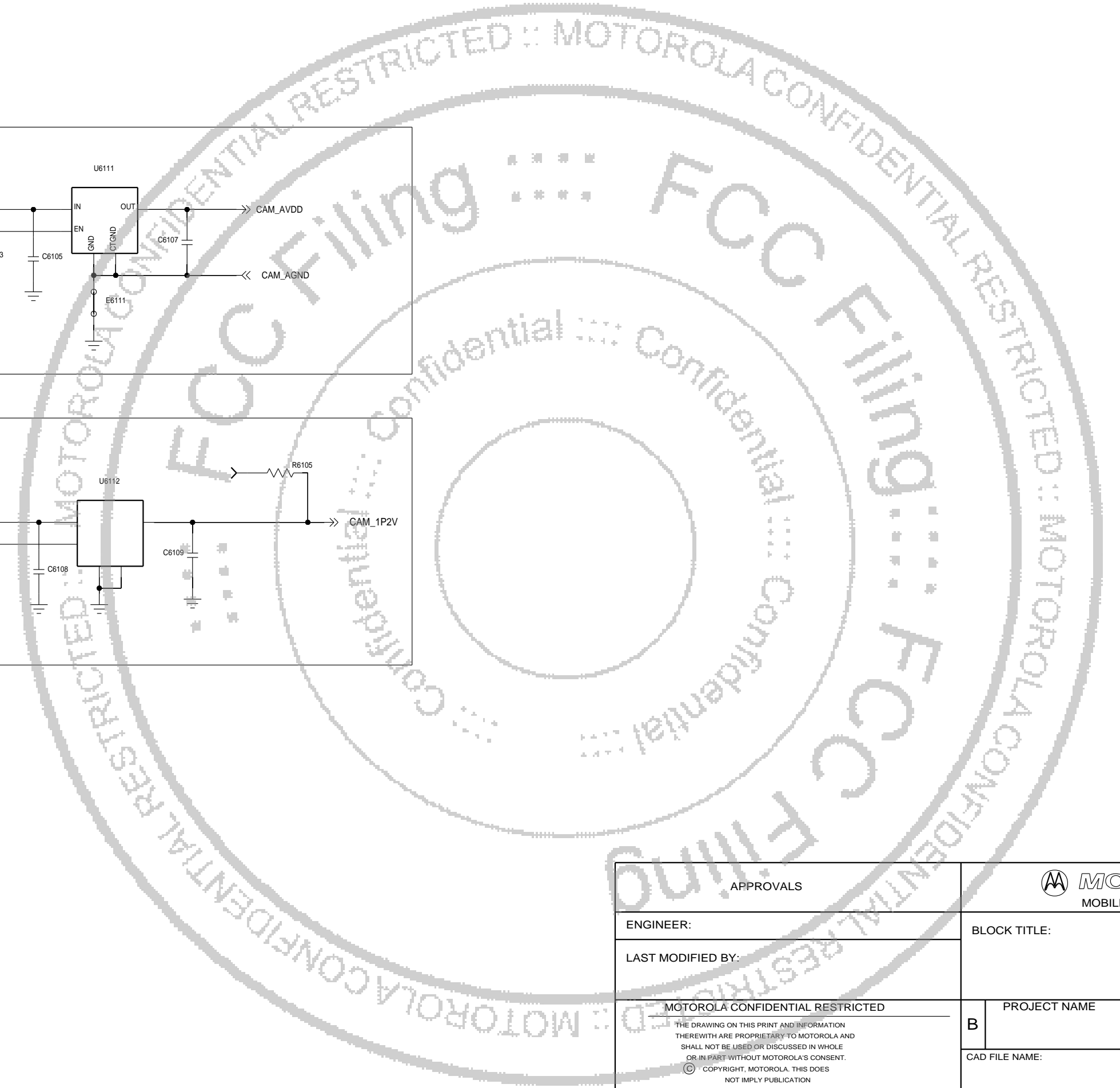
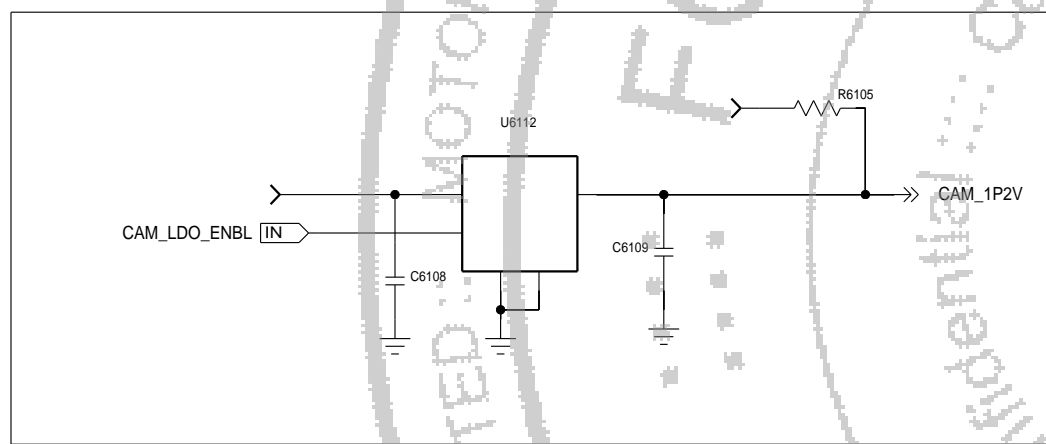
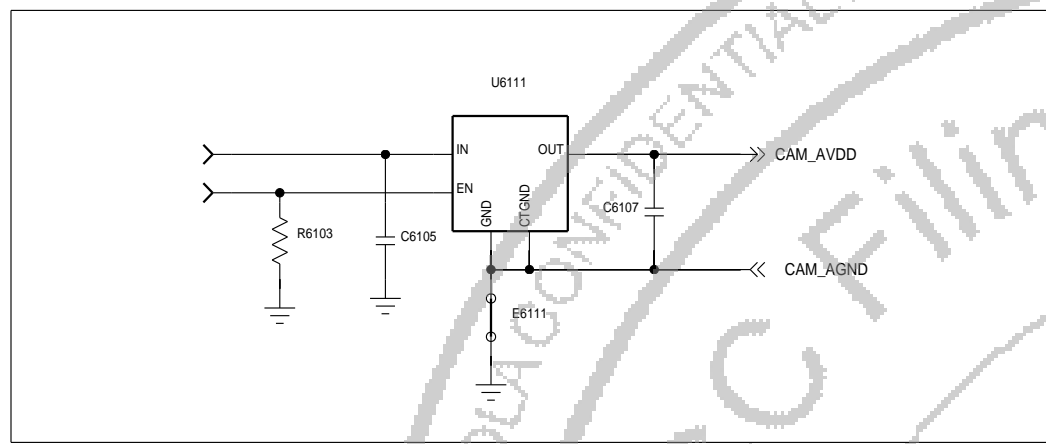
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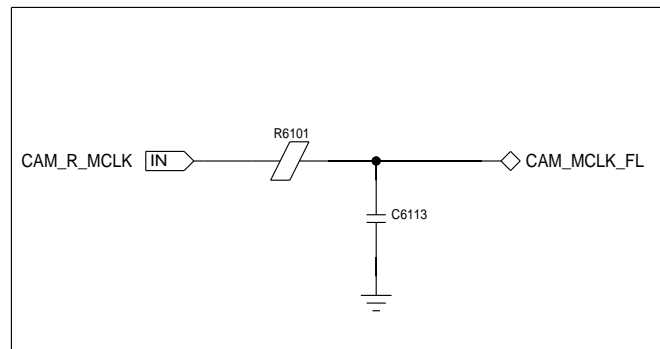
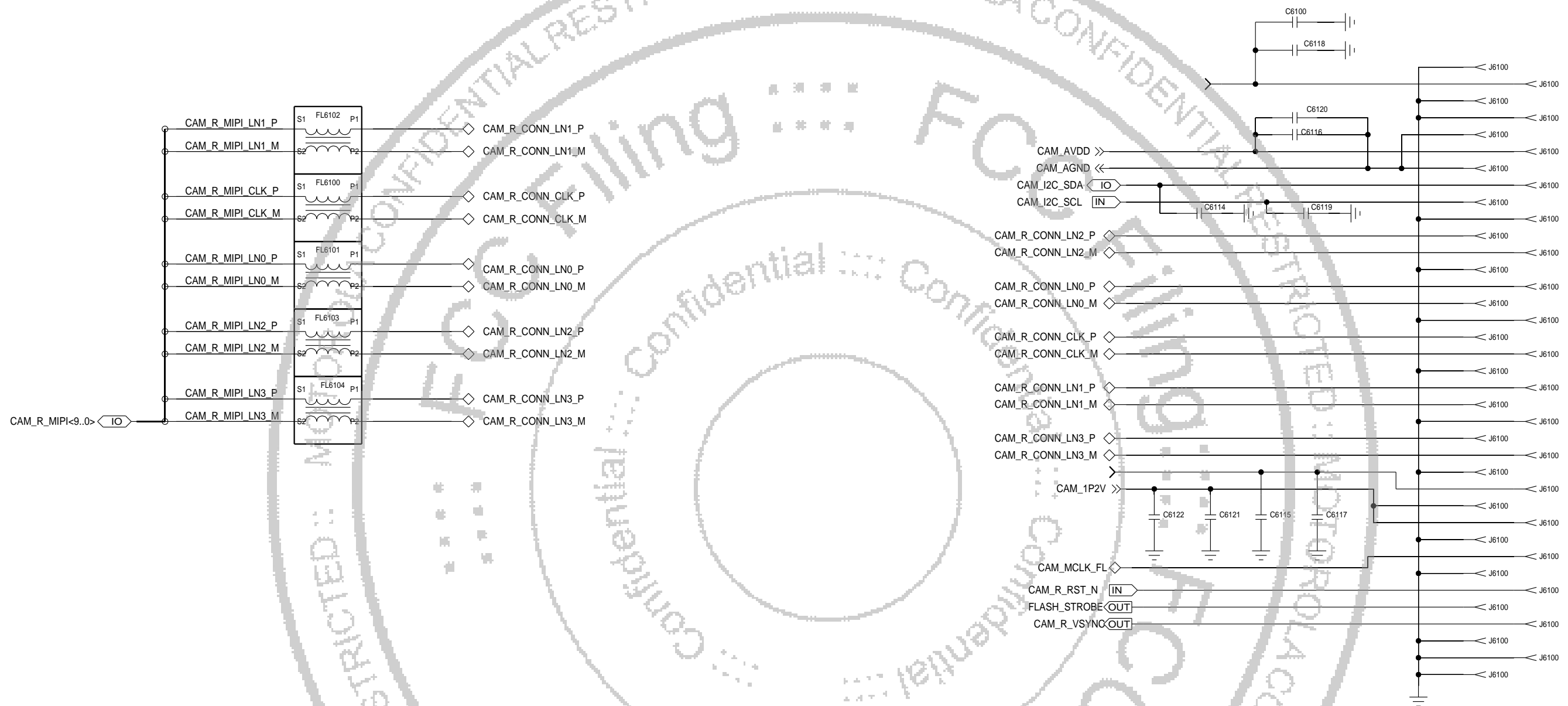
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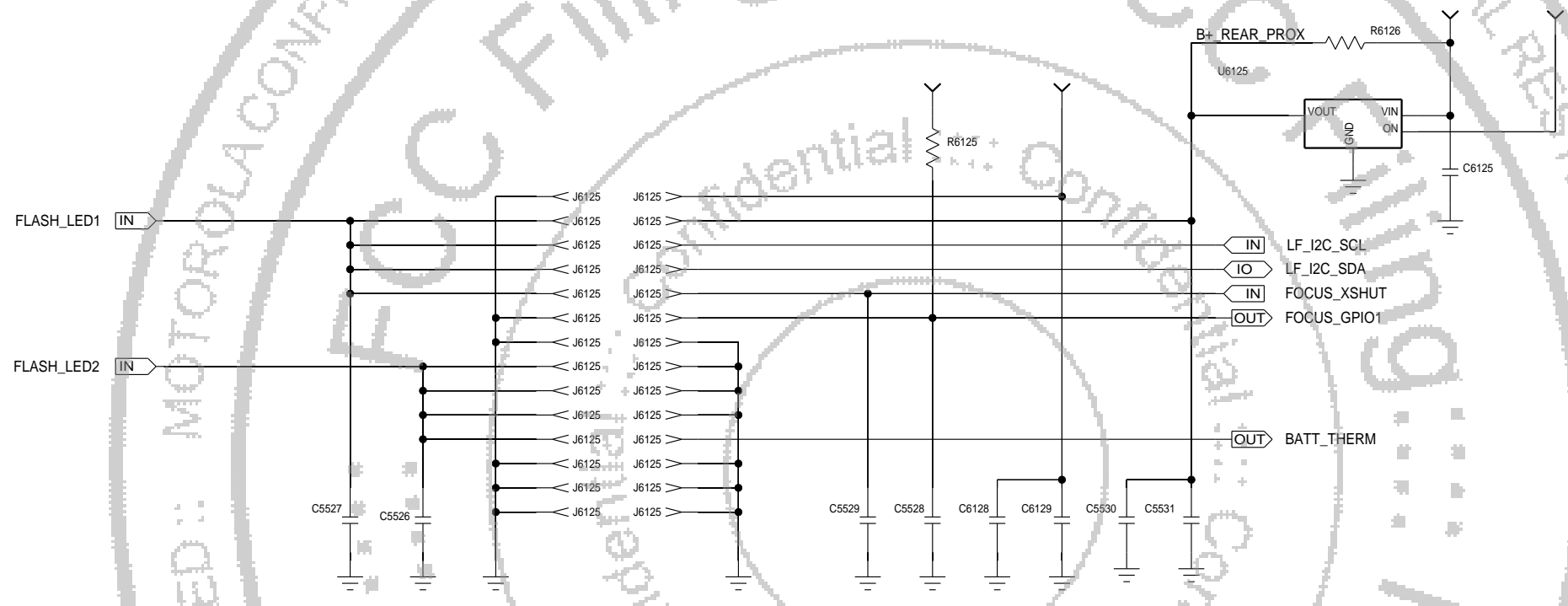
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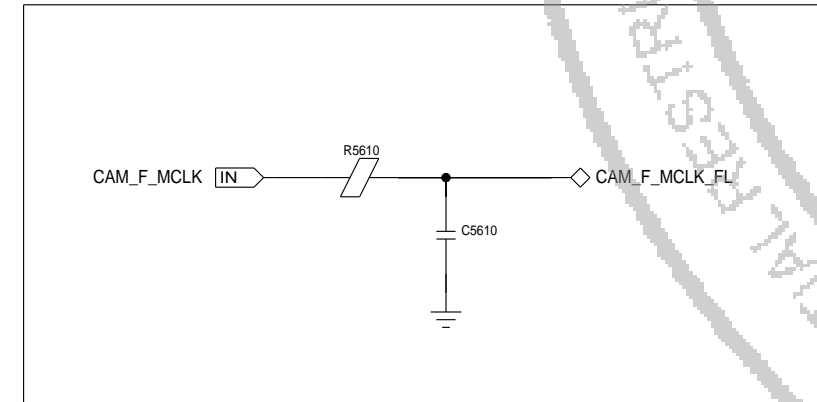
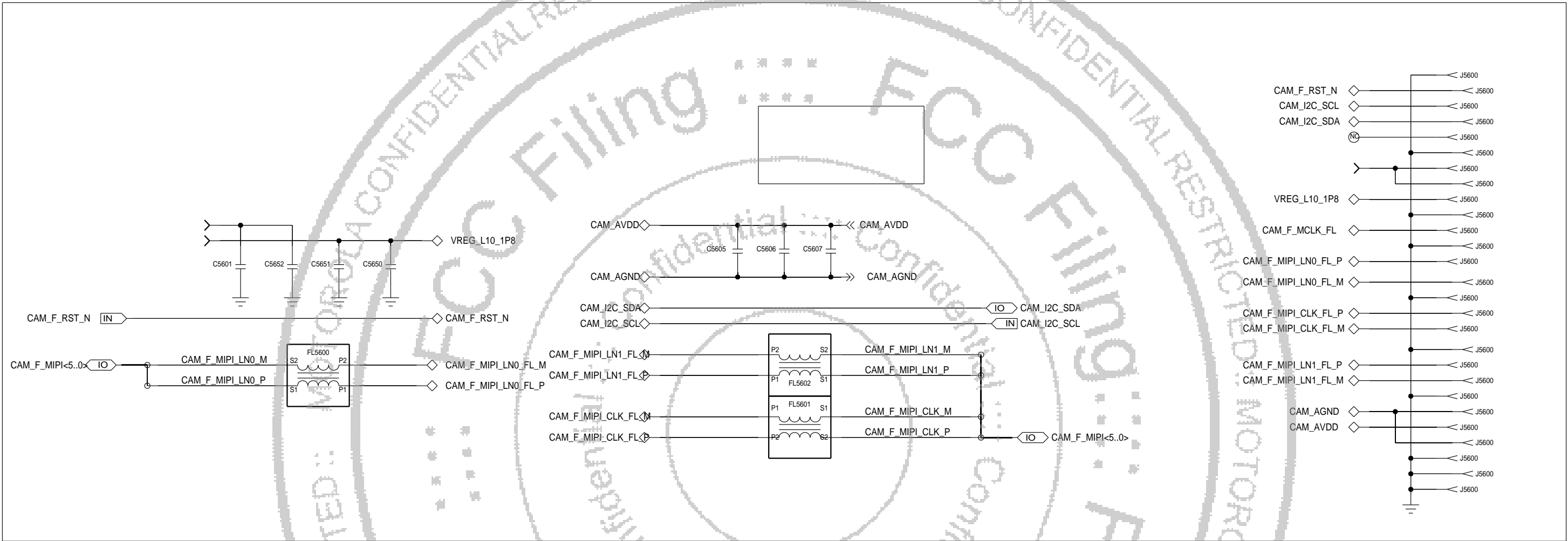
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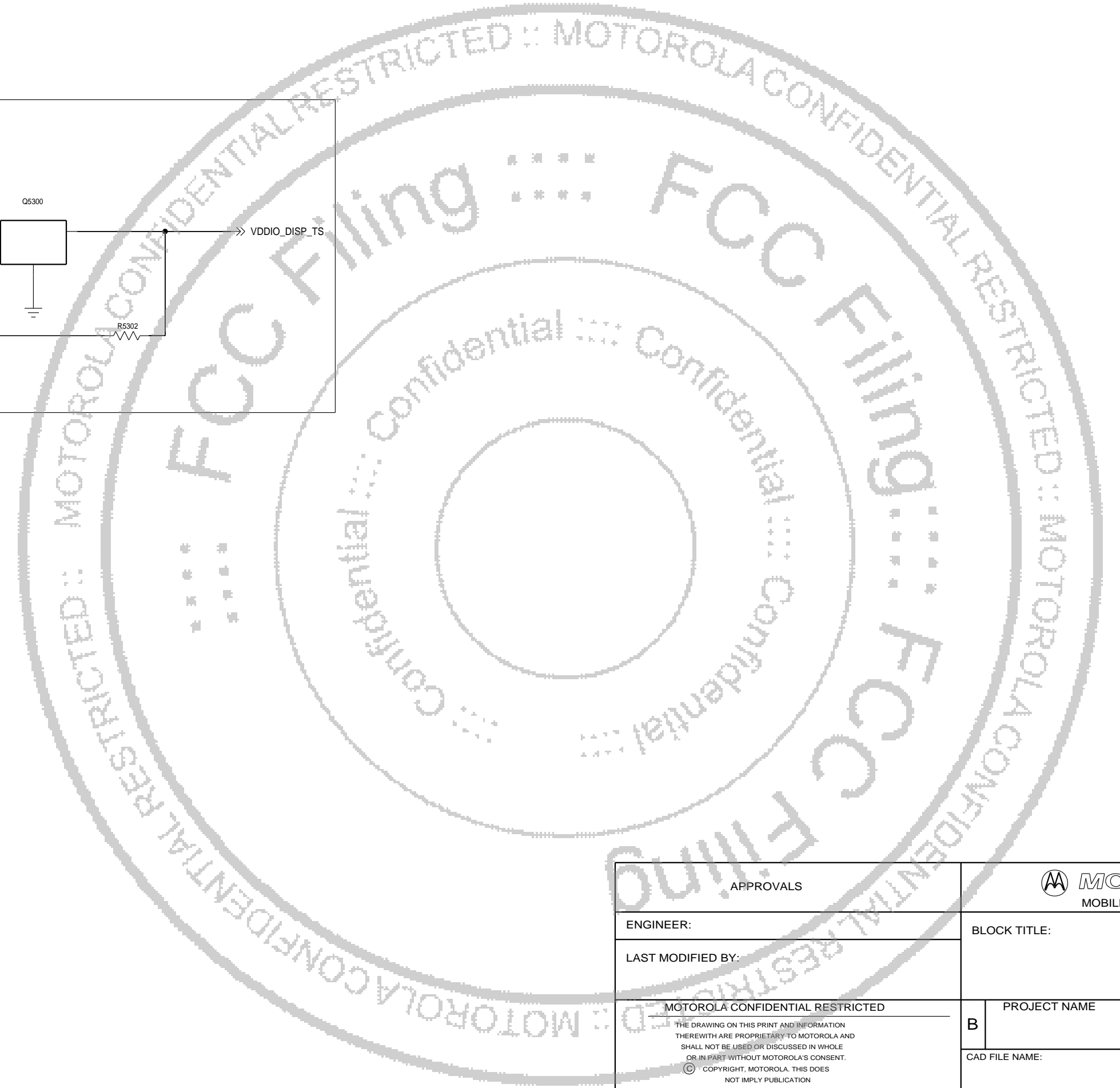
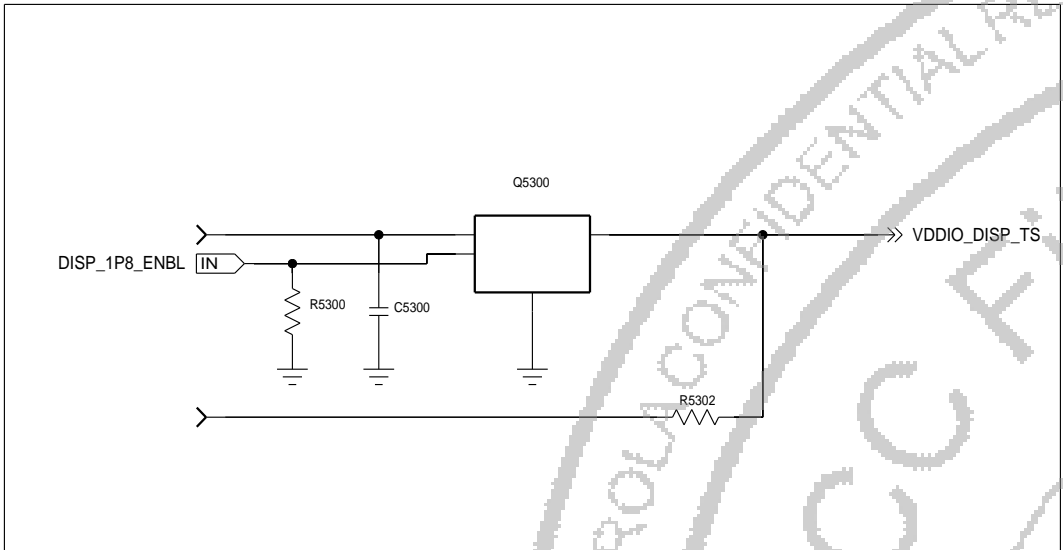



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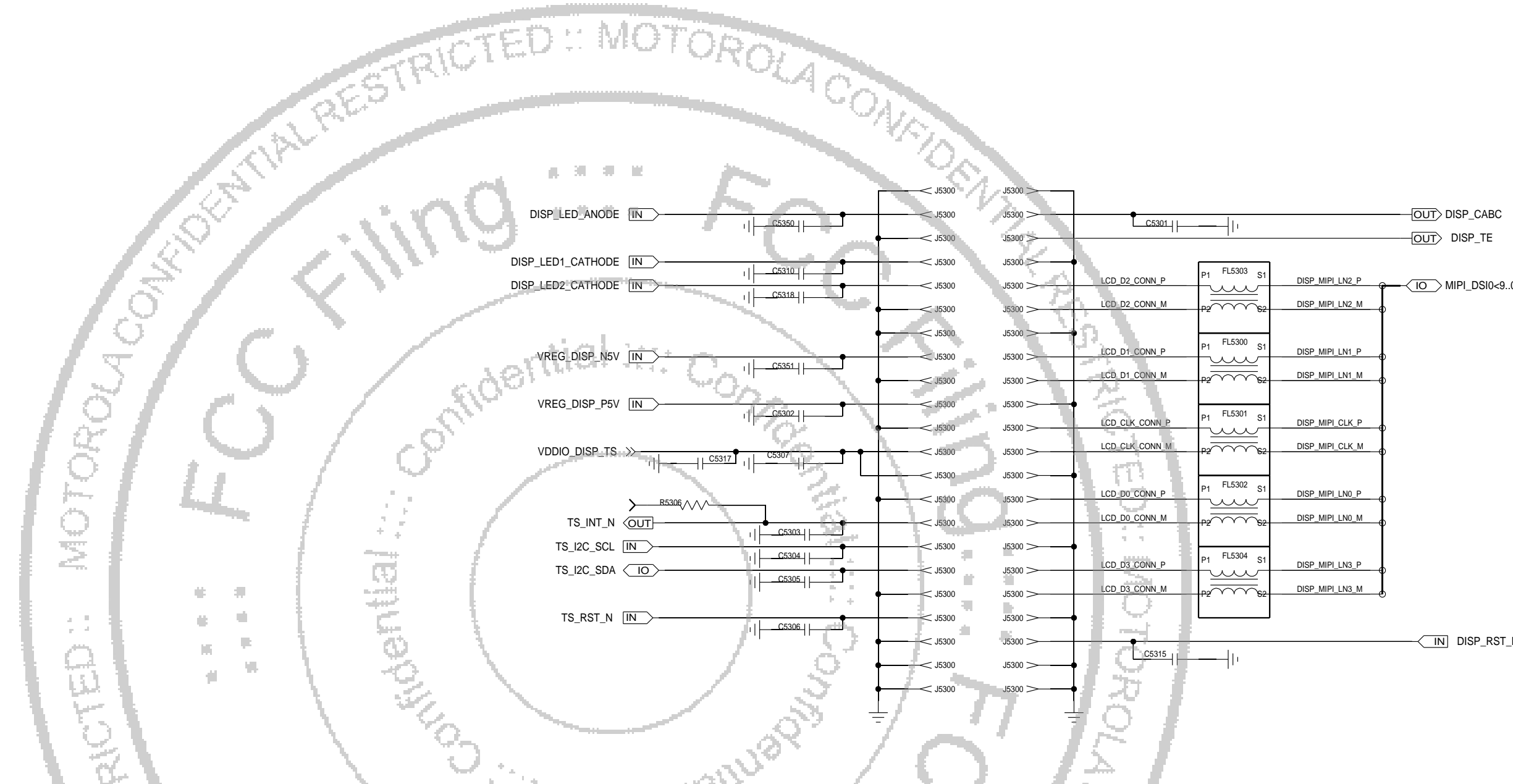
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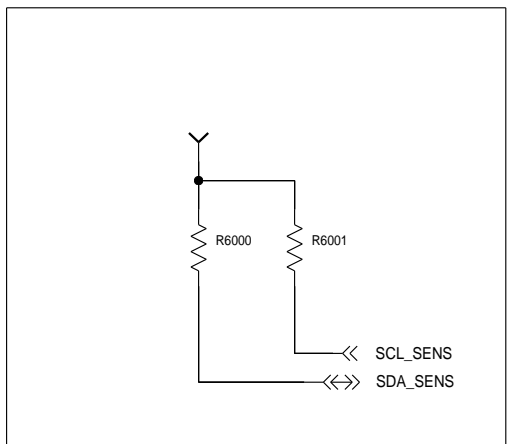
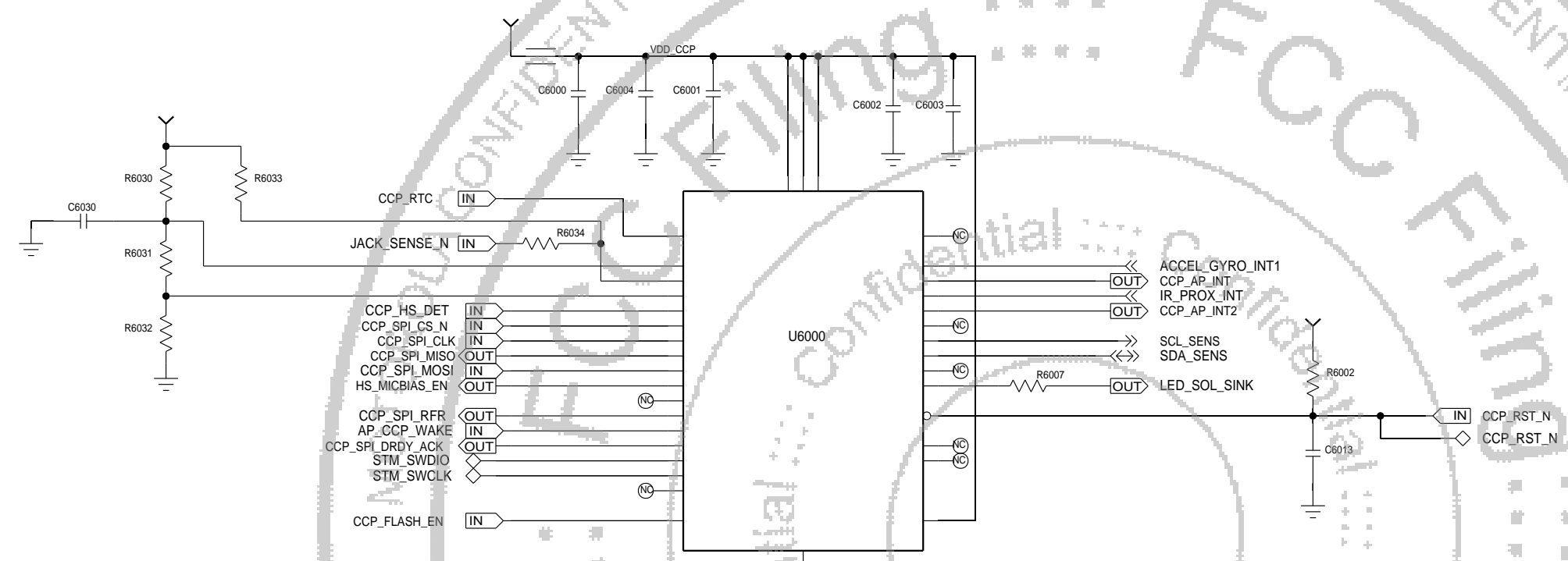
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LCD_D1_CONN_M	R5403	DISP_MIPI_LN1_M
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CCP_FLASH_EN	TP_STM_BOOT0
CCP_AP_INT	TP_CCP_AP_INT
CCP_SPI_CLK	TP_SCK_CCP
CCP_SPI_MOSI	TP_MOSI_CCP
CCP_SPI_MISO	TP_MISO_CCP
CCP_SPI_CS_N	TP_CS_CCP
STM_SWDIO	TP_SWDIO
STM_SWCLK	TP_SWCLK

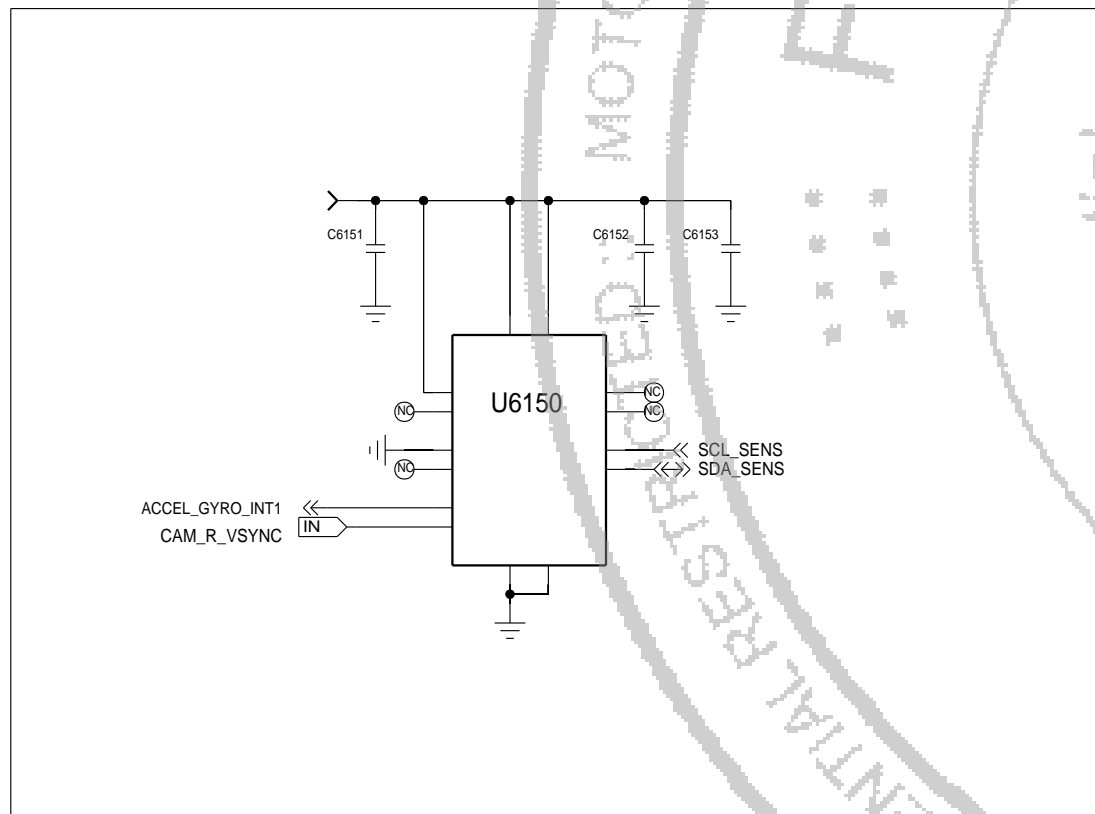
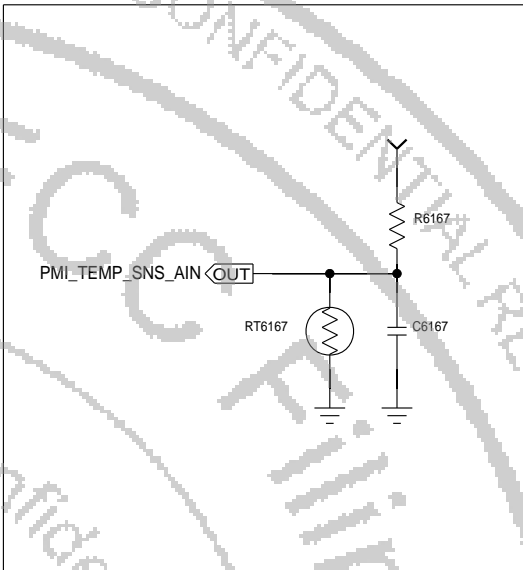
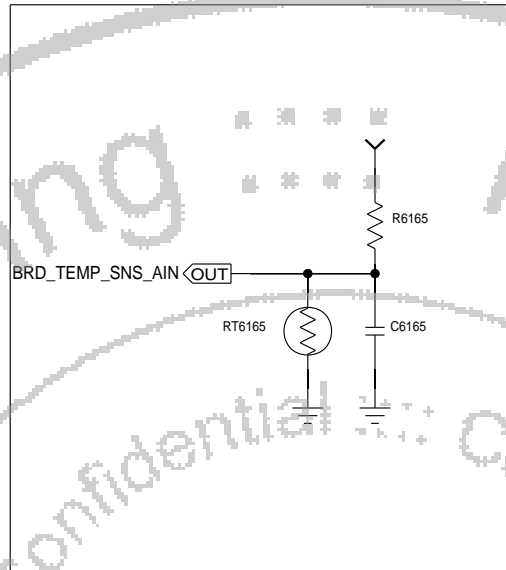
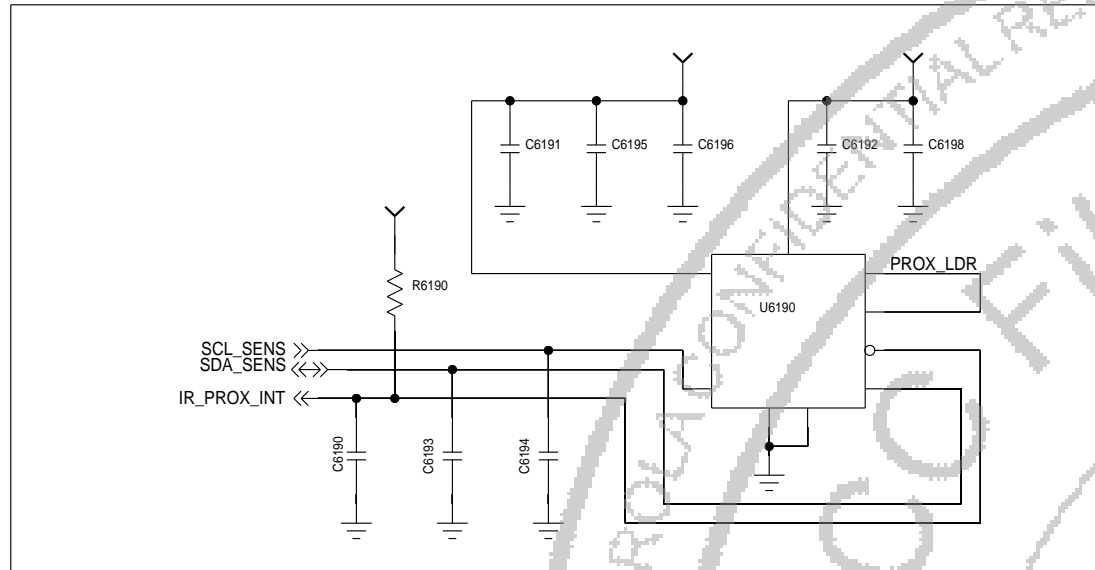
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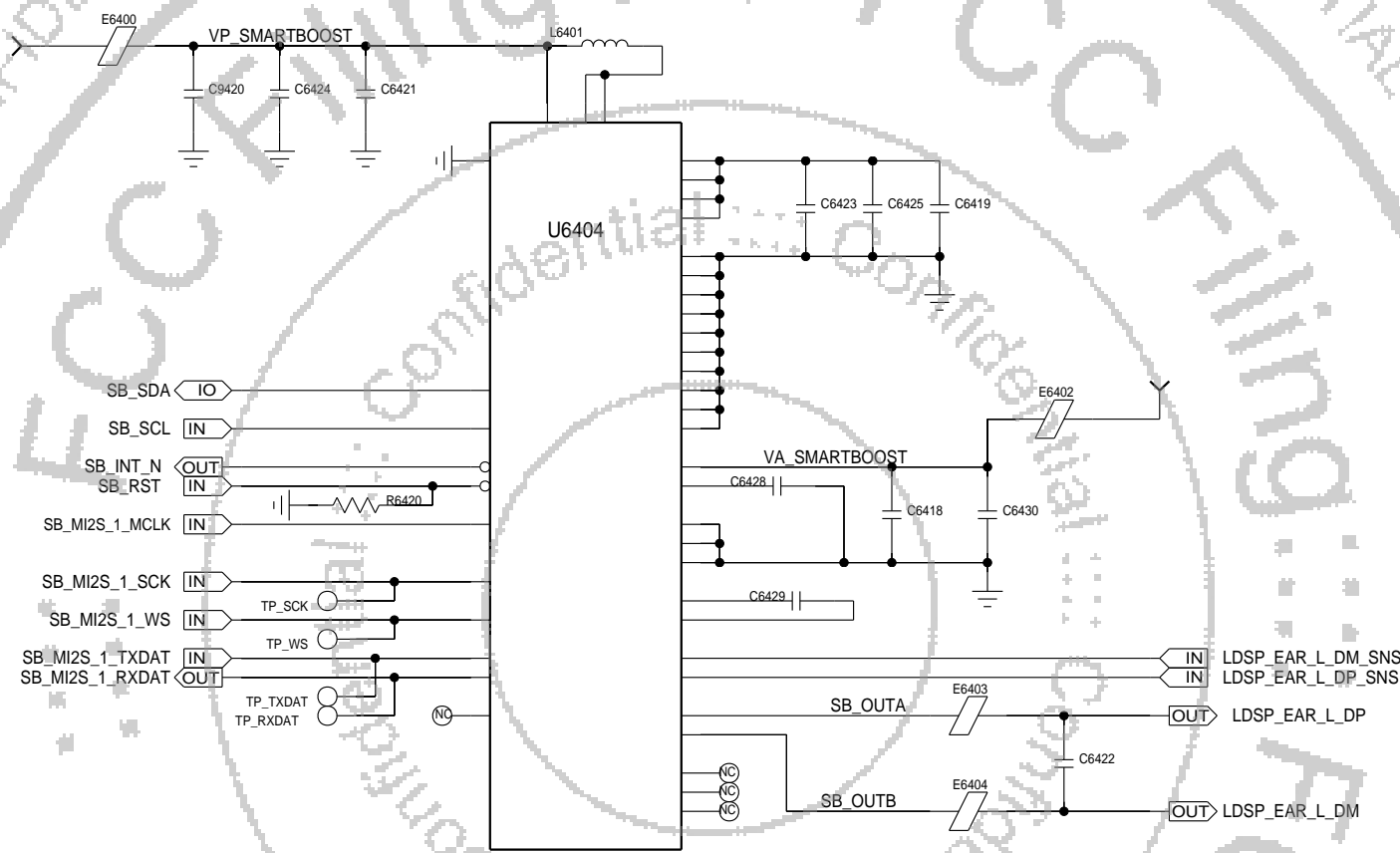
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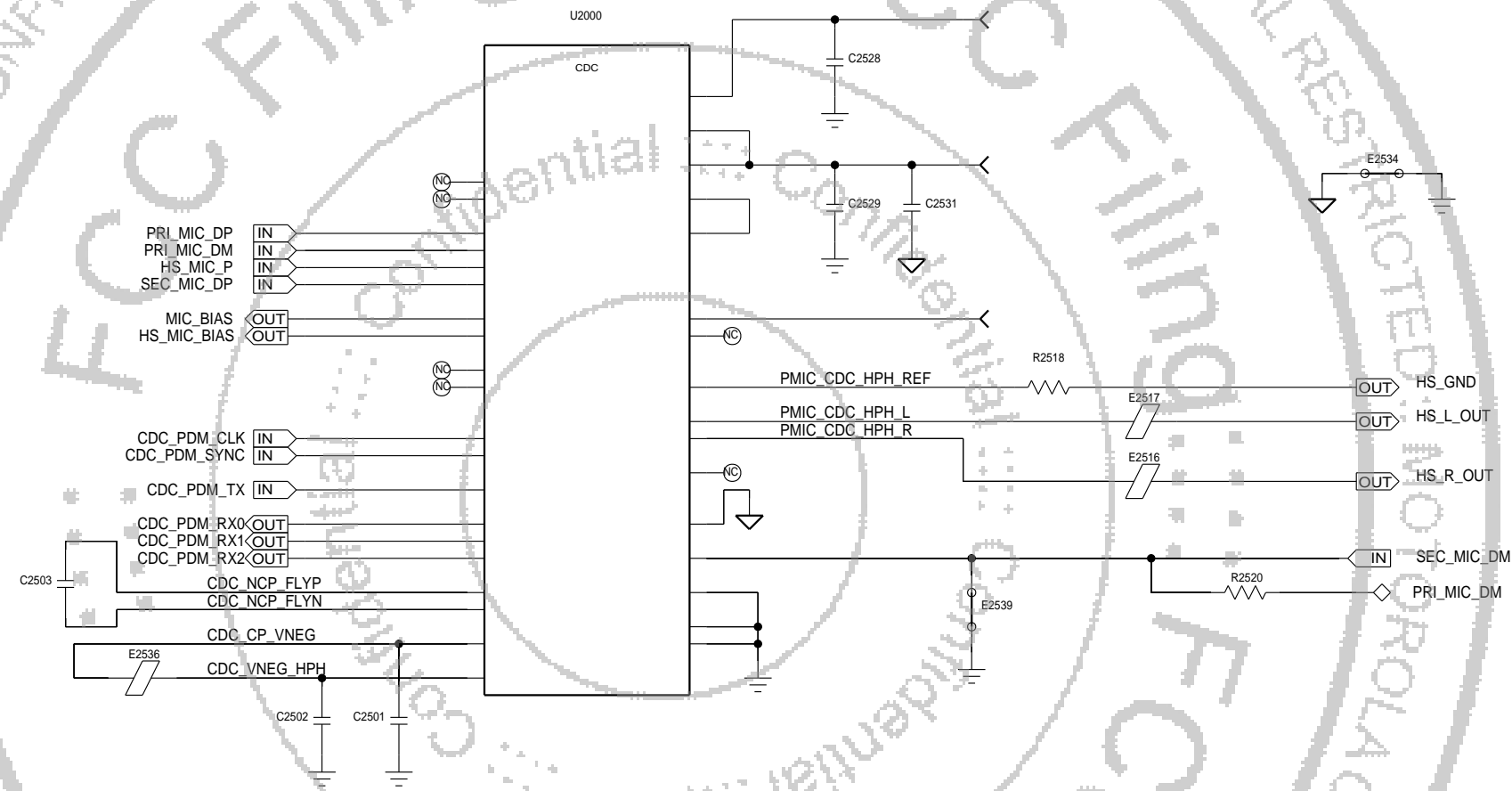


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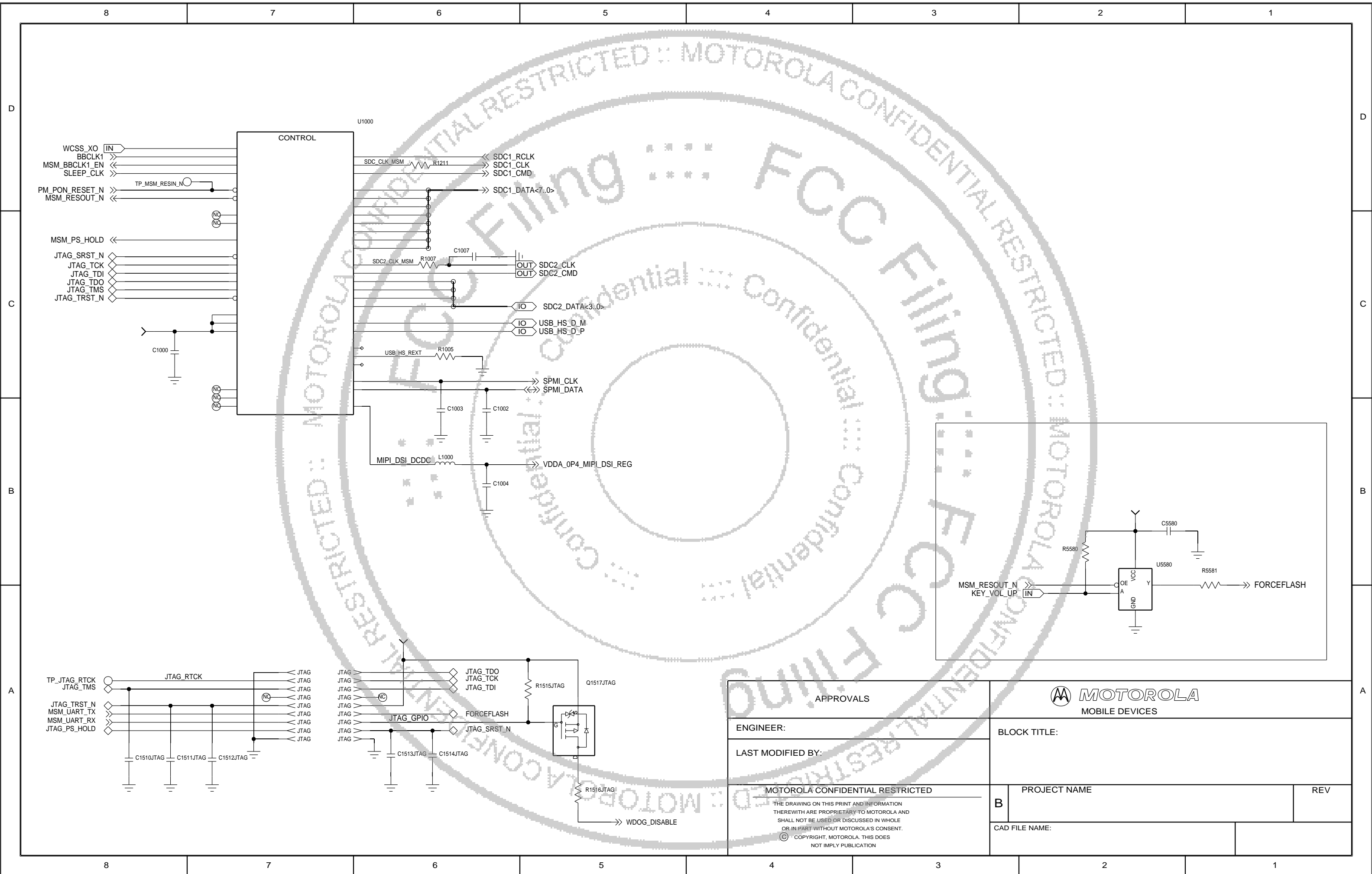
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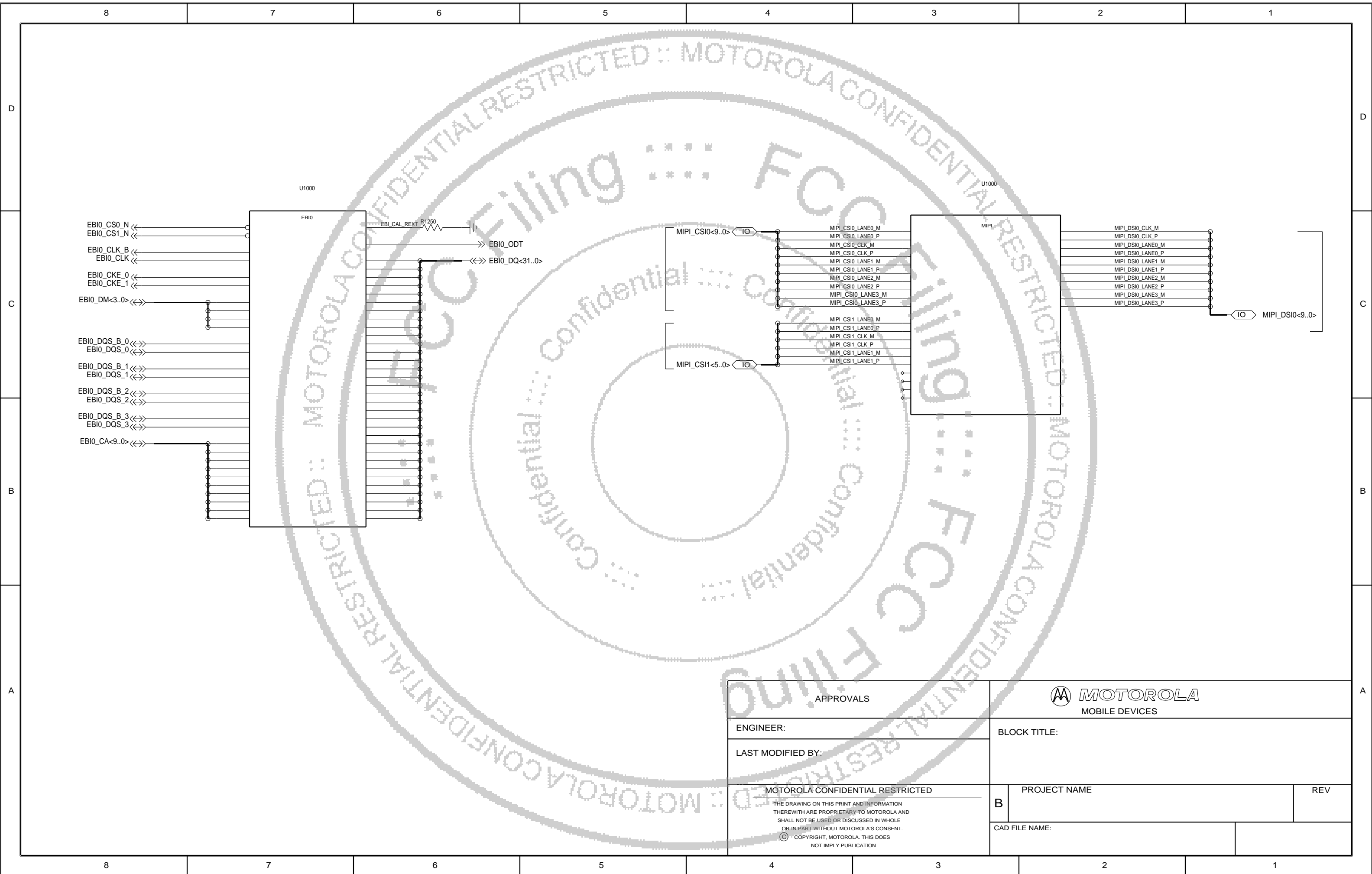
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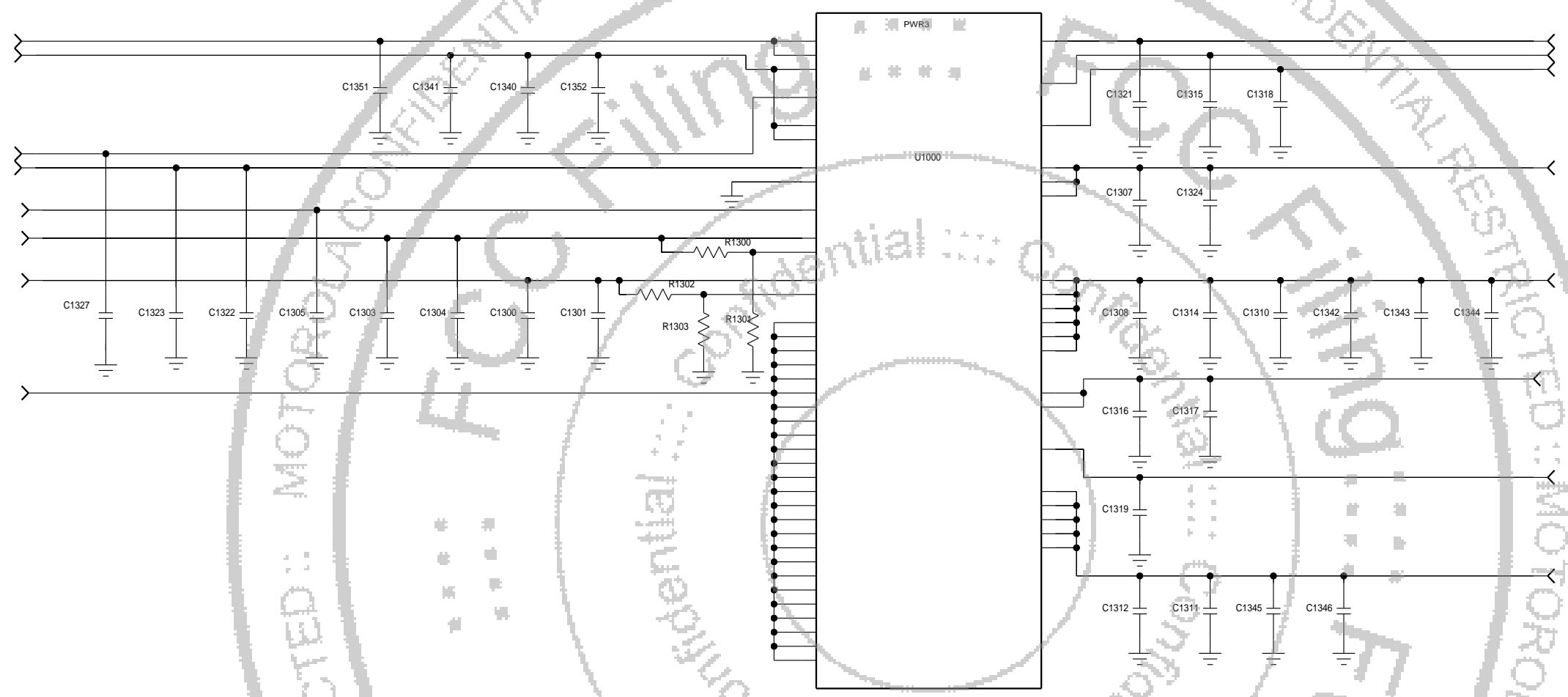
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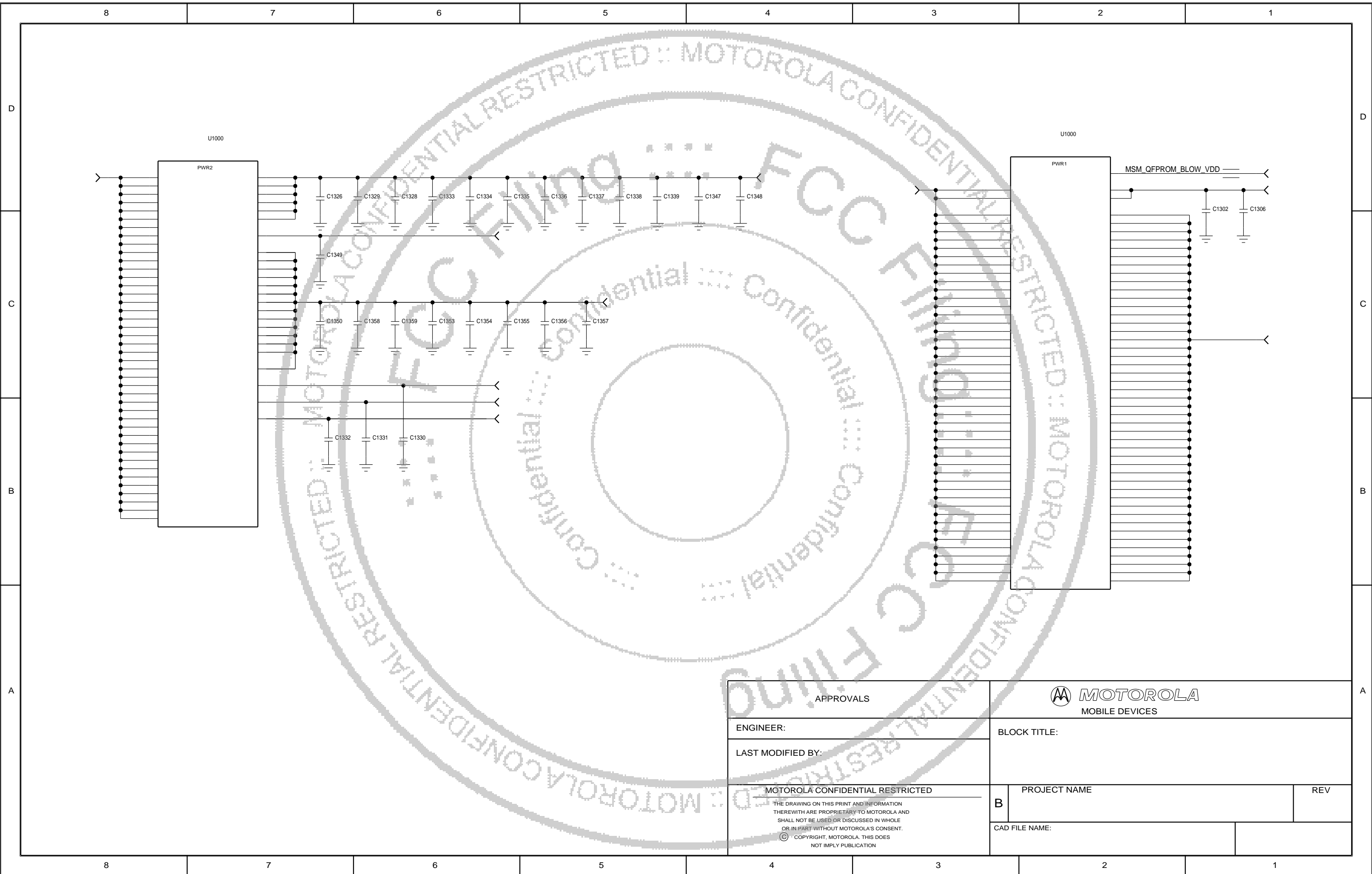
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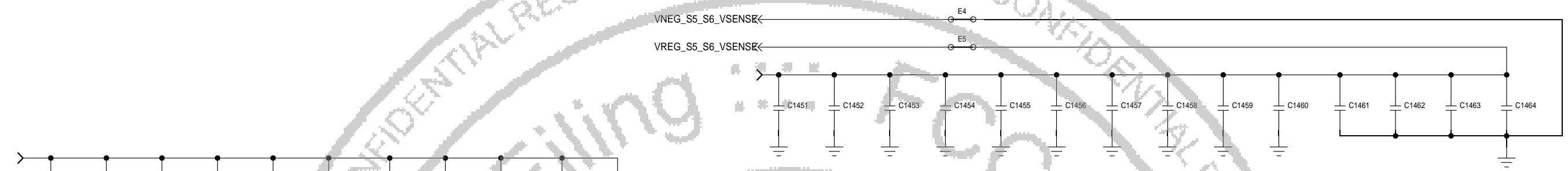


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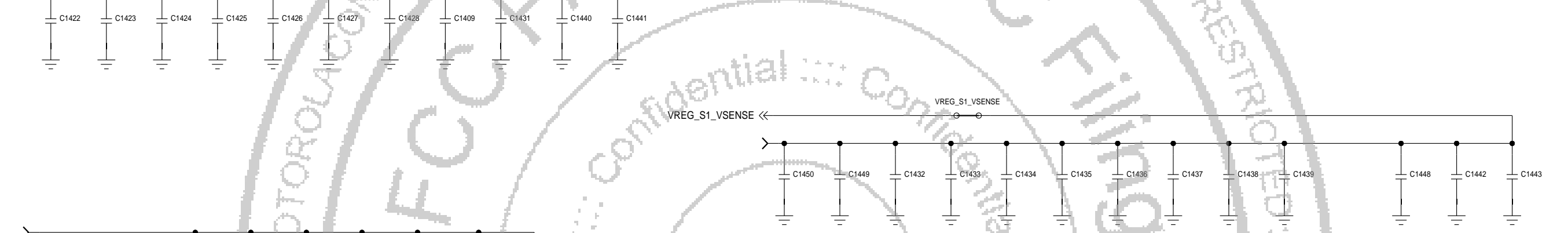
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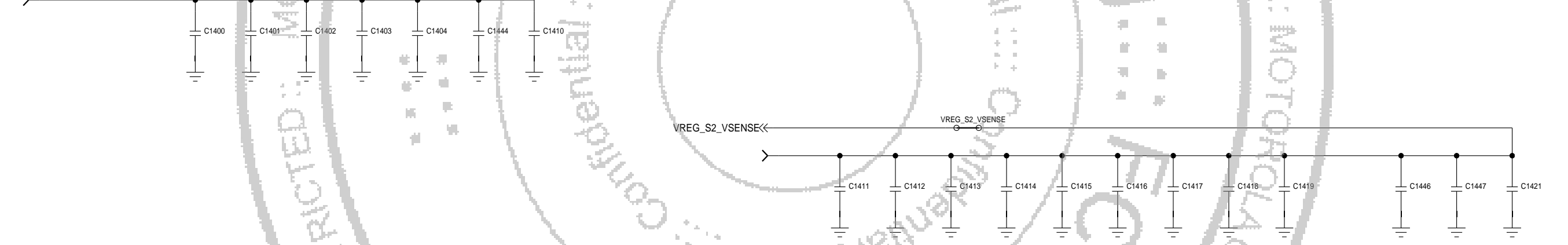
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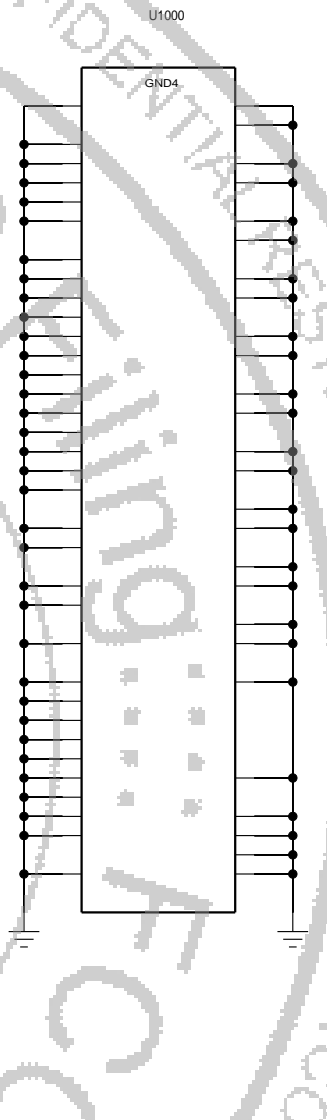
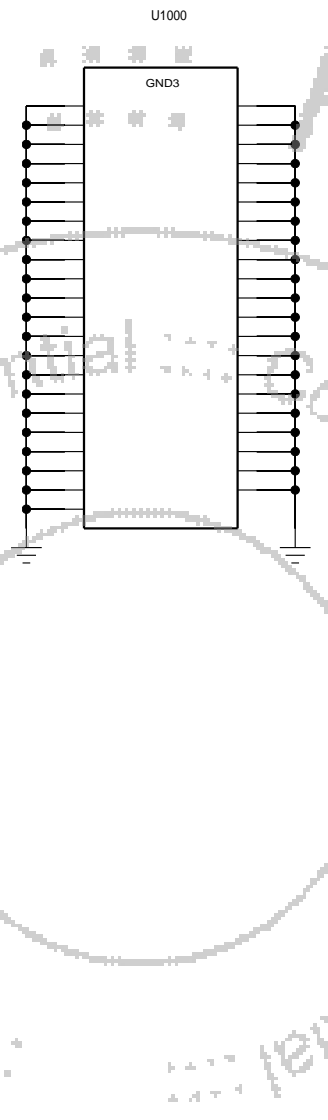
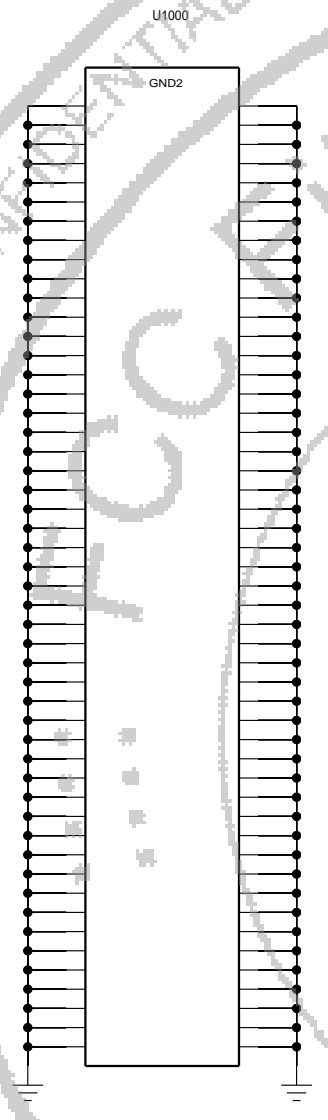
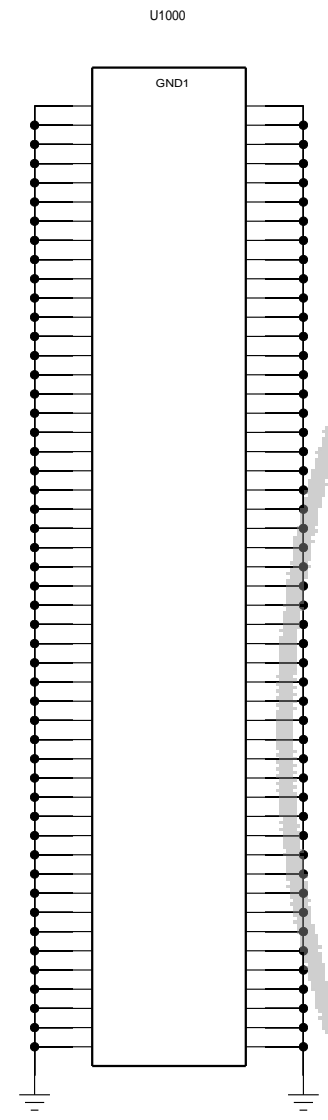
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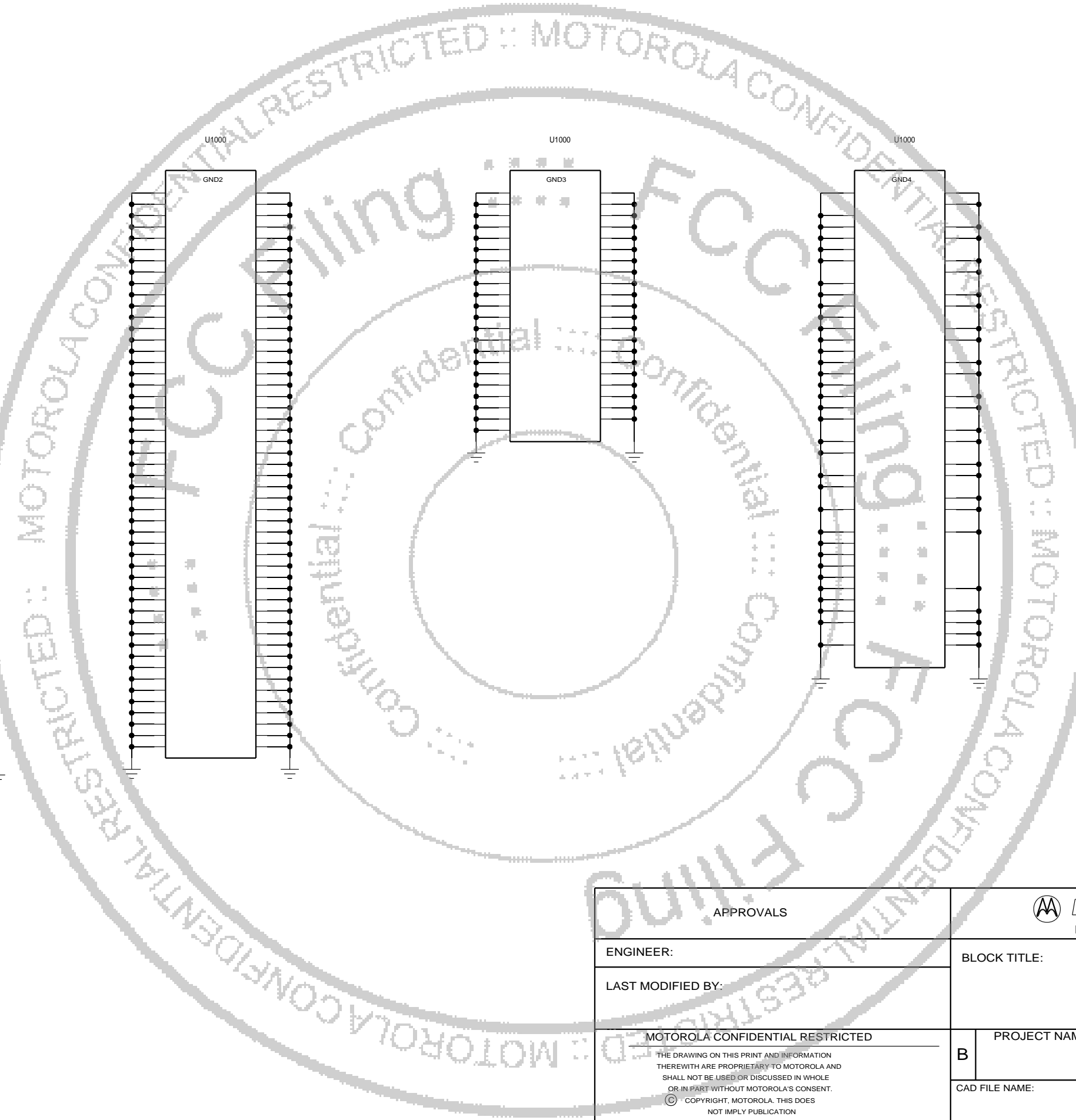
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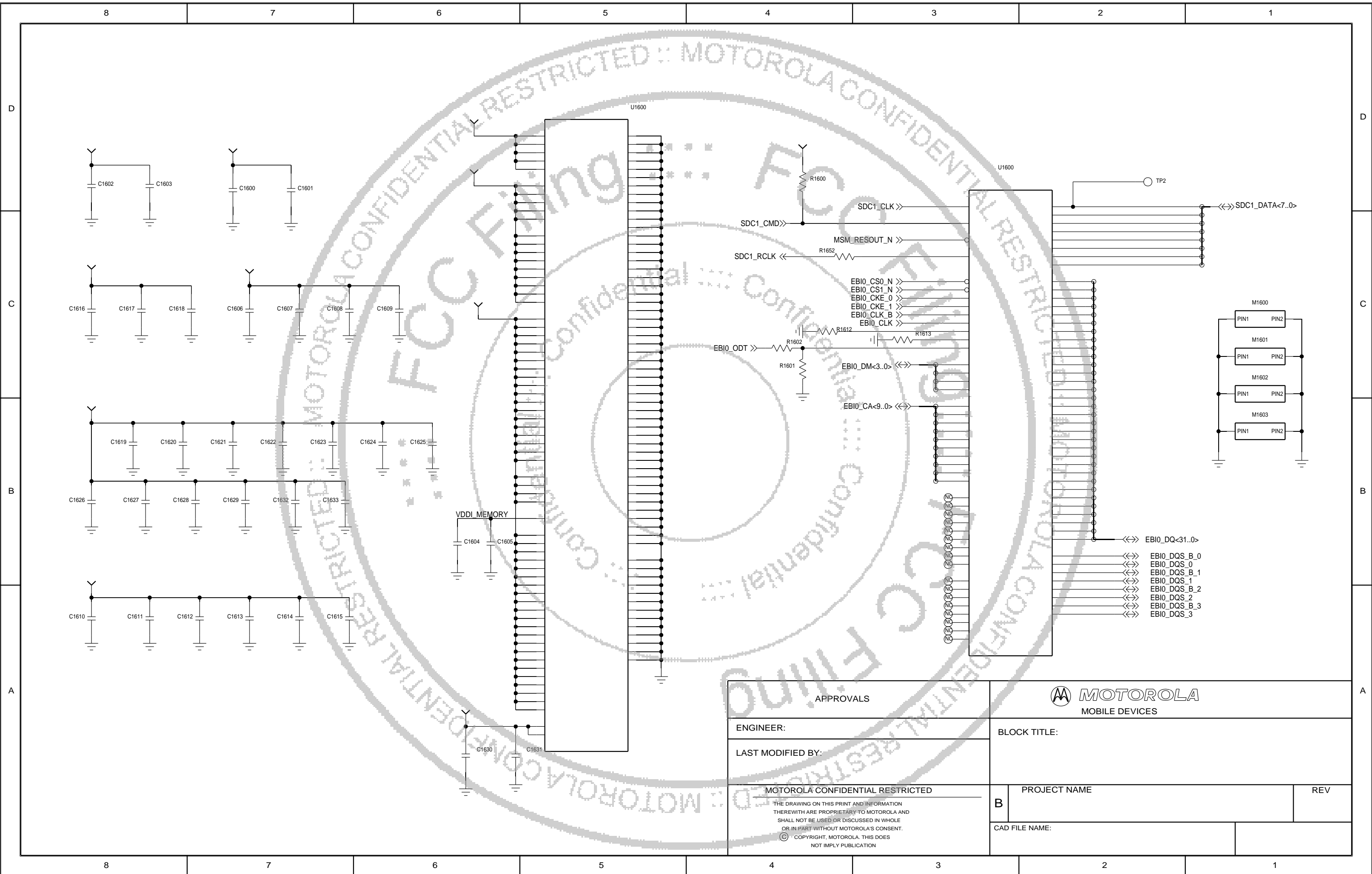
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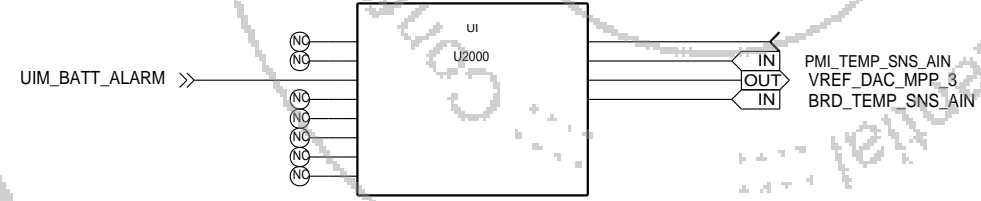
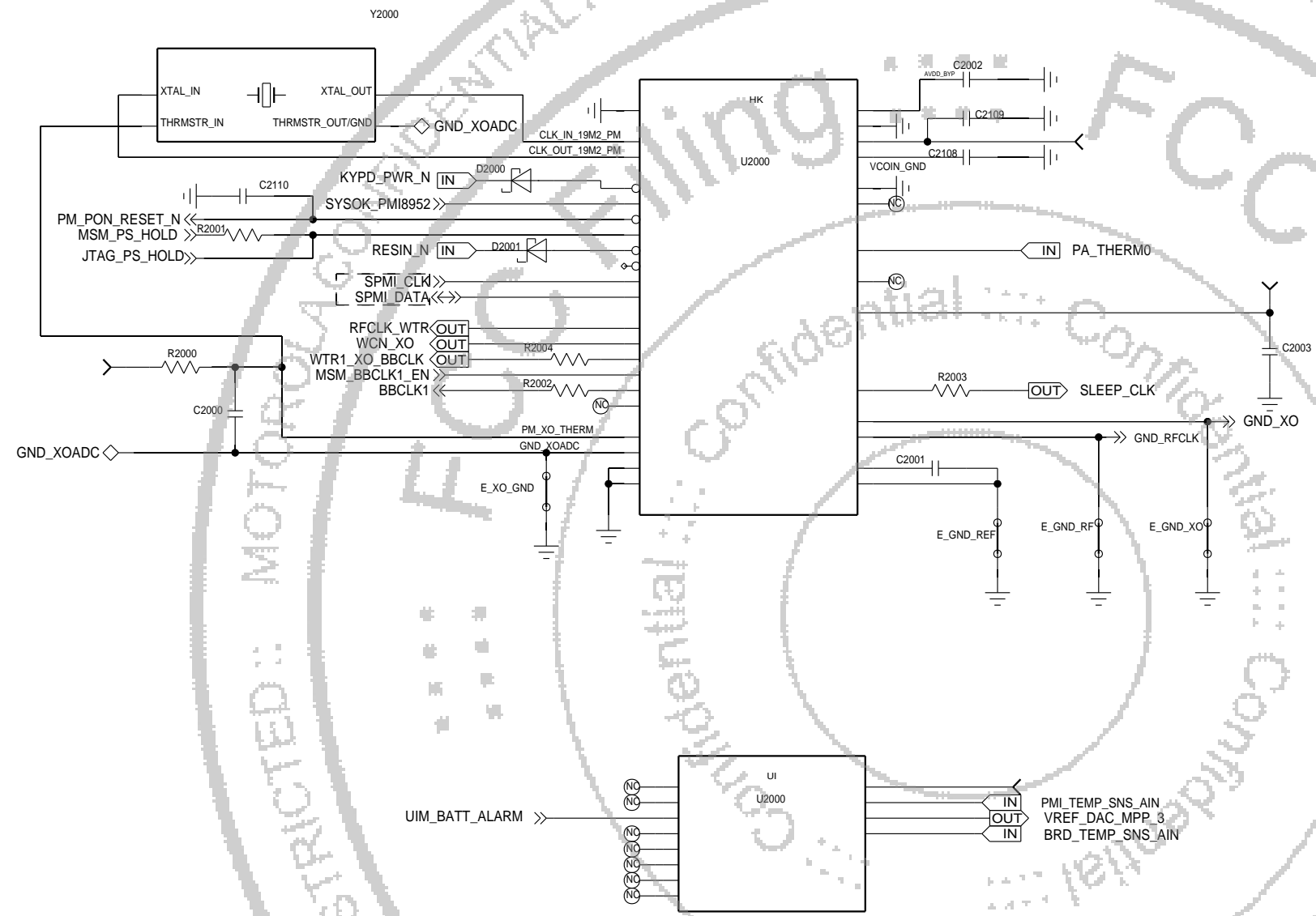
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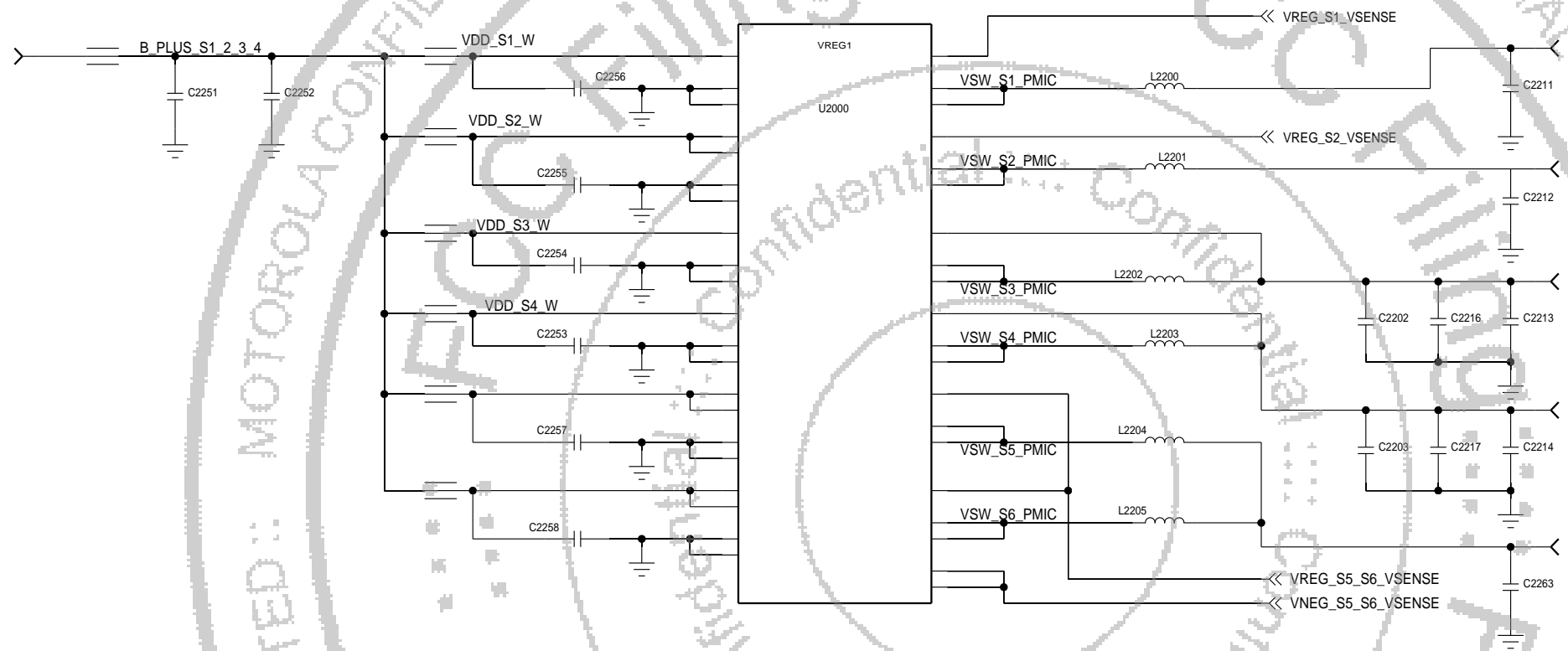





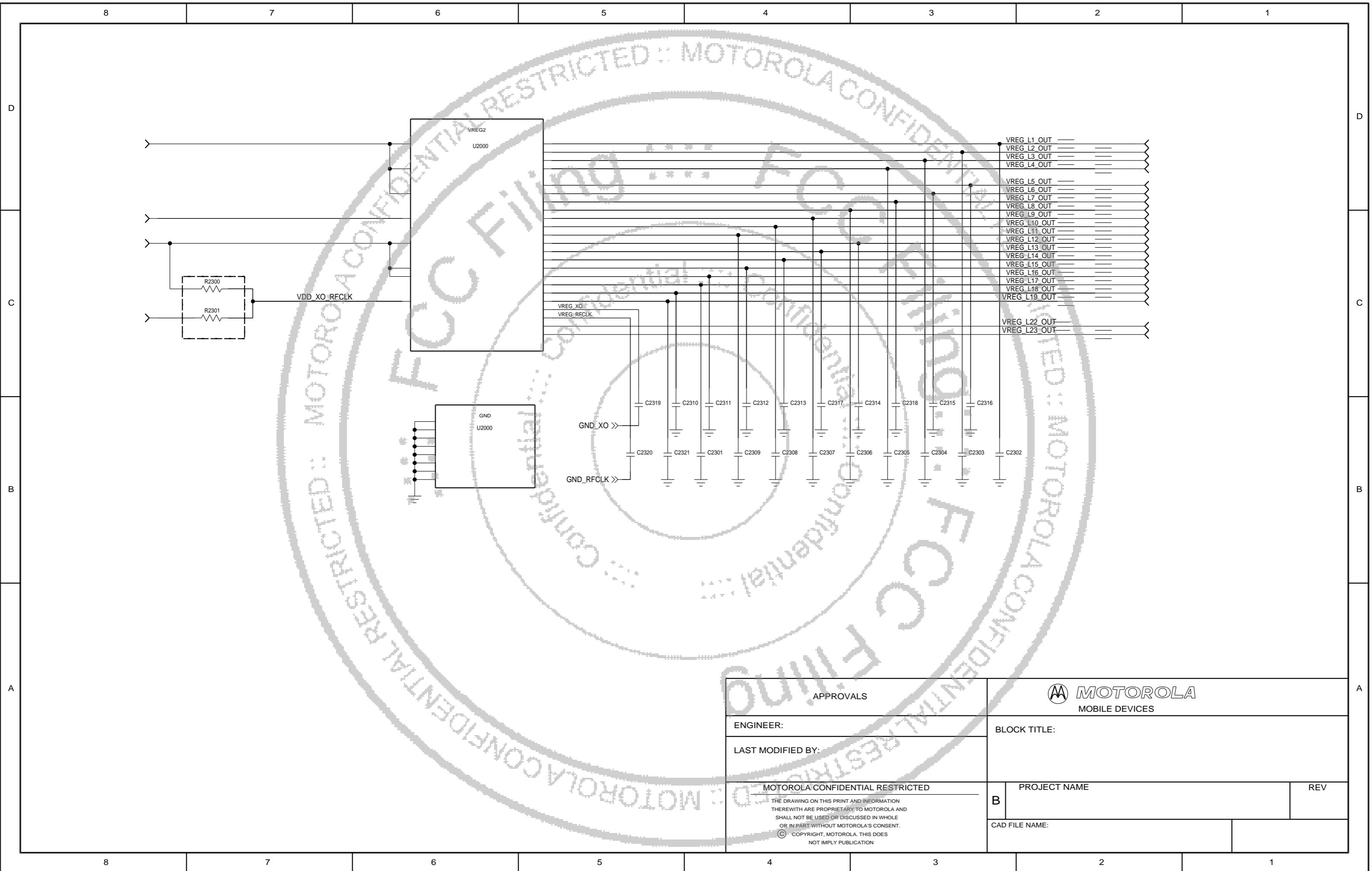
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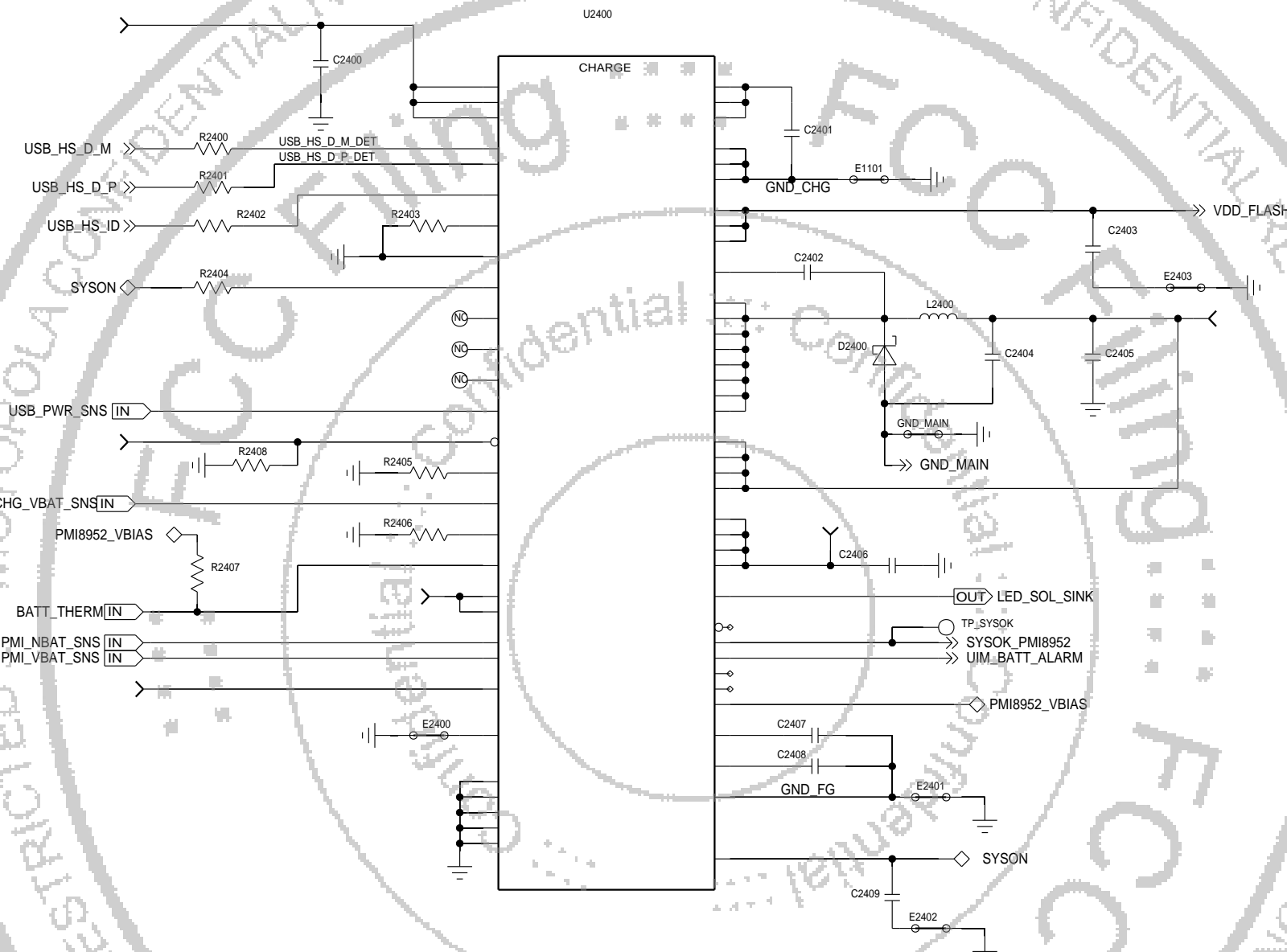
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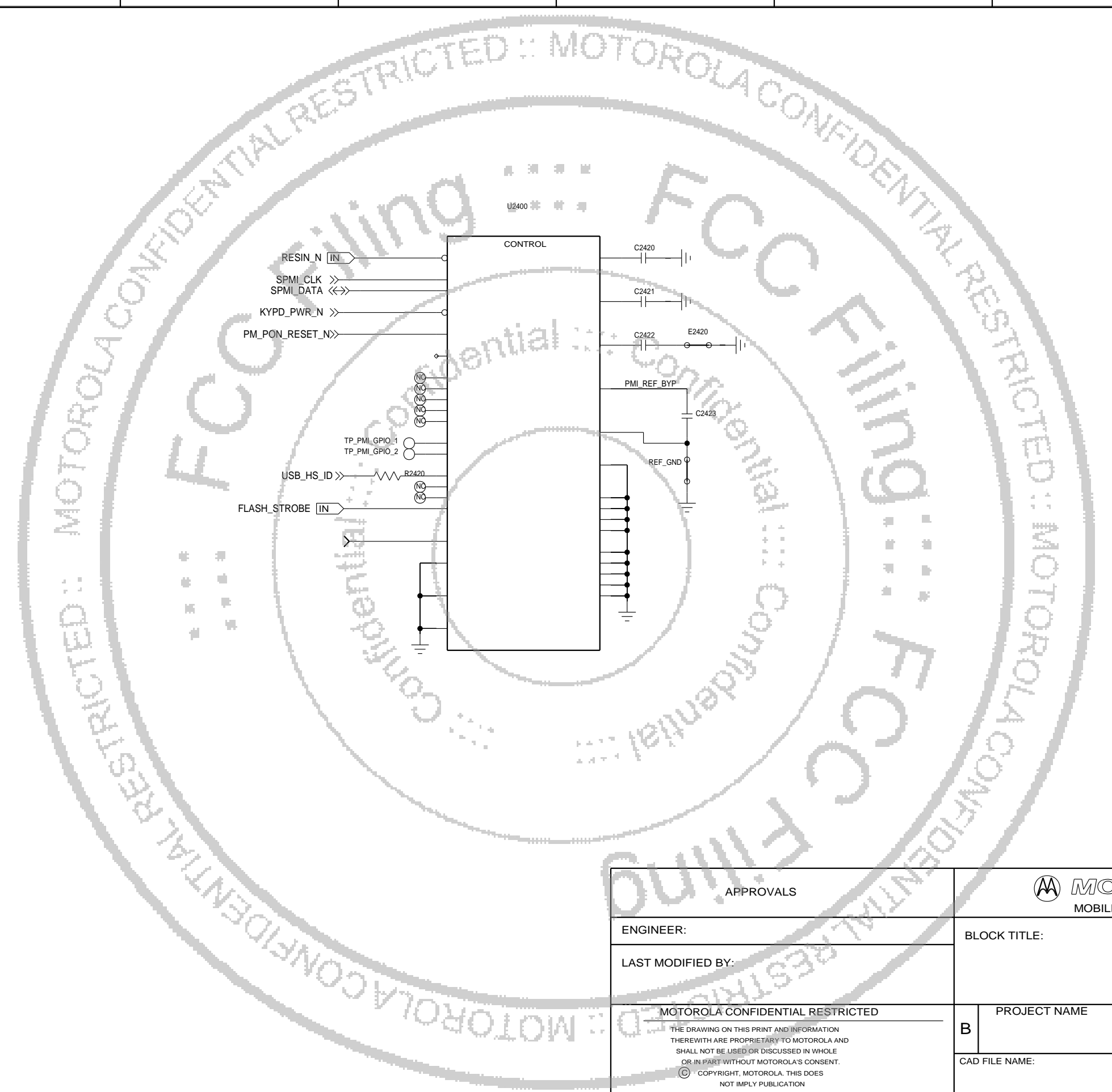
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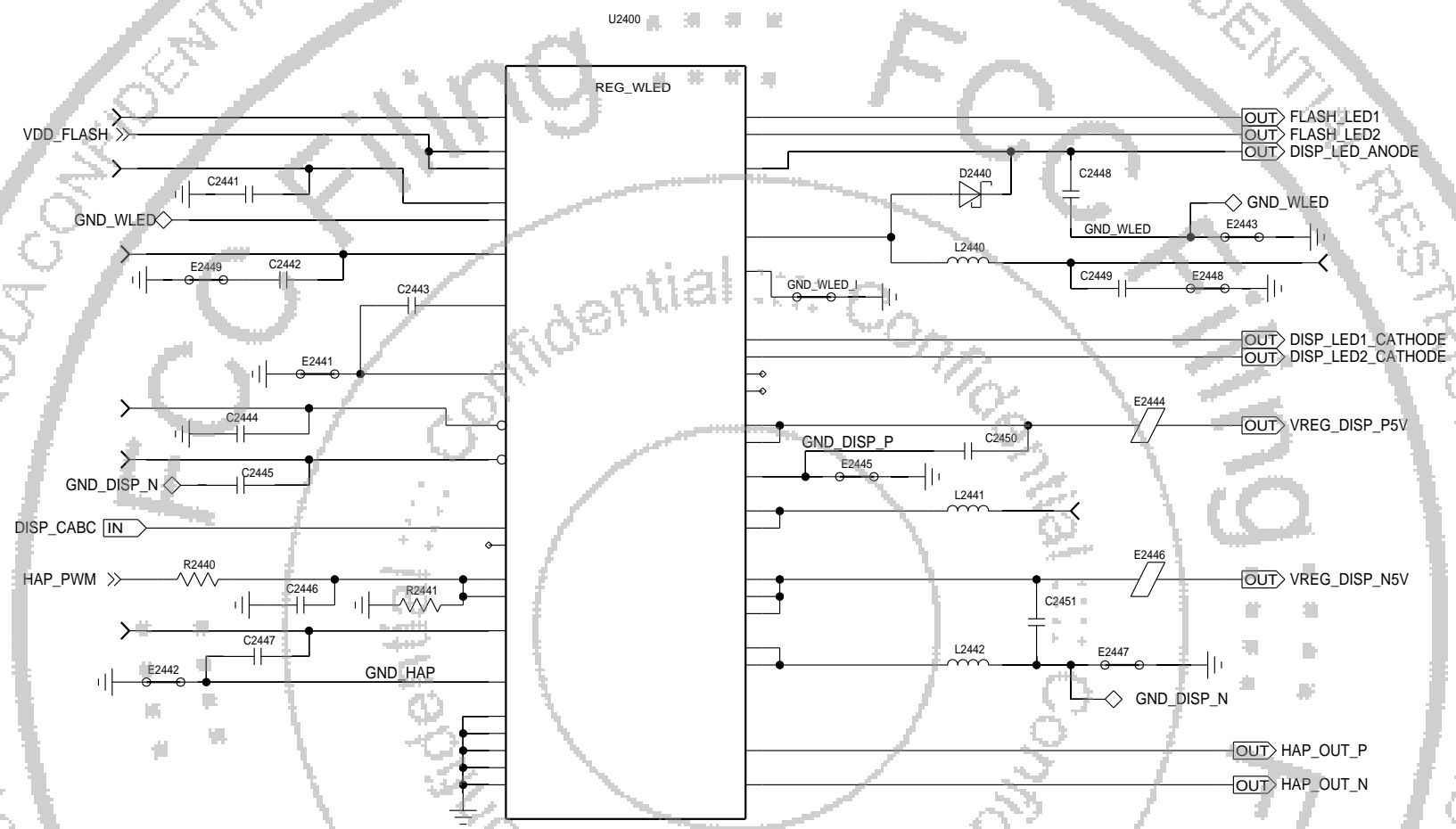
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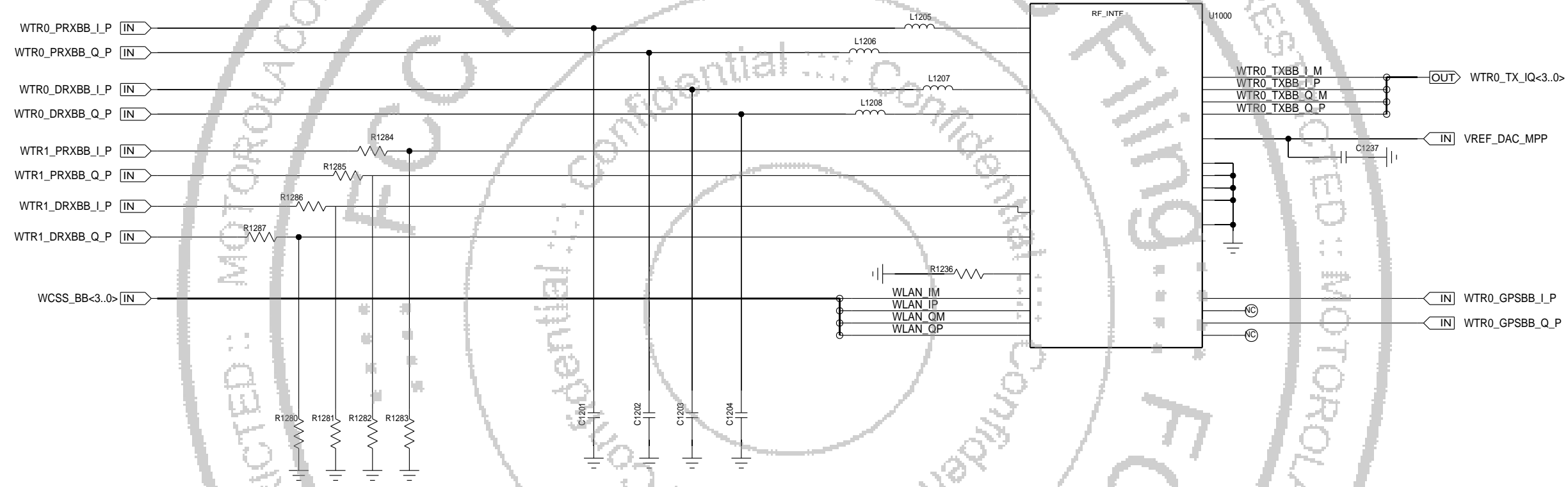
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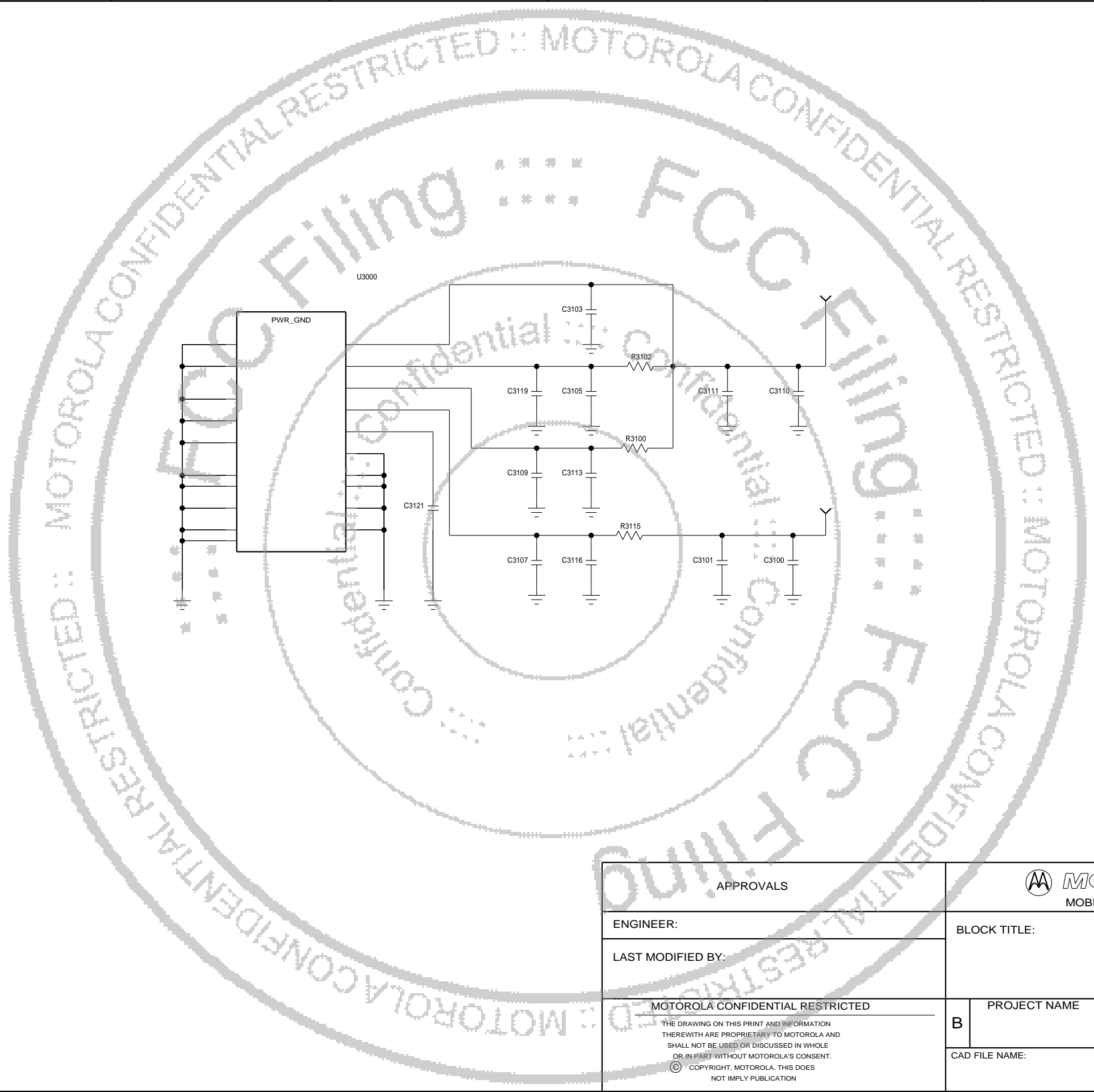
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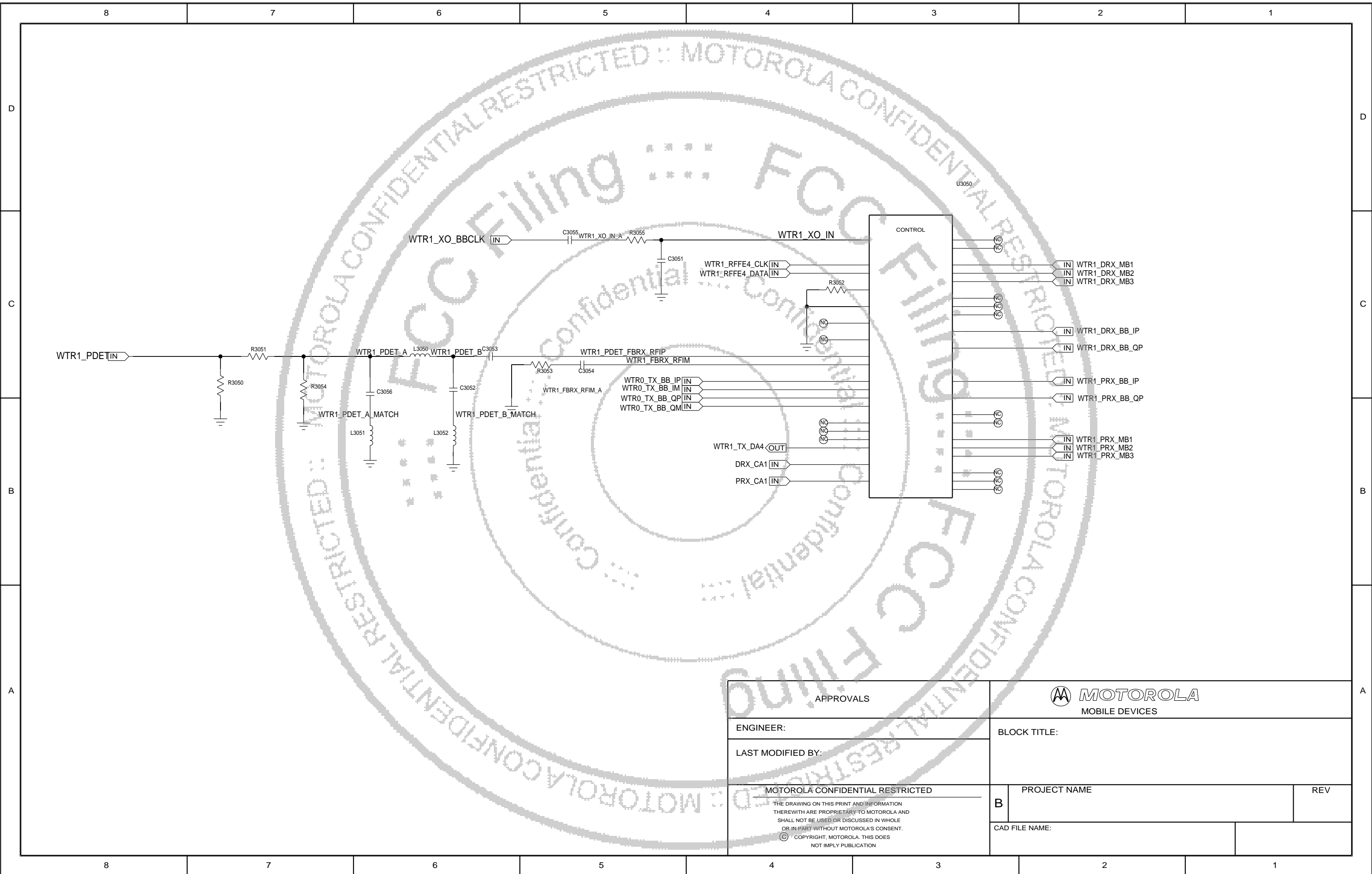
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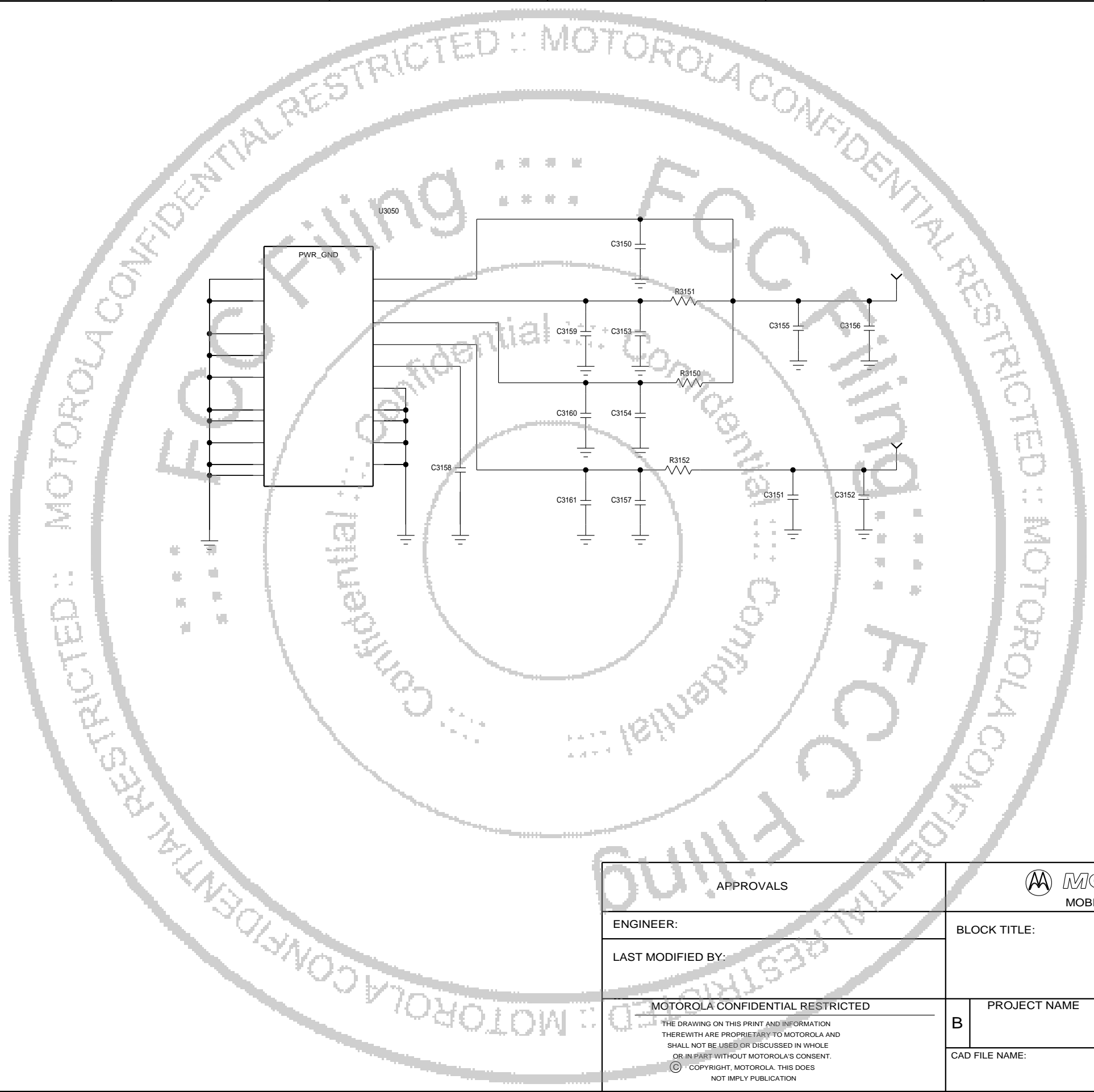
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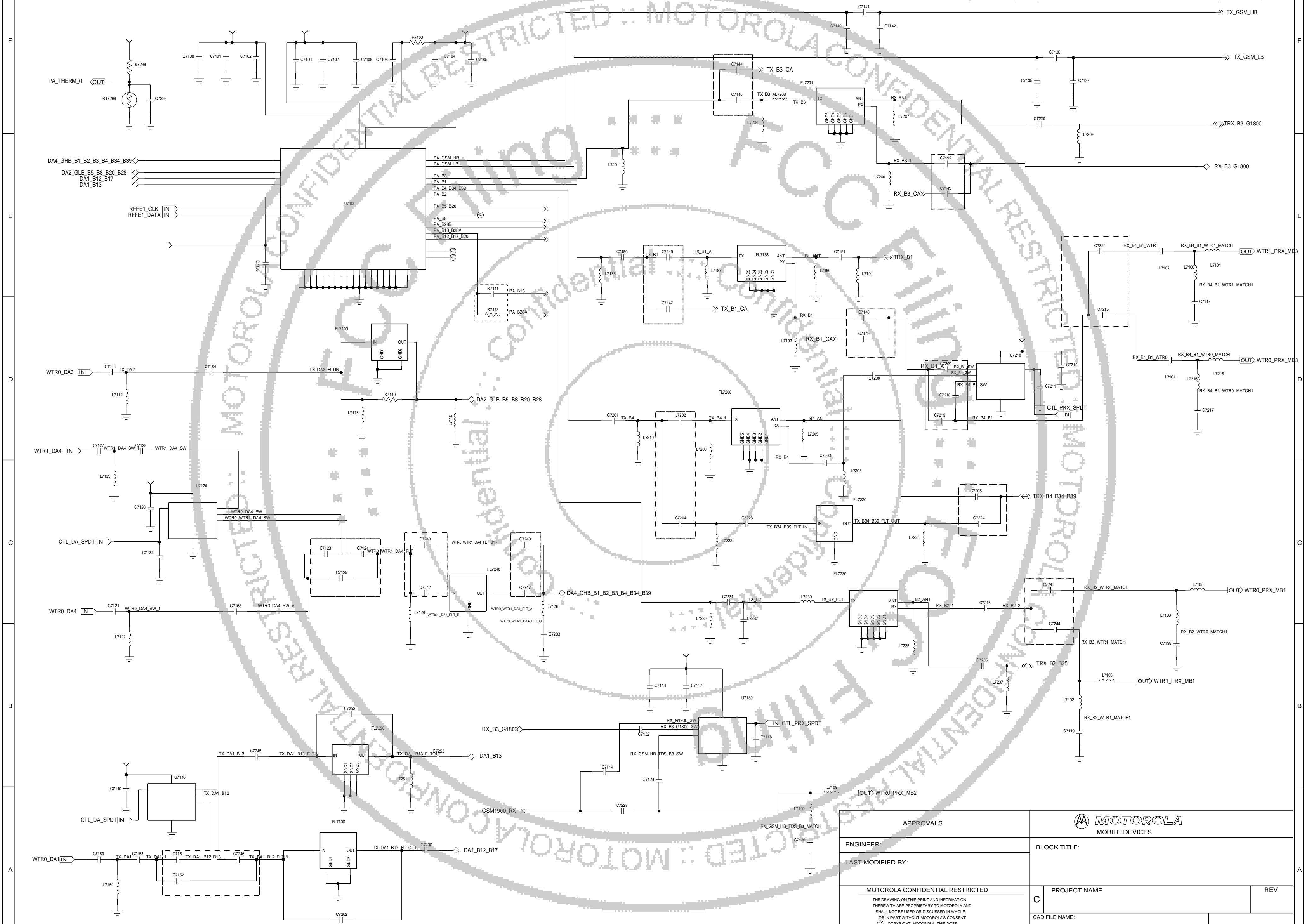
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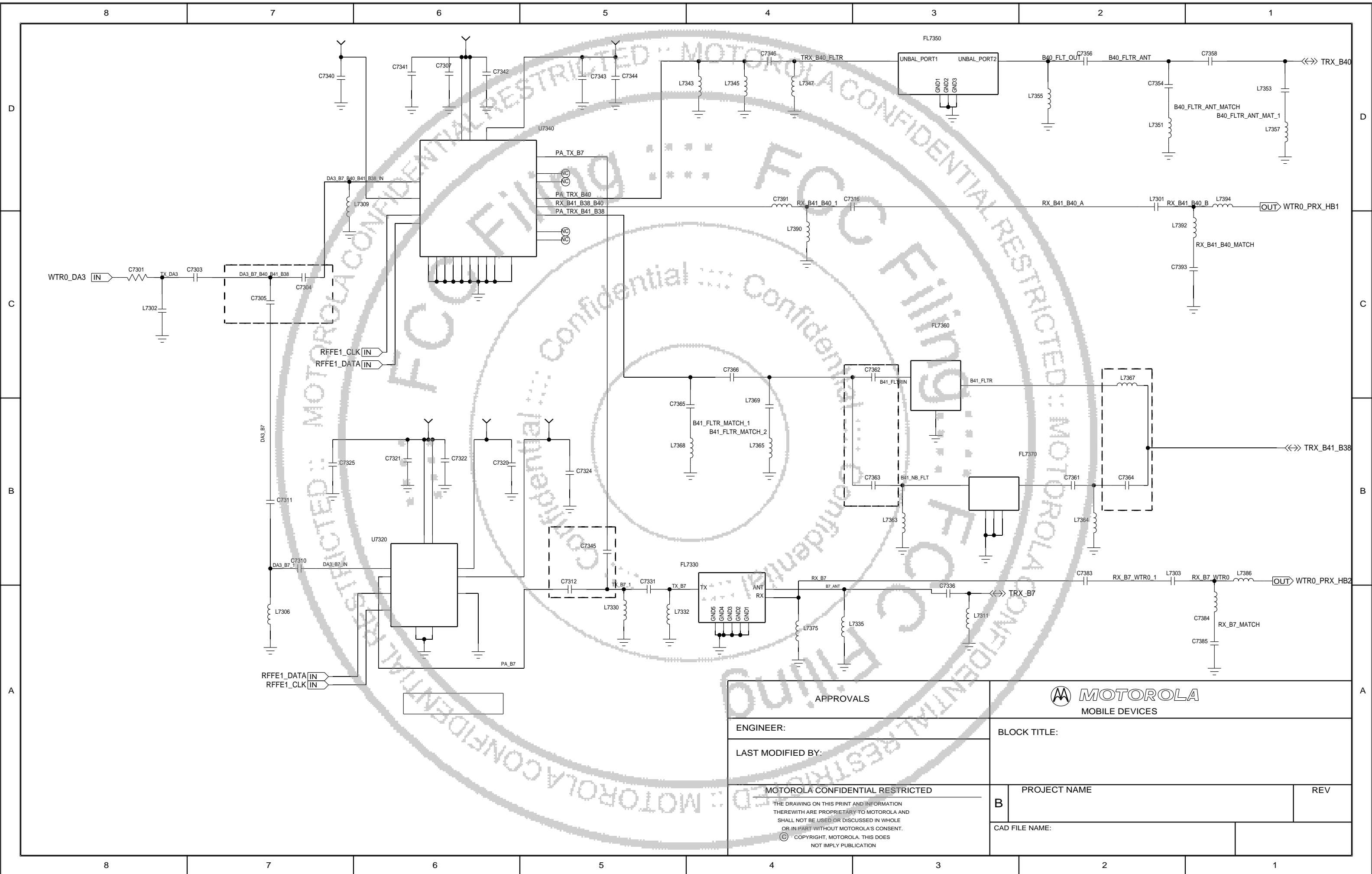
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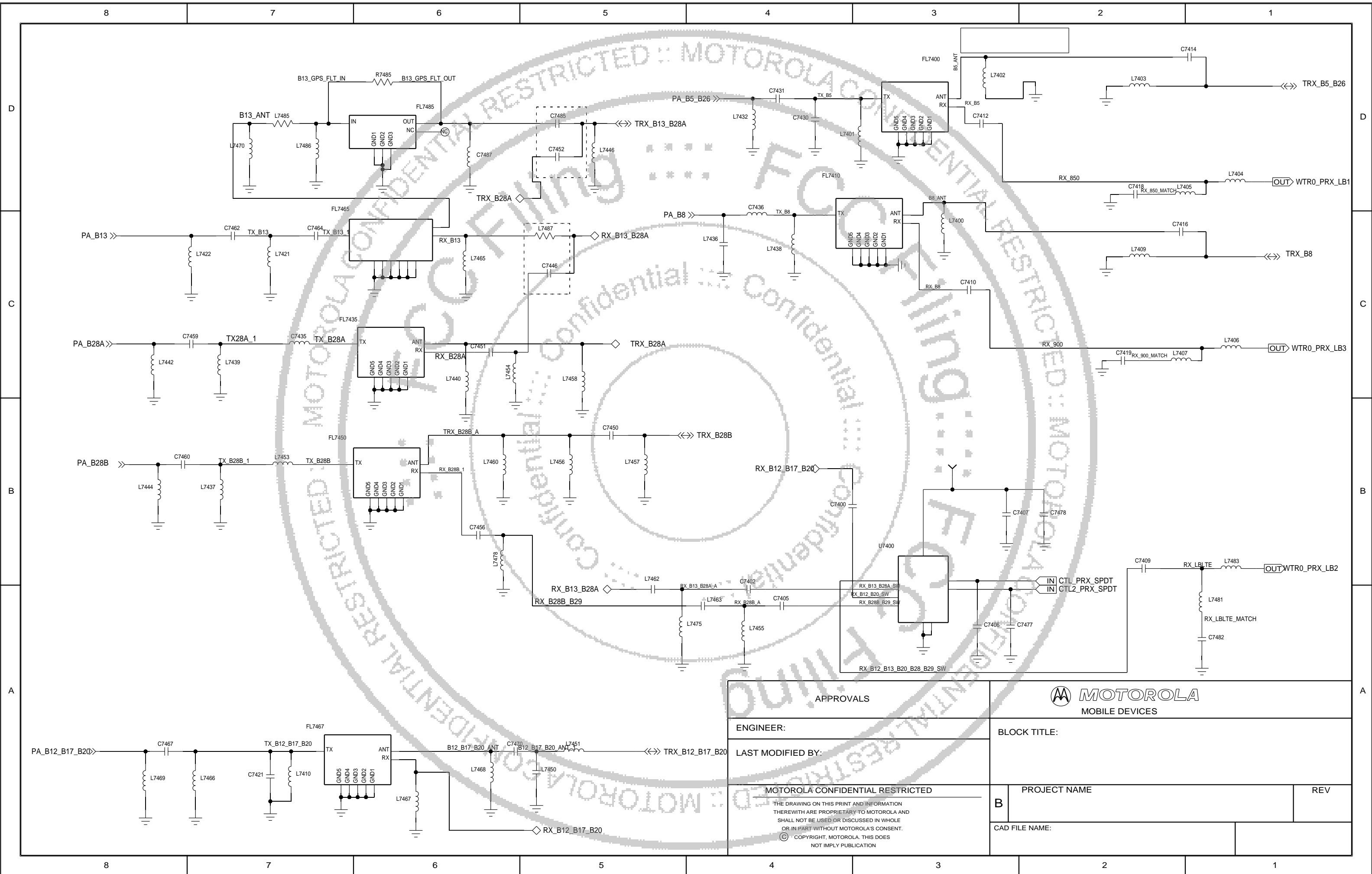
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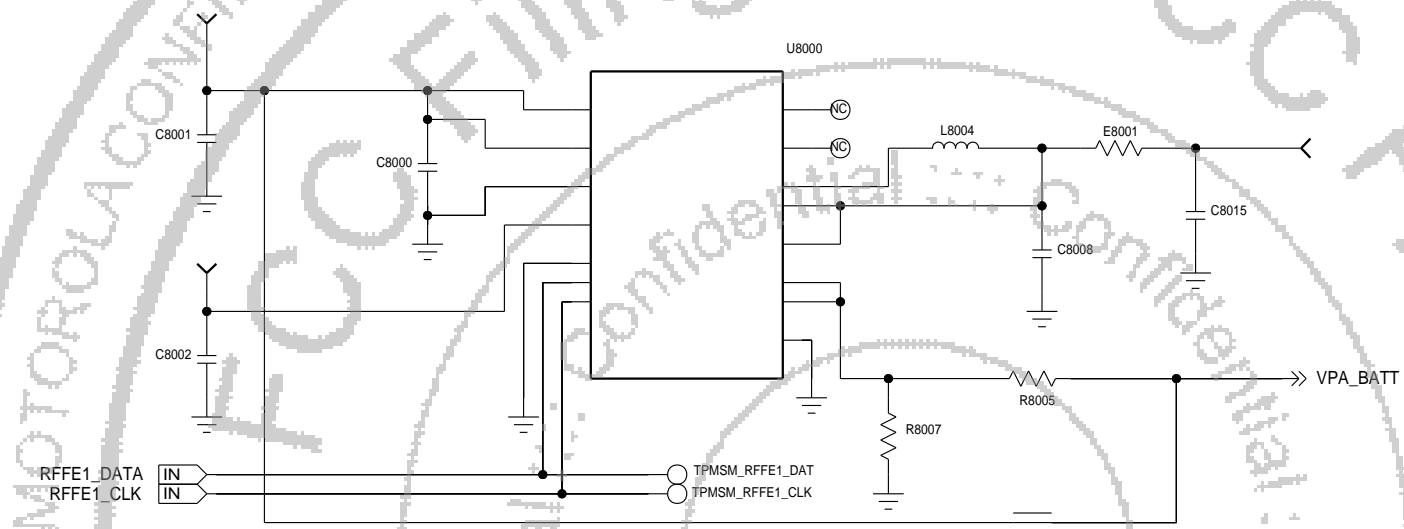
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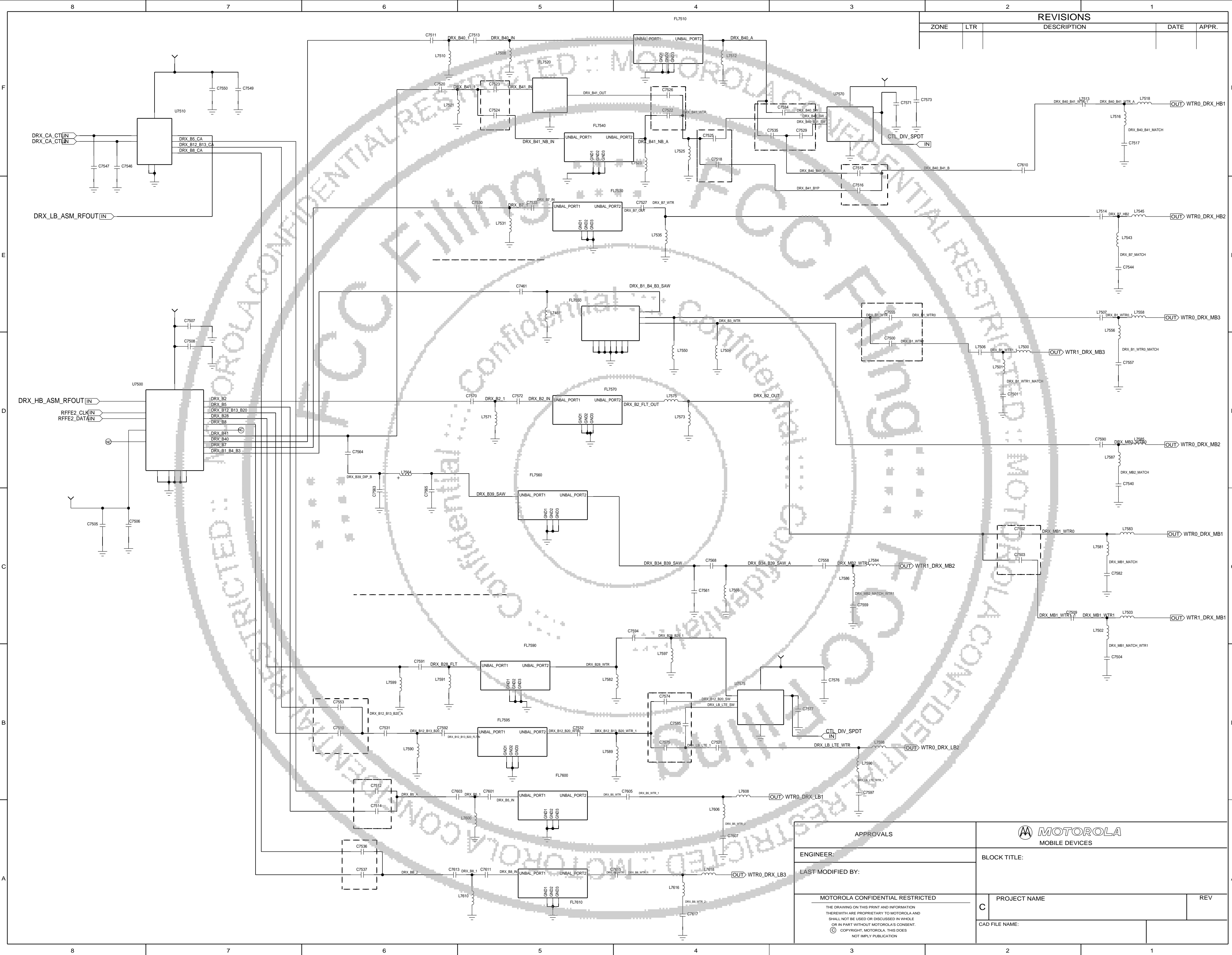


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