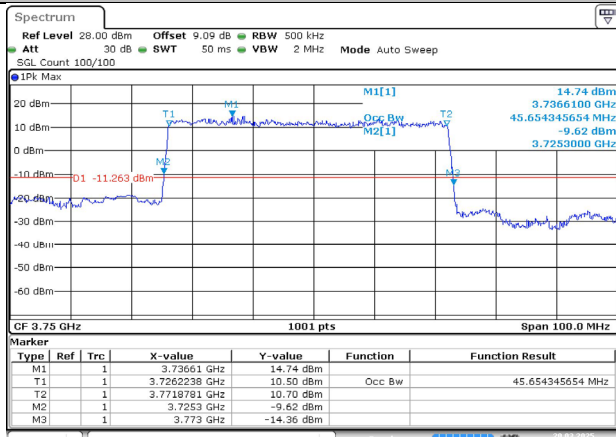


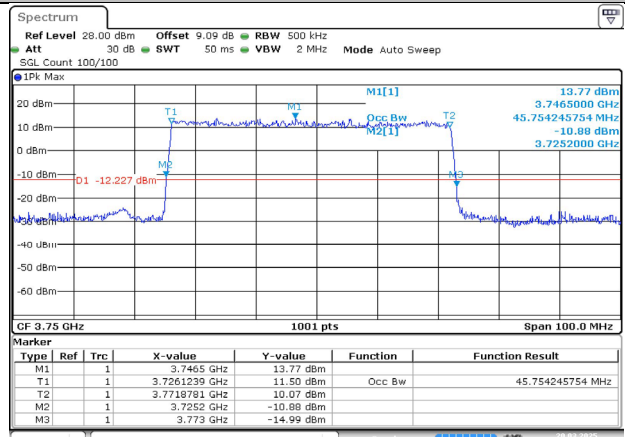
n78A / 30KHz / 50MHz

MCH / DFT-Pi2BPSK / Outer_Full



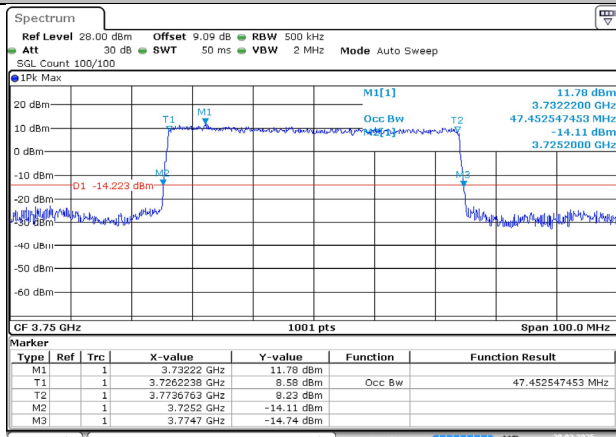
Date: 20 MAR 2025 20:00:12

MCH / DFT-QPSK / Outer_Full



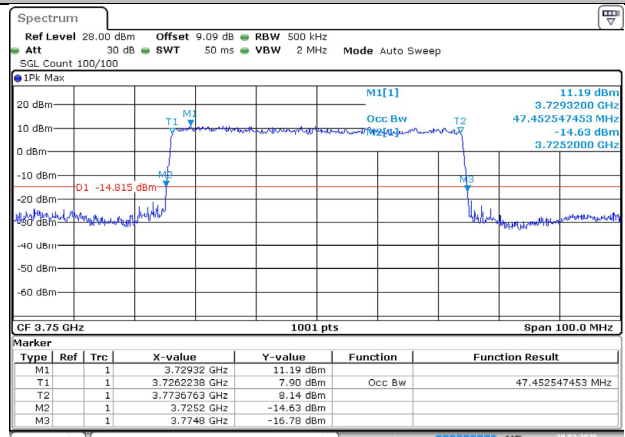
Date: 20 MAR 2025 20:00:31

MCH / CP-QPSK / Outer_Full



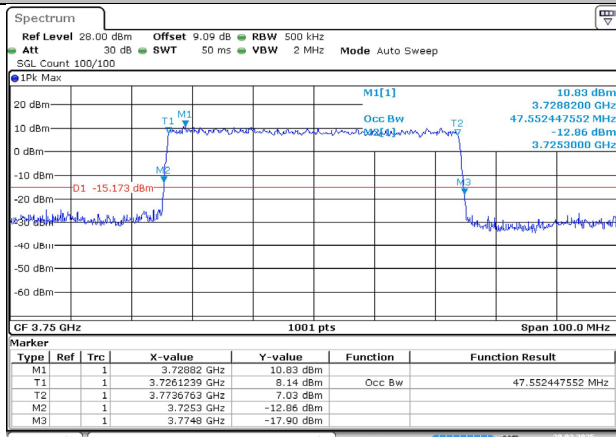
Date: 20 MAR 2025 20:01:06

MCH / CP-16QAM / Outer_Full



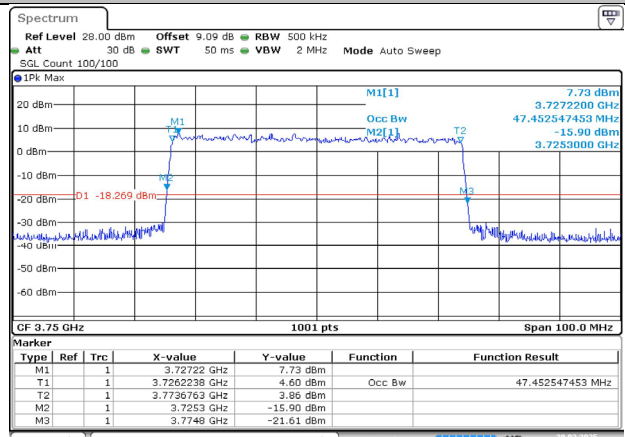
Date: 20 MAR 2025 20:01:14

MCH / CP-64QAM / Outer_Full



Date: 20 MAR 2025 20:01:21

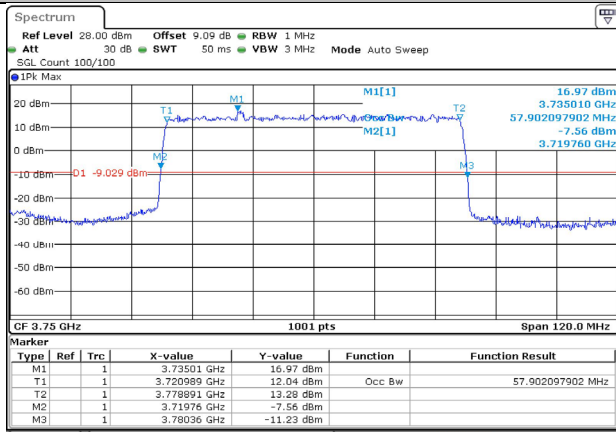
MCH / CP-256QAM / Outer_Full



Date: 20 MAR 2025 20:01:32

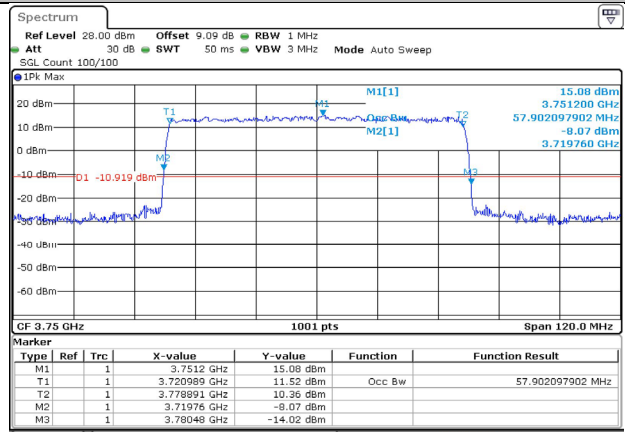
n78A / 30KHz / 60MHz

MCH / DFT-Pi2BPSK / Outer_Full



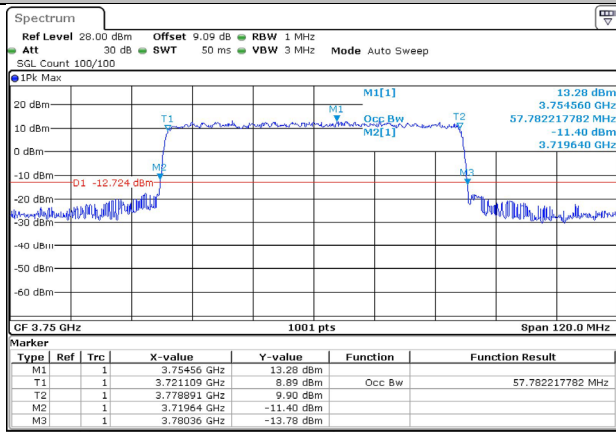
Date: 20 MAR 2025 20:01:58

MCH / DFT-QPSK / Outer_Full



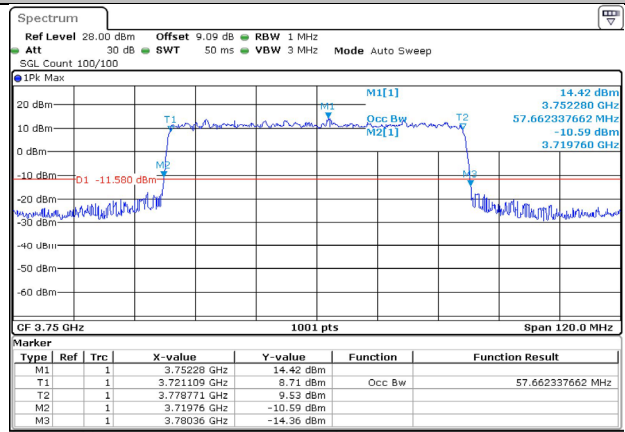
Date: 20 MAR 2025 20:02:17

MCH / CP-QPSK / Outer_Full



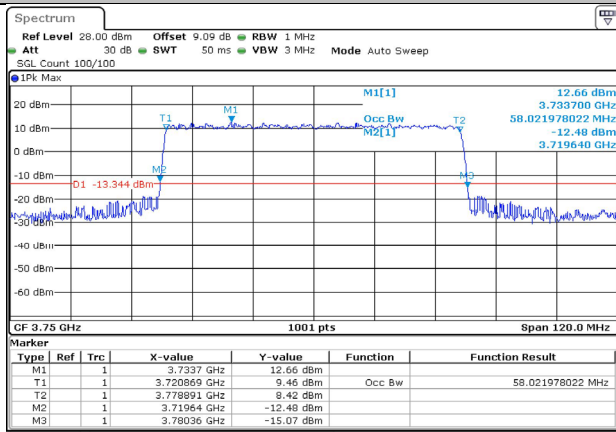
Date: 20 MAR 2025 20:02:51

MCH / CP-16QAM / Outer_Full



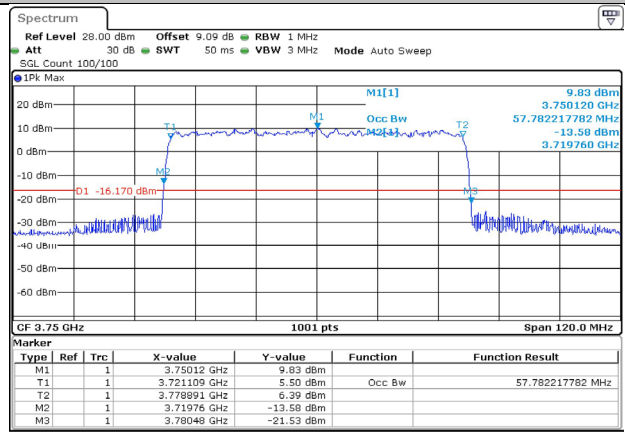
Date: 20 MAR 2025 20:02:59

MCH / CP-64QAM / Outer_Full



Date: 20 MAR 2025 20:03:06

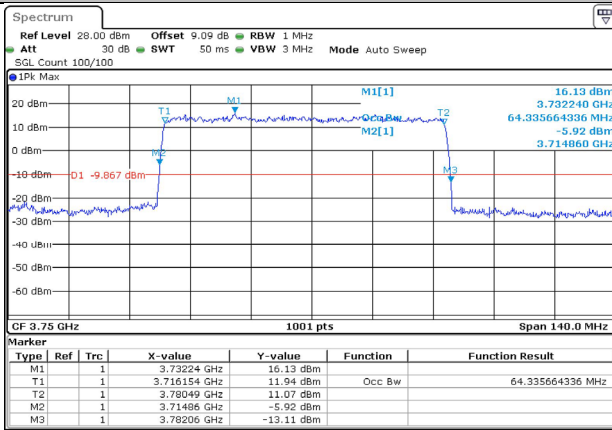
MCH / CP-256QAM / Outer_Full



Date: 20 MAR 2025 20:03:16

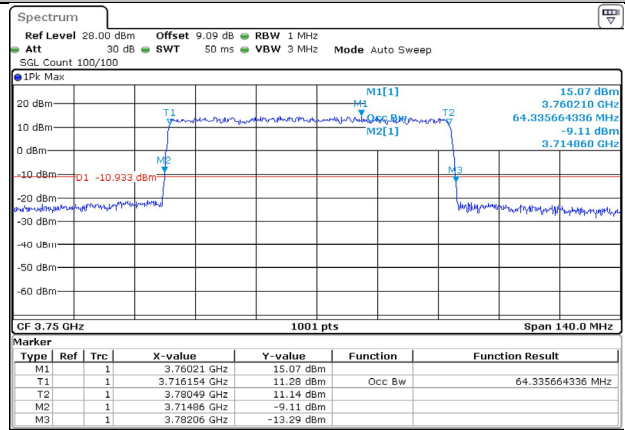
n78A / 30KHz / 70MHz

MCH / DFT-Pi2BPSK / Outer_Full



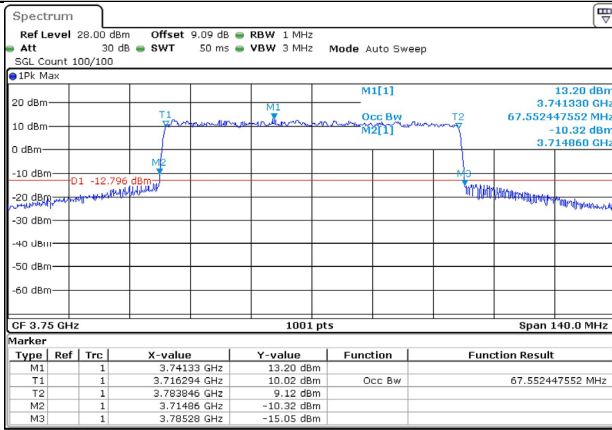
Date: 20 MAR 2025 20:03:37

MCH / DFT-QPSK / Outer_Full



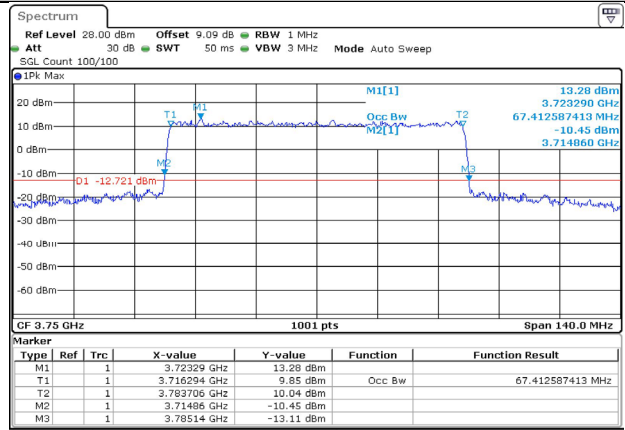
Date: 20 MAR 2025 20:03:55

MCH / CP-QPSK / Outer_Full



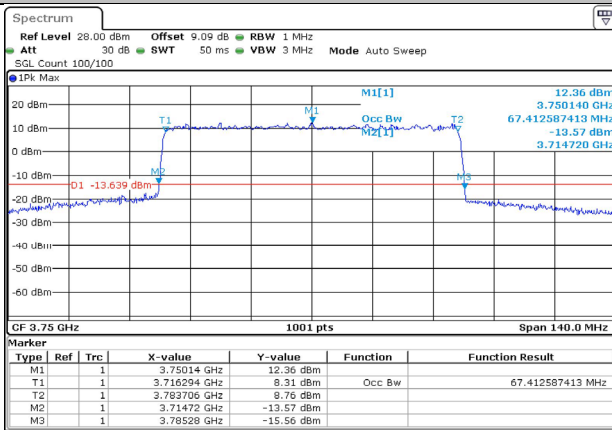
Date: 20 MAR 2025 20:04:32

MCH / CP-16QAM / Outer_Full



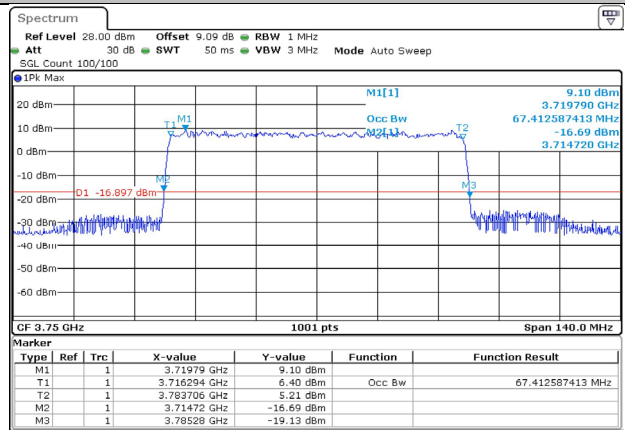
Date: 20 MAR 2025 20:04:39

MCH / CP-64QAM / Outer_Full



Date: 20 MAR 2025 20:04:47

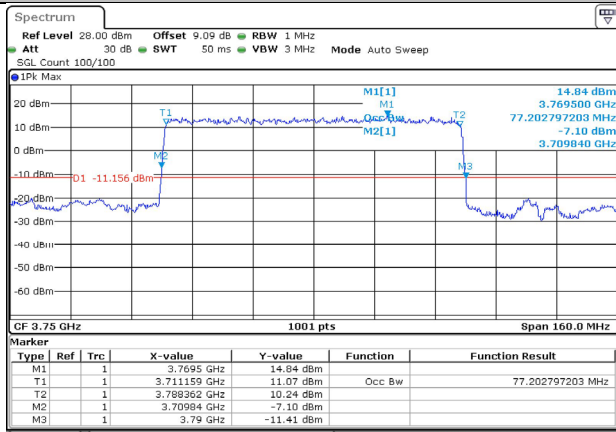
MCH / CP-256QAM / Outer_Full



Date: 20 MAR 2025 20:04:56

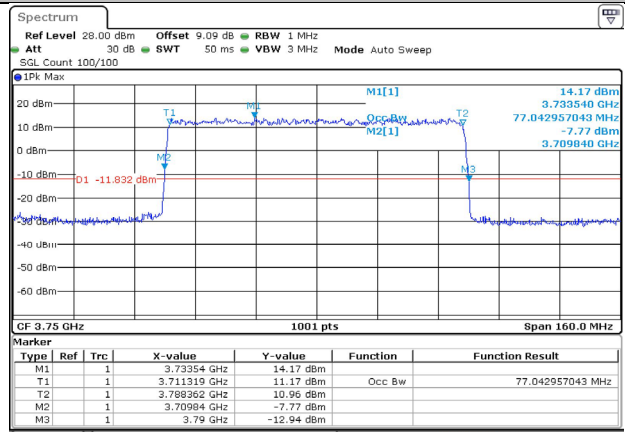
n78A / 30KHz / 80MHz

MCH / DFT-Pi2BPSK / Outer_Full



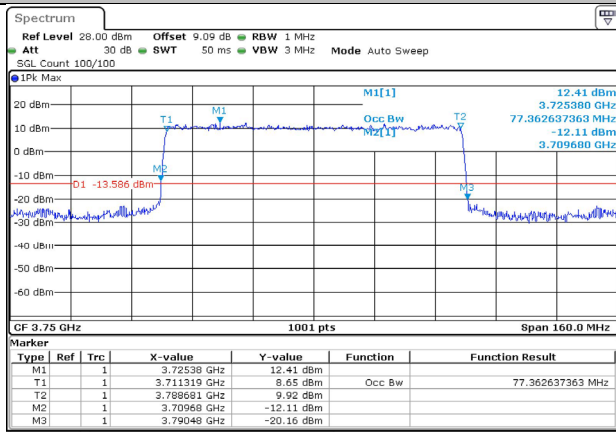
Date: 20 MAR 2025 20:05:17

MCH / DFT-QPSK / Outer_Full



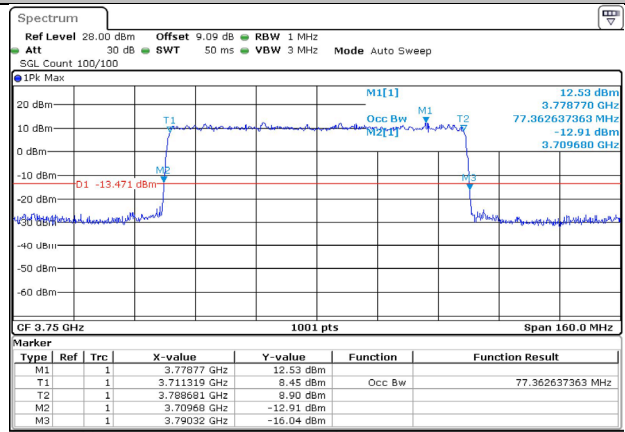
Date: 20 MAR 2025 20:05:41

MCH / CP-QPSK / Outer_Full



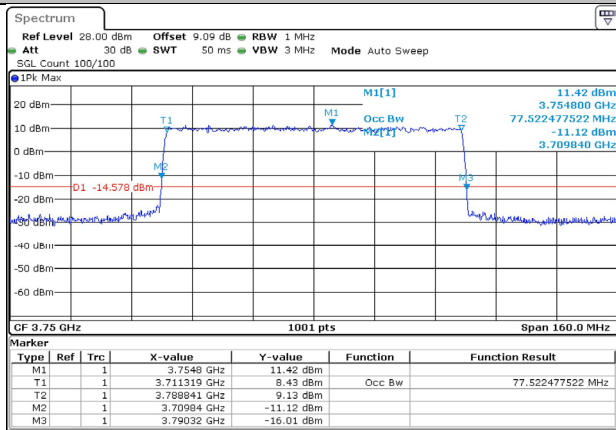
Date: 20 MAR 2025 20:06:18

MCH / CP-16QAM / Outer_Full



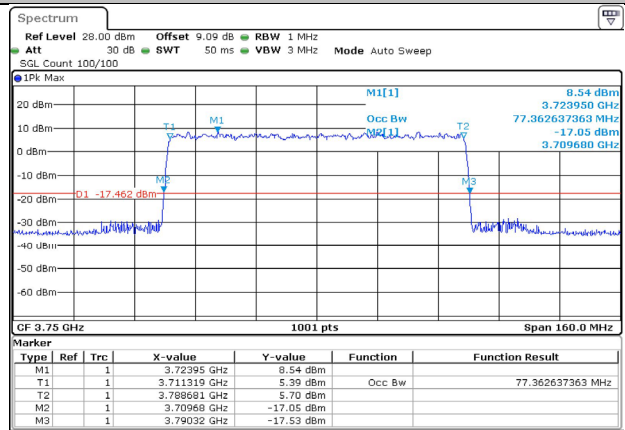
Date: 20 MAR 2025 20:06:26

MCH / CP-64QAM / Outer_Full



Date: 20 MAR 2025 20:06:33

MCH / CP-256QAM / Outer_Full



Date: 20 MAR 2025 20:06:43