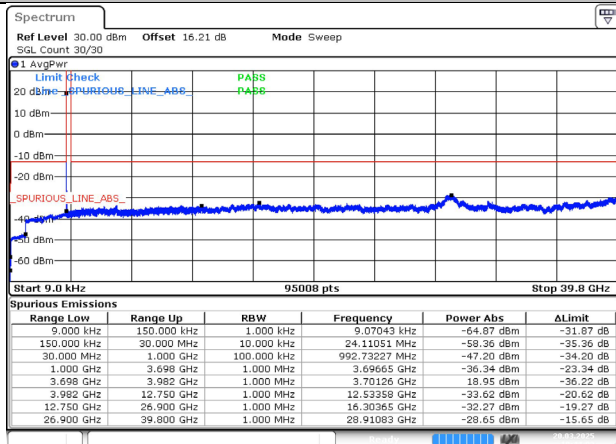


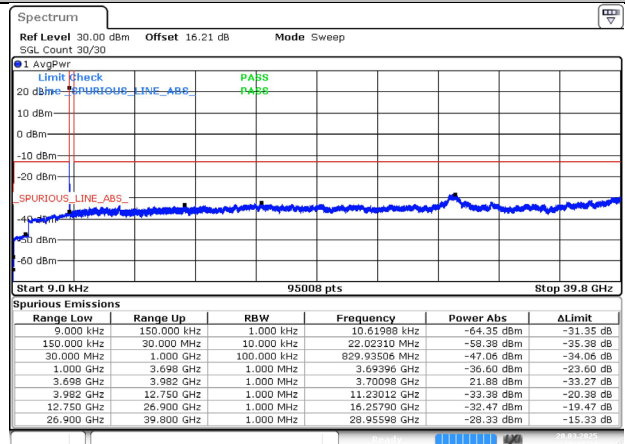
n77A / 30KHz / 20MHz

LCH / DFT-Pi2BPSK / Edge_1RB_Left



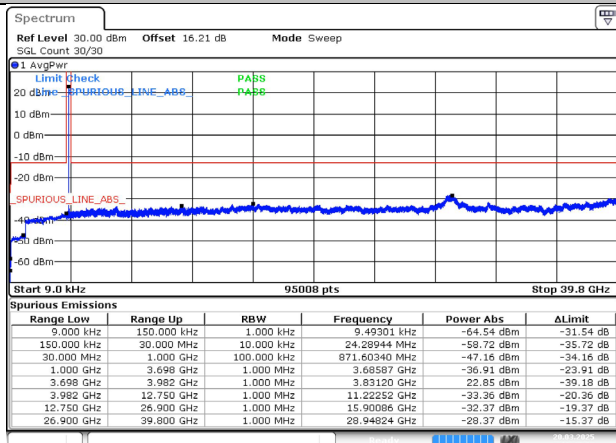
Date: 20 MAR 2025 18:44:02

LCH / DFT-QPSK / Edge_1RB_Left



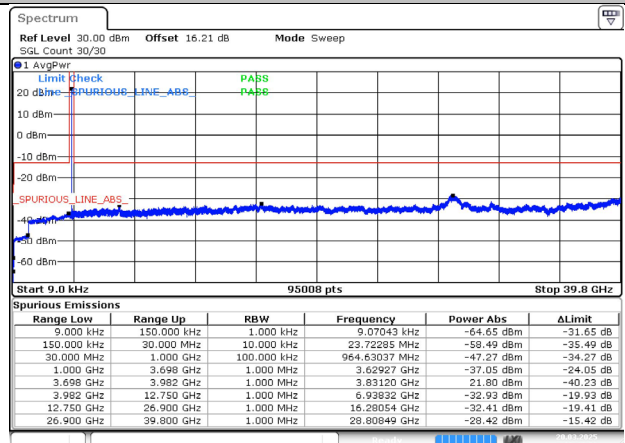
Date: 20 MAR 2025 18:44:33

MCH / DFT-Pi2BPSK / Edge_1RB_Left



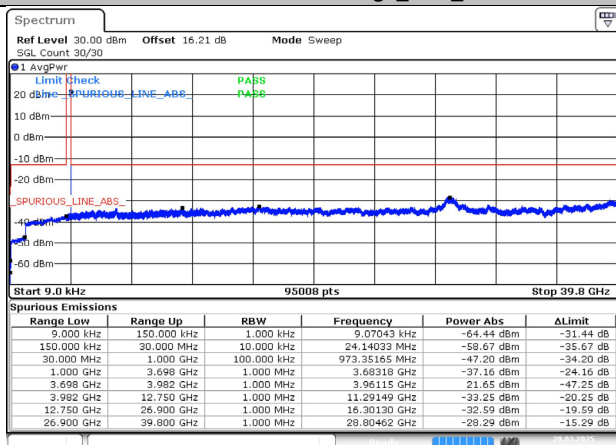
Date: 20 MAR 2025 18:45:05

MCH / DFT-QPSK / Edge_1RB_Left



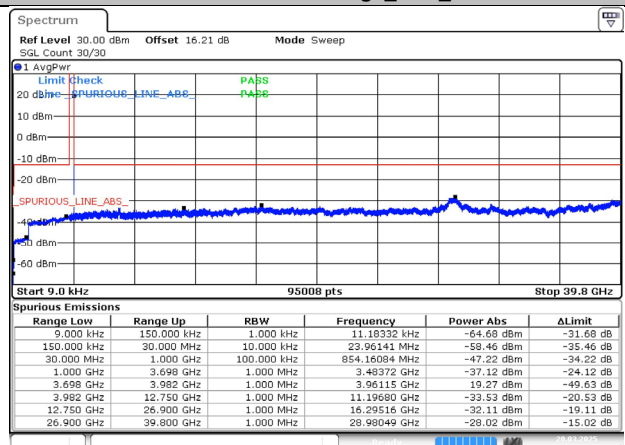
Date: 20 MAR 2025 18:45:37

HCH / DFT-Pi2BPSK / Edge_1RB_Left



Date: 20 MAR 2025 18:46:10

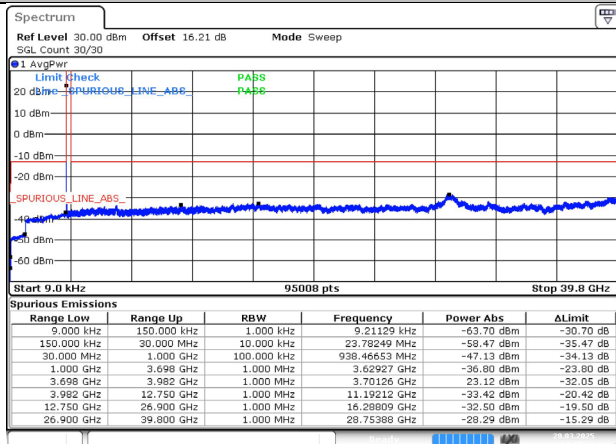
HCH / DFT-QPSK / Edge_1RB_Left



Date: 20 MAR 2025 18:46:47

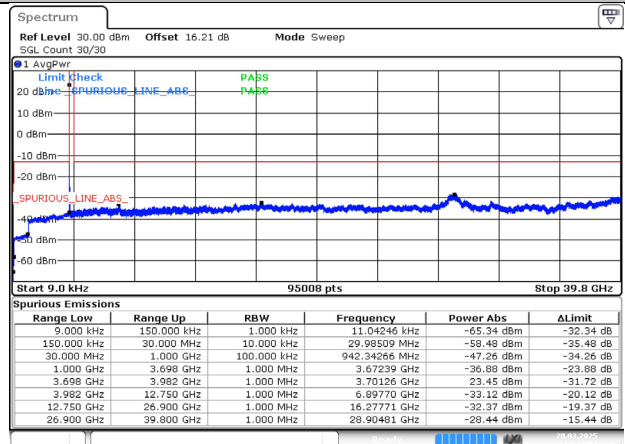
n77A / 30KHz / 25MHz

LCH / DFT-Pi2BPSK / Edge_1RB_Left



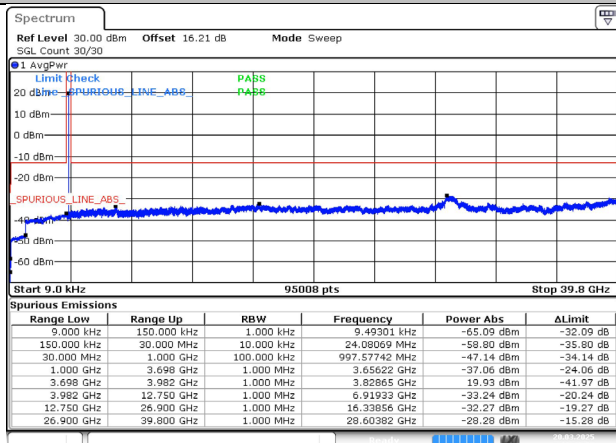
Date: 20 MAR 2025 18:47:21

LCH / DFT-QPSK / Edge_1RB_Left



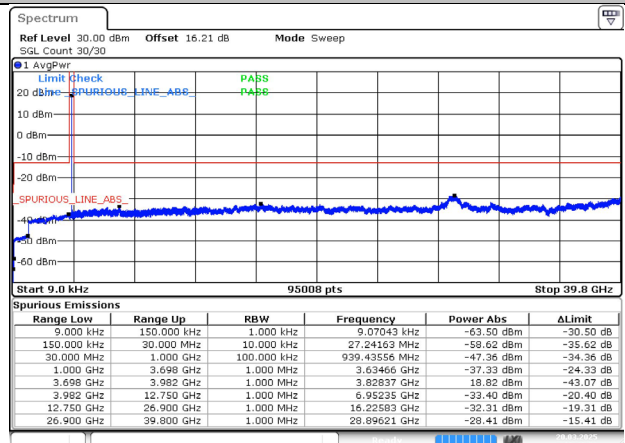
Date: 20 MAR 2025 18:47:52

MCH / DFT-Pi2BPSK / Edge_1RB_Left



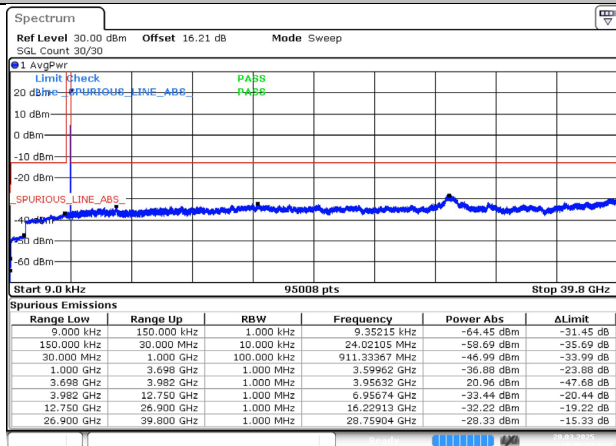
Date: 20 MAR 2025 18:48:25

MCH / DFT-QPSK / Edge_1RB_Left



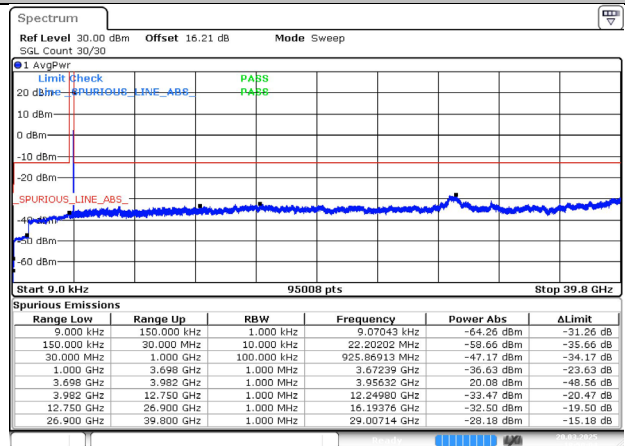
Date: 20 MAR 2025 18:48:55

HCH / DFT-Pi2BPSK / Edge_1RB_Left



Date: 20 MAR 2025 18:49:33

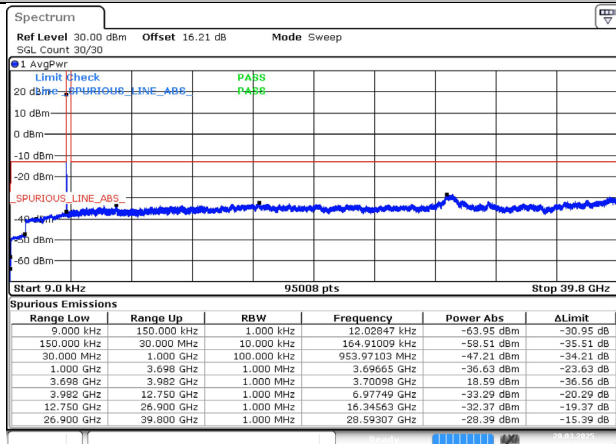
HCH / DFT-QPSK / Edge_1RB_Left



Date: 20 MAR 2025 18:50:04

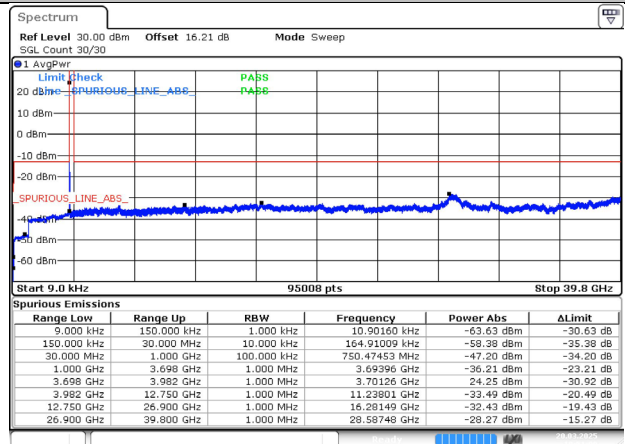
n77A / 30KHz / 30MHz

LCH / DFT-Pi2BPSK / Edge_1RB_Left



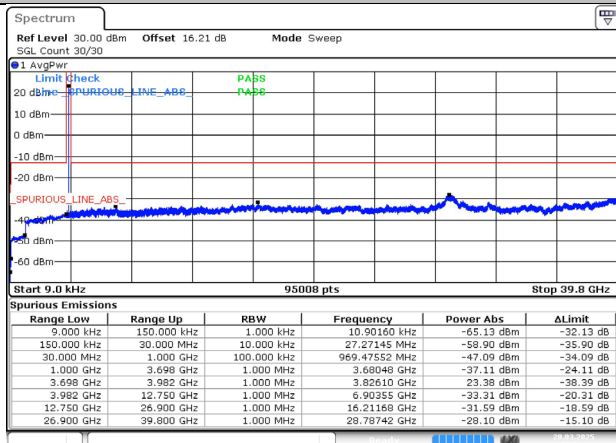
Date: 20 MAR 2025 18:50:38

LCH / DFT-QPSK / Edge_1RB_Left



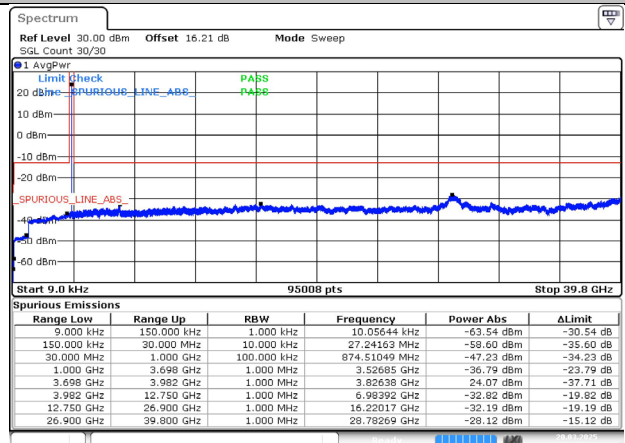
Date: 20 MAR 2025 18:51:09

MCH / DFT-Pi2BPSK / Edge_1RB_Left



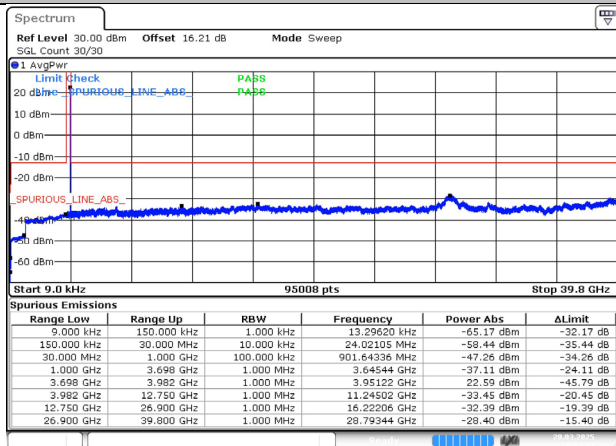
Date: 20 MAR 2025 18:51:41

MCH / DFT-QPSK / Edge_1RB_Left



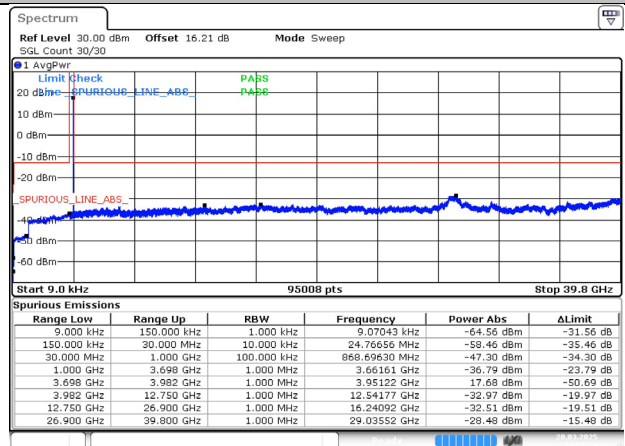
Date: 20 MAR 2025 18:52:18

HCH / DFT-Pi2BPSK / Edge_1RB_Left



Date: 20 MAR 2025 18:52:50

HCH / DFT-QPSK / Edge_1RB_Left



Date: 20 MAR 2025 18:53:21

