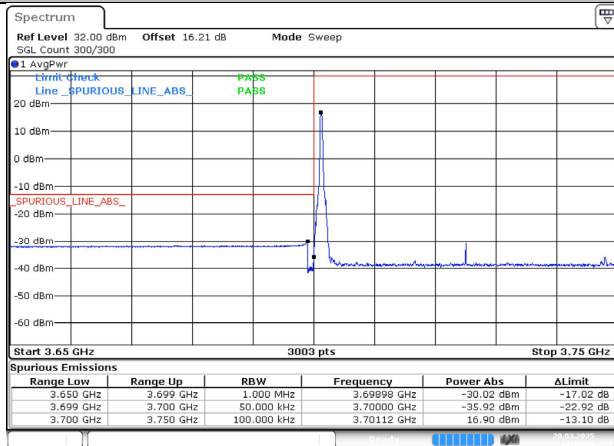


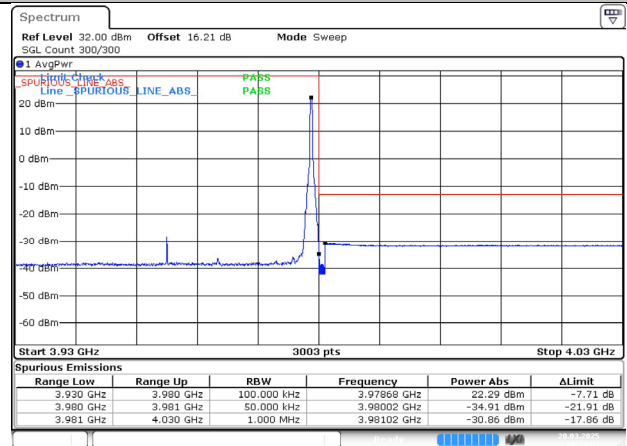
n77A / 30KHz / 50MHz

LCH / DFT-Pi2BPSK / Edge_1RB_Left



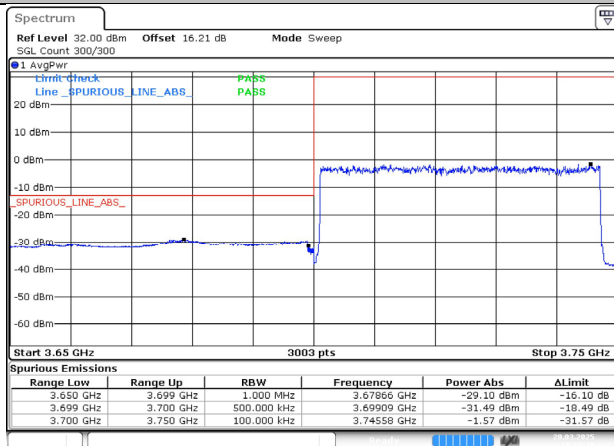
Date: 20 MAR 2025 18:12:58

HCH / DFT-Pi2BPSK / Edge_1RB_Right



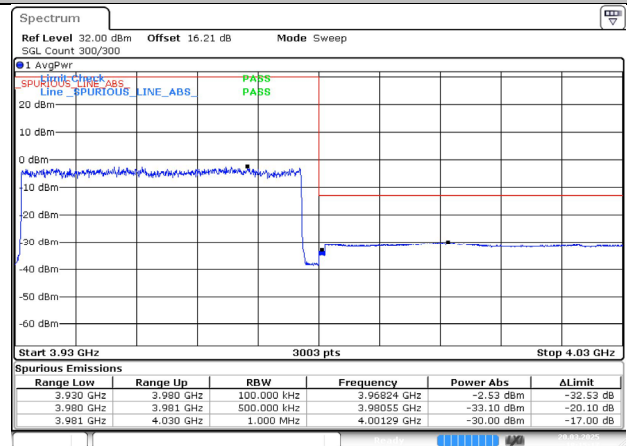
Date: 20 MAR 2025 18:15:04

LCH / DFT-Pi2BPSK / Outer_Full



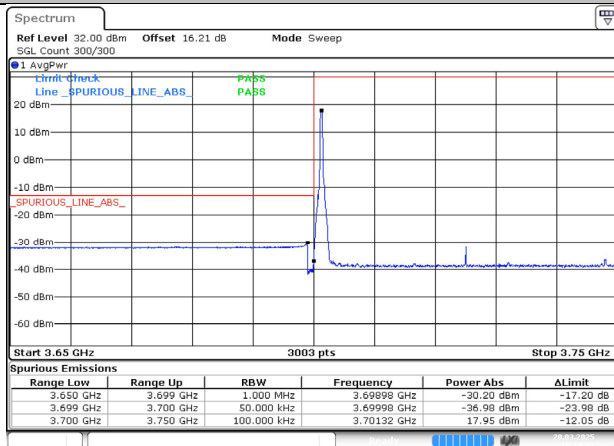
Date: 20 MAR 2025 18:13:10

HCH / DFT-Pi2BPSK / Outer_Full



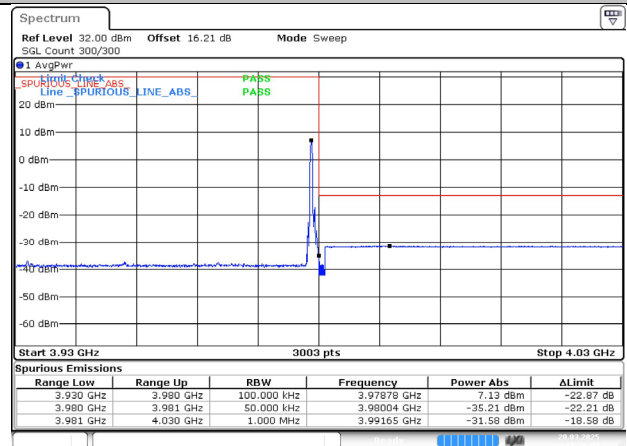
Date: 20 MAR 2025 18:15:16

LCH / DFT-QPSK / Edge_1RB_Left

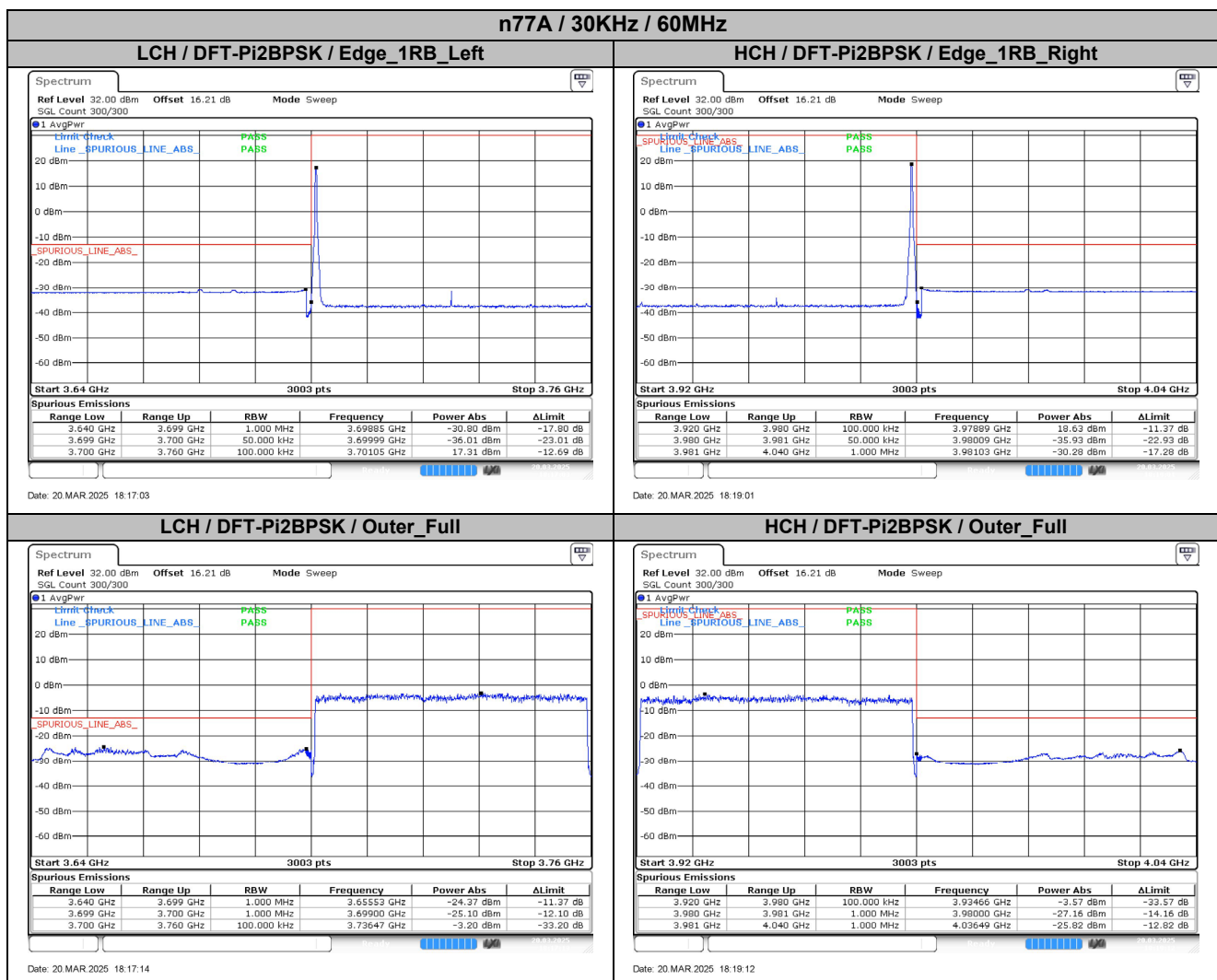
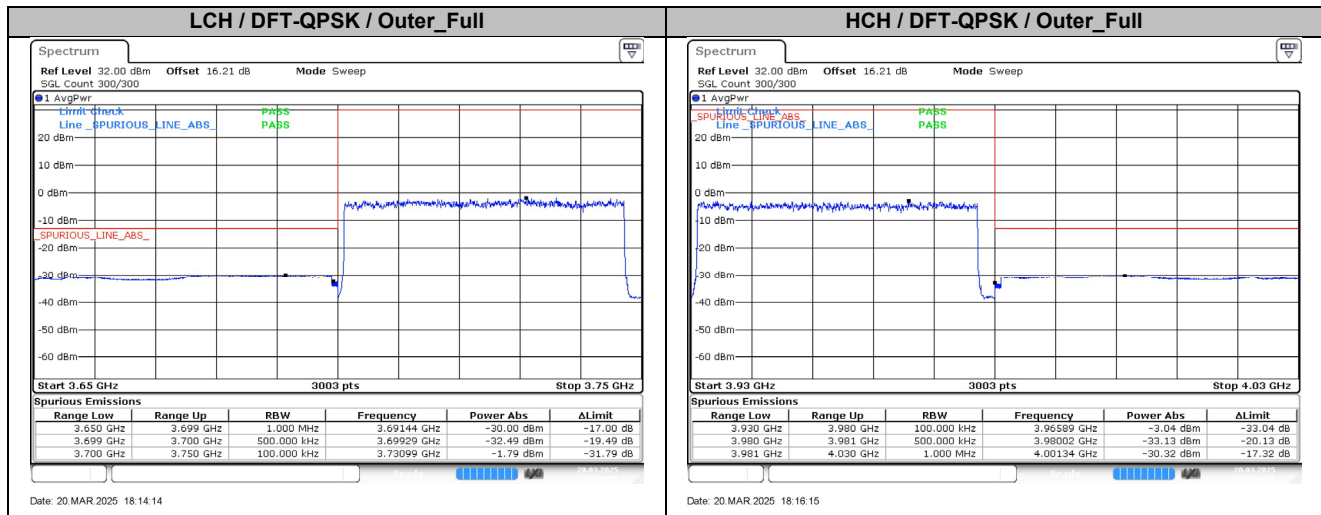


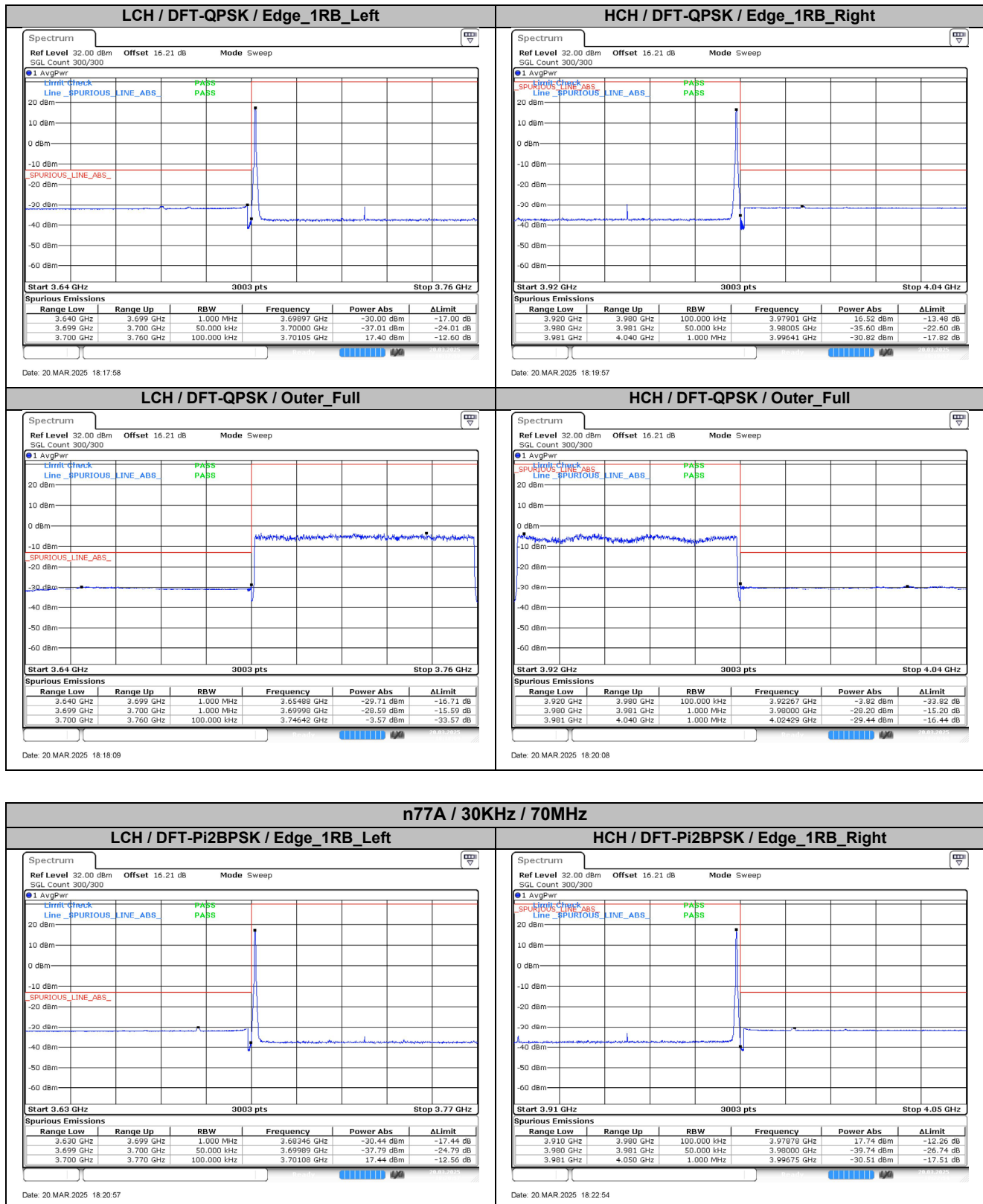
Date: 20 MAR 2025 18:14:02

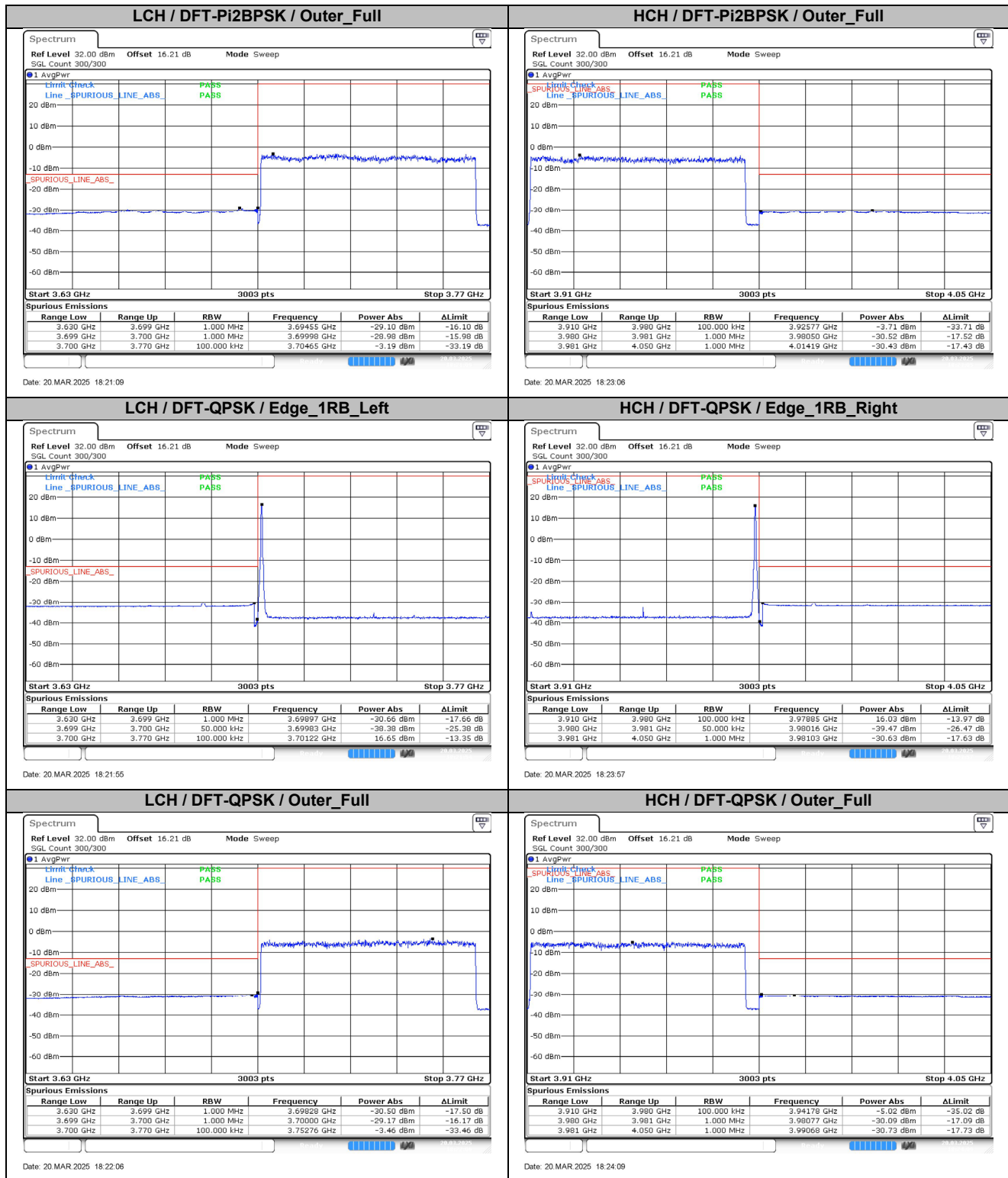
HCH / DFT-QPSK / Edge_1RB_Right



Date: 20 MAR 2025 18:16:03

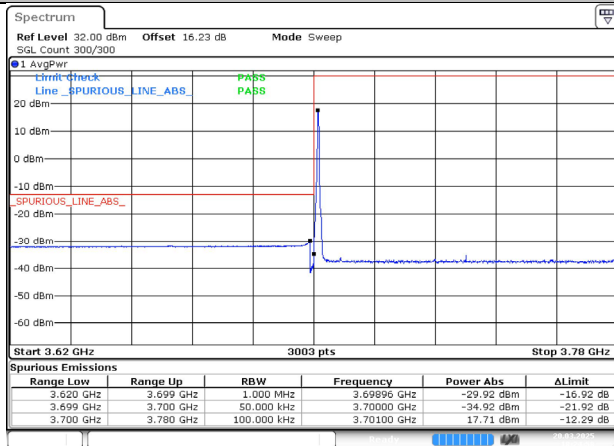




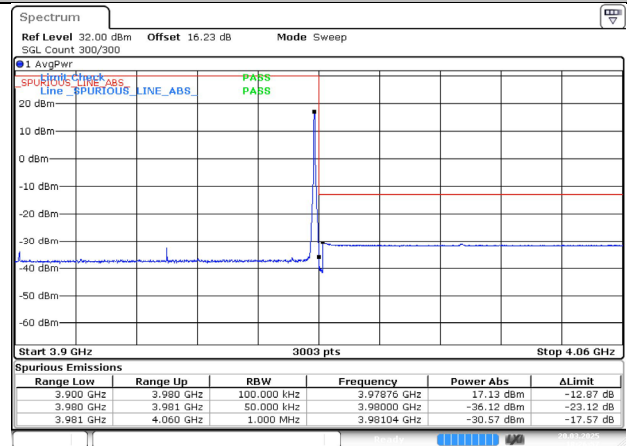


n77A / 30KHz / 80MHz

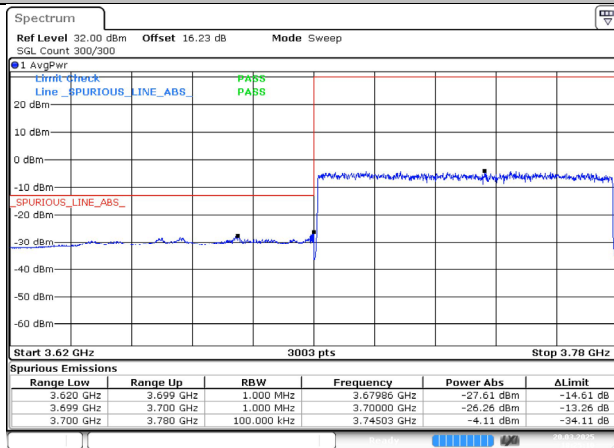
LCH / DFT-Pi2BPSK / Edge_1RB_Left



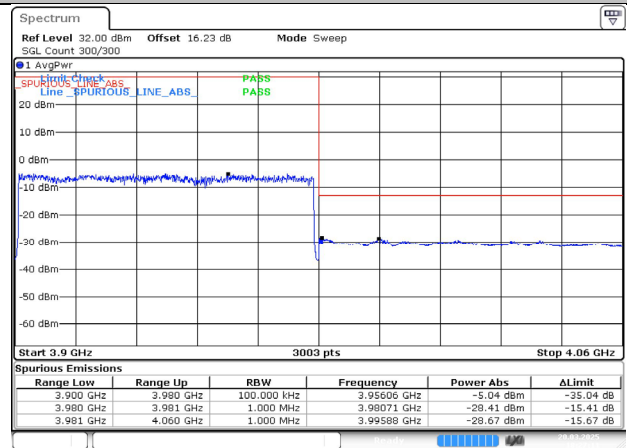
HCH / DFT-Pi2BPSK / Edge_1RB_Right



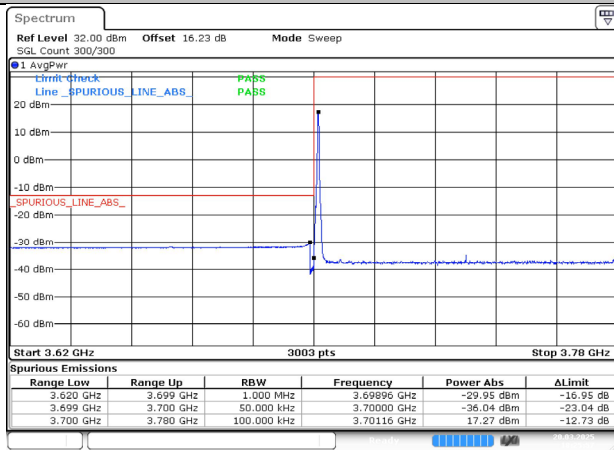
LCH / DFT-Pi2BPSK / Outer_Full



HCH / DFT-Pi2BPSK / Outer_Full



LCH / DFT-QPSK / Edge_1RB_Left



HCH / DFT-QPSK / Edge_1RB_Right

