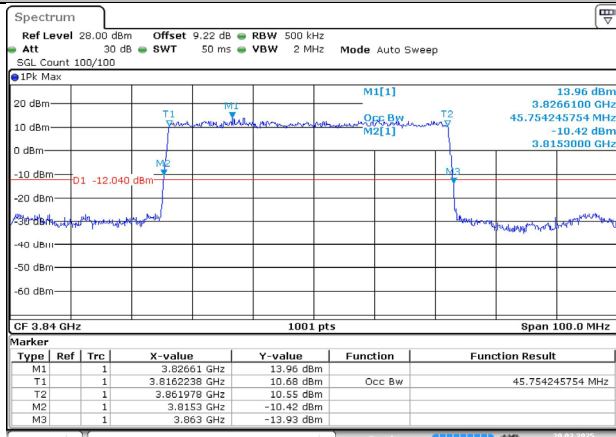


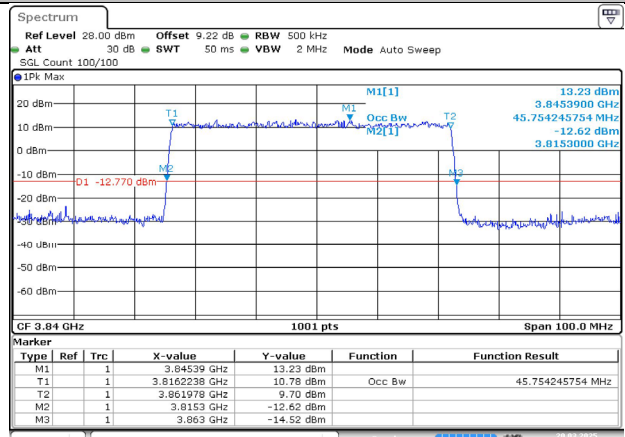
n77A / 30KHz / 50MHz

MCH / DFT-Pi2BPSK / Outer_Full



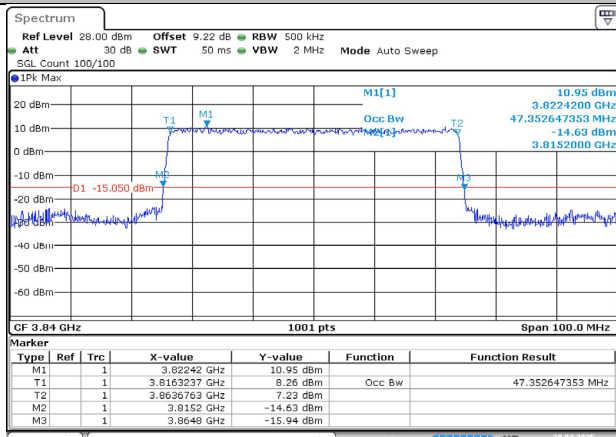
Date: 20 MAR 2025 17:39:54

MCH / DFT-QPSK / Outer_Full



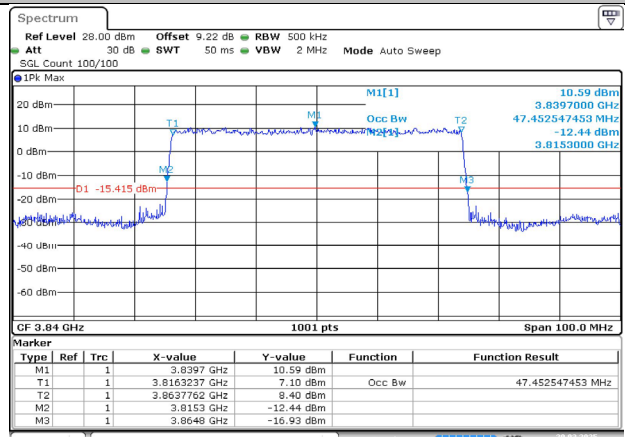
Date: 20 MAR 2025 17:40:12

MCH / CP-QPSK / Outer_Full



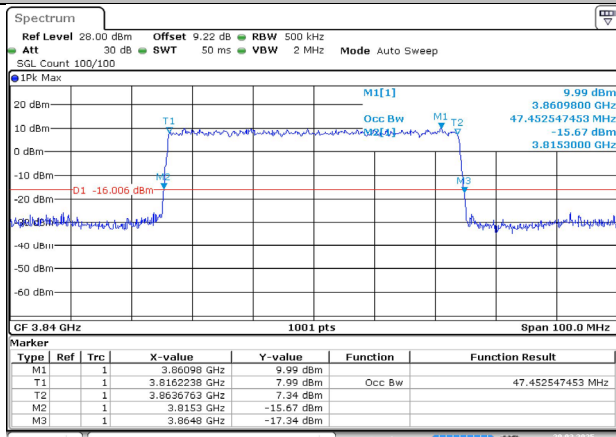
Date: 20 MAR 2025 17:40:48

MCH / CP-16QAM / Outer_Full



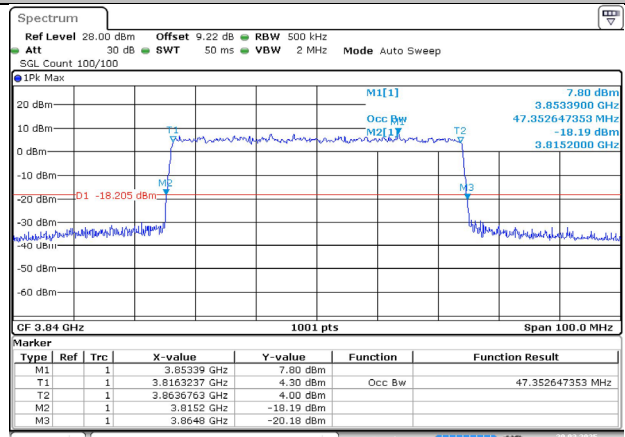
Date: 20 MAR 2025 17:40:56

MCH / CP-64QAM / Outer_Full



Date: 20 MAR 2025 17:41:04

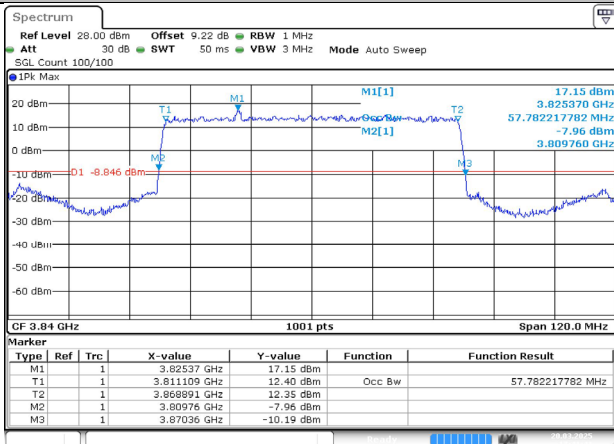
MCH / CP-256QAM / Outer_Full



Date: 20 MAR 2025 17:41:14

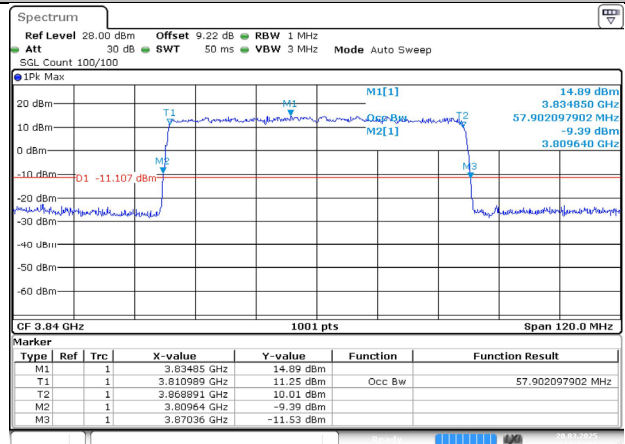
n77A / 30KHz / 60MHz

MCH / DFT-Pi2BPSK / Outer_Full



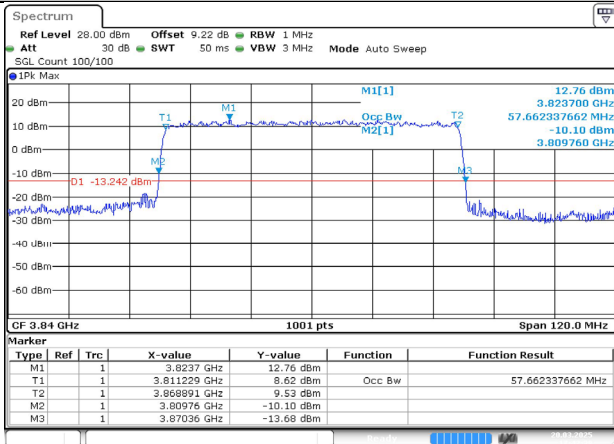
Date: 20 MAR 2025 17:41:41

MCH / DFT-QPSK / Outer_Full



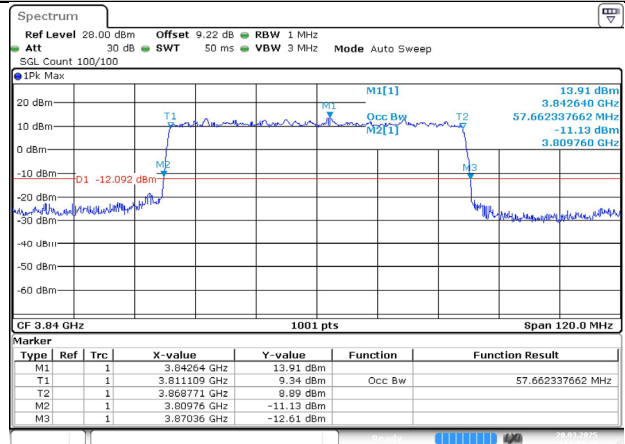
Date: 20 MAR 2025 17:42:01

MCH / CP-QPSK / Outer_Full



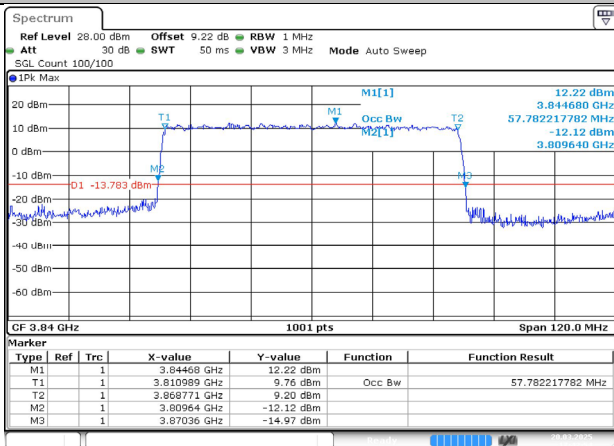
Date: 20 MAR 2025 17:42:38

MCH / CP-16QAM / Outer_Full



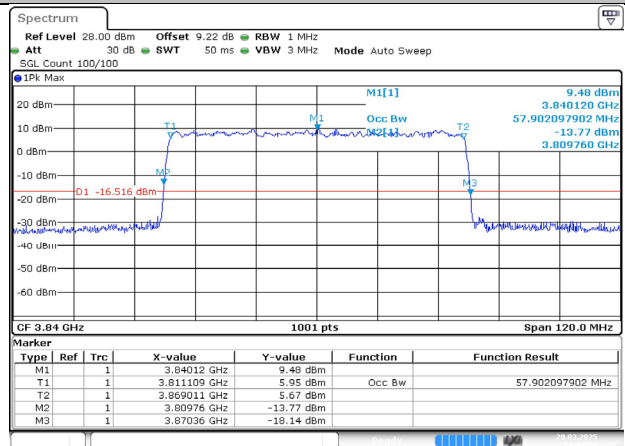
Date: 20 MAR 2025 17:42:46

MCH / CP-64QAM / Outer_Full



Date: 20 MAR 2025 17:42:54

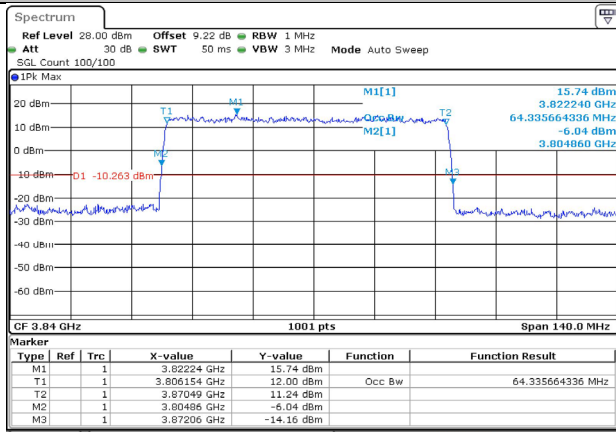
MCH / CP-256QAM / Outer_Full



Date: 20 MAR 2025 17:43:03

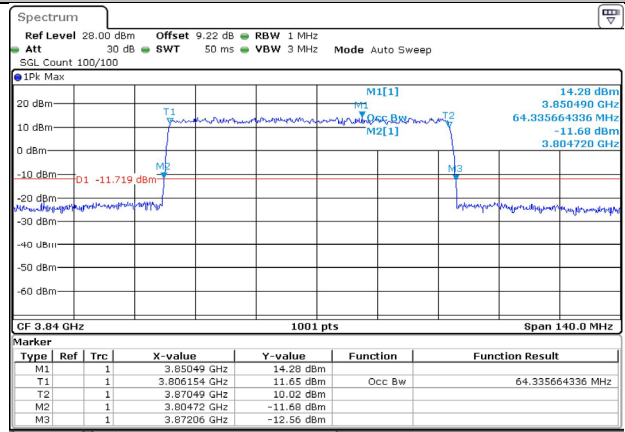
n77A / 30KHz / 70MHz

MCH / DFT-Pi2BPSK / Outer_Full



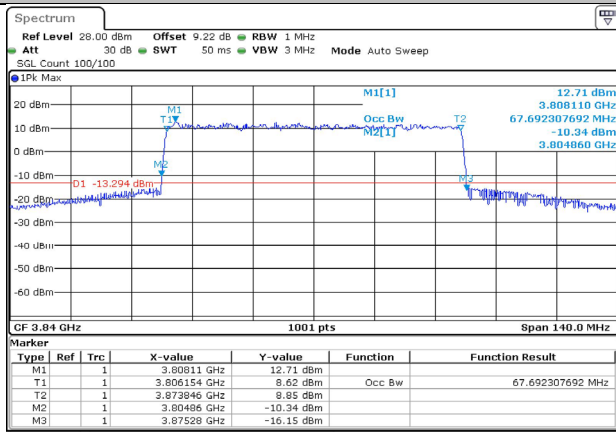
Date: 20 MAR 2025 17:43:25

MCH / DFT-QPSK / Outer_Full



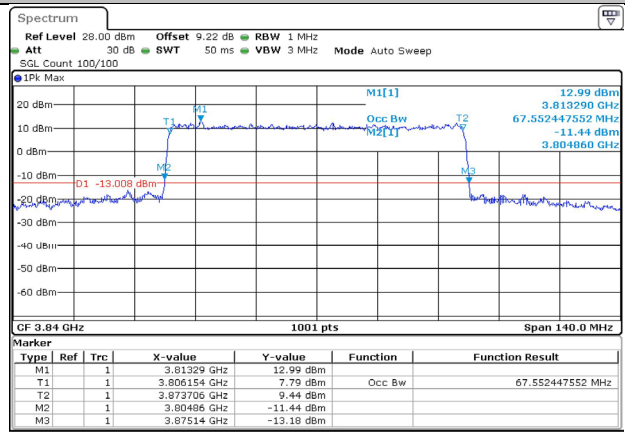
Date: 20 MAR 2025 17:43:43

MCH / CP-QPSK / Outer_Full



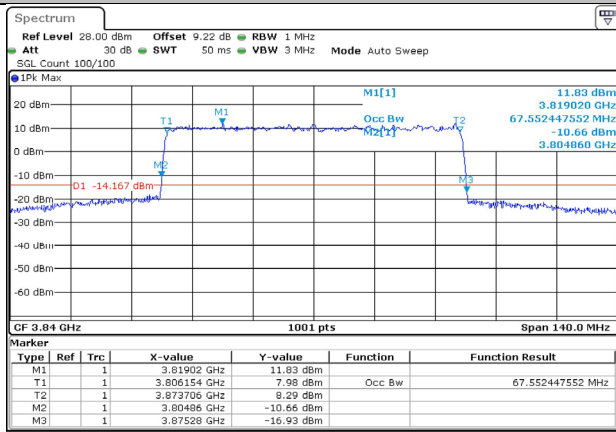
Date: 20 MAR 2025 17:44:21

MCH / CP-16QAM / Outer_Full



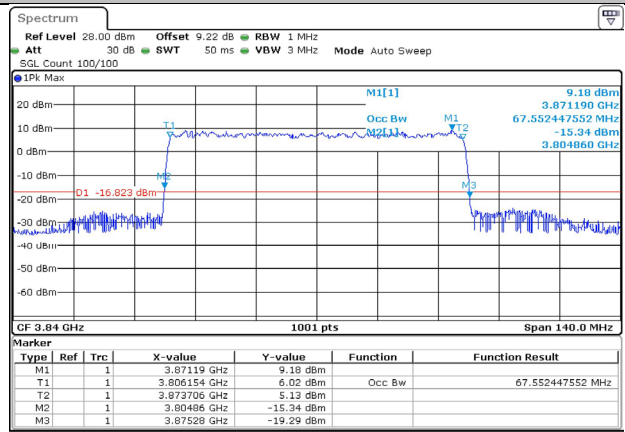
Date: 20 MAR 2025 17:44:29

MCH / CP-64QAM / Outer_Full



Date: 20 MAR 2025 17:44:37

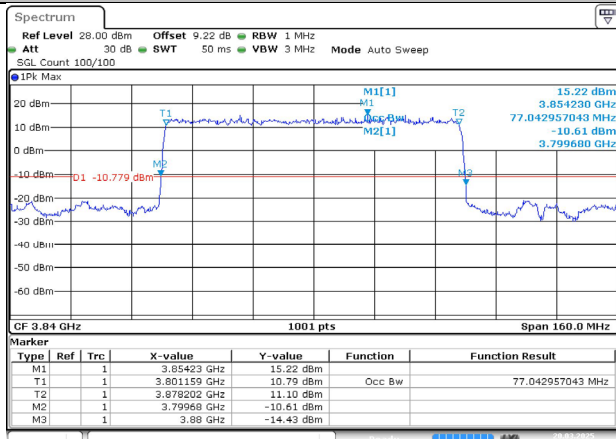
MCH / CP-256QAM / Outer_Full



Date: 20 MAR 2025 17:44:47

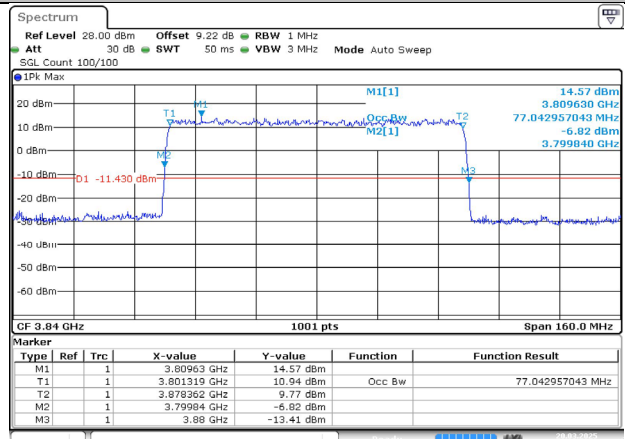
n77A / 30KHz / 80MHz

MCH / DFT-Pi2BPSK / Outer_Full



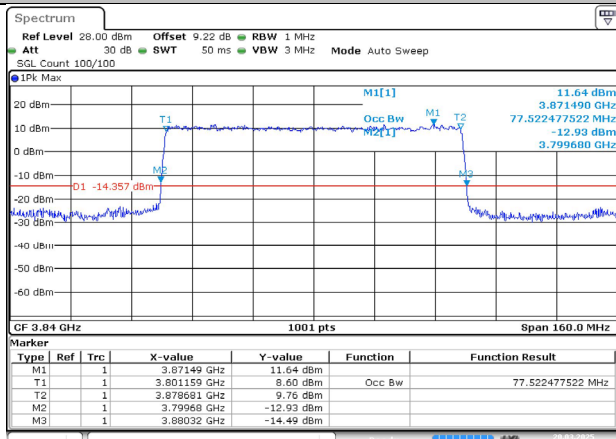
Date: 20 MAR 2025 17:45:09

MCH / DFT-QPSK / Outer_Full



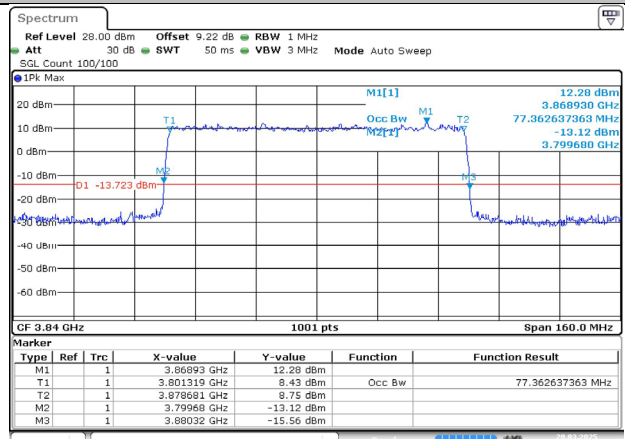
Date: 20 MAR 2025 17:45:34

MCH / CP-QPSK / Outer_Full



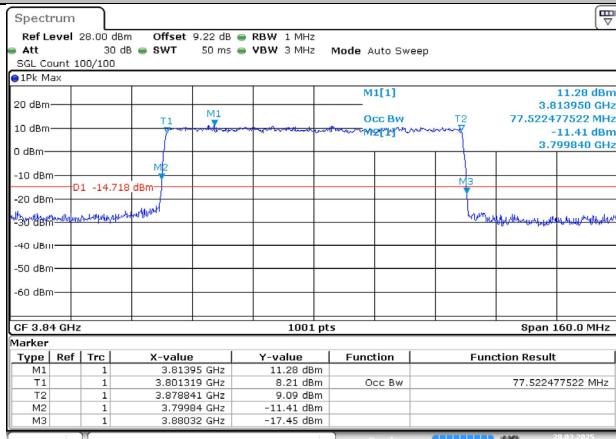
Date: 20 MAR 2025 17:46:12

MCH / CP-16QAM / Outer_Full



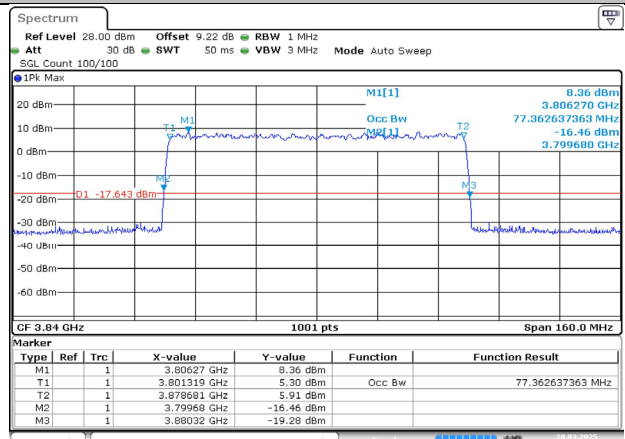
Date: 20 MAR 2025 17:46:21

MCH / CP-64QAM / Outer_Full



Date: 20 MAR 2025 17:46:29

MCH / CP-256QAM / Outer_Full



Date: 20 MAR 2025 17:46:39