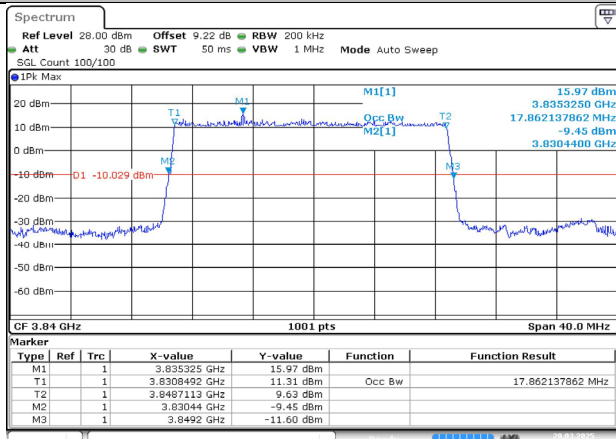


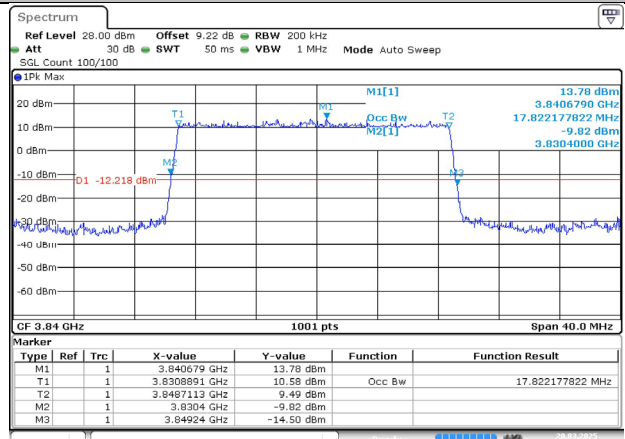
n77A / 30KHz / 20MHz

MCH / DFT-Pi2BPSK / Outer_Full



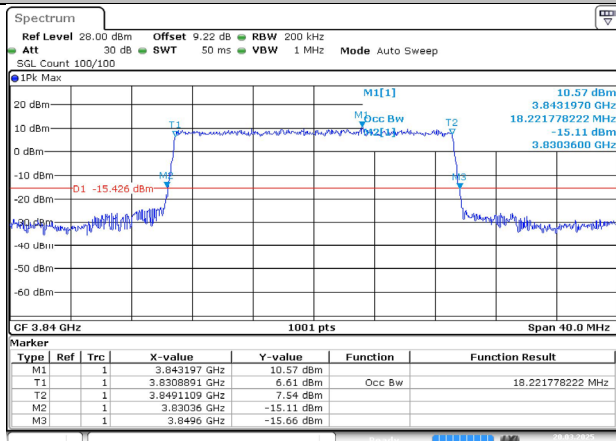
Date: 20 MAR 2025 17:32:50

MCH / DFT-QPSK / Outer_Full



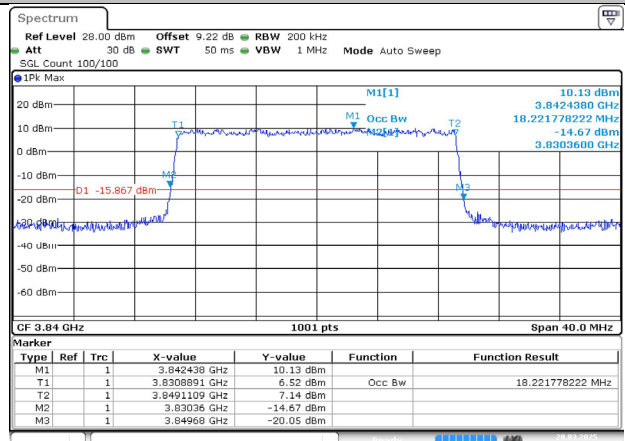
Date: 20 MAR 2025 17:33:10

MCH / CP-QPSK / Outer_Full



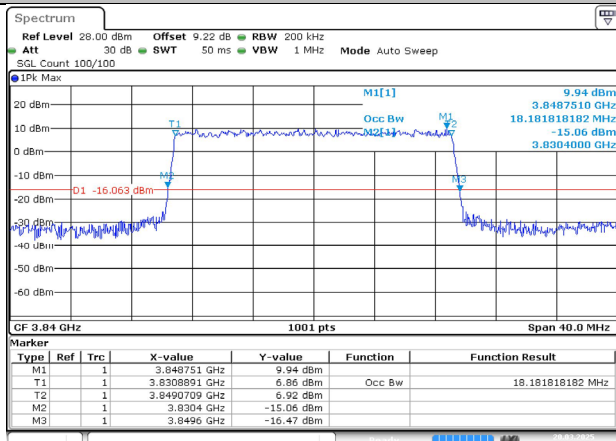
Date: 20 MAR 2025 17:33:54

MCH / CP-16QAM / Outer_Full



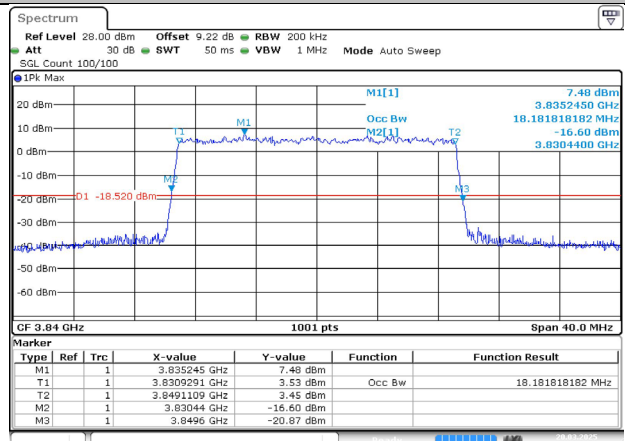
Date: 20 MAR 2025 17:34:03

MCH / CP-64QAM / Outer_Full



Date: 20 MAR 2025 17:34:13

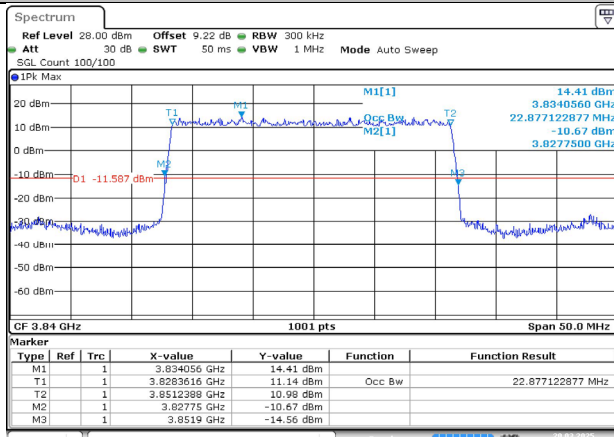
MCH / CP-256QAM / Outer_Full



Date: 20 MAR 2025 17:34:24

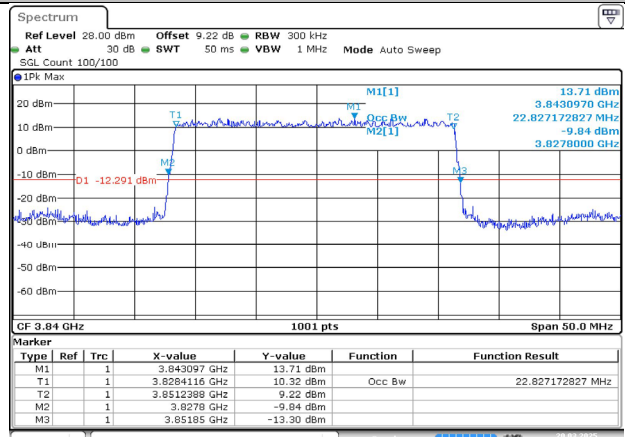
n77A / 30KHz / 25MHz

MCH / DFT-Pi2BPSK / Outer_Full



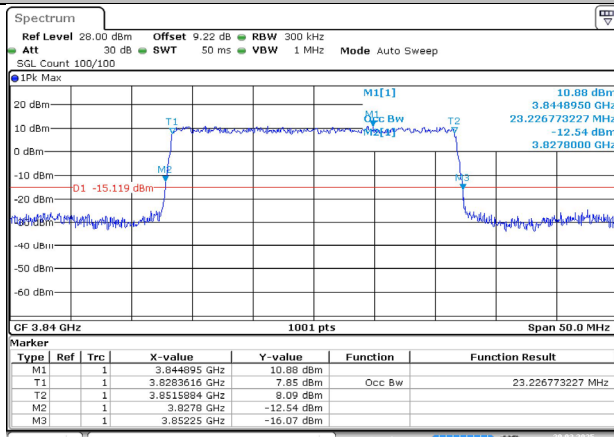
Date: 20 MAR 2025 17:34:45

MCH / DFT-QPSK / Outer_Full



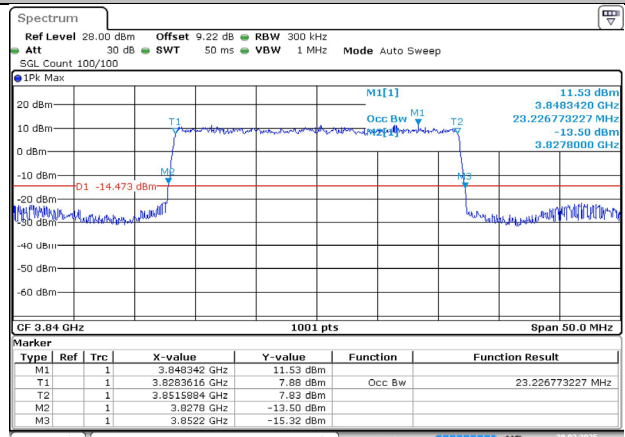
Date: 20 MAR 2025 17:35:03

MCH / CP-QPSK / Outer_Full



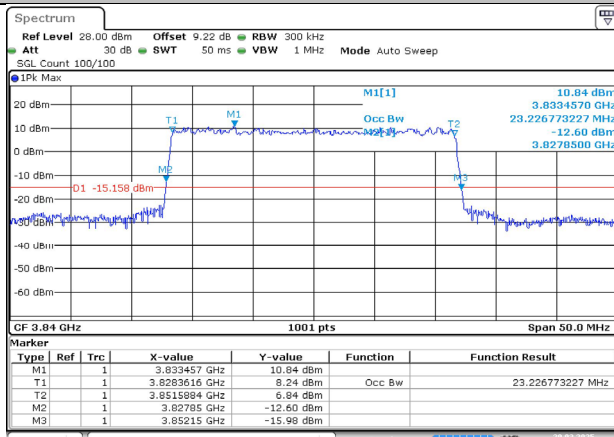
Date: 20 MAR 2025 17:35:40

MCH / CP-16QAM / Outer_Full



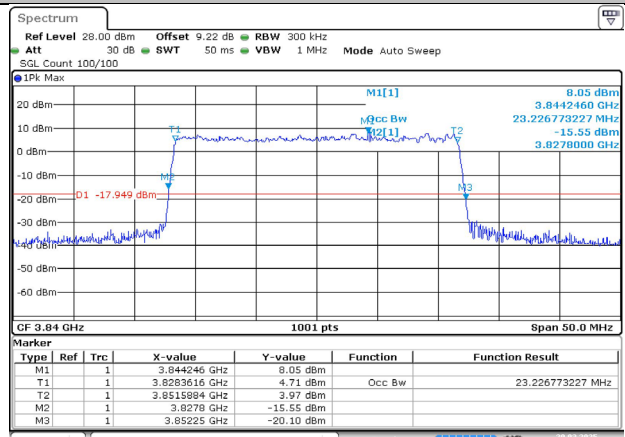
Date: 20 MAR 2025 17:35:48

MCH / CP-64QAM / Outer_Full



Date: 20 MAR 2025 17:35:56

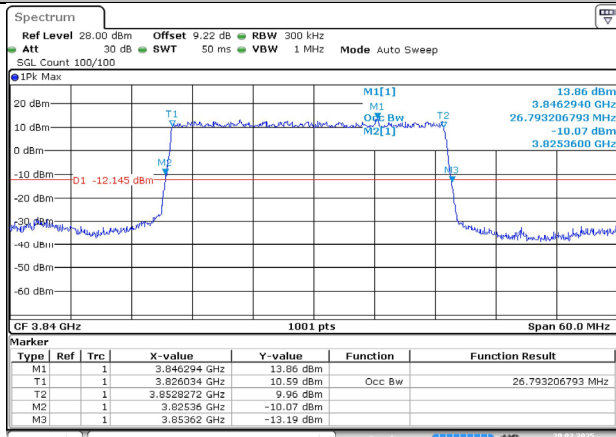
MCH / CP-256QAM / Outer_Full



Date: 20 MAR 2025 17:36:05

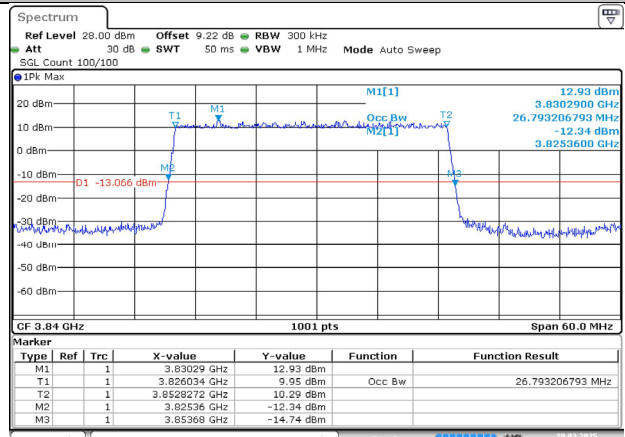
n77A / 30KHz / 30MHz

MCH / DFT-Pi2BPSK / Outer_Full



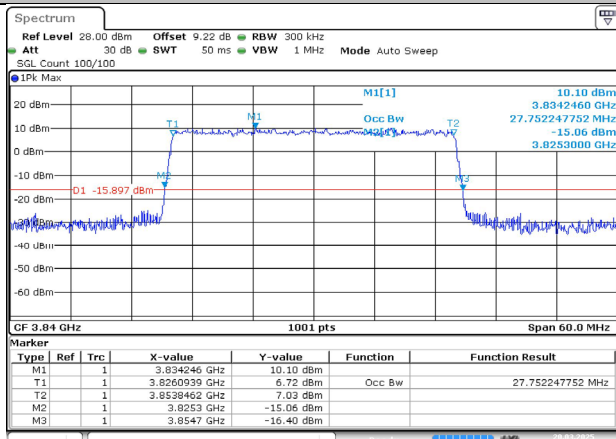
Date: 20 MAR 2025 17:36:25

MCH / DFT-QPSK / Outer_Full



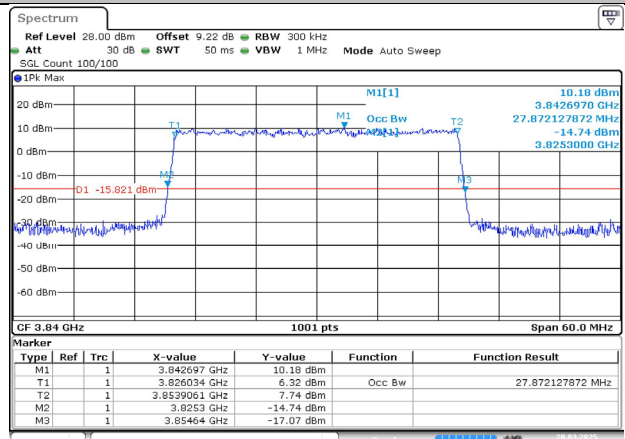
Date: 20 MAR 2025 17:36:50

MCH / CP-QPSK / Outer_Full



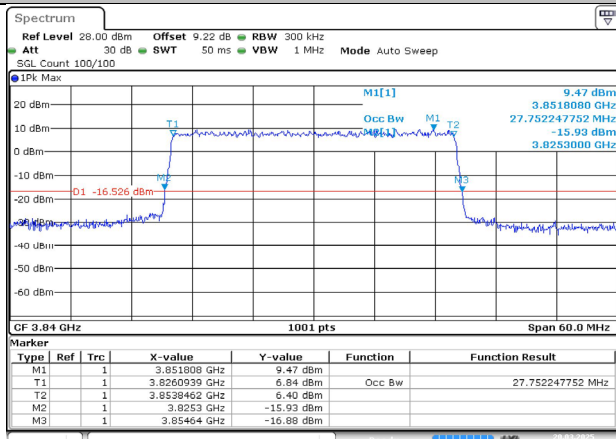
Date: 20 MAR 2025 17:37:25

MCH / CP-16QAM / Outer_Full



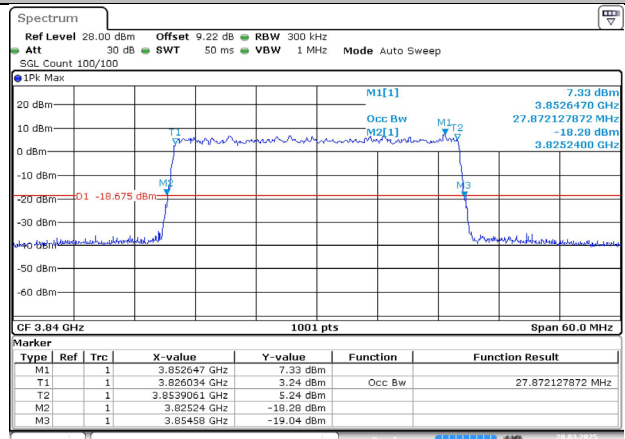
Date: 20 MAR 2025 17:37:33

MCH / CP-64QAM / Outer_Full



Date: 20 MAR 2025 17:37:41

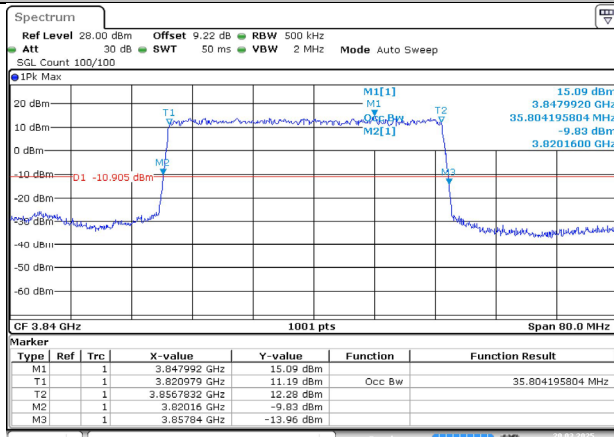
MCH / CP-256QAM / Outer_Full



Date: 20 MAR 2025 17:37:50

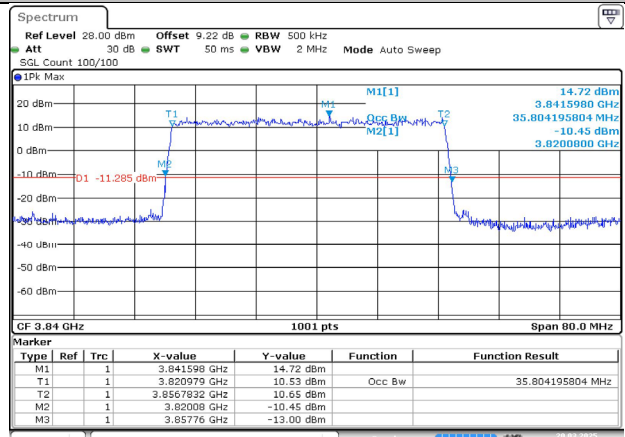
n77A / 30KHz / 40MHz

MCH / DFT-Pi2BPSK / Outer_Full



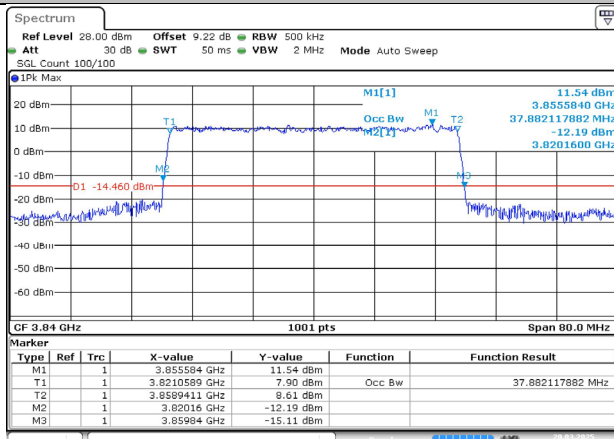
Date: 20 MAR 2025 17:38:11

MCH / DFT-QPSK / Outer_Full



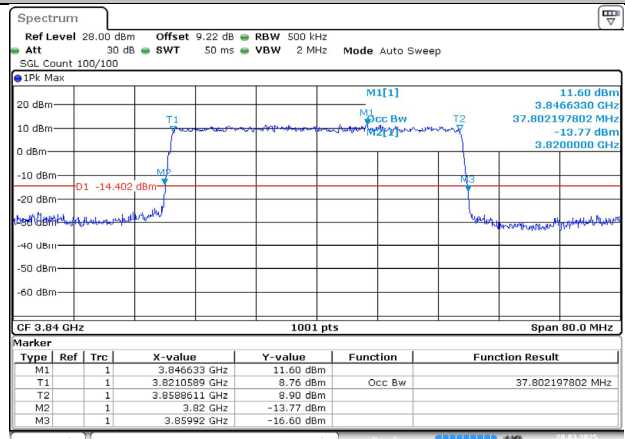
Date: 20 MAR 2025 17:38:30

MCH / CP-QPSK / Outer_Full



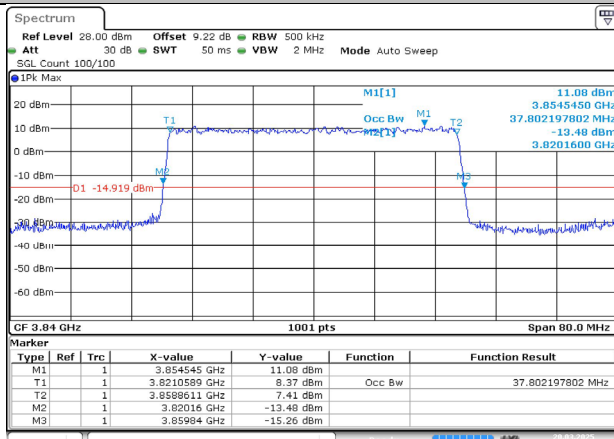
Date: 20 MAR 2025 17:39:06

MCH / CP-16QAM / Outer_Full



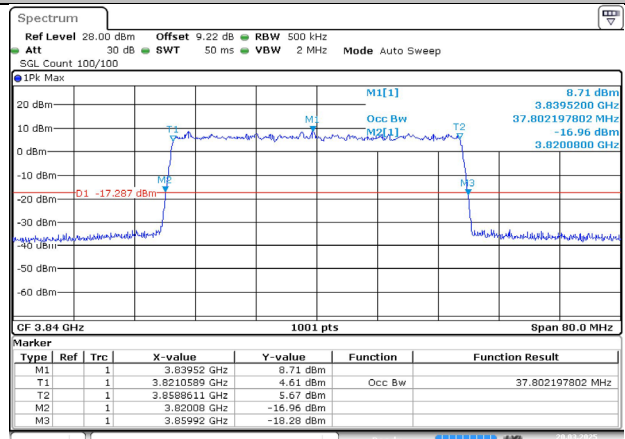
Date: 20 MAR 2025 17:39:14

MCH / CP-64QAM / Outer_Full



Date: 20 MAR 2025 17:39:22

MCH / CP-256QAM / Outer_Full



Date: 20 MAR 2025 17:39:31