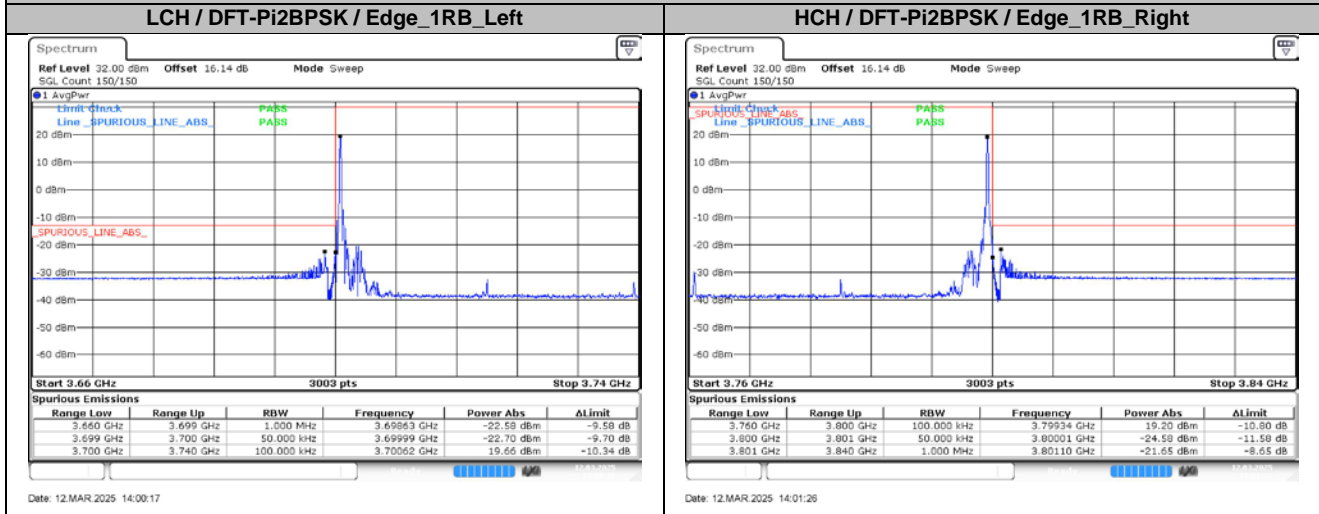
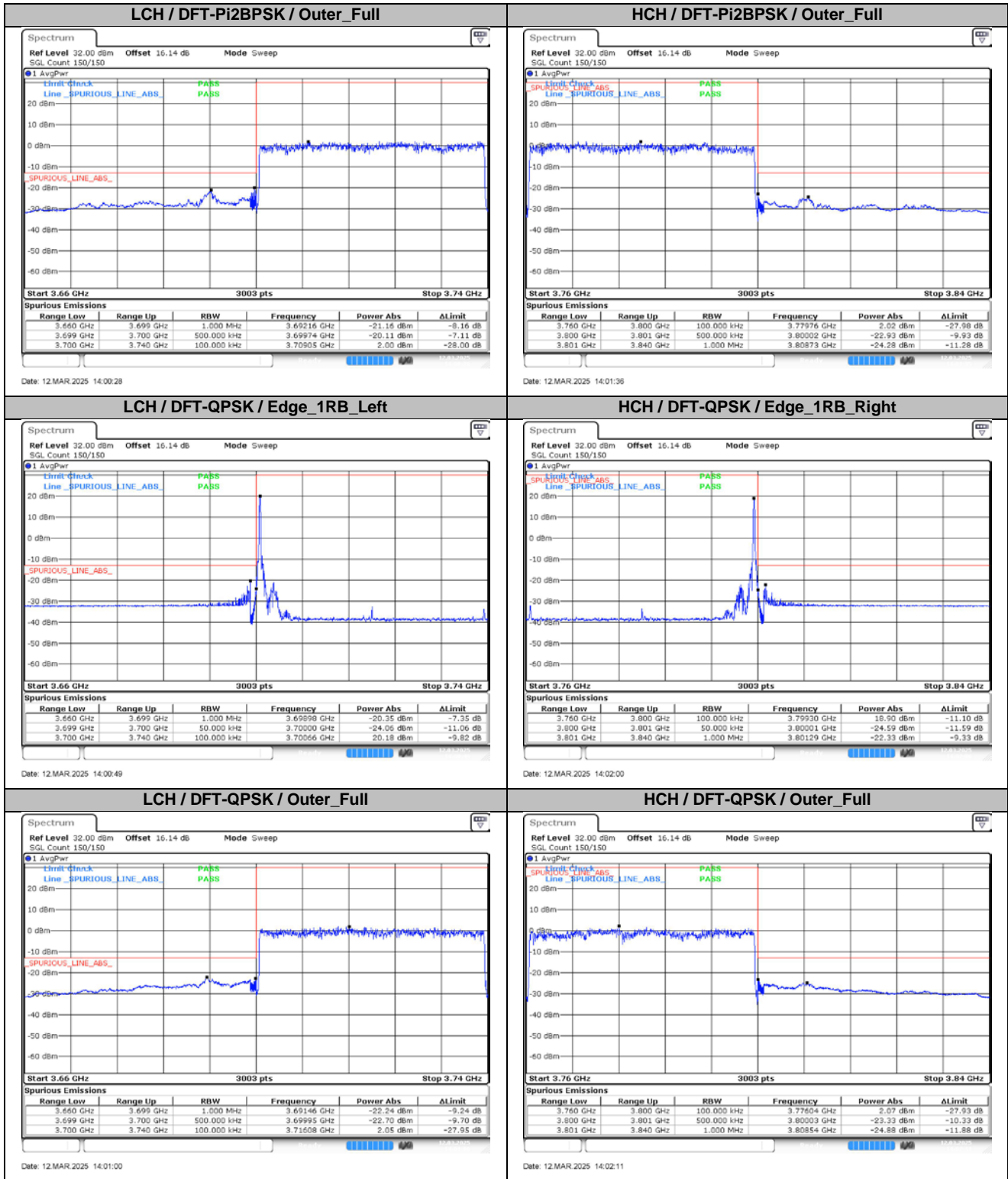


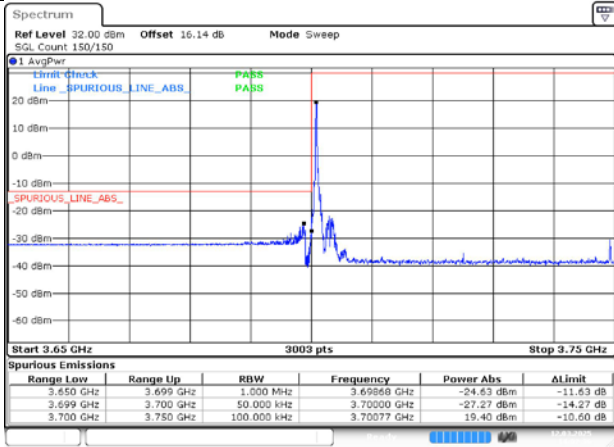
n78A / 15KHz / 40MHz





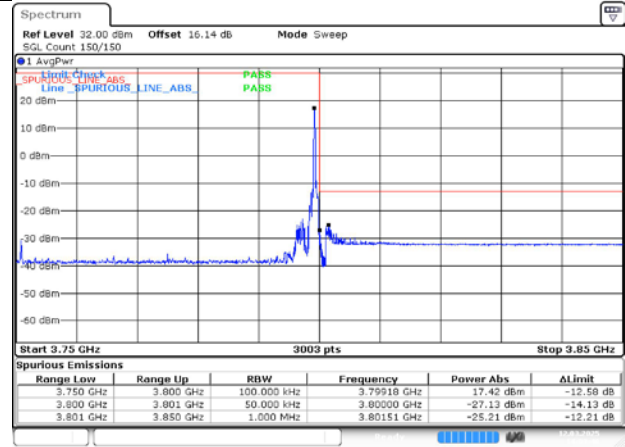
n78A / 15KHz / 50MHz

LCH / DFT-Pi2BPSK / Edge_1RB_Left



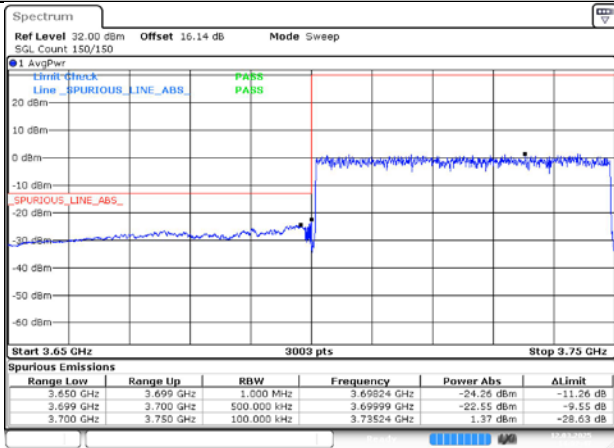
Date: 12.MAR.2025 14:02:36

HCH / DFT-Pi2BPSK / Edge_1RB_Right



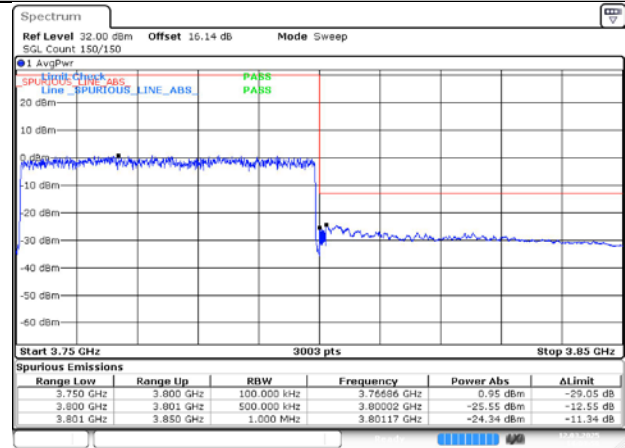
Date: 12.MAR.2025 14:03:48

LCH / DFT-Pi2BPSK / Outer_Full



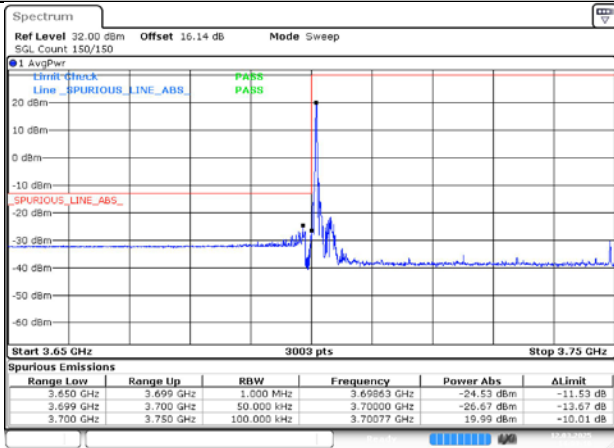
Date: 12.MAR.2025 14:02:48

HCH / DFT-Pi2BPSK / Outer_Full



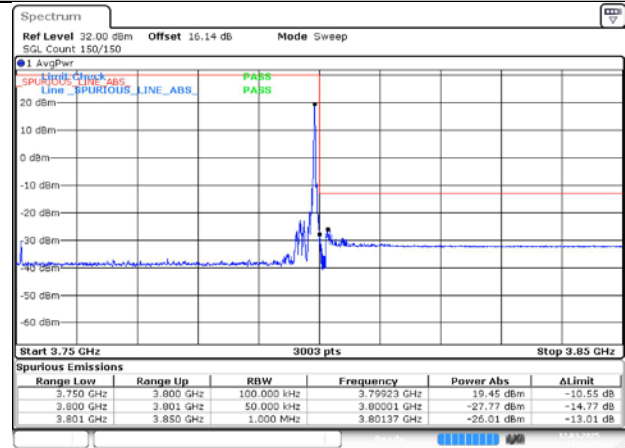
Date: 12.MAR.2025 14:03:59

LCH / DFT-QPSK / Edge_1RB_Left

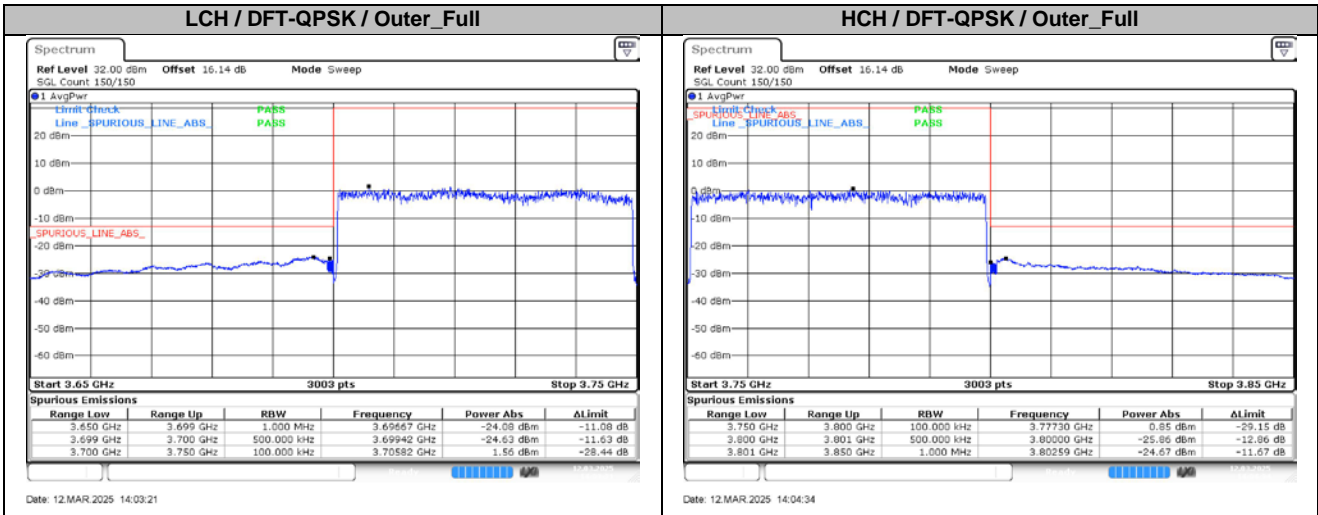


Date: 12.MAR.2025 14:03:10

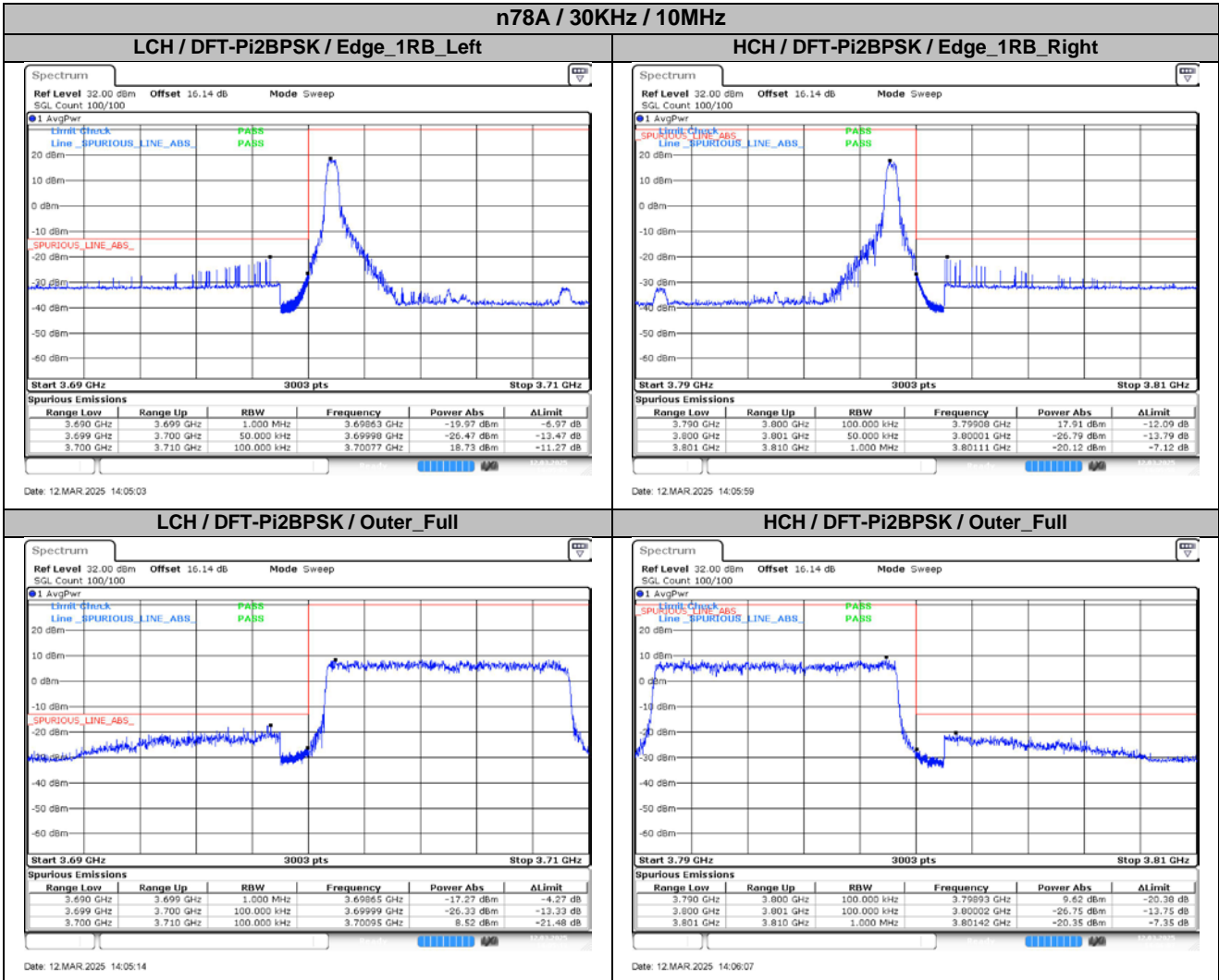
HCH / DFT-QPSK / Edge_1RB_Right

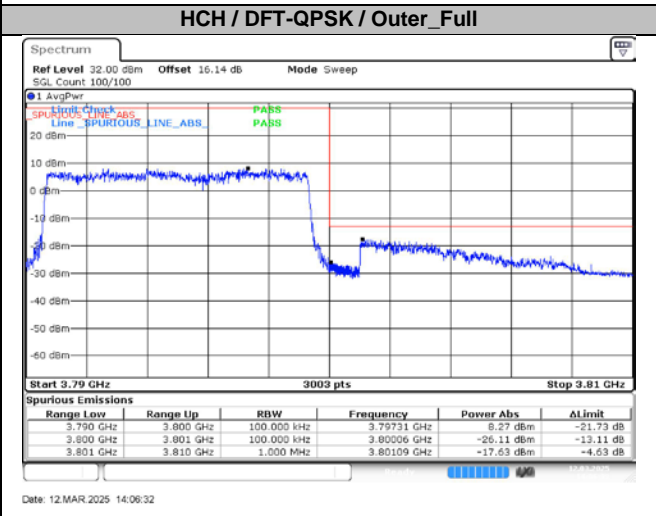
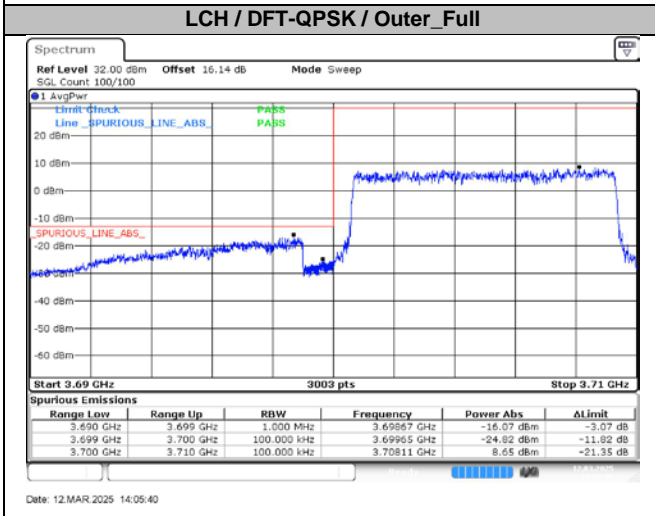
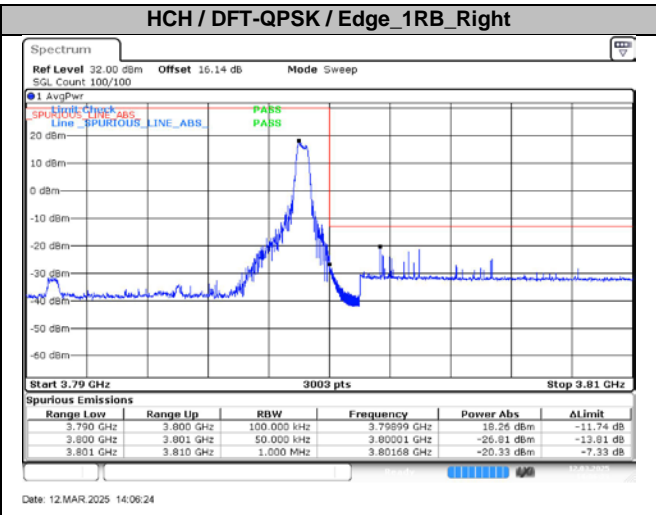
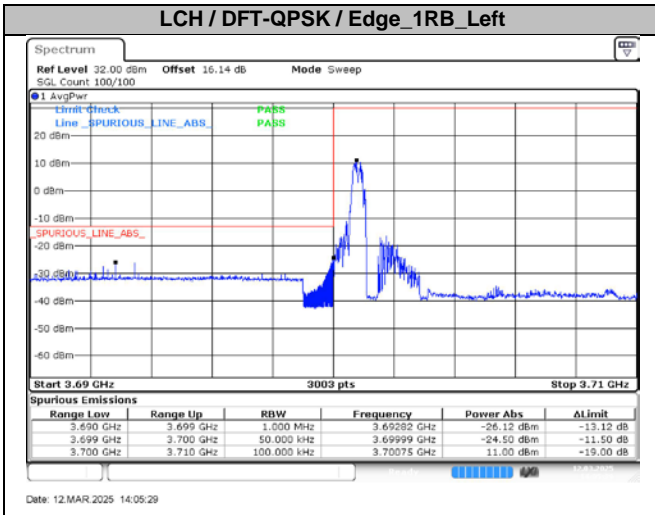


Date: 12.MAR.2025 14:04:24

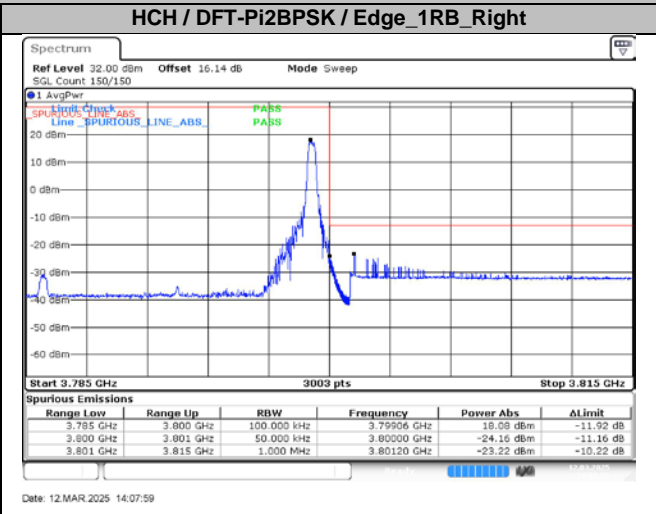
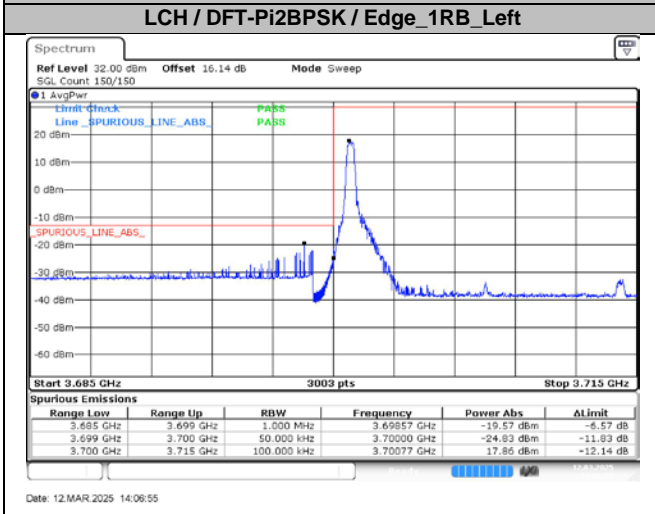


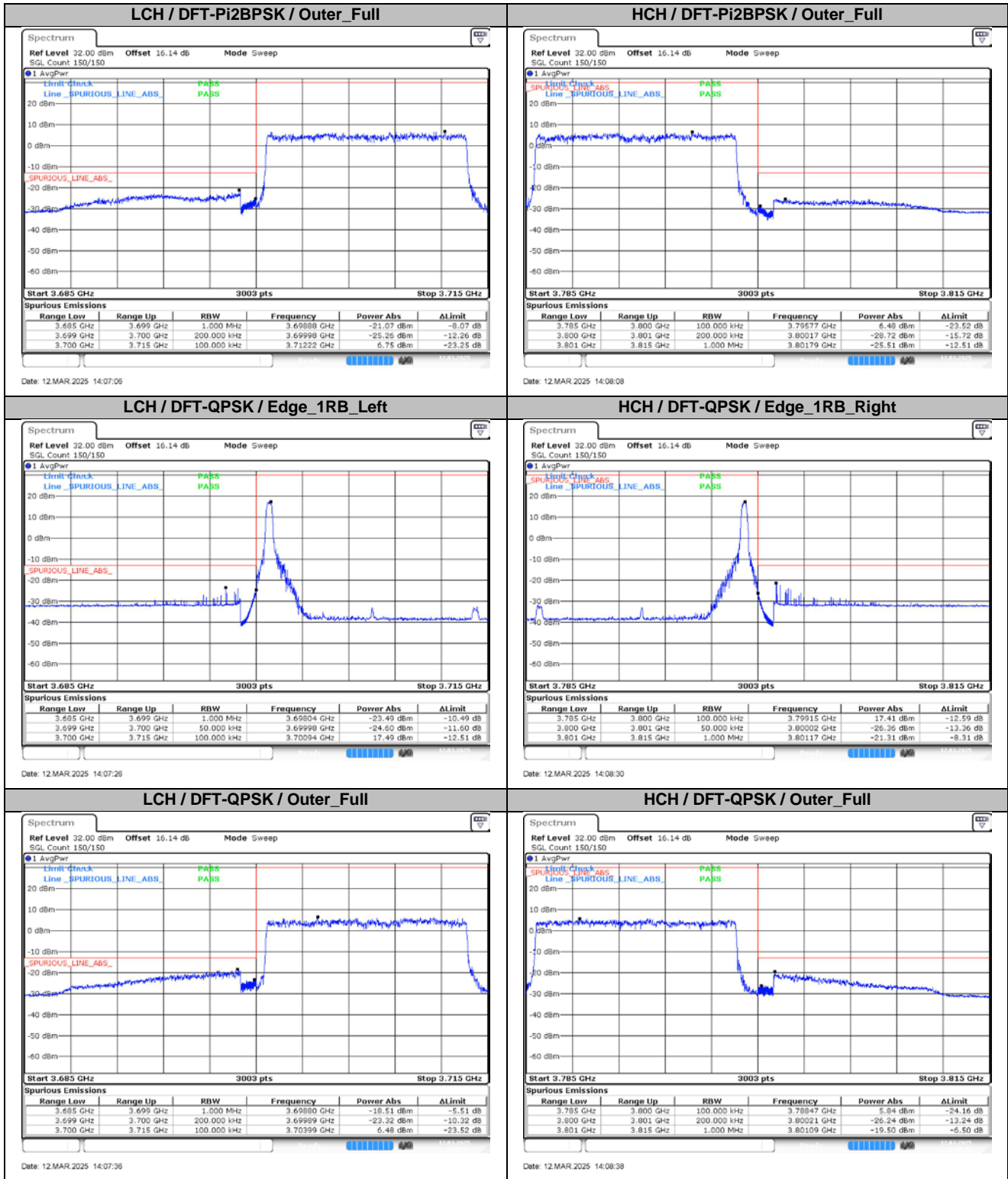
5.2. Test Plots for SCS=30KHz





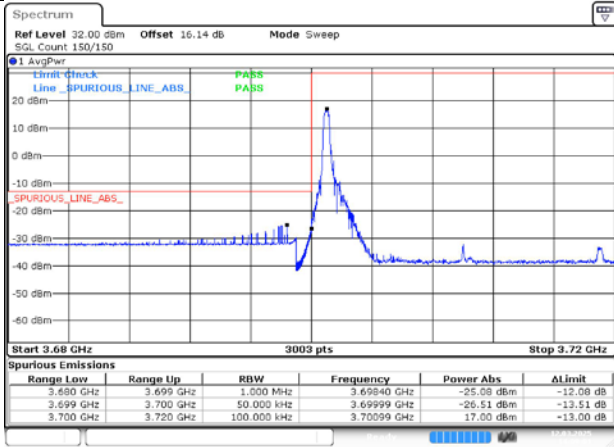
n78A / 30KHz / 15MHz





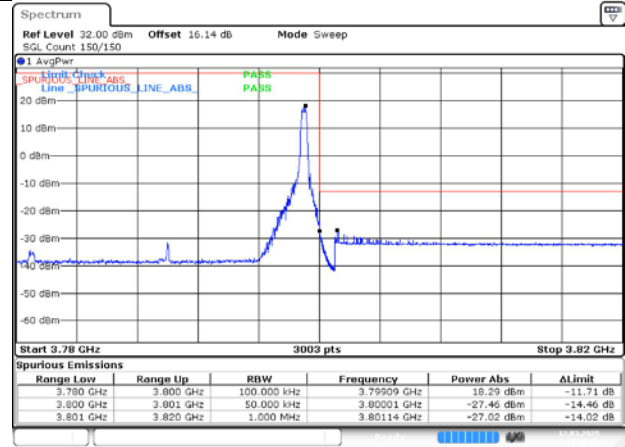
n78A / 30KHz / 20MHz

LCH / DFT-Pi2BPSK / Edge_1RB_Left



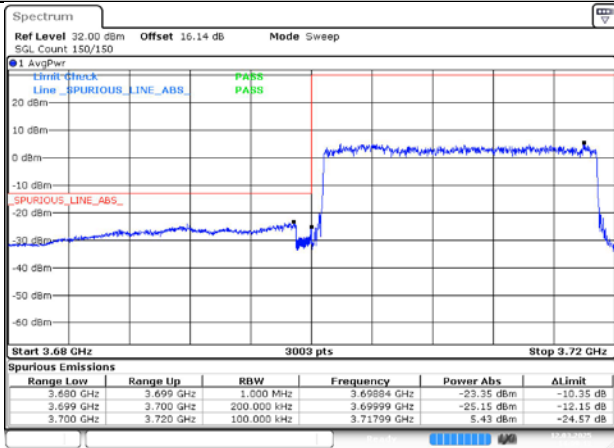
Date: 12.MAR.2025 14:09:01

HCH / DFT-Pi2BPSK / Edge_1RB_Right



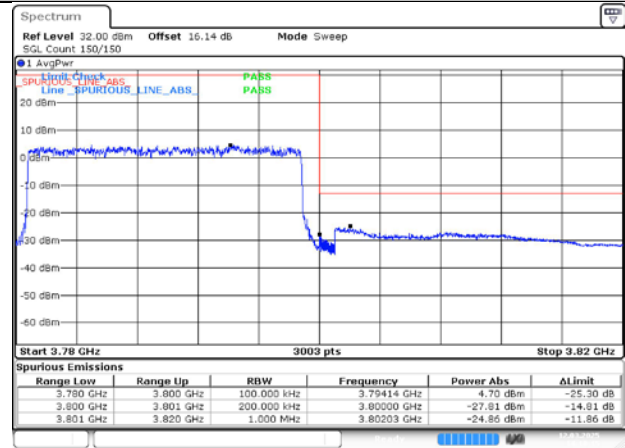
Date: 12.MAR.2025 14:10:06

LCH / DFT-Pi2BPSK / Outer_Full



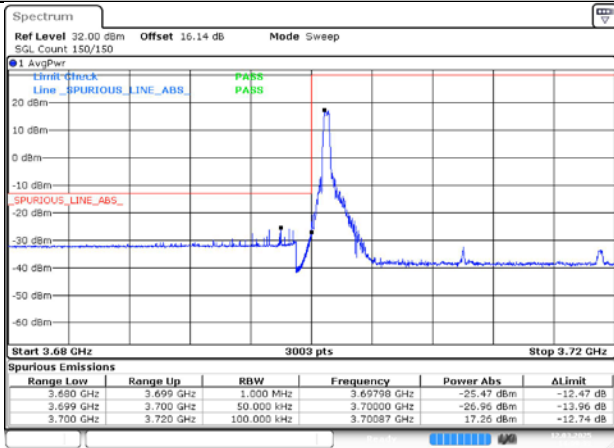
Date: 12.MAR.2025 14:09:12

HCH / DFT-Pi2BPSK / Outer_Full



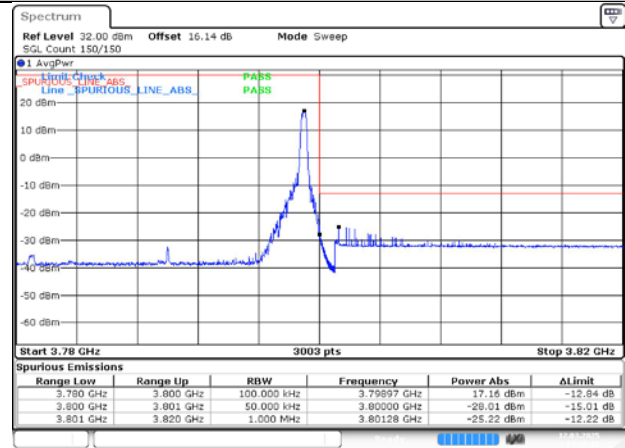
Date: 12.MAR.2025 14:10:15

LCH / DFT-QPSK / Edge_1RB_Left

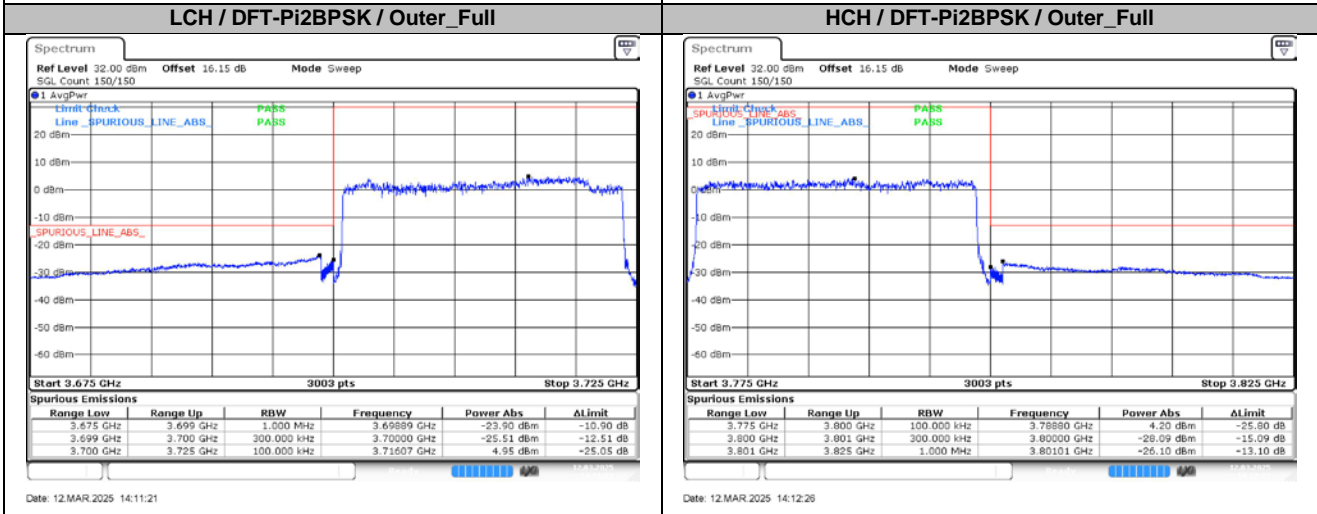
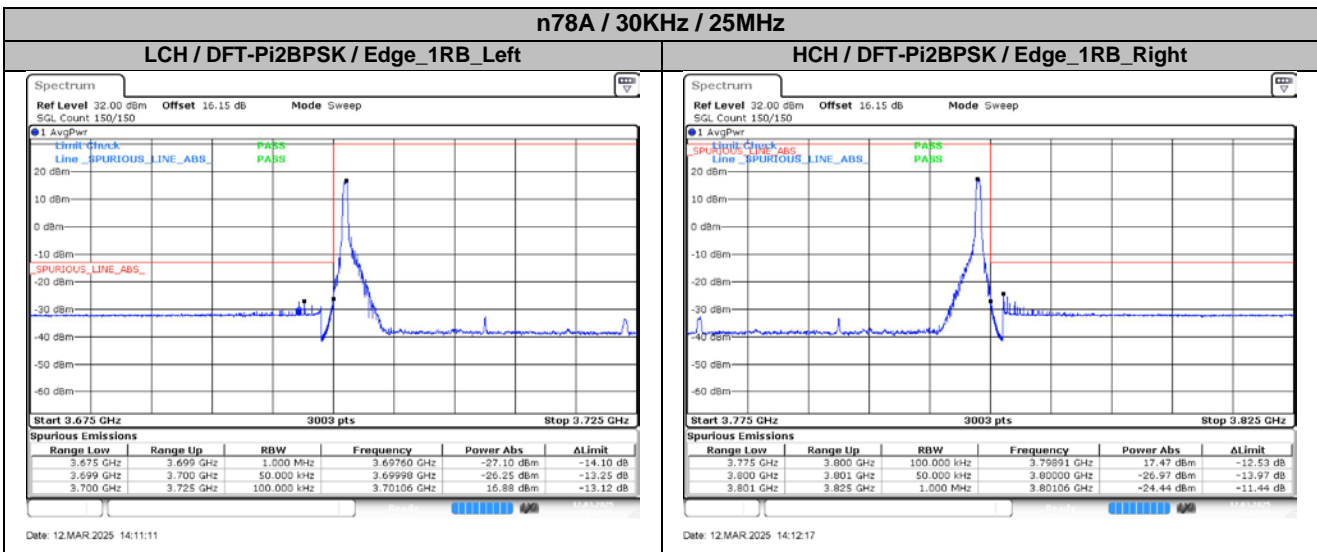
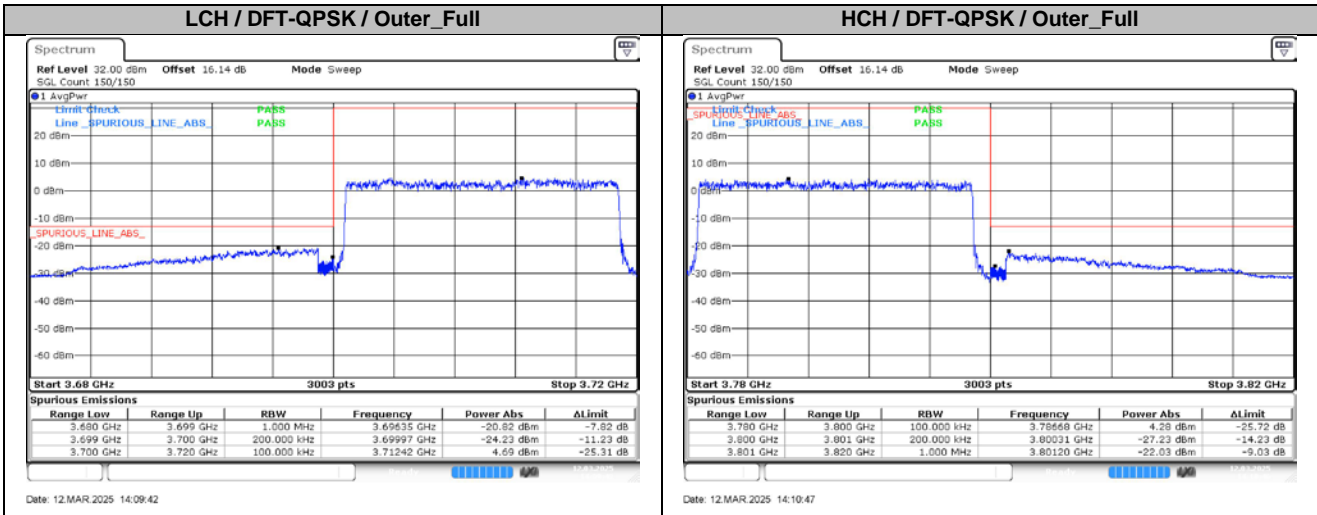


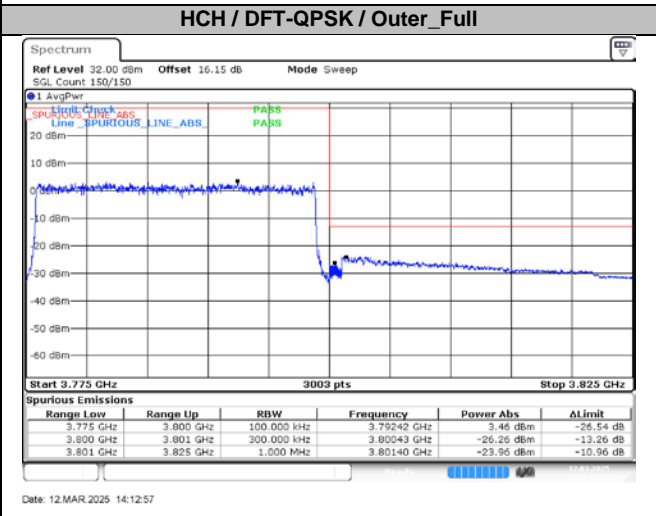
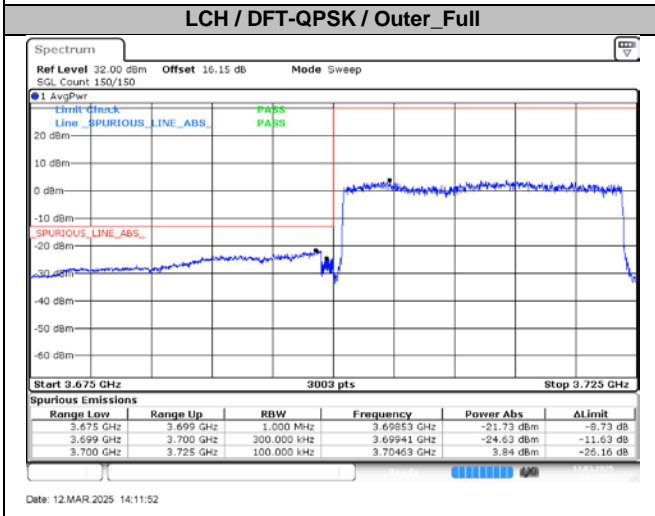
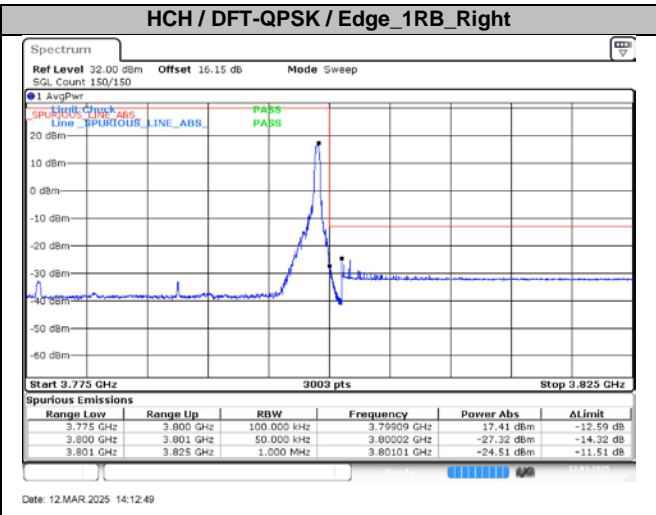
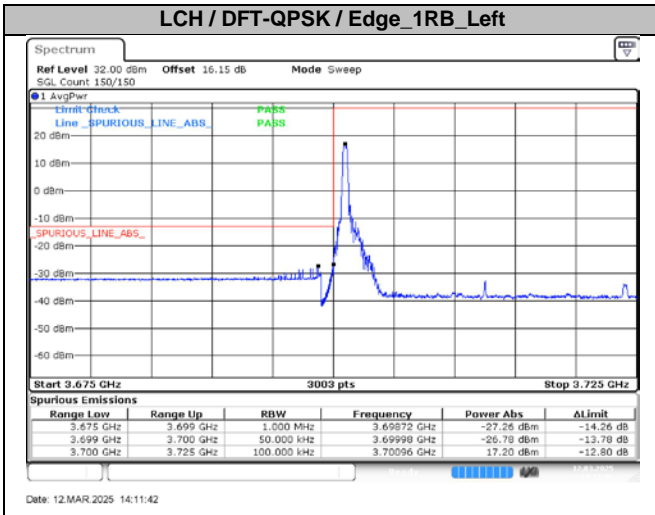
Date: 12.MAR.2025 14:09:32

HCH / DFT-QPSK / Edge_1RB_Right

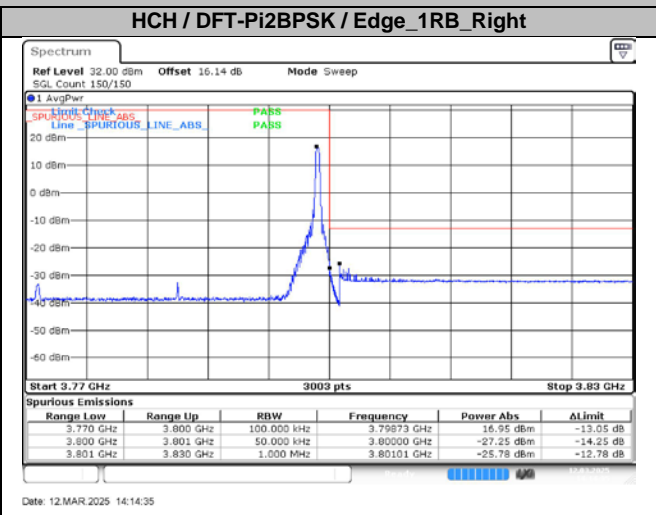
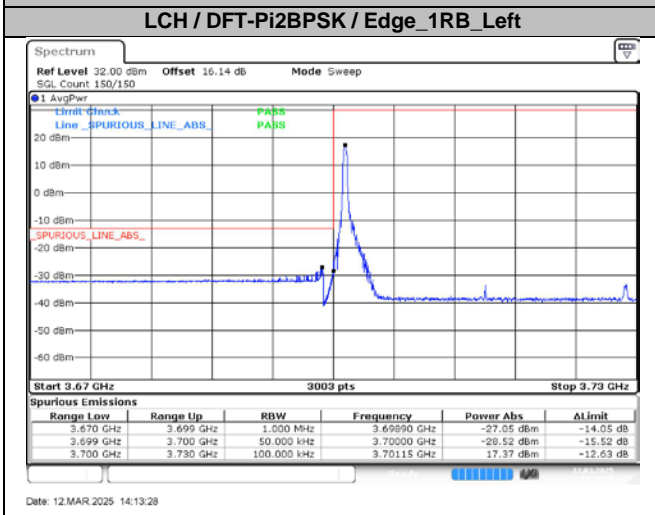


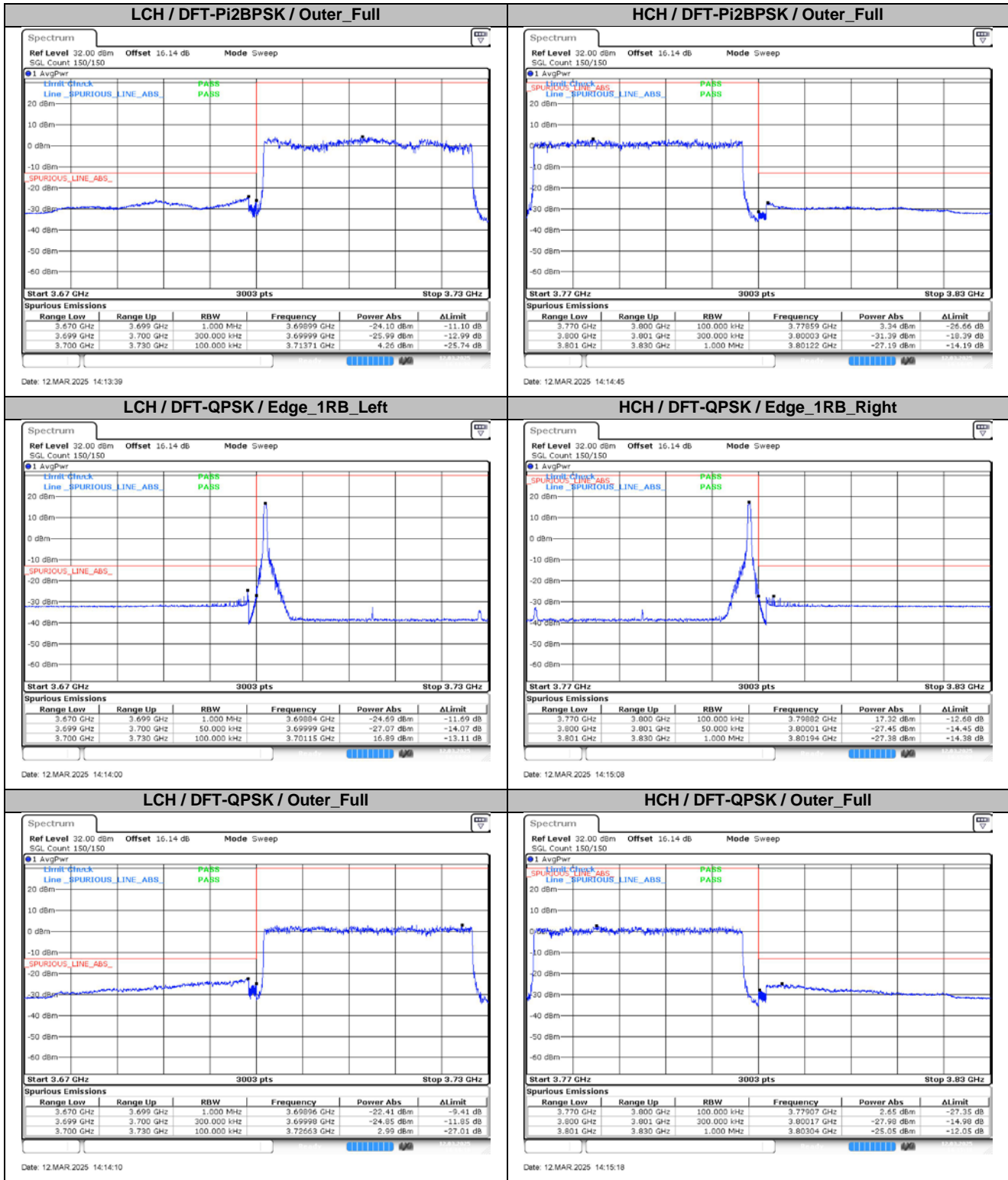
Date: 12.MAR.2025 14:10:38





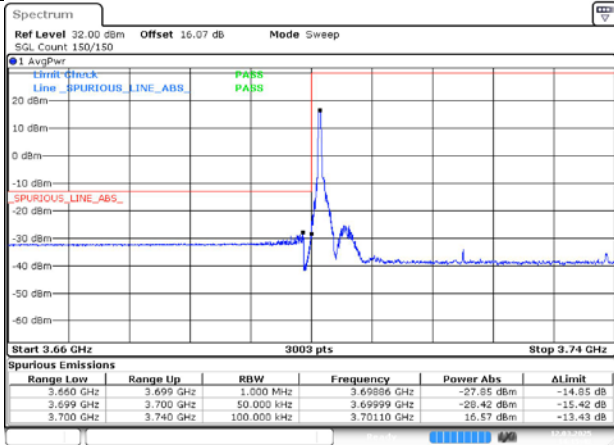
n78A / 30KHz / 30MHz





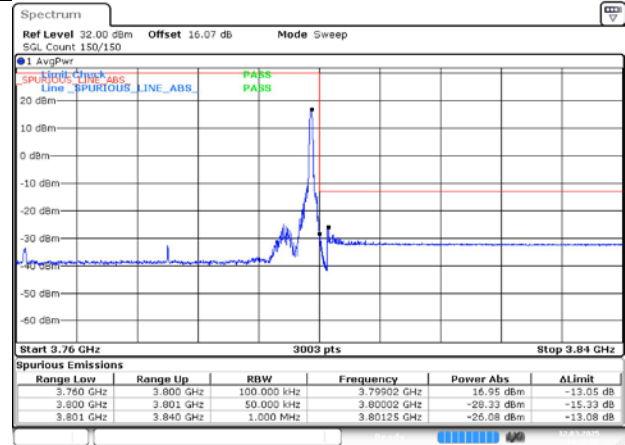
n78A / 30KHz / 40MHz

LCH / DFT-Pi2BPSK / Edge_1RB_Left



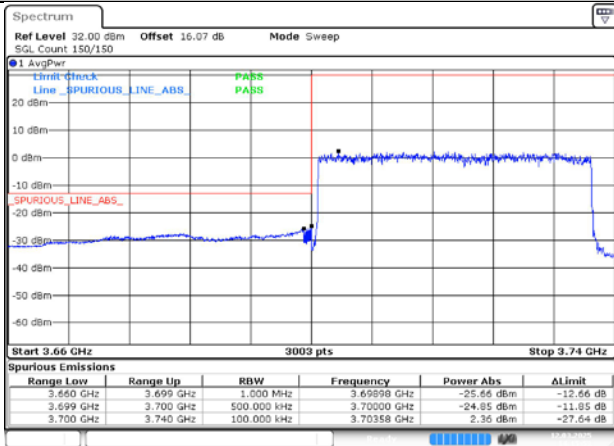
Date: 12.MAR.2025 14:15:42

HCH / DFT-Pi2BPSK / Edge_1RB_Right



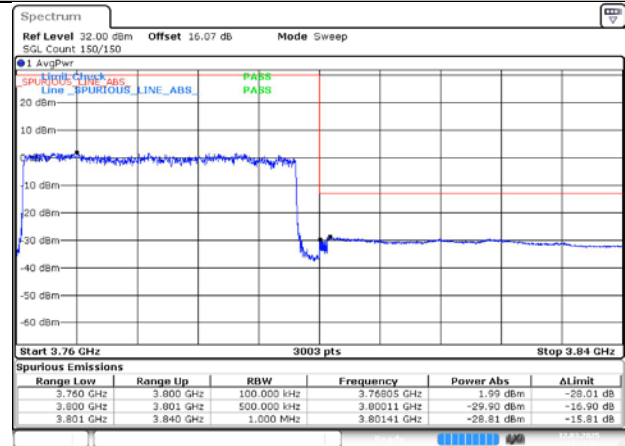
Date: 12.MAR.2025 14:16:50

LCH / DFT-Pi2BPSK / Outer_Full



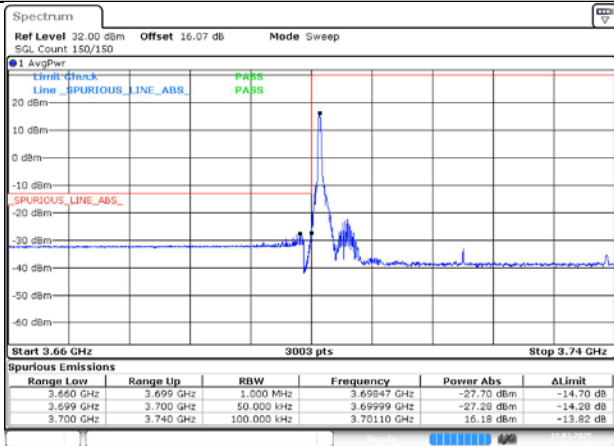
Date: 12.MAR.2025 14:15:53

HCH / DFT-Pi2BPSK / Outer_Full



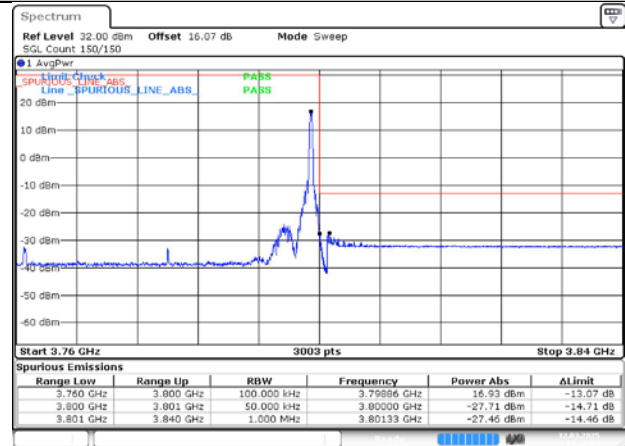
Date: 12.MAR.2025 14:17:00

LCH / DFT-QPSK / Edge_1RB_Left

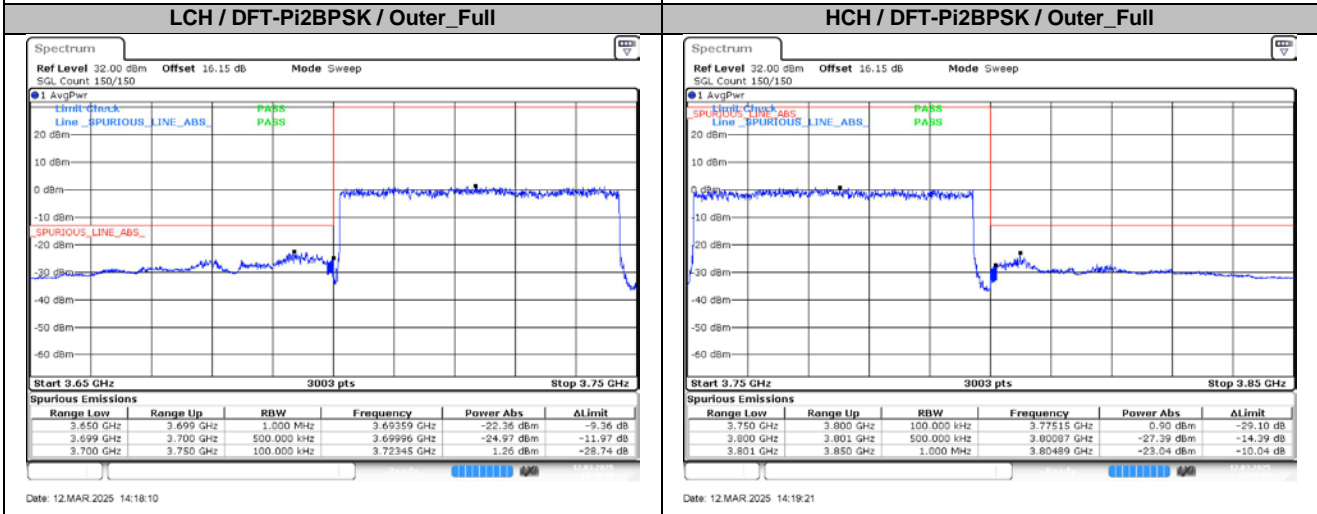
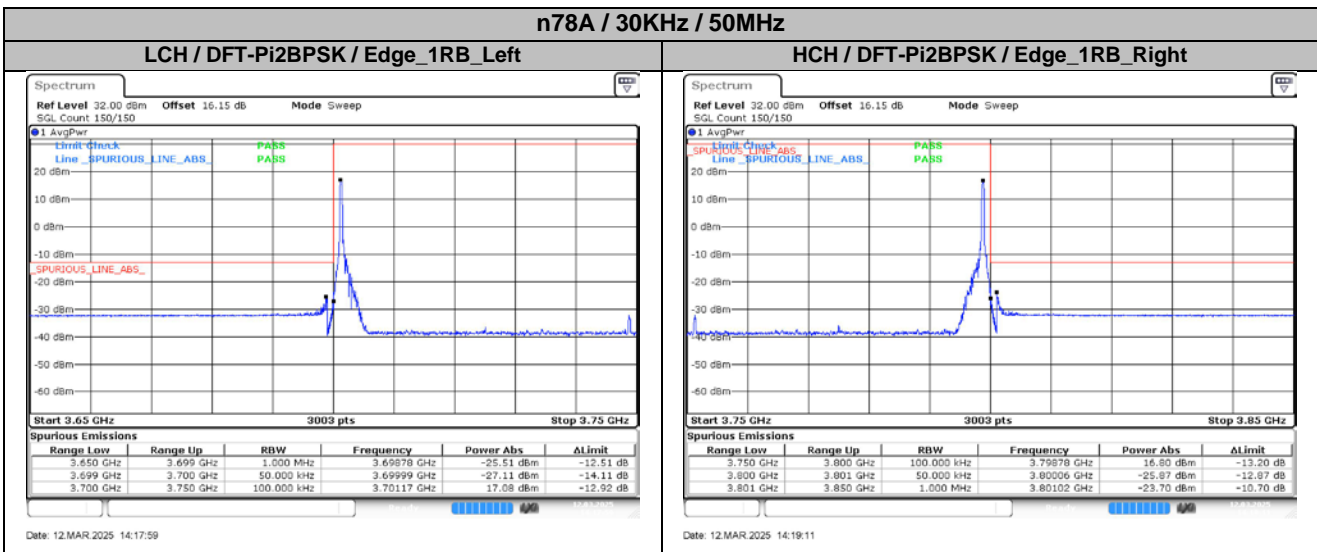
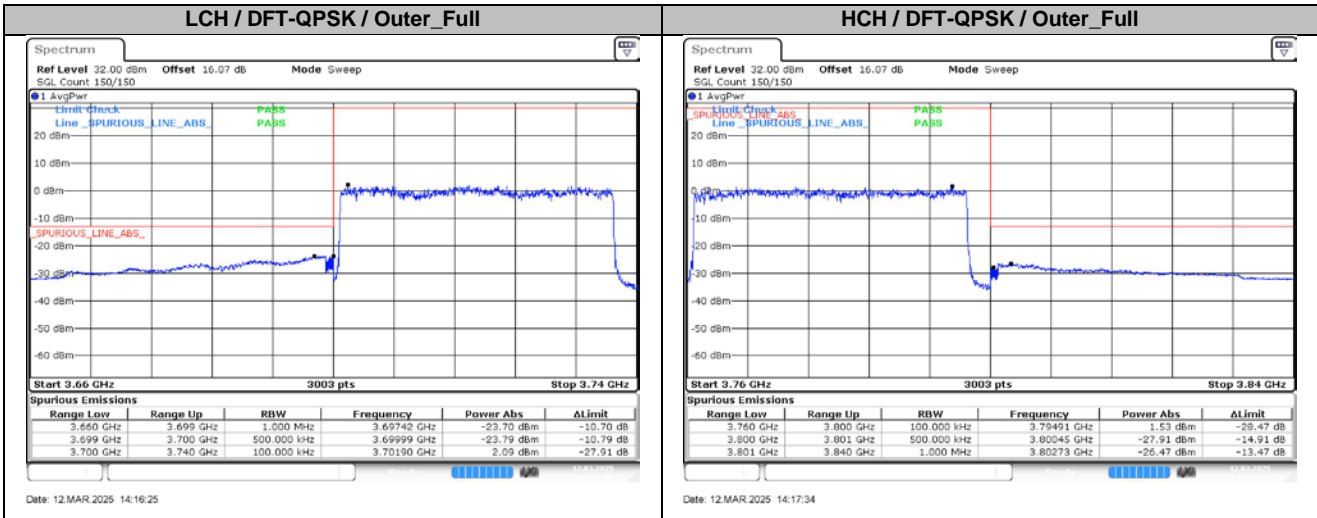


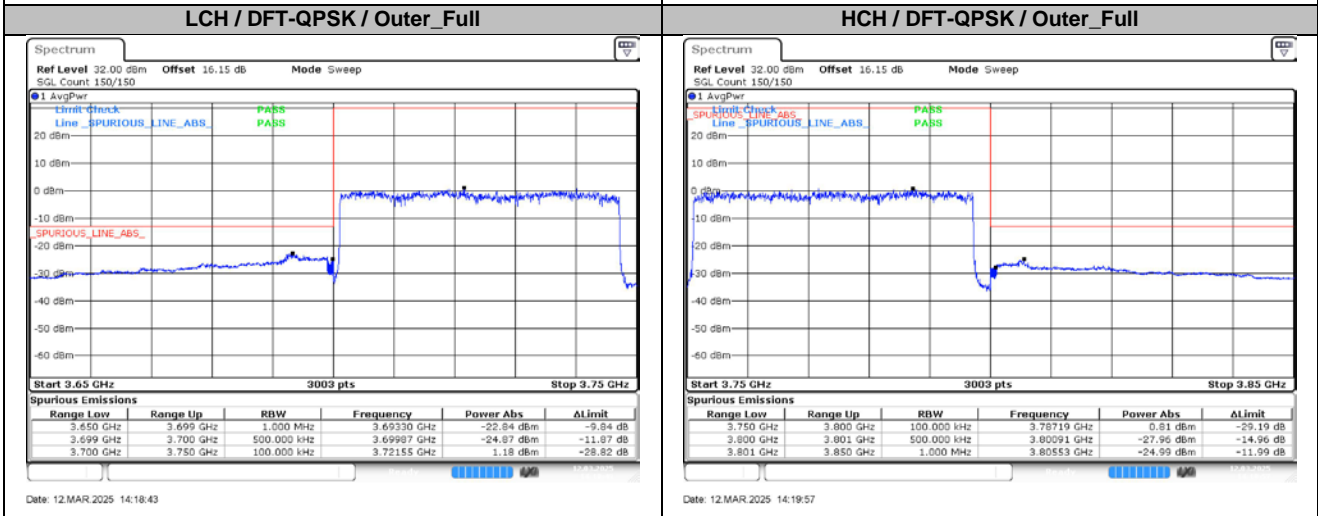
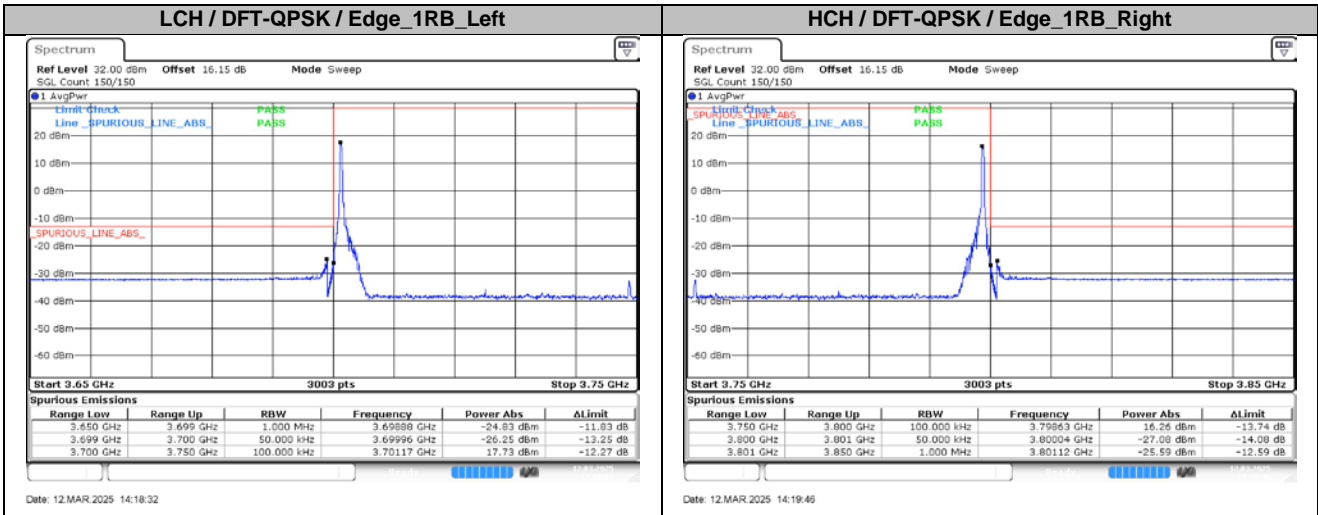
Date: 12.MAR.2025 14:16:14

HCH / DFT-QPSK / Edge_1RB_Right

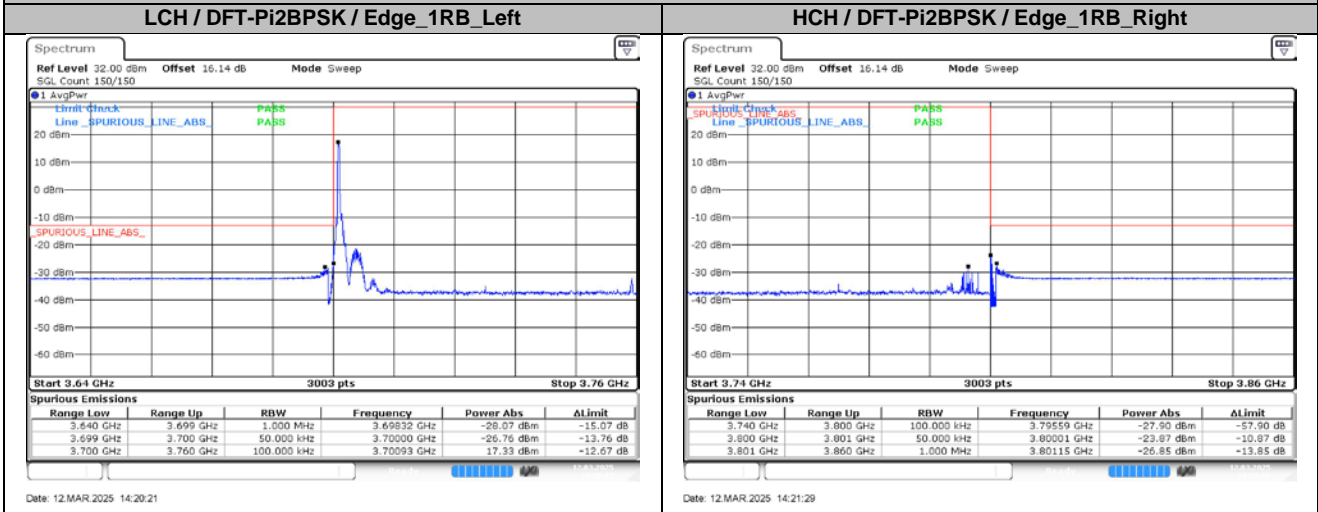


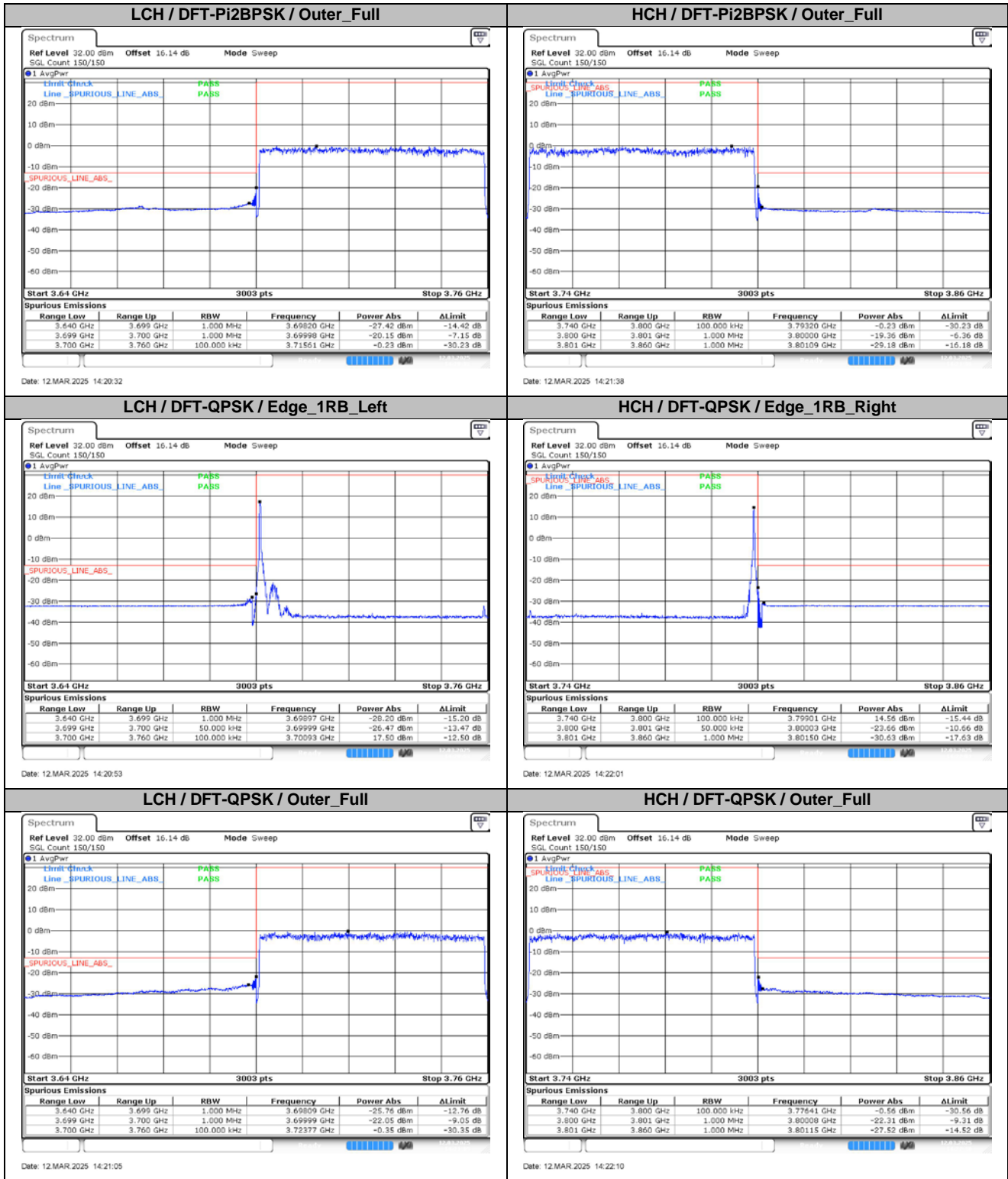
Date: 12.MAR.2025 14:17:24





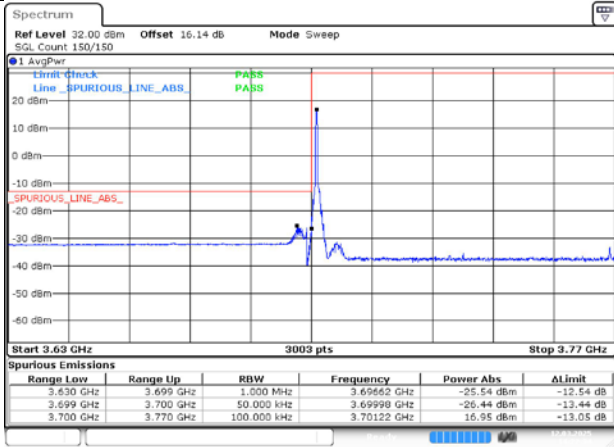
n78A / 30KHz / 60MHz





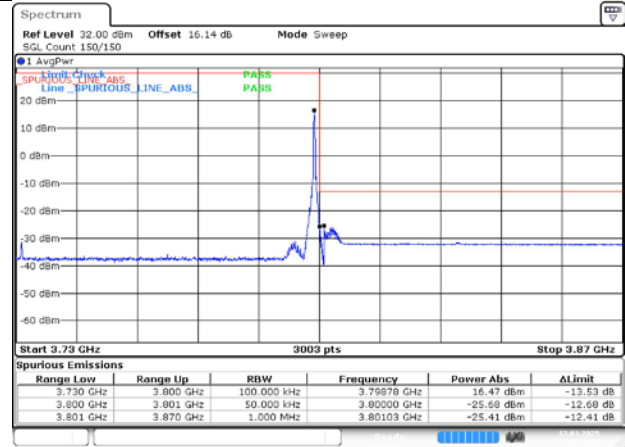
n78A / 30KHz / 70MHz

LCH / DFT-Pi2BPSK / Edge_1RB_Left



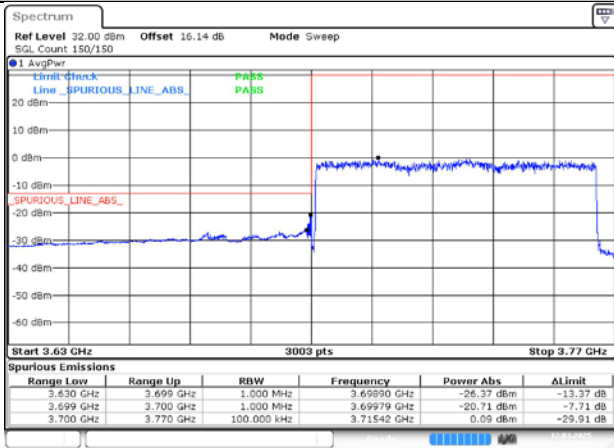
Date: 12.MAR.2025 14:22:34

HCH / DFT-Pi2BPSK / Edge_1RB_Right



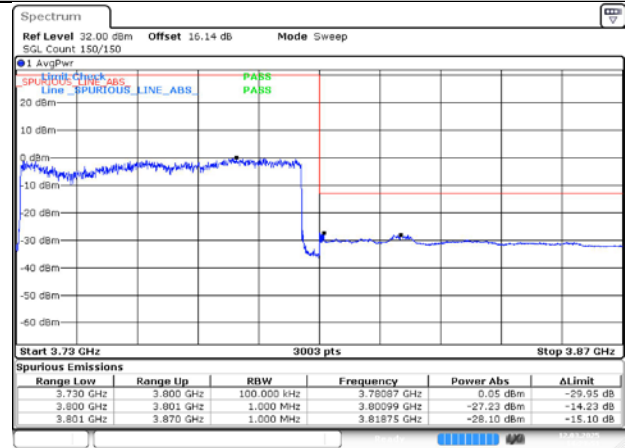
Date: 12.MAR.2025 14:23:42

LCH / DFT-Pi2BPSK / Outer_Full



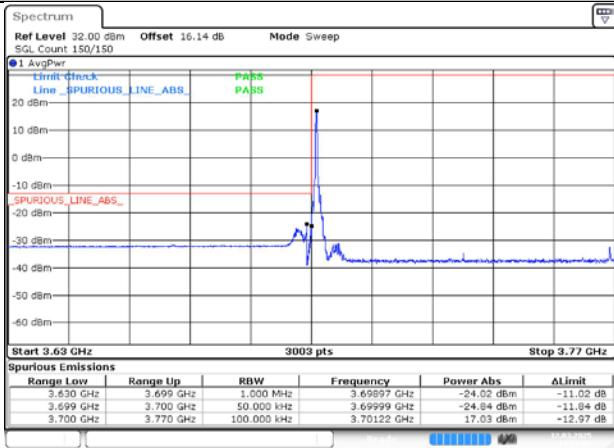
Date: 12.MAR.2025 14:22:45

HCH / DFT-Pi2BPSK / Outer_Full



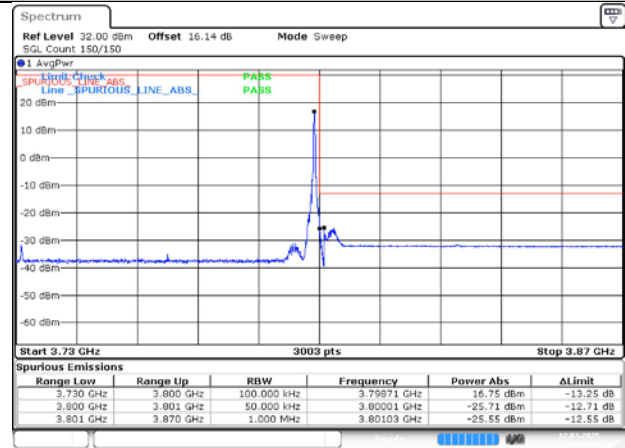
Date: 12.MAR.2025 14:23:51

LCH / DFT-QPSK / Edge_1RB_Left



Date: 12.MAR.2025 14:23:06

HCH / DFT-QPSK / Edge_1RB_Right



Date: 12.MAR.2025 14:24:14