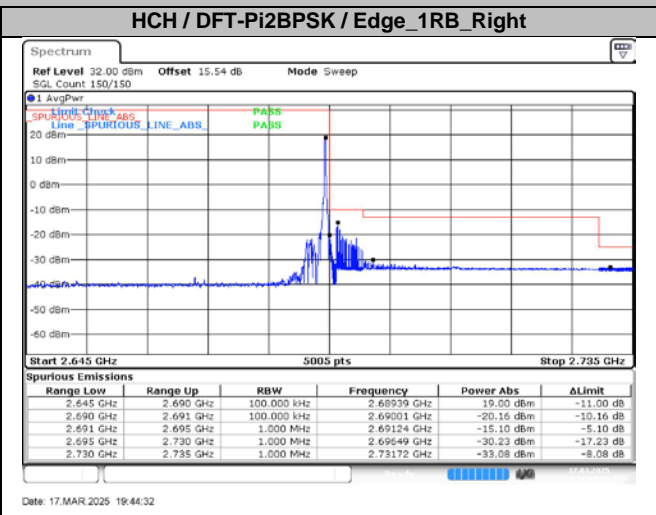
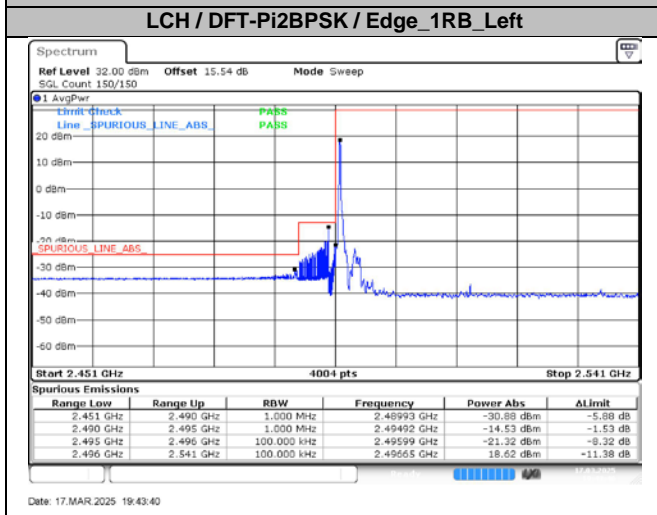
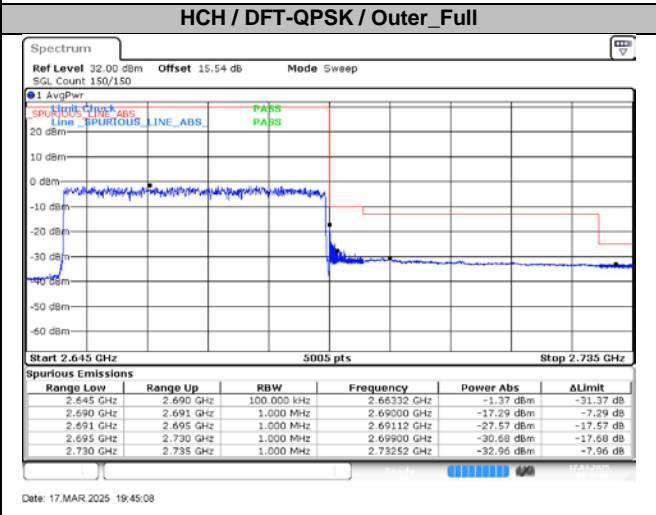
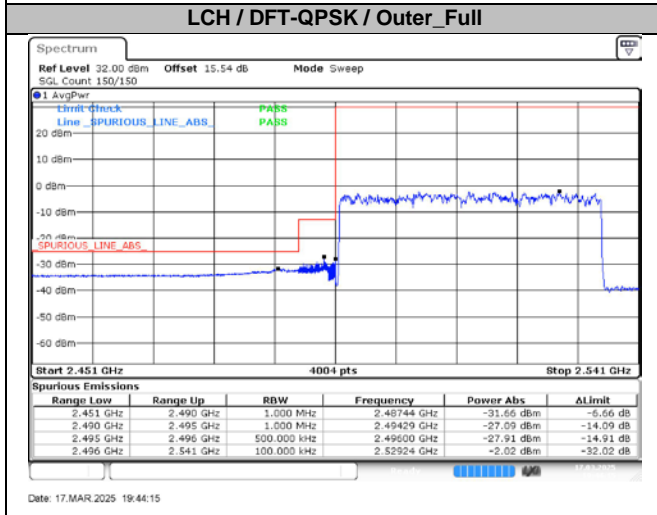
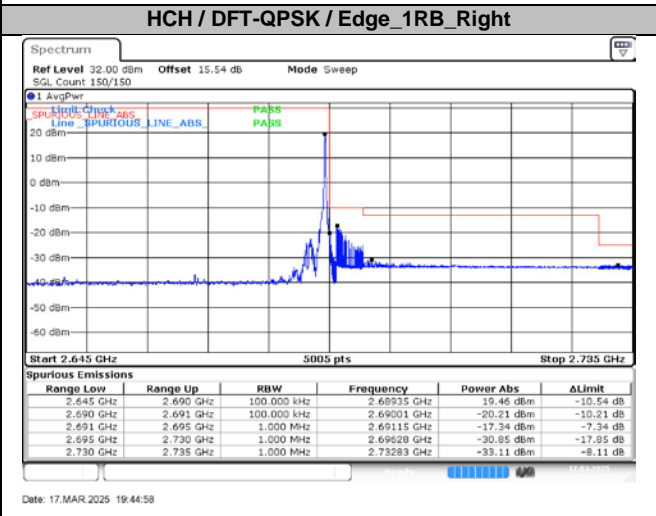
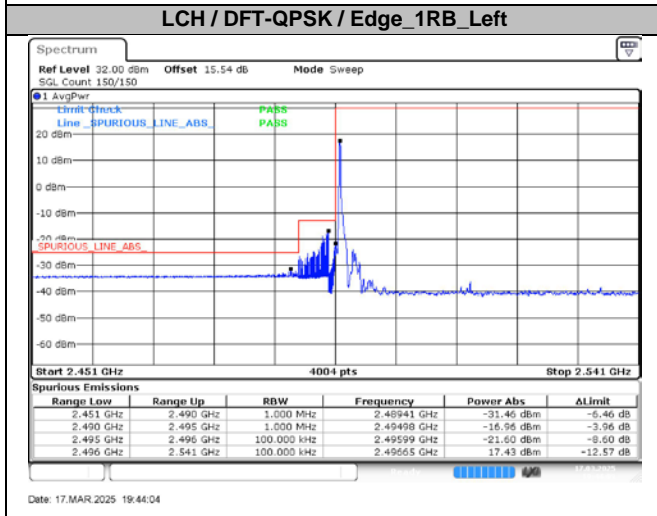
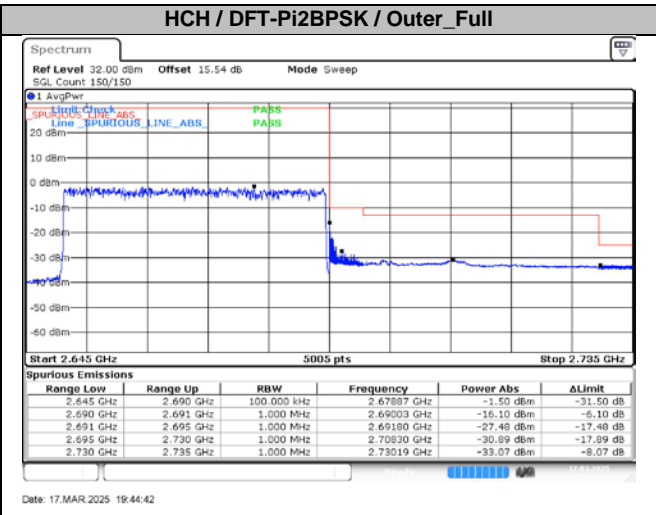
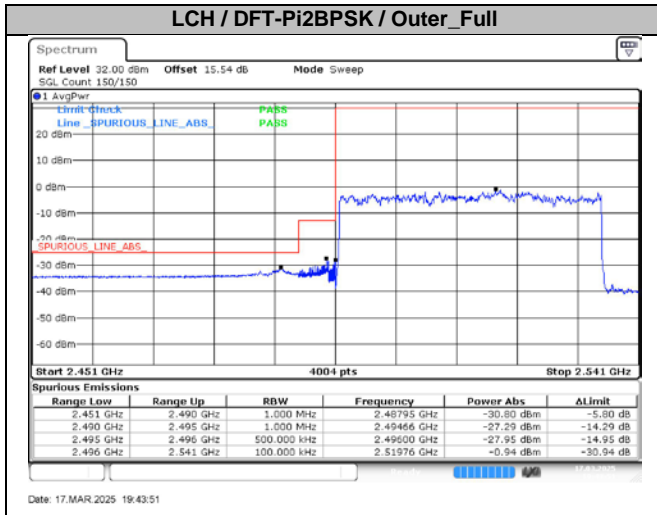


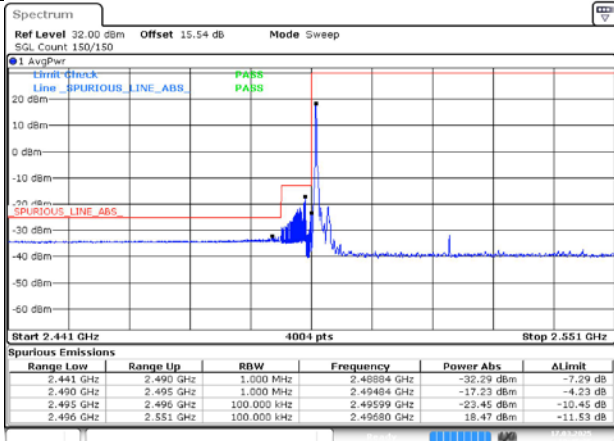
n41A / 15KHz / 40MHz





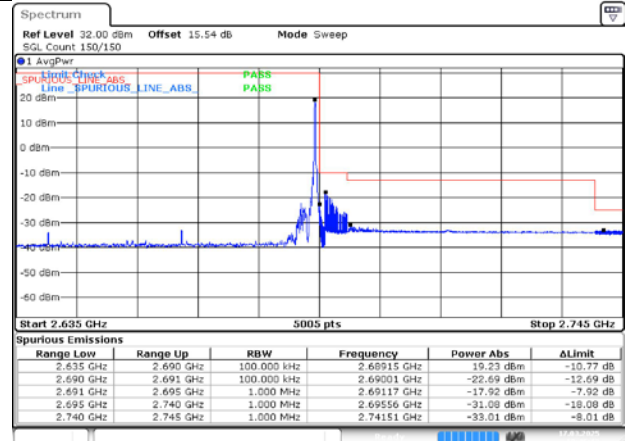
n41A / 15KHz / 50MHz

LCH / DFT-Pi2BPSK / Edge_1RB_Left



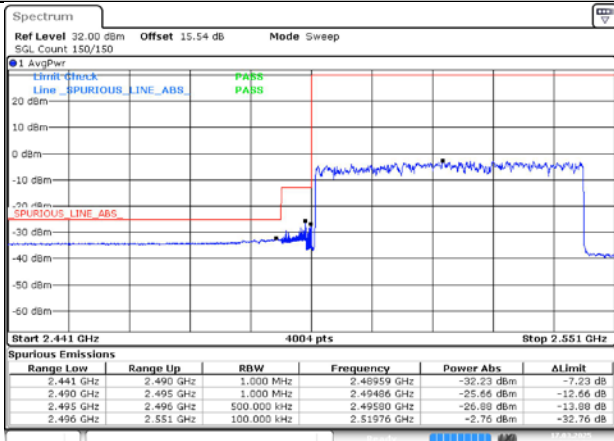
Date: 17.MAR.2025 19:45:25

HCH / DFT-Pi2BPSK / Edge_1RB_Right



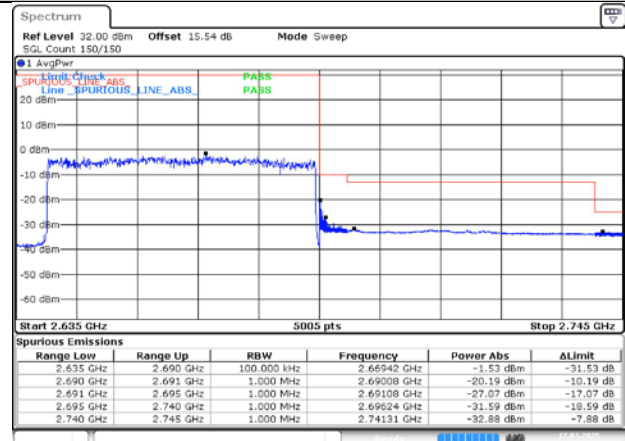
Date: 17.MAR.2025 19:46:12

LCH / DFT-Pi2BPSK / Outer_Full



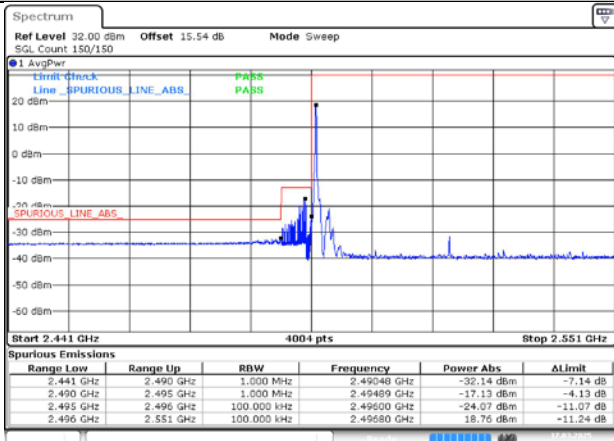
Date: 17.MAR.2025 19:45:35

HCH / DFT-Pi2BPSK / Outer_Full



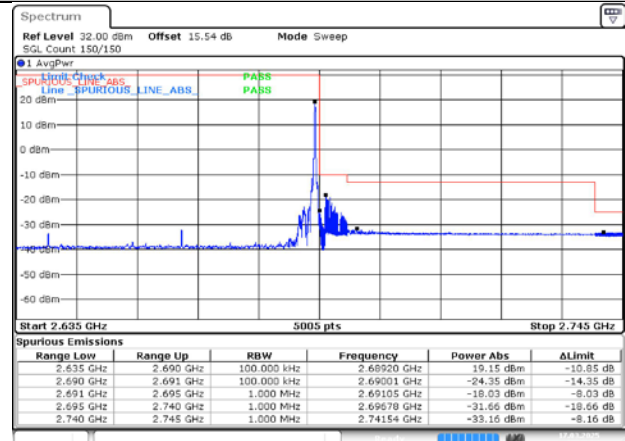
Date: 17.MAR.2025 19:46:22

LCH / DFT-QPSK / Edge_1RB_Left

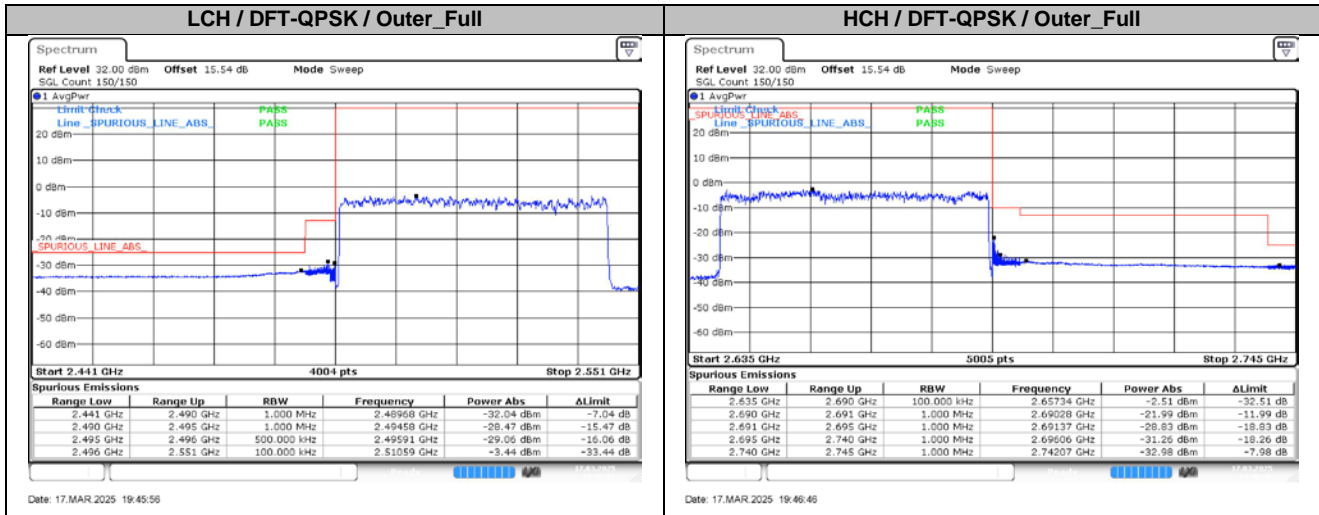


Date: 17.MAR.2025 19:45:46

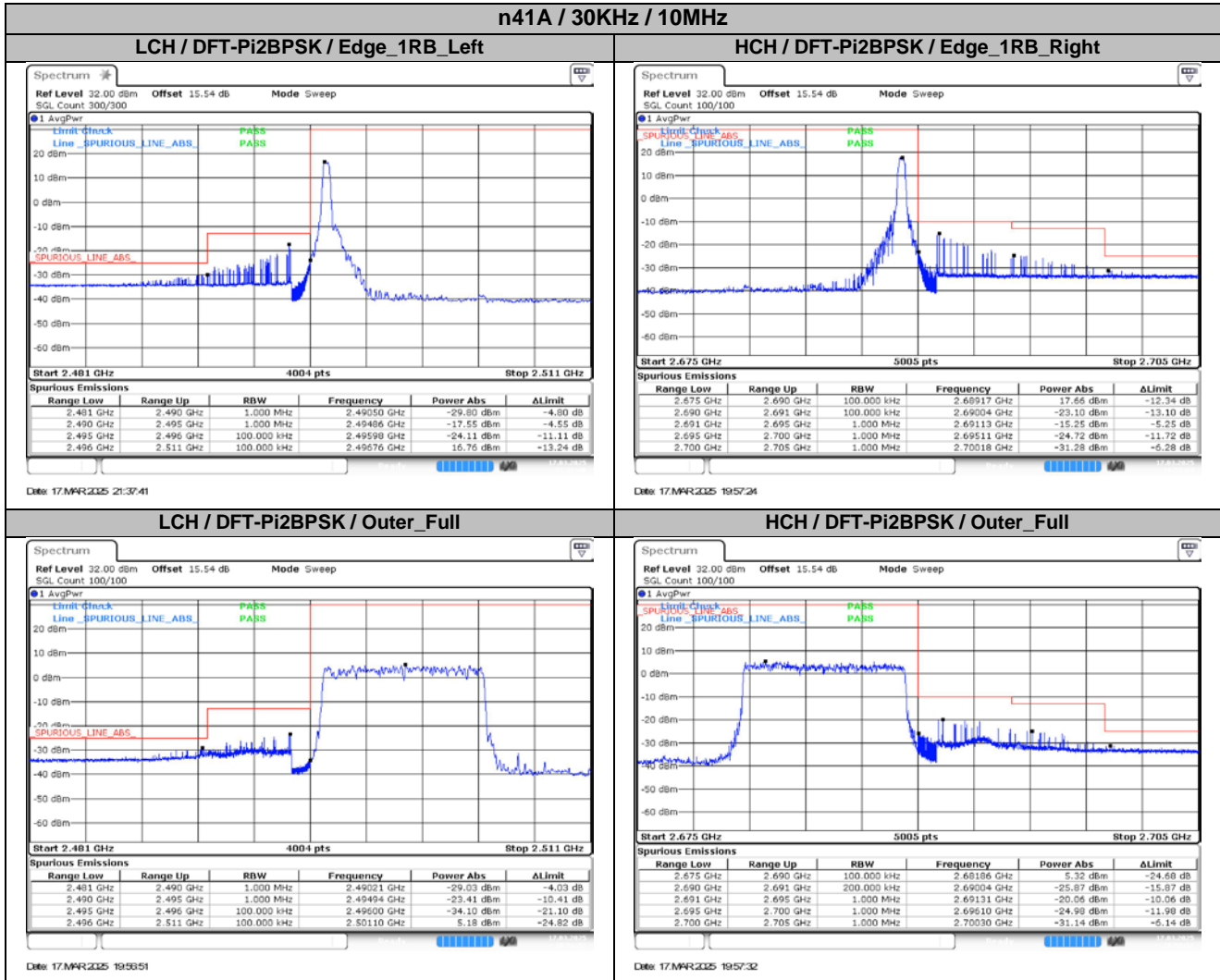
HCH / DFT-QPSK / Edge_1RB_Right

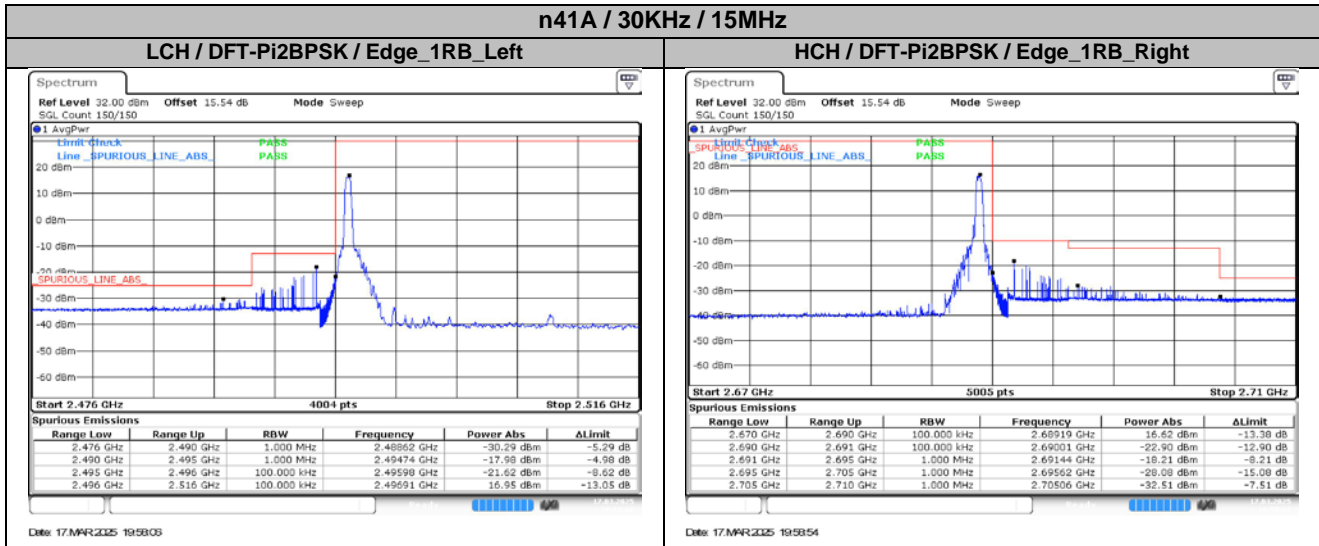
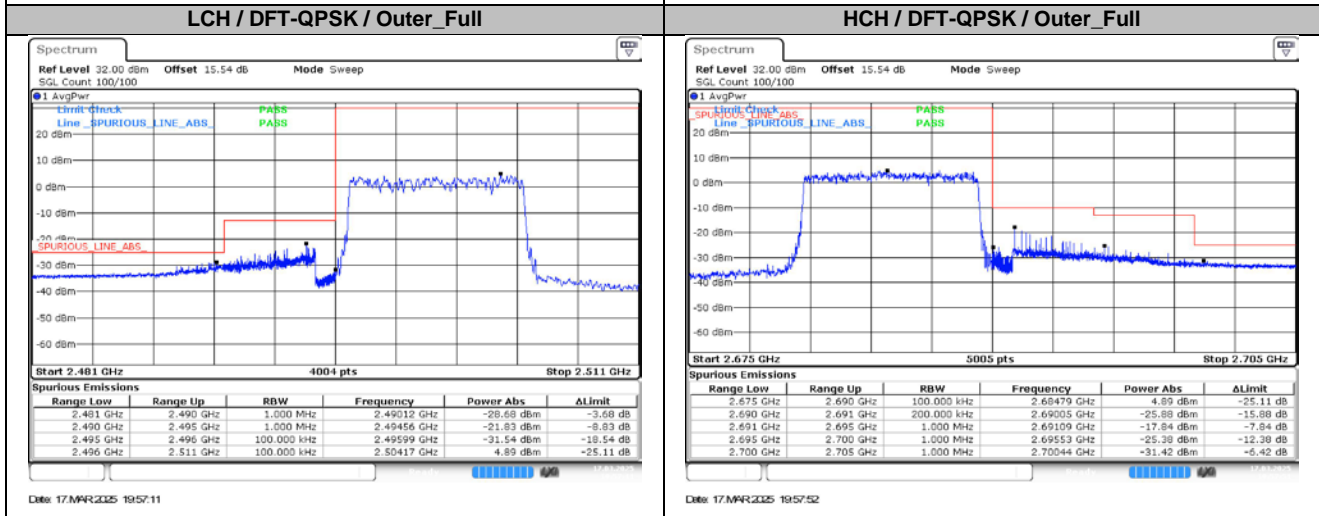
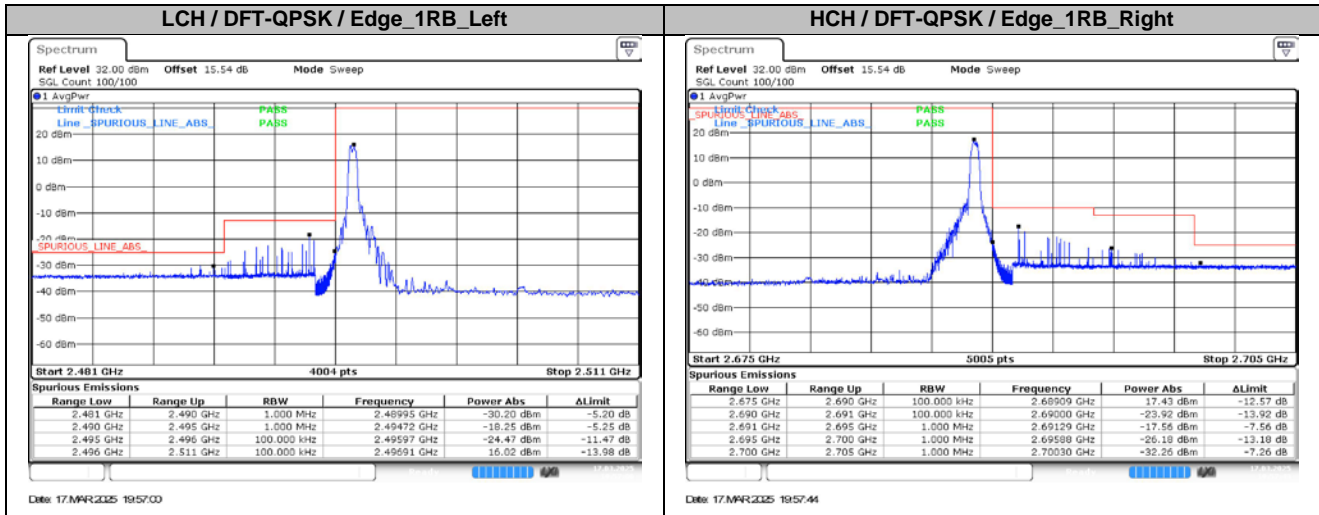


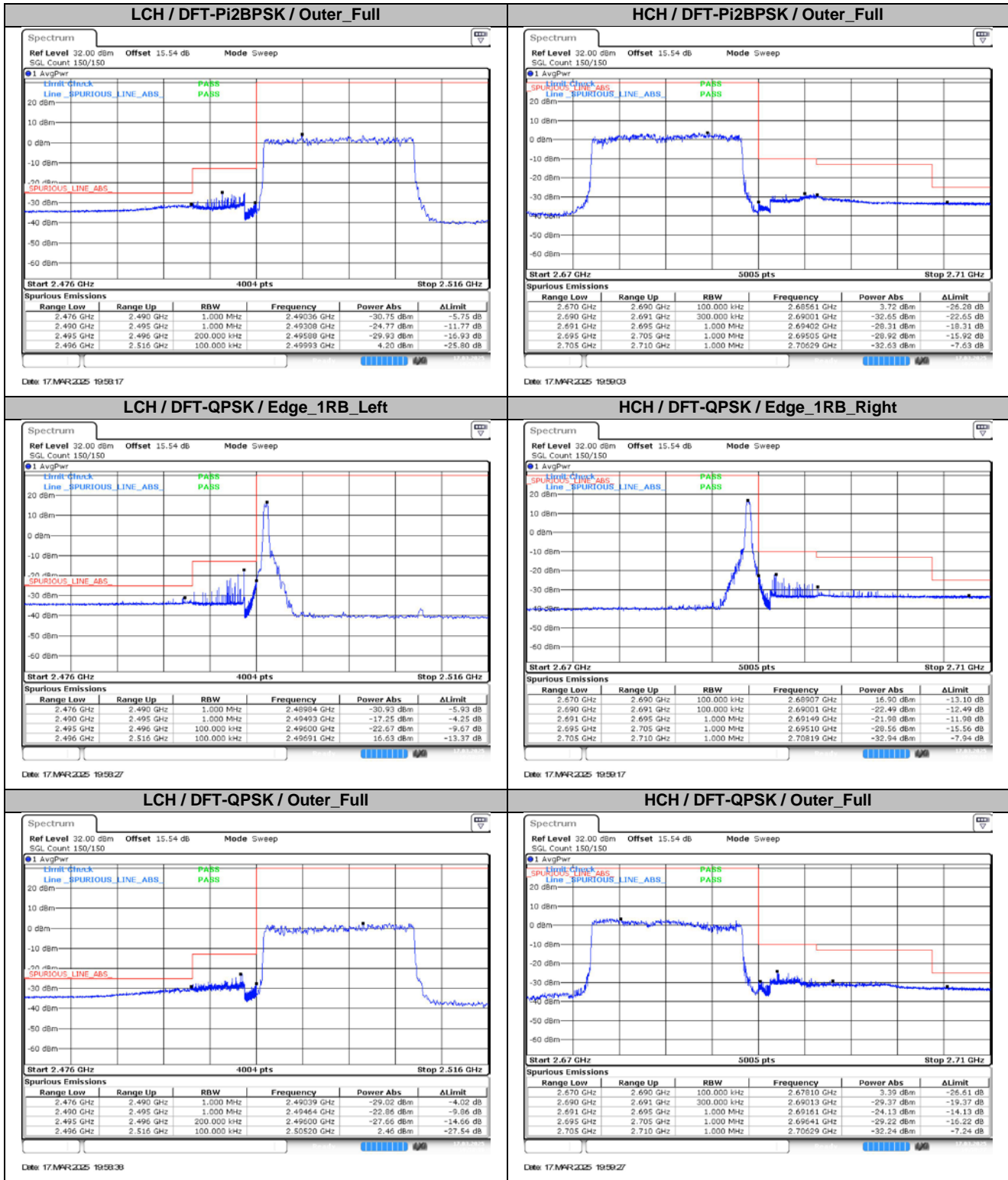
Date: 17.MAR.2025 19:46:37



5.2. Test Plots for SCS=30KHz

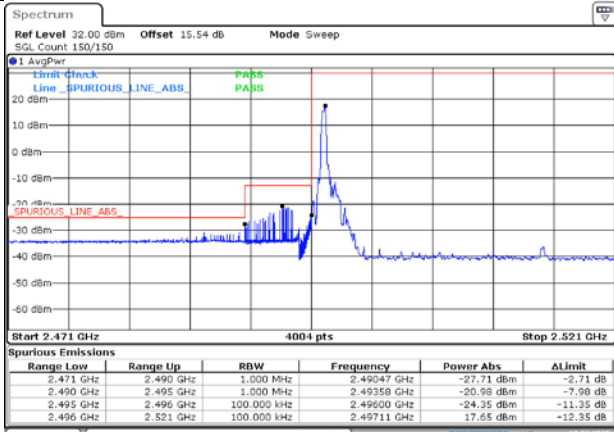






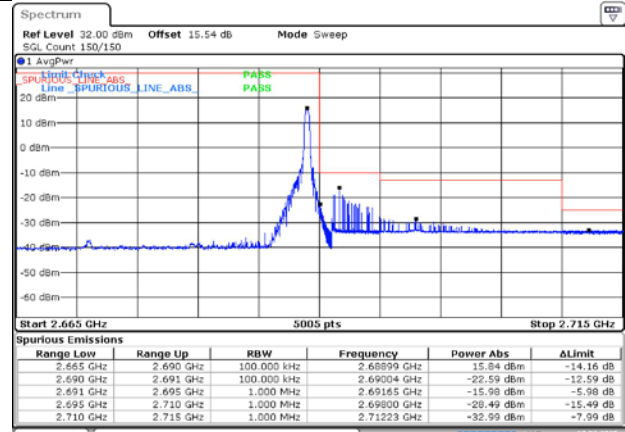
n41A / 30KHz / 20MHz

LCH / DFT-Pi2BPSK / Edge_1RB_Left



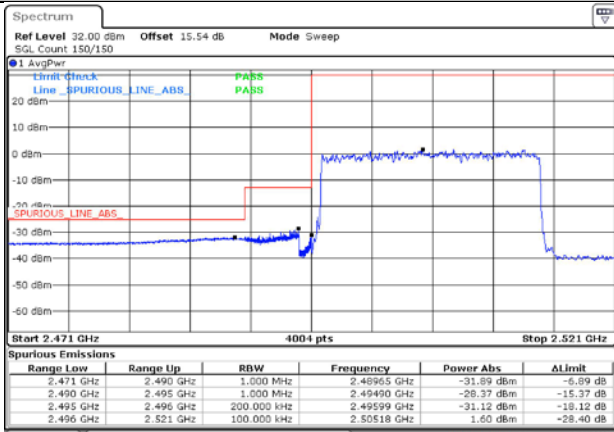
Date: 17/MAR/2025 19:50:41

HCH / DFT-Pi2BPSK / Edge_1RB_Right



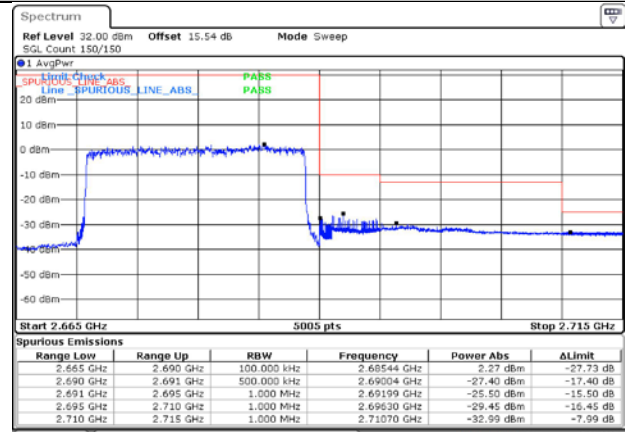
Date: 17/MAR/2025 20:00:41

LCH / DFT-Pi2BPSK / Outer_Full



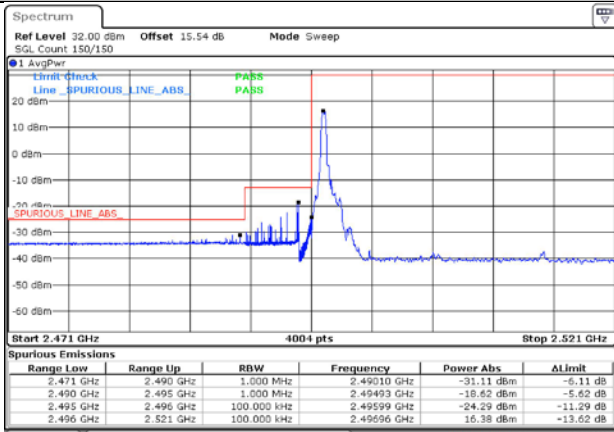
Date: 17/MAR/2025 19:50:52

HCH / DFT-Pi2BPSK / Outer_Full



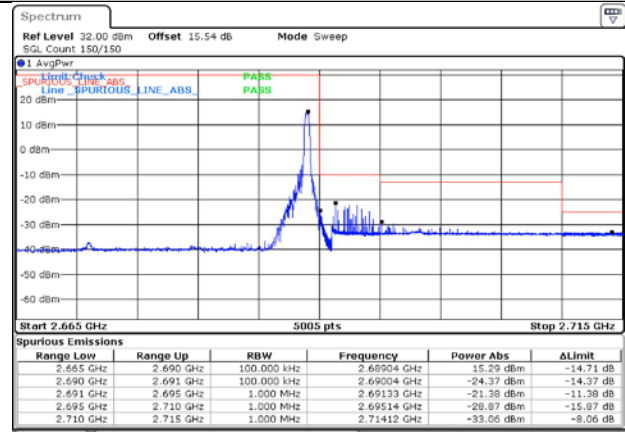
Date: 17/MAR/2025 20:00:50

LCH / DFT-QPSK / Edge_1RB_Left

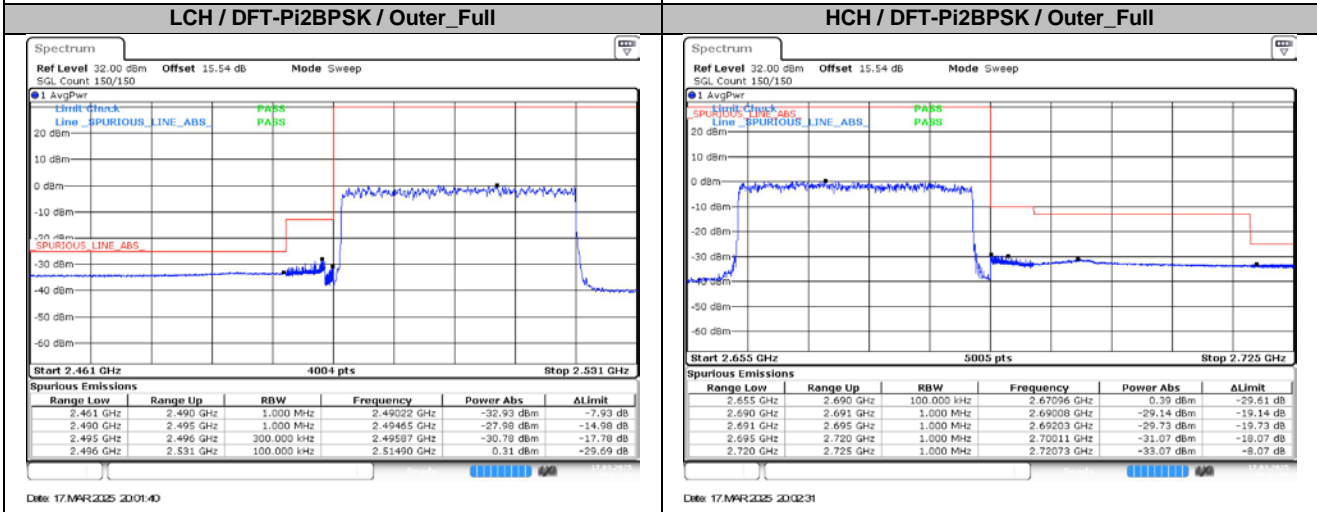
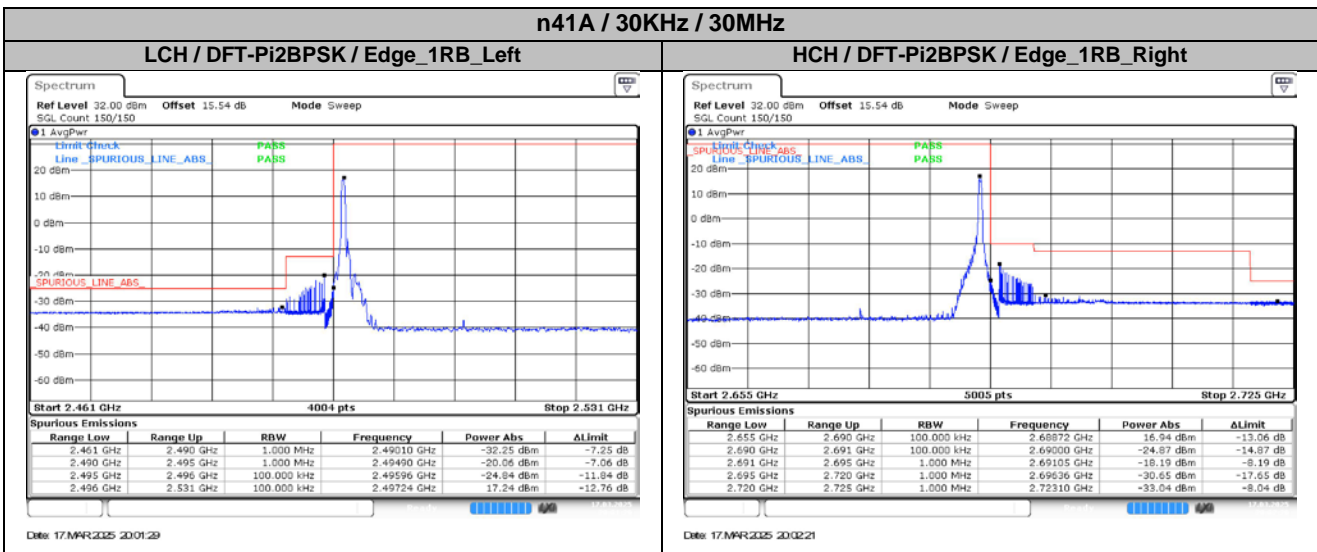
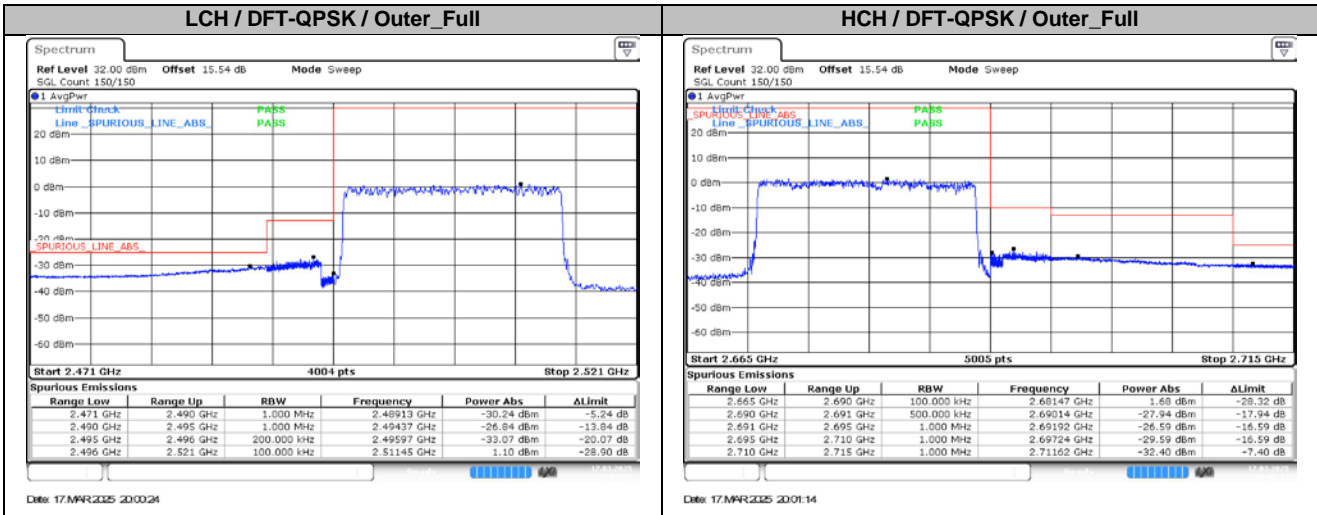


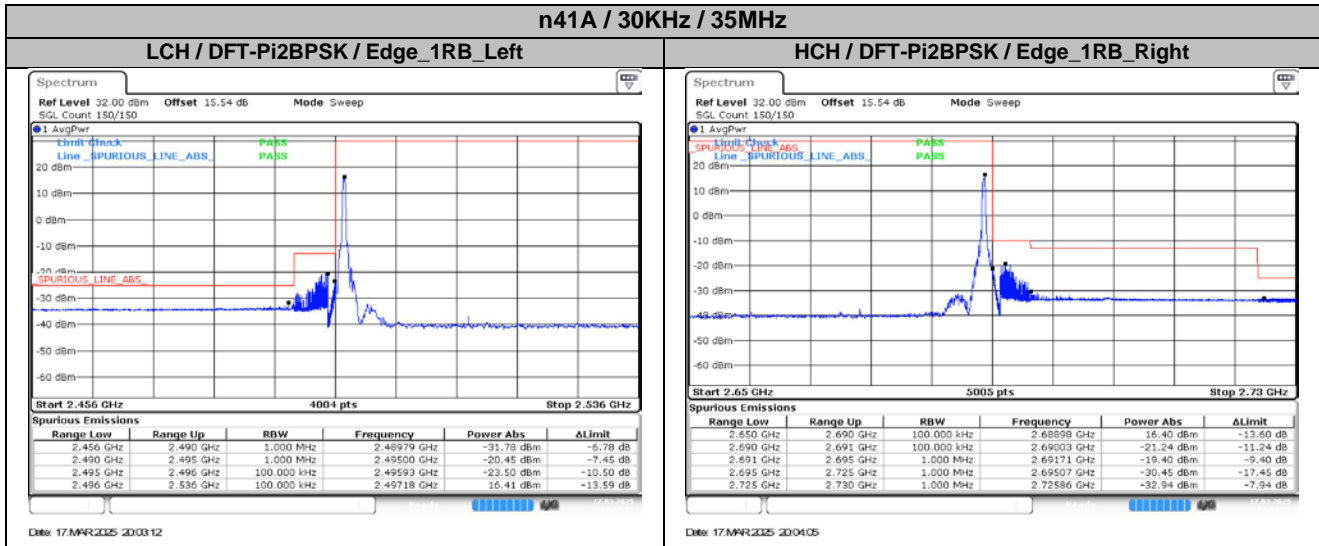
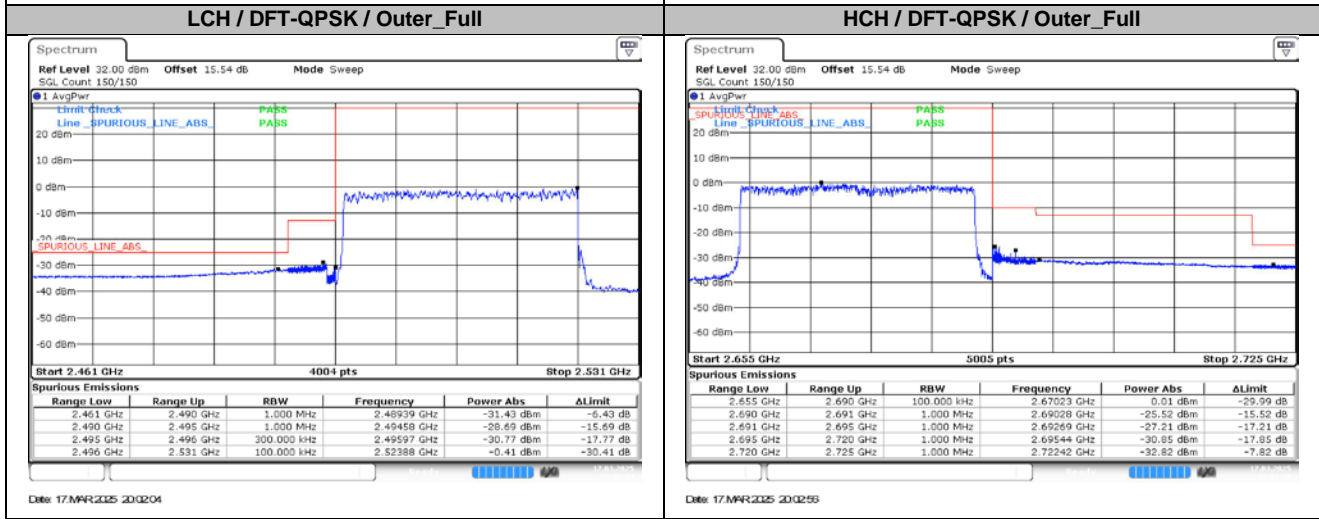
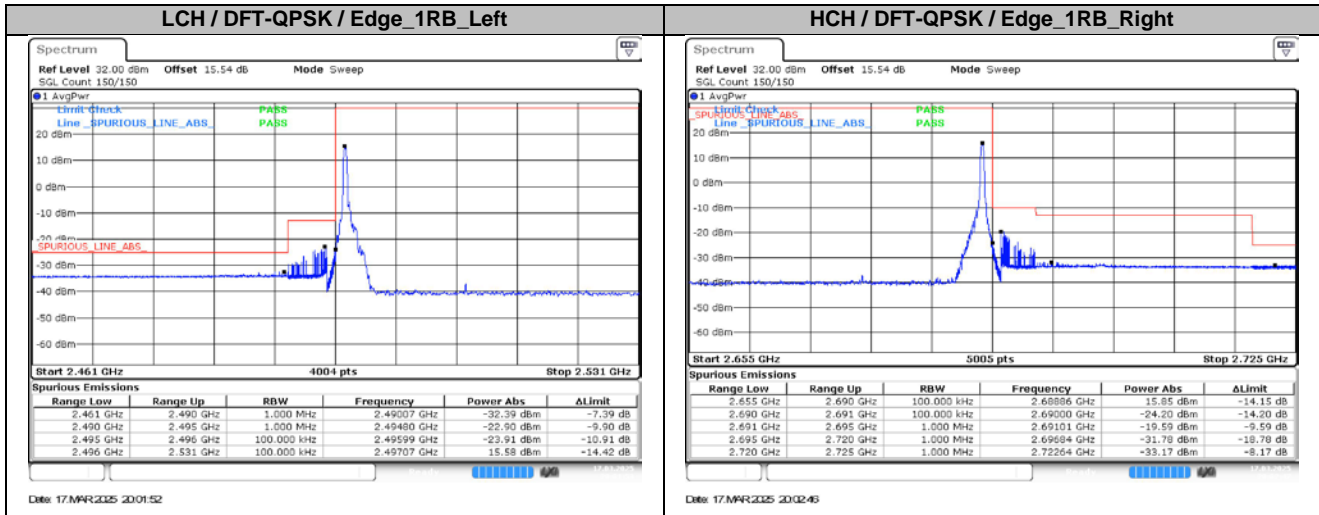
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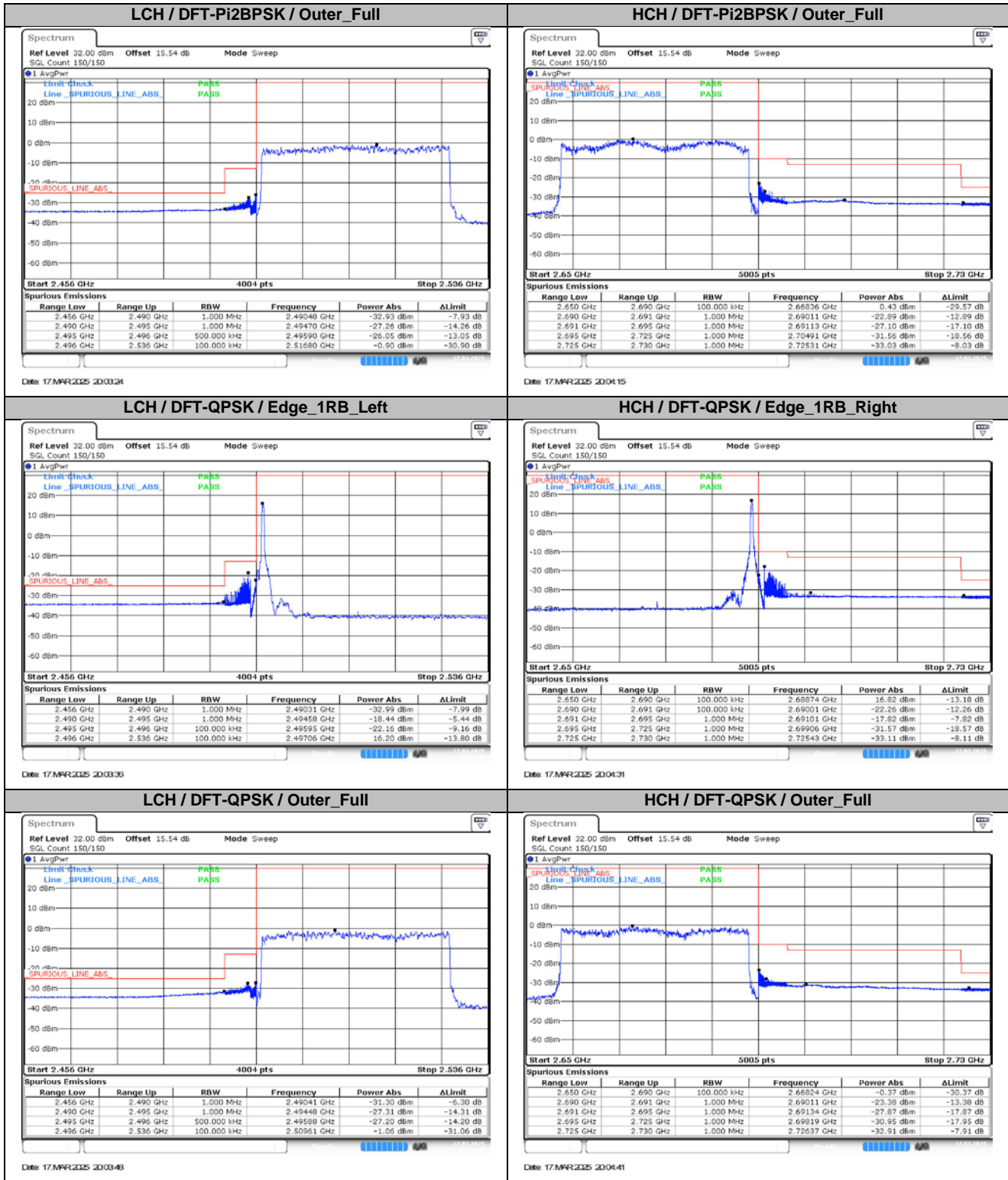
HCH / DFT-QPSK / Edge_1RB_Right

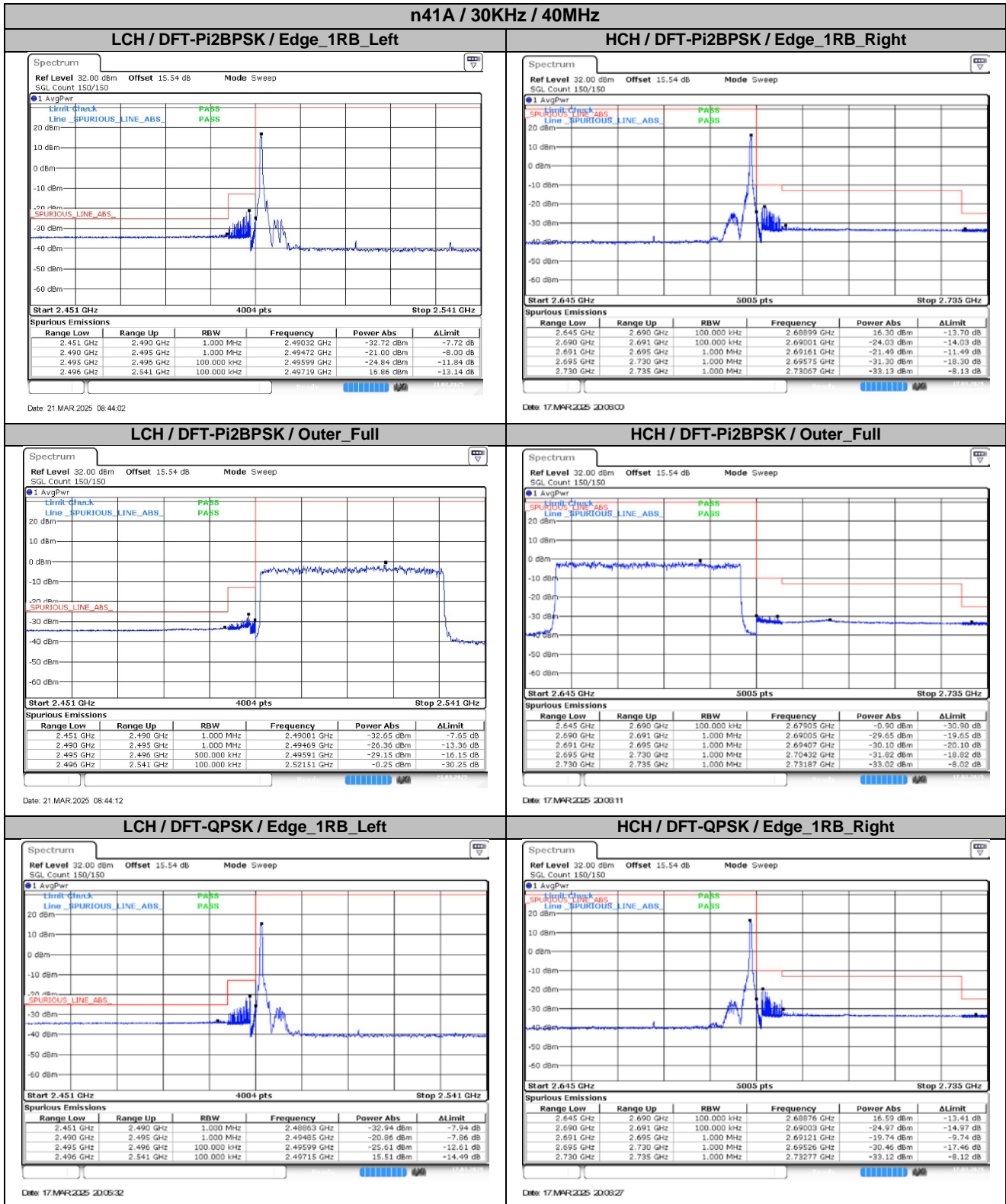


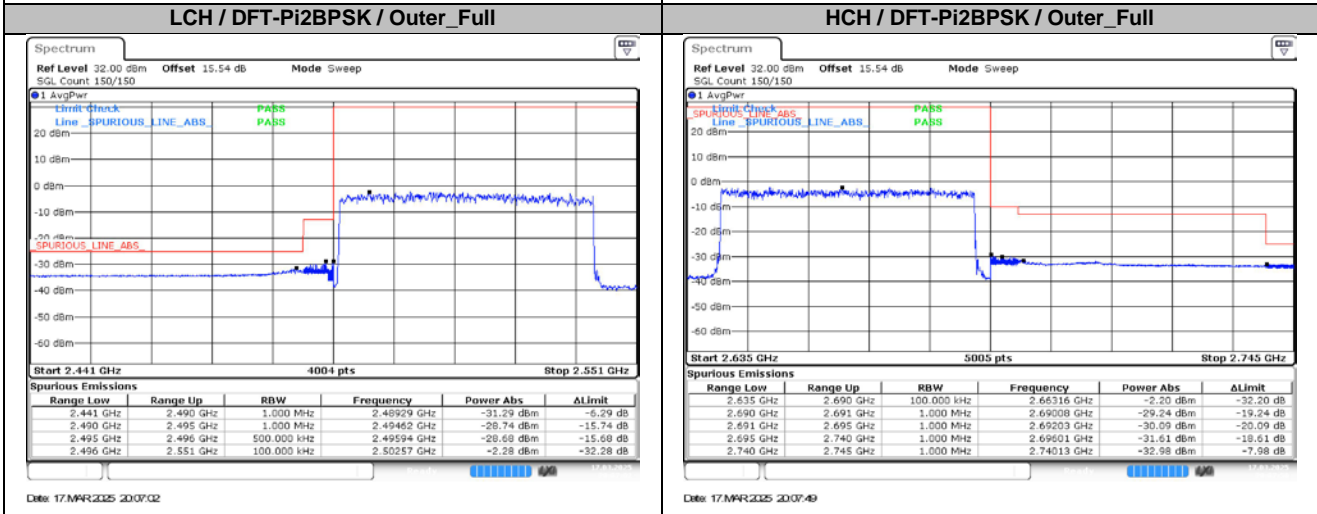
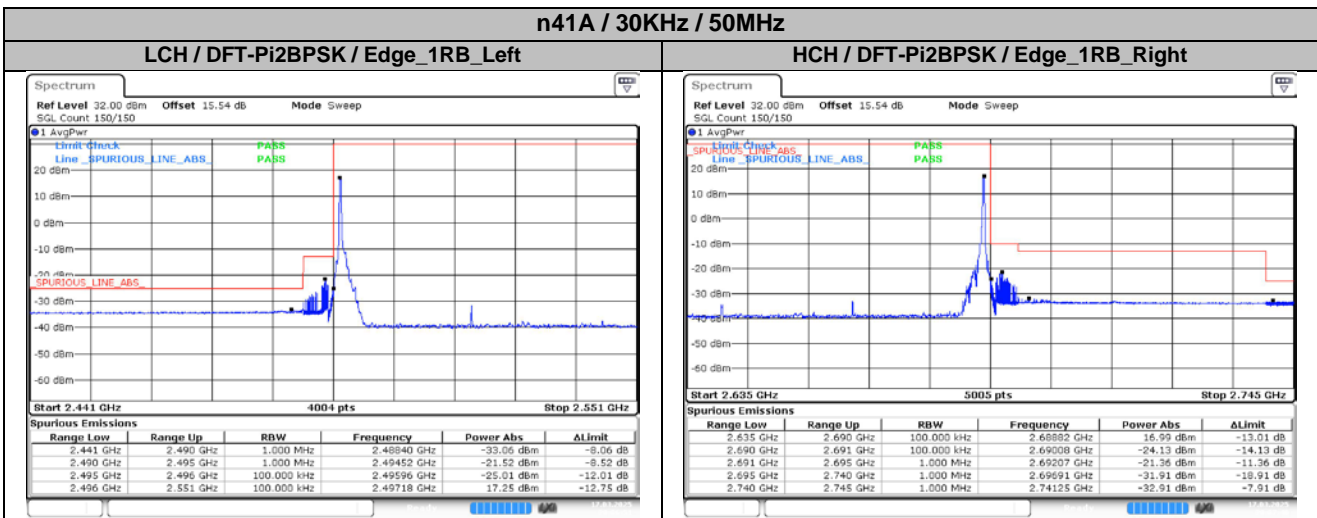
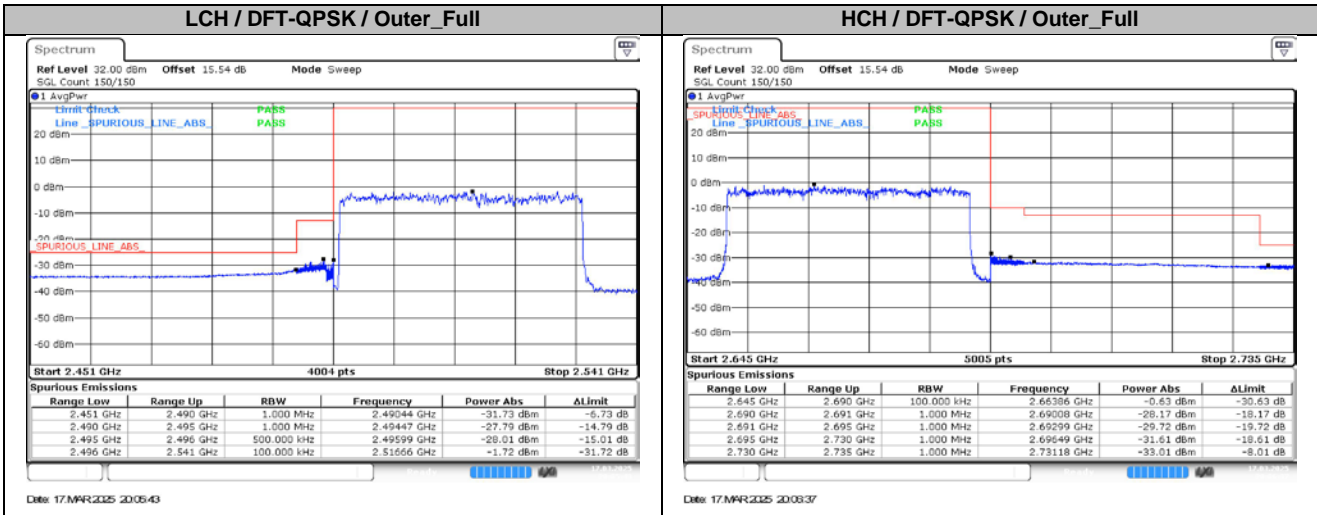
Date: 17/MAR/2025 20:00:04

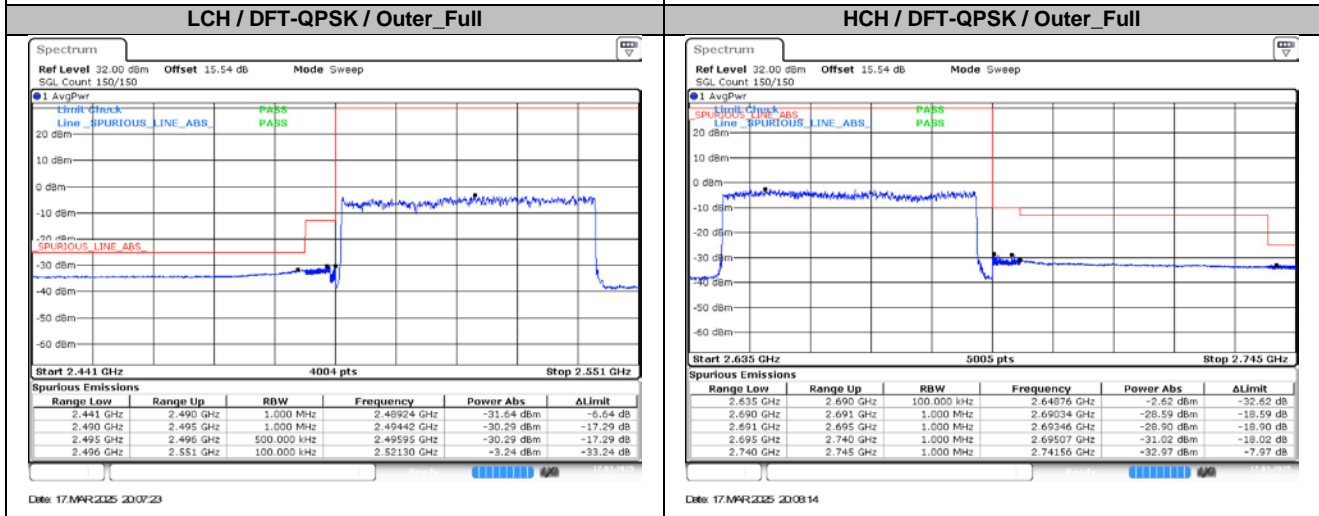
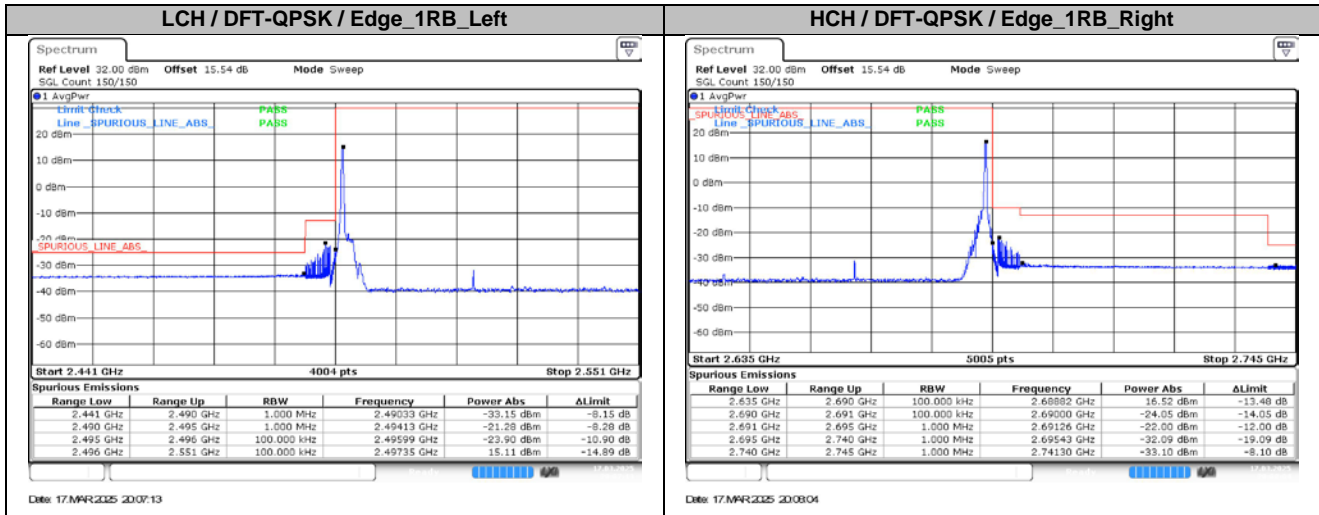












n41A / 30kHz / 60MHz

