

Logic Schematics



Revision History

Rev	Description	Date	Author
A	First Version	19 November 2002	G.Bala Krishnan
B	Incorporated one resistor each in series with the TXD & RXD lines, to improve ESD immunity. Included a line interface logic to eliminate back drive voltage from BGM. Also two ferrite cores have been added on either side of the PCB overmold to suppress EMI.	28 March 2003	G.Bala Krishnan
C	Removed the ferrite core on 3 core cable side of PCB over mold and modified the length of 3 core cable and USB cable. Added options to use 3 pin tranzorbs on locations TZ1and TZ2.	11 June 2003	S.Dhanapal

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Designed by: 	EXTERNAL REVIEWER (Client)	DEPT.	APPROVAL	DATE	INTERNAL REVIEWER	SIGN	DATE	Title: Lifescan USB Cable	
	D.Hernandez	OPS			DRAWN S.DHANAPAL			Doc Name: USB Communication Interface	
					REVIEWED S.T.MARBAN			Rev: C	
					QC CHECK R.SHEYAMALA			Size: B SHEET 1 OF 2	
CAD SOFTWARE: OrCAD V9.2					IV & V R.RAJAMURUGAN				

