## Cidco FCC ID: HOLCL980

Duty Cycle corrections can be determined\ by T1 and T2 from table 3 of the following page. Given by:

```
Ton = 1.975msec

Toff = 2.025msec

Duty Cycle calculation:

Correction Factor (dB) = 10 \log(\text{Ton} / (\text{Toff} + \text{Ton})) dB

= 10 \log (1.975/ 2.025 + 1.975)) dB

= 10 \log (0.494) dB

= 3.06 dB
```

## Applying the Duty Cycle:

E (field strength) = 122 dBuV/m @ 3 meters

$$122 dBuV/m - 3.06 dB = 119 dBuV/m @3 meters$$
  
P (Power) = (Ed)<sup>2</sup>/30 Watts

Corresponds to 238mWatts

The Power is less than 300mWatts (corrected) and thus **SAR testing is not necessary** for this device.

## Chips per Bit

The Chips per bit is determined by T7 and T13 of table 3 on the following page.

```
T7 Data frame time = 133 bits wide x 12.5 usec per bit
T13 Chip time = 1.041usec
chips per bit = 12.5 usec per bit / 1.041 usec per chip = 12.01 chips/bit
```

This illustrates a rate of 12.01 Chips Per Bit. This rate is greater than the minimum required rate of 11 Chips Per Bit. Timing diagrams are also provided on the following page.

## **RF Modem Control Timing**

Figure 4 and Figure 5 show the timing relationship of TXRX, TXEN, RXEN and the baseband transmit signal (TXDATA) and received signals (RXI, RXQ). Table 3 lists the timing parameters.

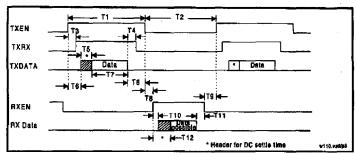


Figure 4. RF Timing Diagram

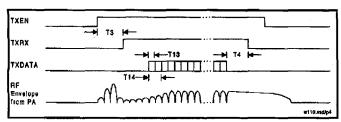


Figure 5. RF Envelope Timing Diagram

Table 3. RF Modern Timing Parameters

Name	Description	Value
T1	TXEN-On Time	1.975 ms
T2	TXEN-Off Time	2,025 ms
Т3	TXEN-On to TXRX-On	8.3 µs
T4	Data-Off to TXRX-Off	8.3 µs
Tō	DC Settling Time	23 × 12.5 µs
T6	TXEN-On to Data-On and Data-Off to TXEN-Off	12.5 µs
T7	Data Frame Time	133 x t2.5 μs
T8	TXEN-Off to RXEN-On	12.5 µs
T9	RXEN-Off to TXEN-On	> 0 µs
T10	RXEN-On to Expected RX Data	≥ 12.5 µs
T11	RX Data-Off to RXEN-Off	12.5 µs
T12	RXEN-On to RX Data DC and Gain Settle	< 300 µa
T13	Chip Time	1.041 µs (1/960 KHz)
T14	TX Settling	< 300 μs*

\*

Preliminary

W116