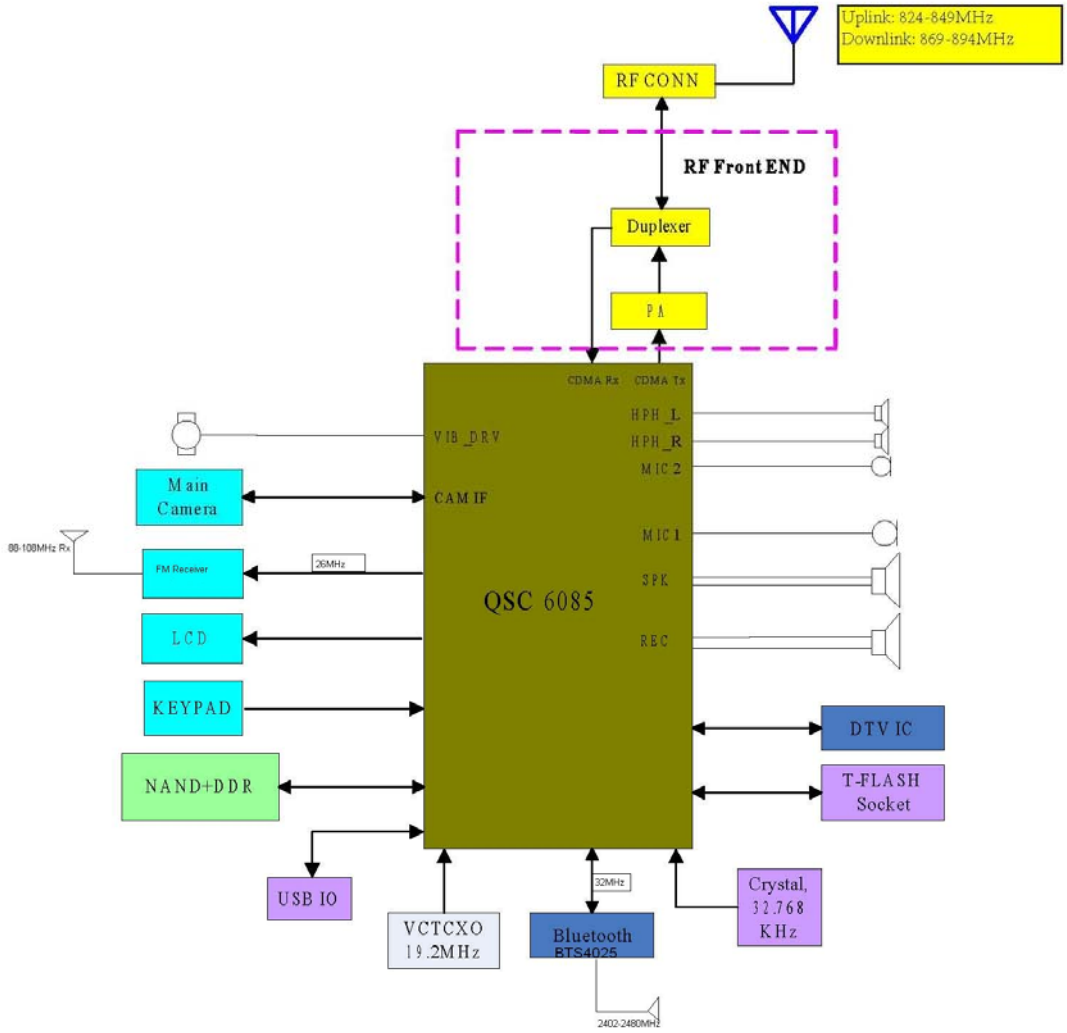
Operation Description

E3240 BLOCK diagram



E3240 is based on the Qualcomm QSC6085-1 platform, with the following components.

1. CPU: QSC6085-1-1
2. PA : WS1103-TR1
3. NAND&DDR: MT29C1G12MAVNAJC-6 IT

2.2 Circuit of Functional Unit

2.2.1 Baseband Unit

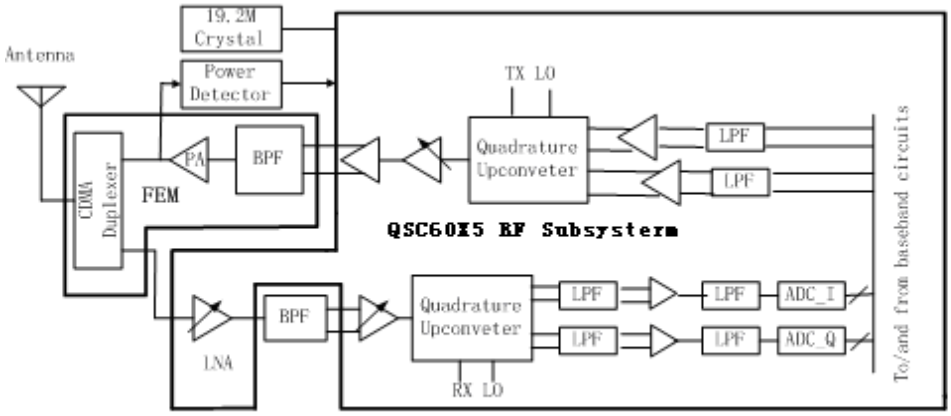
The baseband is made up of CPU, memory and some peripheral drive circuits in the main. CPU integrates multiple processor on-chip: one ARM microprocessor (ARM926EJ-S) and one DSP processor (mDSP). mDSP is dedicated for modem functions and CDMA process. ARM9 offers different interface such as RF interface, UIM card interface, USB interface, I2C interface, UART interface and JTAG interface.

2.2.2 RF Unit

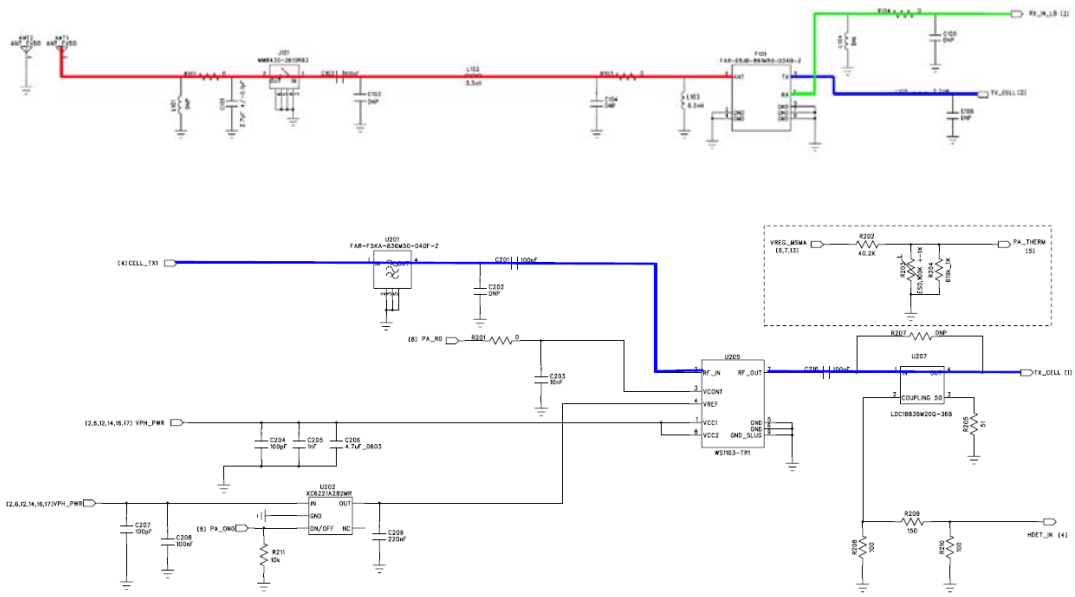
The RF circuit of E3240 includes: antenna, RF connector, duplexer, PA, TX SAW filter and RX SAW filter.

QSC6085-1 device (adding CDMA2000 diversity and CDMA2000 EV-DO rev. A support) devices.
Modulation: QPSK
RF transmitter Cellular-CDMA, band class 0: 824 to 849 MHz
RF receivers Cellular-CDMA, band class 0: 869 to 894 MHz
QSC6085-1 data rate is FL 3.1Mbps / RL 1.8Mbps
QSC6085-1 single chip integrates the RF subsystem, which includes RF transmitter, receiver, Frequency synthesizer, and power distribution circuit. The RF subsystem inside E3240 support CDMA800 (BC0), and the transmitter and receiver are zero intermediate frequency (ZIF) architecture, thus those image filter and IF filter for super heterodyne architecture system are not required.

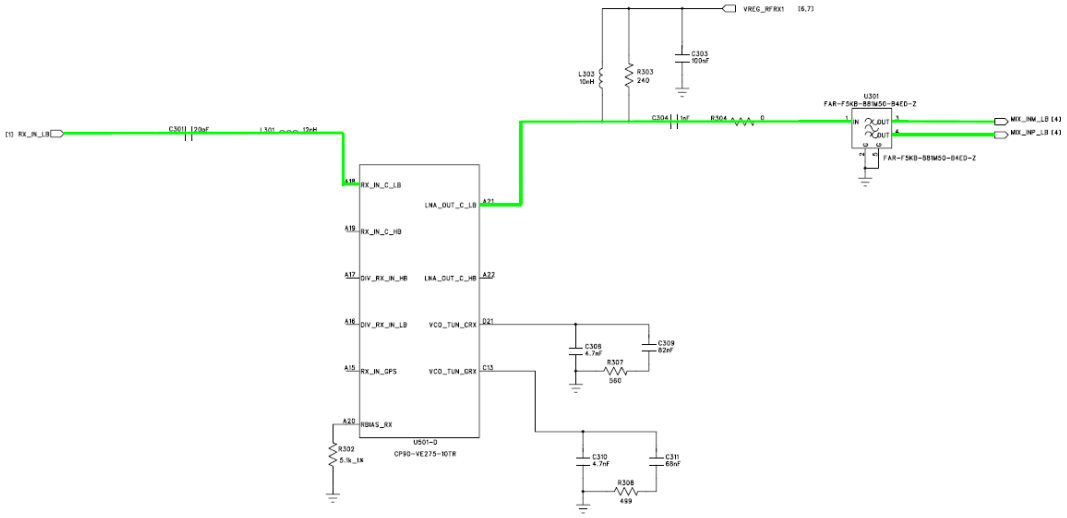
VGAs (variable-gain amplifier) in the transmitter and receiver are controlled by baseband circuits. The LO signals for the direct up-converter and direct down-converter are generated by the PLL, and the frequency is variable according to the channel ID.



Transmission: The transmit signal is directly up-converted from the baseband to RF, and amplified by the VGA, then amplified by the PA, and finally radiated by the antenna.



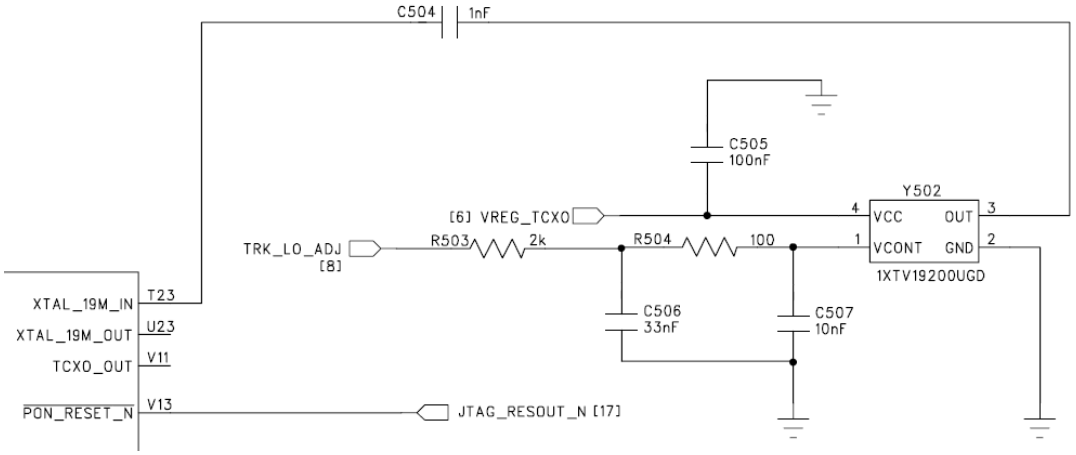
Receiving: The received signal is fed in through the antenna and duplexer, and is amplified by internal LNA, filtered by balun filter and then directly down-converted from RF to baseband. Before demodulation, the signal should be filtered, amplified and converted from analog signal to digital signal



Red: signal to / from antenna; Green: Rx signal; Blue: Tx signal

Local oscillation

Y502 is a 19.2M+/-10ppm.



Power supply

Type/name	Default conditions	Voltage range and increment	Low power	Intended use
SMPS - buck (500 mA)				
MSMC	On, 1.300 V	0.750 to 3.050 V; 25 mV steps	PFM	Core processor at 1.3 V or adjusted dynamically
Linear - 300 mA				
MSMP	On, 2.600 V	1.500 to 3.050 V; 50 mV steps	LP	Periphery circuits; should be on at default voltage
Linear - 150 mA				
MSMA	On, 2.600 V	1.500 to 3.050 V; 50 mV steps	LP	Analog circuits
MSME1	On, 1.800 V	1.500 to 3.050 V; 50 mV steps	LP	Devices on EBI #1 bus
MSME2	On, 2.900 V	1.500 to 3.050 V; 50 mV steps	LP	Devices on EBI #2 bus
RFRX	Off, 2.600 V	1.500 to 3.050 V; 50 mV steps	LP	RF receiver circuits
RFTX	Off, 2.600 V	1.500 to 3.050 V; 50 mV steps	LP	RF transmitter circuits
RUIM	Off, 2.850 V	1.500 to 3.050 V; 50 mV steps	LP	RUIM module
Linear - 50 mA				
TCXO	On, 2.850 V	1.500 to 3.050 V; 50 mV steps	LP	TCXO circuits
USB	Off, 3.300 V	3.000 to 6.100 V; 100 mV steps	LP	Internal USB transceiver; not for external loads

2.2.3 Bluetooth Unit

The BTS4025 device is a 0.13 μm CMOS system-on-chip (SoC) with integrated baseband and 2.4 GHz radio for Bluetooth wireless technology applications with enhanced data rates (EDR) up to 3 Mbps.
The BTS4025 IC supports both class 2 and class 1 power level transmission without requiring an external power amplifier.
The BTS4025 device is intended for use in mobile phone systems and other applications requiring Bluetooth functionality with a pulse coded modulation (PCM) interface, and a host controller interface (HCI) using a UART transport.
The BTS4025 has the option to control sleep/wakeup by using either software or hardware. Low power page scan function reduces device power consumption significantly.
The BTS4025 offers high levels of performance with increased output power to 6 dBm, and a significant reduction in page scanning current. The device is offered in an ultra-small wafer level chip scale package (WLCSP) with industry standard BGA ball pitch and ball diameter. The package design, along with no requirement for underfill and a small number of external components, reduces the overall footprint and system costs substantially.
The hardware and ROM-resident firmware are fully compliant with the Bluetooth V2.1 + EDR specification, including all mandatory and optional features, except for multiple SCO/Esco connections; only one SCO or eSCO connection at a time is supported. The BTS4025 packet traffic arbitration (PTA) coexistence feature provides reliable performance of both the Bluetooth when used in a collocated environment.