

WA3101-07

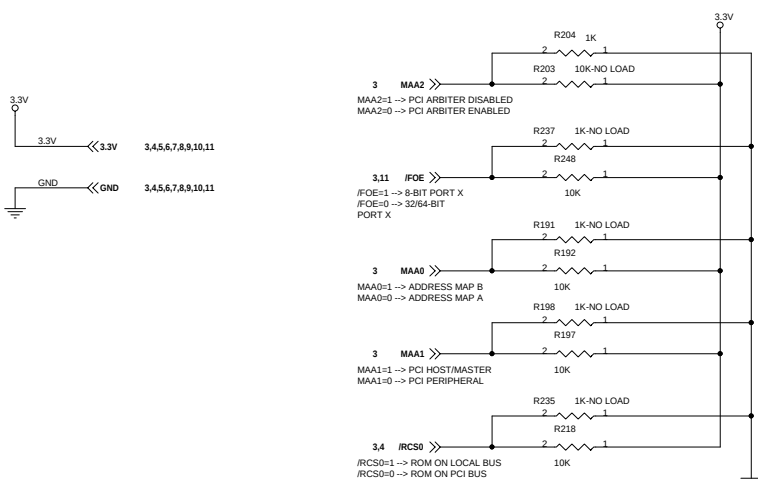
REVISIONS and UPDATES

REV/UP	DESCRIPTION	APPROVAL/DATE

PROPRIETARY INFORMATION
PRELIMINARY

 Accton Technology Corporation 3F, No. 9, Nan-Ke 3th Rd., Taiwan Science-Based Industrial Park, Hsin-Shi, Taiwan 744 Taiwan, R.O.C.	Title COVER_PAGE			Document Number : WA3101-07
	Size A4	Rev R01	Sheet 1 of 11	Date: Thursday, March 06, 2003

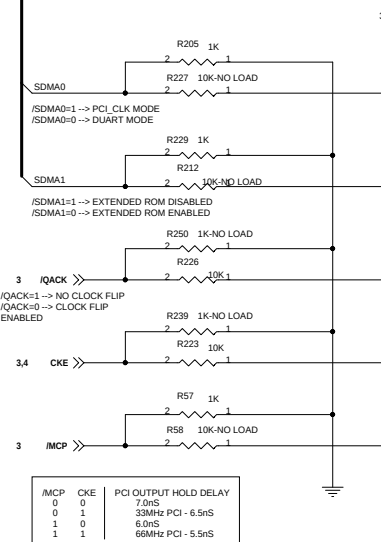
PCI CLOCKS



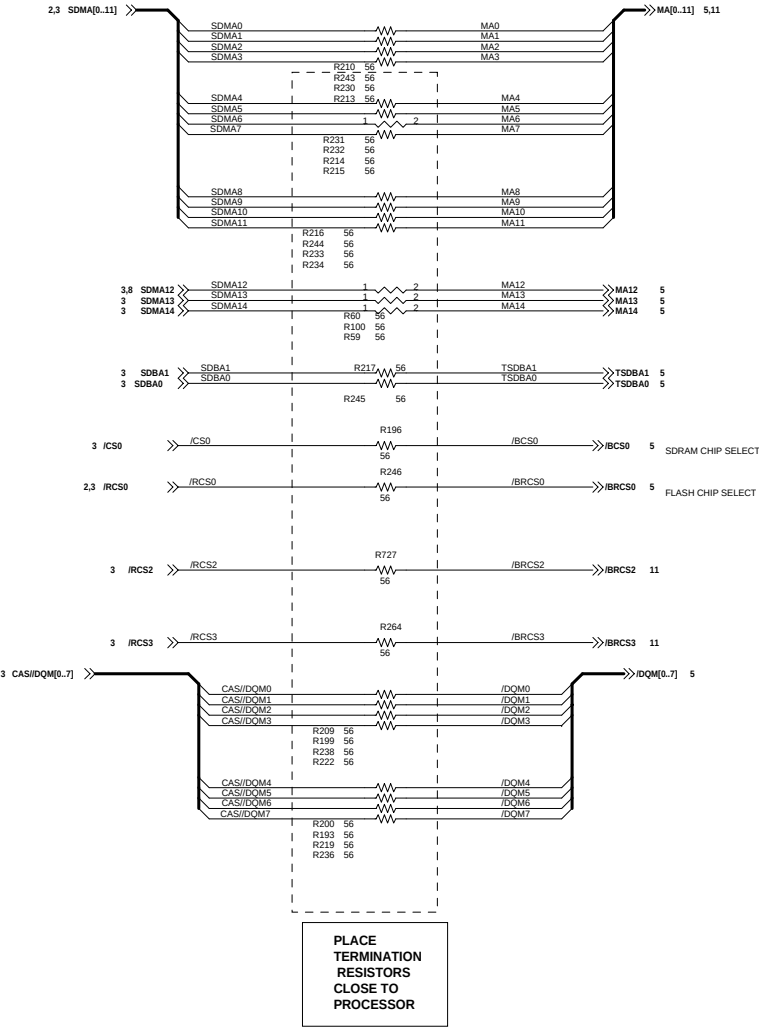
PMAA0	PMAA1	DATA BUS	ADDRESS BUS	
0	0	40 OHM	40 OHM	MEDIUM HERCULEA ZEUS
0	1	40 OHM	20 OHM	
1	0	20 OHM	13.3 OHM	
1	1	20 OHM	8 OHM	

PLL_CFG[0:4]	MAX PCI CLK INPUT (MHz)	MAX MEMORY CLK (MHz)	MAX CPU CLK (MHz)
0x00 = 0 0000	33	100	250
0x01 = 0 0001	27	87	243
0x02 = 0 0010	55	175	500
0x03 = 0 0011	66	66	133
0x04 = 0 0100	42	84	168
0x05 = 0 0101	66	66	168
0x07 = 0 0111	66	66	200
0x08 = 0 1000	66	66	200
0x0A = 0 1010	27	58	243
0x0C = 0 1100	42	84	210
0x0E = 0 1011	41	84	244
0x10 = 0 1000	33	100	200
0x12 = 0 1100	66	100	200
0x14 = 0 1010	33	100	175
0x16 = 0 1011	31	66	248
0x18 = 0 1101	33	66	248
0x1A = 0 1100	62	66	248
0x1C = 1 1010	65	89	248
0x1E = 1 1011	65	89	248

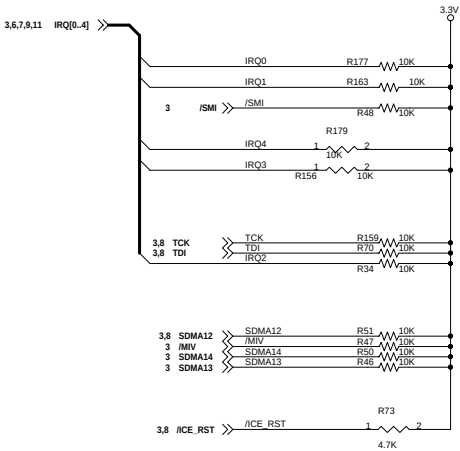
The schematic diagram illustrates the PLL output divider circuit. It features five PLL output signals (PLL_CFG0 to PLL_CFG4) connected to a common output bus. Each signal passes through a resistor (R56, R55, R188, R187, R185, R186, R61, R52, R49, R53) and is then connected to a 1K-NO LOAD. The output bus is connected to a 1K-NO LOAD.



SDRAM
MEMORY
TERMINATION

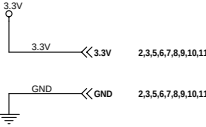
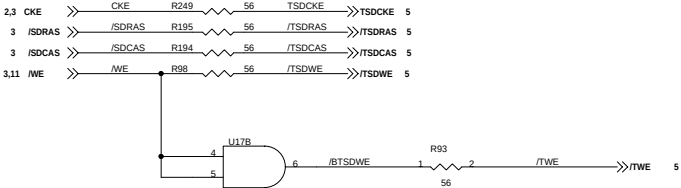


TERMINATION



PLACE
TERMINATION
RESISTORS
CLOSE TO
PROCESSOR

SHORT TRACES

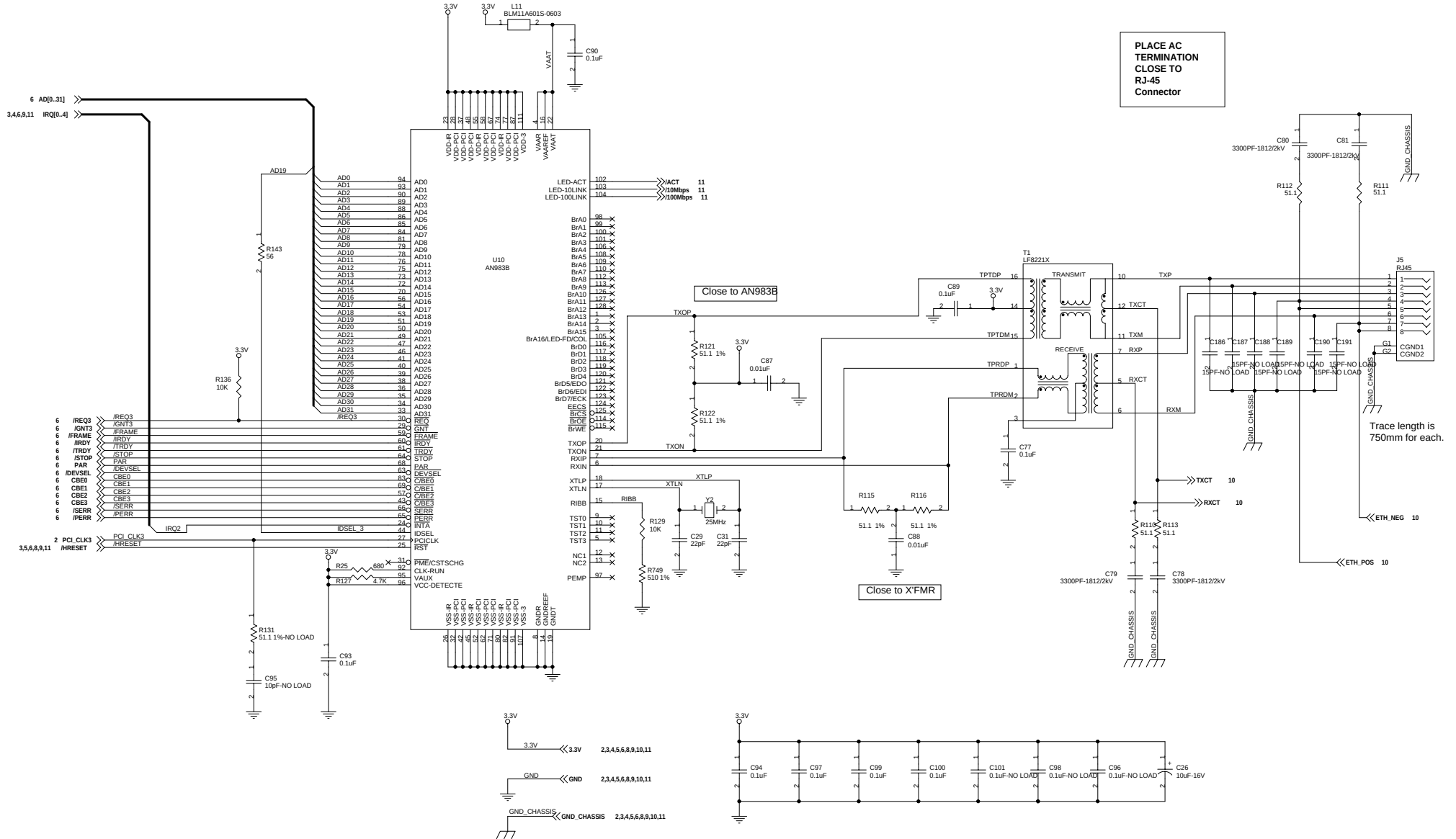


SH



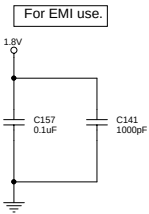
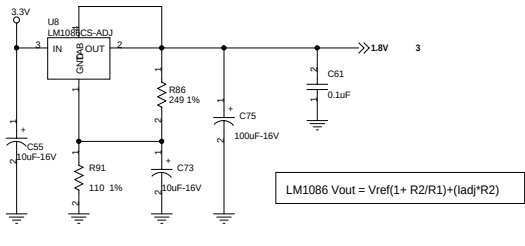
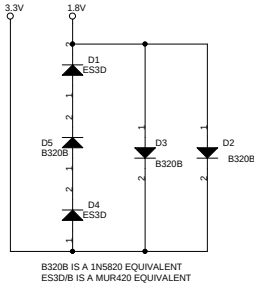
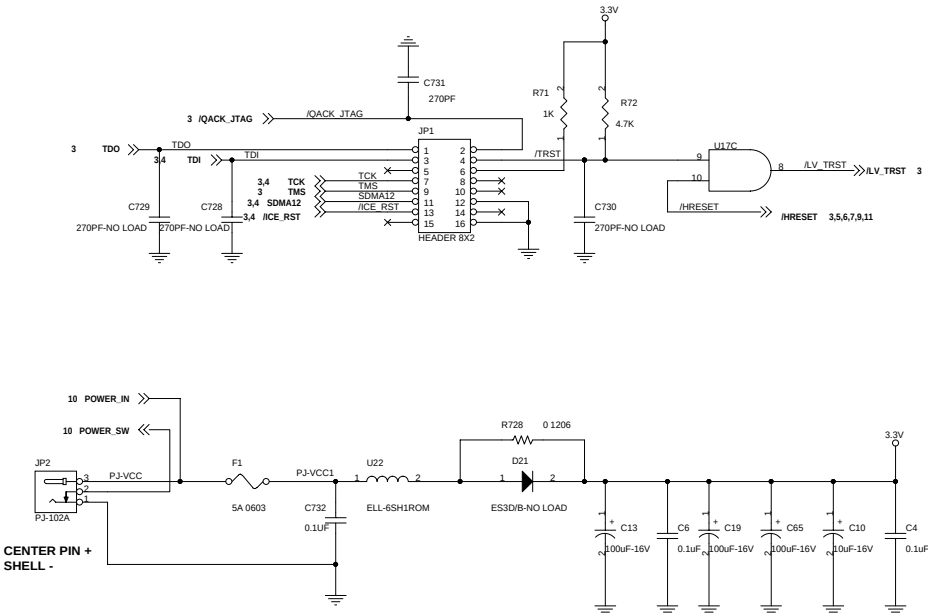


10/100 ETHERNET



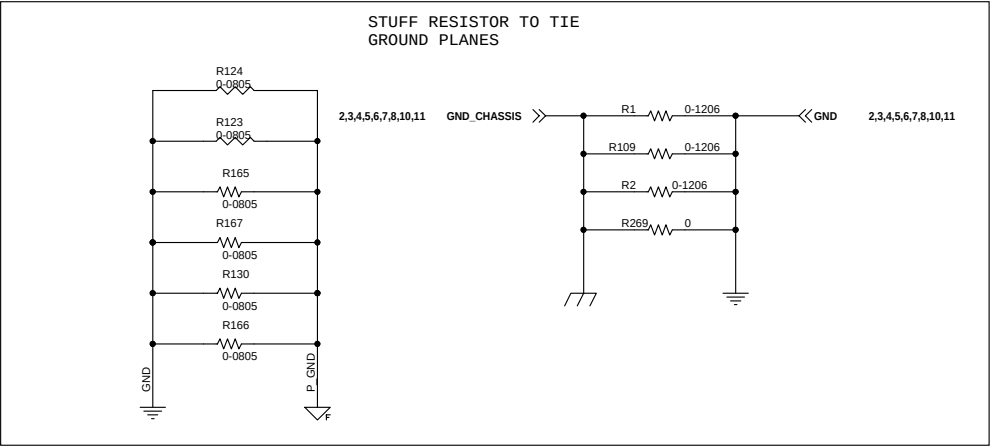
JTAG INTERFACE
FOR VISION ICE

VOLTAGE
SEQUENCING

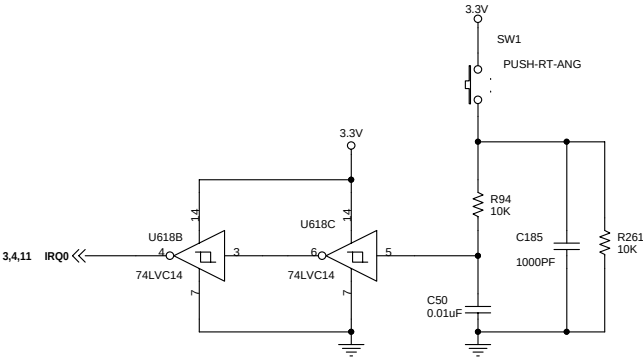
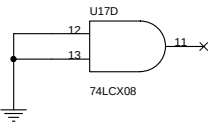
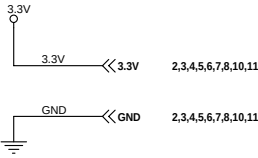
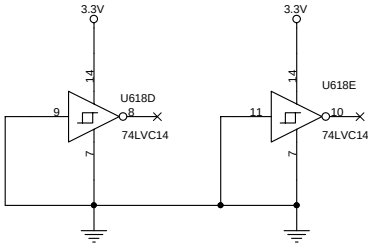
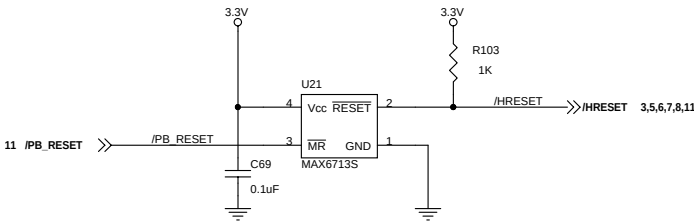


MPC8245 Motorola Power Supplies	MPC8245 Worst Case Power Sizing
LVdd = 3.3V or 5.0V - Ref.	GVdd Power --> 0.9W --> 273mA
GVdd = 3.3V - Memory Drivers	OVdd Power --> 0.6W --> 182mA
OVdd = 3.3V - PCI Stnd.	
Vdd = 2.0V - Core	2.0V Power --> 2.1W --> 1.05A
LA Vdd = 2.0V - DLL	
AVdd = 2.0V - PLL	
AVdd2 = 2.0V - PLL	

ACCTON CONFIDENTIAL
PRELIMINARY



RESET MONITOR



Accton Technology Corporation 3F, No. 9, Nan-Ke 3th Rd., Hsin-Sai Science-Based Industrial Park, Hsin-Shi, Taiwan 744 Taiwan, R.O.C.	Title				Document Number :	
	MPC8241 Based Access Point + Mini PCI				WA3101-07	
	Size	Rev	Sheet		Date:	
	C	R01	10 of 11		Thursday, March 06, 2003	

