PB2320 Digital circuit

1. Outline

This product has the function as A/N pager and Voice playing function. The functions of the A/N pager are controlled by the 16bit CPU. The function of the voice playing is controlled by the 16 bit DSP.

2. The function of the A/N pager

This digital unit has the 16bit CPU(Mitsubishi M30610) which controlled all function. The function of this block is below.

(1)The I/F function to the FLEX decode IC
(2)The display function by the LCD
(3)The back light function by the EL
(4)Buzzer(Alert)
(5)LED(Alert)
(6)The vibrator
(7)The ID-ROM(EEPROM)
(8)The I/F function to the ID-ROM Writer
(9)The detection of the Battery voltage
(10)The switch function

Almost all the circuit needs the +3V power. But the final drive of LED, BUZZER, and VIBRATOR and the voltage step up IC of the EL are connected to the battery directly.

2.1 CPU(IC102)

This product use the 16bit CPU. There are five reasons of selecting the CPU.

(1)The pager must manage and accumulate the big size of the voice data.
(2)The pager will handle and accumulate the Chinese characters providing for the future.
(3)The pager must realize the long battery life.
(4)The CPU must manage the voice data through bit handling. So the pager needs high performance by the cpu.
(5)This products has the many big parts rather than normal pager. So this pager control the many functions directly.

The CPU has the external Flash-ROM(4Mbits) and the external S-RAM(2Mbits) and the internal S-RAM(10Kbytes). But this print wire board is designed for connecting either the mask ROM or the Flash-ROM.

This CPU is running through 38.4KHz clock and 3.3024MHz clock. The detail is below.

	High speed clock	low speed clock(sub clock)
clock source	ceramic resonator	supplied by decode IC
frequency	3.3024MHz	38.4KHz
service	initial program running(1/8) normal program running(1/2) clock source of the communication	slow program running timer A, B
clock control	stop if the CPU go to the power down mode	always running

2.2 The interface of the FLEX decode IC

The interface between the FLEX decode IC and the CPU consists of 7 signal lines. The communication from the CPU to the Decode IC is realized by the synchronous serial interface(SSI) and some control signals. The transfer speed is 550Kbps. The details are below.

Signal Name	Signal Description	generating
MOSI	data output line	CPU
MISO	data input line	Decode IC
SCK	The clock signal using the synchronize the data transfer	CPU
SS	This signal is used to enable the SSI slave for transfer. (slave select signal)	CPU
READY	attention signal for CPU	Decode IC
DECRST	The reset signal for decode IC	CPU
F38R4K	The clock signal of 38.4KHz	Decode IC

2.3 The display function by the LCD

The function of displaying to the LCD is realized by the LCD driver(SED1567T0C) which is made by SEIKO EPSON. The products can display 32 X132 dots(4lines X 22characters) and some icons.

This product can display not only 5X7 dots characters but also many graphic icons and large size characters.

This product has two display mode. The one is active mode in which mode the product is active , and the another is power-down mode in which mode products display only icons.

The interface between the CPU and the LCD driver is used memory mapped I/O. The details is below.

Address of memory	Control Description	direction
4000h	The status of LCD driver	read/write
4001h	The display data	read/write

2.4 Lighting

This product adopts the Electro-Luminescent sheet for the lighting. This product use the SM8141AV which is made by NPC for EL driver. The CPU control the SM8141AV through TR101. This EL driver use the +3V for own logic and +1.5V for voltage stepping circuit.

2.5 Buzzer(Alert)

This product has the buzzer for the receive notice tone and time alert. This buzzer is popular as the pager. The speaker for voice is another device.

The program of the CPU manage the pulse width modulate controller of the timer module which is involved the CPU and make alert sound.

2.6 LED

The LED of this products turn on and off during receiving alert or time alert. The program of the CPU manage the pulse width modulate controller of the timer module which is involved the CPU and make the timing of lighting.

The LED(LED101) and it's driver(TR106) are driven by +1.5V.

2.7 Vibrator

The vibrator go on if user select the no beep mode during time alert or receive alert. By the way the CPU control the vibrator but the vibrator and it's driver exist on the RF board.

2.8 EEPROM(ID-ROM)

This product has 4Kbits EEPROM(S-29L394A) which is made by SII. The EEPROM is used as ID-ROM. This pager gets the information of address and another functions from the ID-ROM. This chip is non volatile RAM.

This chip is connected to the CPU by the synchronous serial interface. The transfer speed is 206.5Kbps. This CPU uses this chip only in time of initial processing or use setting.

The details of connection is below.

Name of signals	Signal Description	Generating
DI	write data line	CPU
DO	read data line	EEPROM
SK	the clock of the data transfer	CPU
CS	chip enable	CPU
PROTECT	write protect	CPU

2.9 The interface with ID-ROM writer

The product has the interface between the ID-ROM writer and the CPU. This product connect the ID-ROM write via TL-188 adopter. The interface between TL-188 and ID-ROM writer is RS-232C. The CPU communicate to the ID-ROM writer and read or write to the EEPROM. In this product the circuit use +3V and the TL-188 make the RS-232C level. The transfer speed is used at 4800bps.
The details of this interface is below.

The name of the signal	Signal Description	Direction
TXD	send data	OUT
RXD	receive data	IN
E2ON	The status of connecting this I/F	IN
GND	grand level	GND
+3V	This power is used for status(E2ON)	OUT
+1.5V	The power of this products	IN

2.9 The checking the voltage of the battery

The product has the IC103 which can superintend the voltage of the battery. This chip can detect the BLD(Battery Low Detect) and 4levels of voltage. The detail is below.

Detect voltage [V]	Description	Detect timing
over 1.4	Battery full	60 second
1.33 - 1.37	3/4	60 second
1.27 - 1.30	1/2	60 second
1.185 - 1.215	Low battery notice	60 second
1.089 - 1.111	BLD(Battery Low Detect)	100 m sec 500 m sec

2.10 Switch

This product has 9 switches. Only Power Switch connects to the CPU direct. But other switches are mapped to the memory at 28000h address through IC113. If the product is in active mode then all the switches are sensed each 100m second. If the product is in power-down mode then all witches are sensed ever 500 m second.

3. The function of the voice playing

This digital unit has the 16 bit DSP(IC115:Motorola DSP56LF812) which control all the function of the voice playing. The functions of the voice playing consists of the six parts. The detail is below.

(1)DSP

(2)The interface function to the CPU

(3)CODEC

(4)Audio Amplifier

(5)Speaker

(6)Power down control

3.1 The DSP

This product use the 16 bit DSP. The DSP expands the compressed voice data to original voice data. The DSP controls the CODEC and Audio Amplifier and play the voice and other tone. The DSP generate s the sighn-wave for test or notice tone. The DSP controls the volume of the voice and other tone according to the command from the CPU. The DSP controls the power-down operation to the CODEC and Amplifier.

The DSP is running through 32.0KHz clock and 10.0MHz clock. But the high speed clock (10.0MHz) is generated in the DSP from 32.0KHz. The DSP has four running mode. The detail is below.

MODE	Description		low speed clock
Power Down	all module in the DSP are stopped	STOP	STOP
Waiting for the command	STOP MODE waiting for interrrupt	STOP	RUNNING
processing the command	running	RUNNING	RUNNING
playing the voice	running	RUNNING	RUNING

3.2 The interface function to the CPU

The interface between the DSP and the CPU consists of 8 bit parallel data bus four control lines. The detail is below.

Name of signal	description	Generate
Data bus (8 lines)	8 bits data bus	CPU,DSP(dual direction)
RIN	The attention from the CPU to the DSP	CPU
DSPRAK	The DSP read in the data and send the acknowledge to the CPU.	DSP
DSPRIN	The attention from the DSP to the CPU	DSP
RAK	The CPU send the acknowledge to the DSP for reading the data.	CPU

3.3 CODEC

This product has the CODEC(MC1455483) made by the Motorola. This chip exchanges the digital data to the analog data. This chip consists 13 bits D/A converter and the low-pass-filter. The DSP use the 256KHz clock for the data translating clock.

3.4 Audio Amplifier

This products use the JM2076m made by JRC as the audio amplifier. This chip can operate at 1.5V battery. This chip can amplify the sound by the circuit of BTL..

3.5 Speaker

The audio amplifier out the sound through the dynamic speaker. This speaker has the wide frequency range.

3.6 The power down control circuit

The DSP control the power down control circuit for the CODEC and the audio amplifier.

The DSP control the CODEC direct. But the DSP control the audio amplifier through the power down control circuit that consists of TR104 and C140, C142, etc..

PB2320 RF Circuit

1. Antenna

A metal loop antenna is used, forming a tuning circuit structured by C2,C3,C4 and C61.

2. High frequency amplifier

The high frequency signal inducted by the antenna is amplified by the high frequency amplifier consisting of Q1 , Q2. For the transistor , a low noise type is adopted. The connection type of the Q1 and Q2 is cascode connection.

3. F1(SAW filter)

For the band-pass filter, a SAW filter is used, which is matched with Q2 at L1, C8, C9, and C10 with the mixer part at L2, C11 and C12.

Through this filter, unnecessary waves caused by the receiving wave or the 1st local oscillator are eliminated.

4. 1st local oscillator

The 1st local oscillator consists of Q10, Q4, X1 etc. and its basic oscilation frequency is obtained under the following formula:

$$Fl1 = (FR - 21.4) / 9 \quad [MHz]$$

Fl1 : Basic oscillation frequency

FR : Channel frequency

The 1st local oscillator is consisted of two block. The 1st block oscillation frequency is used as a high frequency three times F0 at L7, C78. The 2nd block oscillation frequency is used as a high frequency three times 3xF0 at L3, C30.

This 1st local oscillation signal is sent to the mixer Q3 via C14, to be mixed with the receiving signal, making 1st IF signal of 21.4 MHz.

5. F2(Crystal filter)

A crystal filter is used for this band-pass filter.

Through this filter unnecessary waves created by 21.4 MHz.

6. 1st IF amplifier

The 1st IF frequency signal is amplified by Q5.

7. 2nd local oscillator / mixer

The 2nd local oscillator consists of IC4, X2, etc.

The basic oscillation frequency of the 2nd local oscillator is obtained under the following formula:

$$Fl2 = (21.4 - 0.455)$$
$$= 20.945 \quad [MHz]$$

The 2nd local oscillation signal is sent to the mixer included in IC4, to be mixed with the 1st IF signal, and making 2nd IF signal of 455KHz.

8. F3(band-pass filter at 455KHz)

This filter is made by ceramic filter and used for the band-pass filter at 455KHz.

Through this filter , band-pass width of 12KHz unnecessary adjacent channel signals can be eliminated.

9. 2nd IF amplifier

The 2nd IF amplifier is includes in IC4.

10. Demodulator

The demodulator consists of IC4, DS1, demodulating FSK wave by Quadrature detection.

The demodulated signal is passing the filter which is consists of IC4. The band width of this filter is controlled by FLEX decode IC for each bound-rate.

11. 2-BIT Analog to Digital converter for FLEX

Two bit A/D converter consists of IC4. This converter is a system level solution to interface a 2 or 4 level baseband audio signal to a digital decoder. 2-BIT digital signals is a direct interface to the FLEX decoder.

12. FLEX decoder

The demodulated digital signal is decoded at IC6. IC6 is XC68175(MC68175) which is made by Motorola. This IC can decode FLEX paging protocol. This chip is running with 38.4KHz crystal clock(divided by 76.8KHz). The primary function of the decoder is to process information received and demodulated from a radio paging channel, select messages addressed to the paging device, and communicate the message information to the host. This IC also operates the paging receiver in an efficient power consumption mode and enables the host to operate in a low power mode when message information for the paging device is not being received.

This chip supplies the 38.4KHz clock to the CPU. The reset signal is supplied by the CPU.

13. Driver

The driver consists of Q8 driving the vibrator(M1).

14. Constant voltage circuit for RF

Batter voltage is stabilized at IC4 and Q6 , etc., supplying to the radio frequency range. Also, the gate circuit is included to control the constant voltage output so that intermittent reception can be performed.

15. AGC circuit

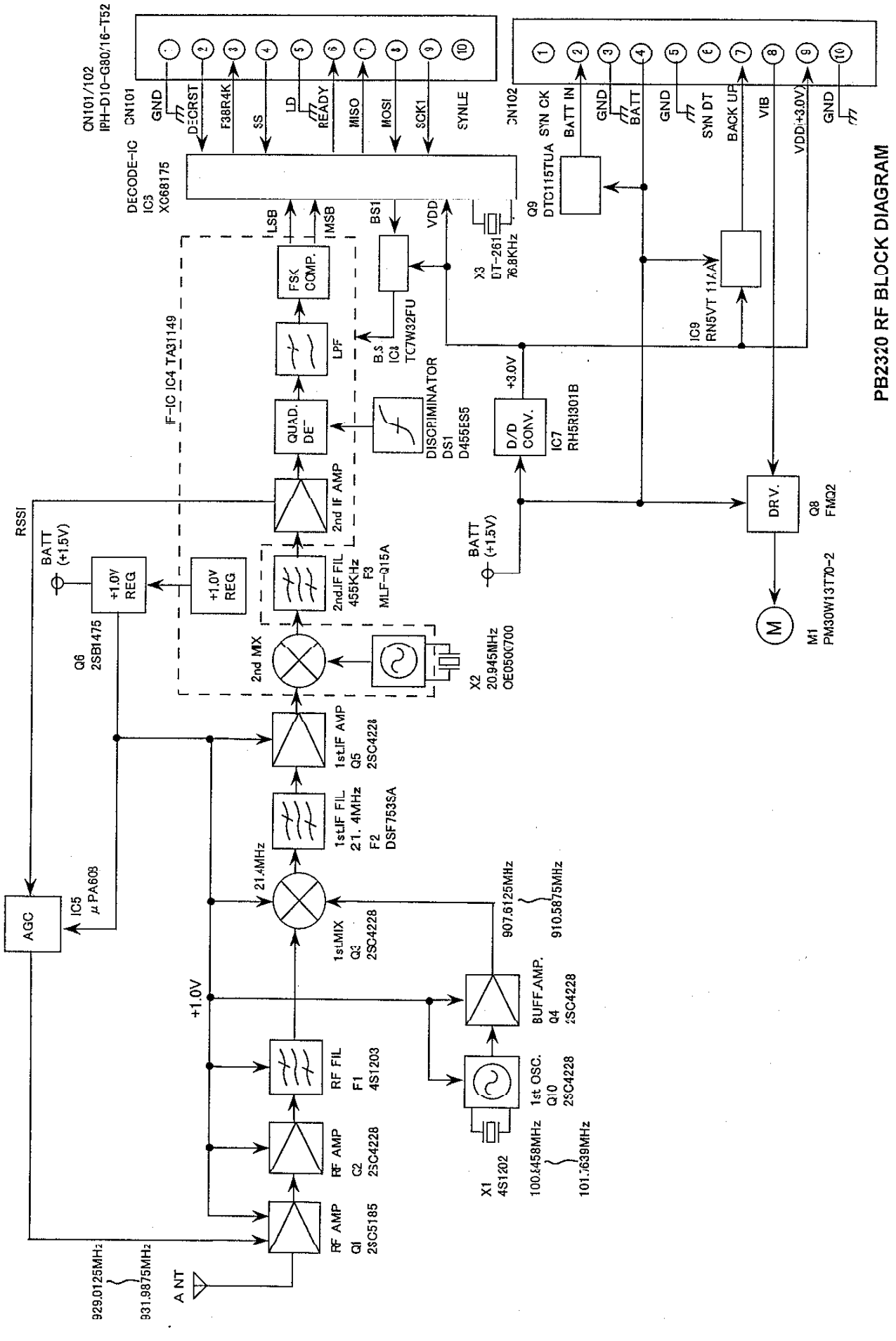
The AGC consisting of IC5 and D1 is activated when the field strength is stronger. It stabilizes the output level of receiver by limiting the receiving level(input level of the high frequency amplifier).

16. D/D converter

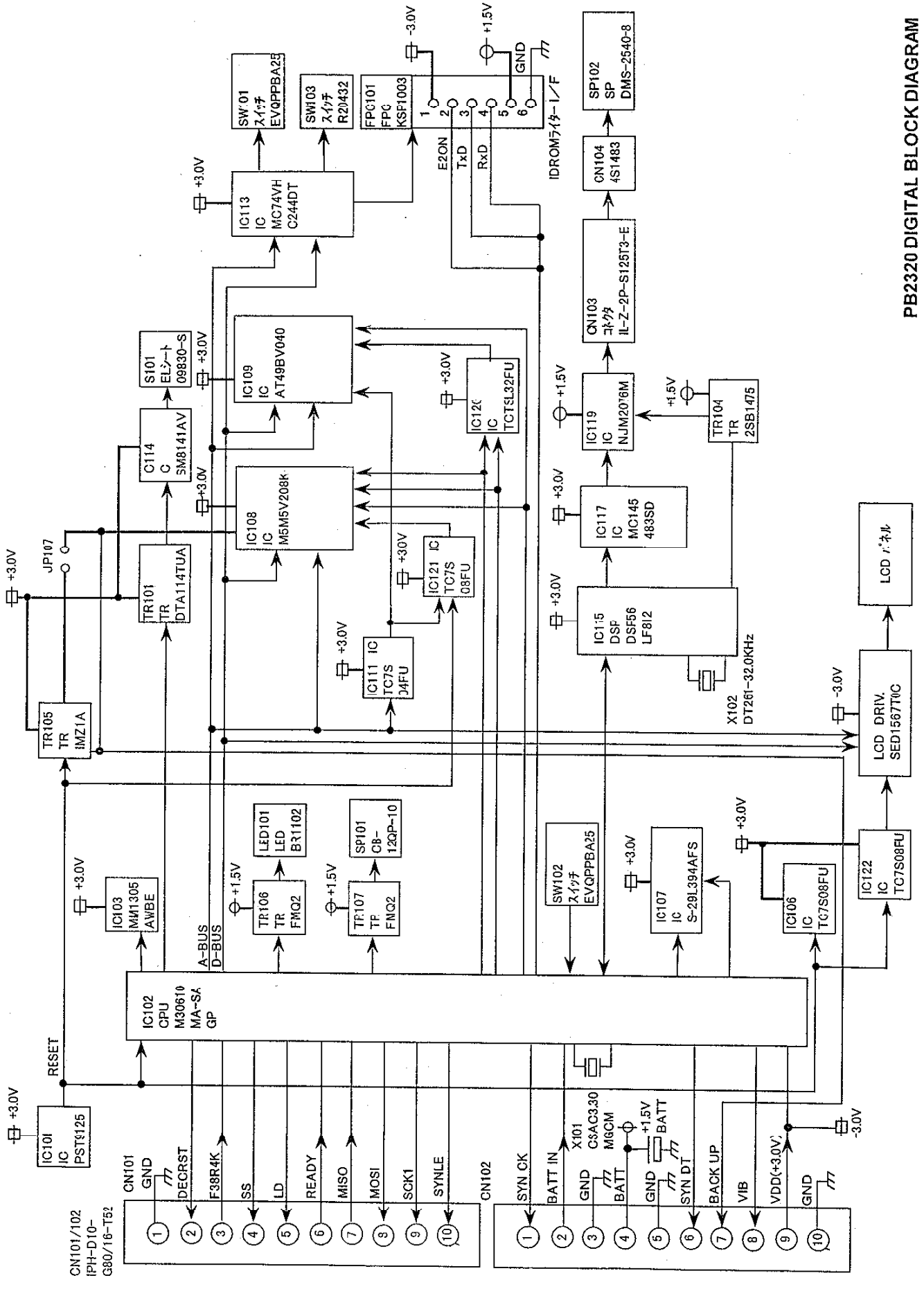
The +3V power is used by almost digital circuit. Battery voltage is transformed into +3V by IC7, L6, D4, C68, and C69.

17. RAM back up

The RAM Back Up circuit consists of IC9, D5, C75, R51, and R52. The C75 is back up battery. The IC9 supervise the back up voltage.



PB2320 RF BLOCK DIAGRAM


PB2320 DIGITAL BLOCK DIAGRAM
IC102 CPU M30610 MA-SA GP
IC101 IC PST9125
IC103 MM1305 AWBE
IC106 IC TC7S08FU
IC107 IC S-29L394AFS
IC108 IC M5M5V208K
IC109 IC AT49BV040
IC111 IC TC7S 04FU
IC113 IC MC74VH C244DT
IC115 DSP DSP56 LF812
IC117 IC MC145 483SD
IC119 IC NJM2076M
IC121 IC TC7S 08FU
IC122 IC TC7S08FU
TR101 TR DTA114TUA
TR103 TR IMZ1A
TR104 TR 2SB1475
TR106 TR FMQ2
TR107 TR FMQ2
C114 C SM8141AV
S101 EL ｼｰﾄ 09830-S
SW101 ｽｲｯﾁ EVQPPBA25
SW102 ｽｲｯﾁ EVQPPBA25
SW103 ｽｲｯﾁ R20432
LED101 LED BR1102
SP101 CB-12QP-10
SP102 SP DMS-2540-8
CN103 ｺﾈｸﾀ IL-Z-2P-S125F3-E
CN104 4S1483
FPC101 FPC KSF1003
X101 CSAC3.30 MGCM
X102 DT26I-32.0KHz
JP107
LCD ﾊﾟﾈﾙ
LCD DRIV. SED1567T0C
CN101/102 IPH-D10-G80/16-T52
CN101
CN102
+3.0V
+1.5V
-3.0V
RESET
A-BUS
D-BUS
E2ON
TxD
RxD
GND
IDROM ﾌﾗｲﾄ-ｲﾝ/F
DECRST
F38R4K
SS
LD
READY
MISO
MOSI
SCK1
SYNLE
SYN CK
BATT IN
BACK UP
VIB
VDD(+3.0V)
SYN DT
BATT