

SIMRAD-NAVICO CIRCUIT DESCRIPTION

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References:

E03656 schematic diagram.

Overview:

The front panel of the RD68W 25W mobile radiotelephone houses all the control circuitry for the radio. This includes; an 8-bit microcontroller, user controls and interfaces, display module, ATIS detection and mute circuitry. The front panel also incorporates a full class D DSC controller, by use of a V.23 modem.

Circuit Description:

All the functions of the radio are controlled from this assembly by the microprocessor IC4. The microprocessor has its own clock controlled by XTAL1 running at 7.15909MHz. Reset generator IC9 ensures that the microprocessor starts up correctly, and resets under low voltage conditions. The microprocessor has a data bus interface driving the front panel display module. External controls consist of a 21 push button key matrix, rotary squelch and volume control VR1 and VR3 respectively. The level of illumination on the LCD and keypad is controlled by TR7 driving LED's 1 to 10 and the integral LED's on the LCD module.

Configuration data, MMSI and channel information is stored in the non volatile memory IC5. This interfaces to IC4 via a 4 wire serial interface shared with the synthesiser data to the Rx / Tx PCB assembly. Separate enables ensure that the data is routed correctly.

Volume control VR3 controls the level of audio in the loudspeaker. Amplifier IC2a boosts the level delivered to the handset earpiece. Individual mutes of the handset and speaker audio are provided by TR3 and TR4 respectively, under control of the microprocessor. The voltage on the squelch control and noise input from the Rx/Tx PCB are read and the audio muted as appropriate. Additionally the state of the handset is detected from SKT1 to mute the speaker when the handset is off cradle (optional).

The handset interface is via connector SKT1. The microphone input is biased for use with Electret microphones and may be muted by IC1a. The 12V output is current limited by TR5 and TR6. The cradle and PTT lines are also used for external data connections to a PC or third party accessories.

Data interfaces are provided for external programming via TR1 and TR2. NMEA data is received from the Rx/Tx PCB via PLG2 and passed onto the microprocessor, IC4, via IC1c.

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Optional circuitry for ATIS detection consists of IC6, IC7, D1 and TR8. The inclusion of IC7 allows the ATIS signal to be muted during reception. The received audio is filtered by IC6c and IC6d which are followed by a zero crossing detector formed by IC6a, IC6b, D1 and TR8. This signal is sent to a second microprocessor, IC7, which measures the period of each half cycle of the incoming signal. By counting the number of periods which might be an ATIS signal the micro can decide whether ATIS is being received or not. When this decision is made, after about 10ms, IC7 sets an output to inform IC4 to mute the audio for 300ms. IC7 derives its clock and reset from the main microprocessor IC4.

The ATIS and DSC signals are generated and decoded by the modem, IC8 and surrounding components. TR9 switches the modulation index between that required for DSC and ATIS. The output signal is then passed onto the microphone audio via IC1b. Note that the microphone is muted by IC1a during transmission of the ATIS or DSC signals.

The audio level required for alarms is controlled by IC1d. For normal key 'beeps' the microprocessor, IC4, generates a square wave which is filtered and reduced in level by R15, R75, C14 and C105 and then fed into the audio amplifier via PLG1. For alarm generation IC1d short circuits R75 to increase the level of signal being fed to the audio amplifier.

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