Circuit Description - AXIS RT1200/1400

Introduction.

The AXIS RT1200 consists of two PCB assemblies. The main RF PCB assembly , Navico part No. E02957, contains all the transmitter and receiver circuitry, including the synthesiser, modulator and audio power amplifiers. The control PCB assembly, Navico part No. E02960, contains the microprocessor, user controls, the LCD display and external interfaces.

The AXIS RT1400 has an additional Channel 70 watchkeeping receiver, Navico part No. E03211, fitted to the main Rx/Tx assembly. There are no differences to the front panel assembly in this version.

E02957 Rx/Tx PCB Assembly.

The circuitry on this assembly is shown on drawing No. E02955.

Receiver. RF from the antenna socket passes through the low pass PA filter to a quarter wave match/switch L5, L6 and pin diode D1. In transmit D1 is on to protect the receiver. There then follows an optional attenuator and power splitter, not used on the RT1200. In this model C214 is a 1nF coupling capacitor. L7, L8 and the associated capacitors form a bandpass filter before the R.F. pre-amp, TR1. L9 and L11 form a further bandpass section before the mixer. The RF signal is fed to the source of TR2 and the local oscillator fed to Gate 1. Low side injection is used, i.e. the LO is 21.4 MHz below the receive frequency. L13 forms the drain load before matching through C25 and C26 to the 4 pole crystal filter, XTAL1 and XTAL2. The output of the filter is coupled by L14, C28 and C29 to the integrated IF amplifier/demodulator IC1. This uses a second local oscillator at 21.855MHz giving a second IF of 455kHz. XTAL4 is a 6 pole ceramic filter completing the necessary bandwidth definition. Quadrature coil L16 provides the demodulation.

Audio from pin 9 of IC1 is de-emphasised by R20 and C43, buffered by TR120 before distribution to the various audio stages on the control PCB. The audio from pin 9 is also passed through a very high gain amplifier, within IC1, configured as a band pass filter to detector D2 to provide a voltage proportional to the received signal strength. This level also goes to the control panel to provide squelch control. The AF signal is returned from the control panel after the volume and squelch controls to two audio power amplifiers in Bridge mode. The speaker output is switched at the external speaker socket to mute the internal speaker when an external speaker is connected.

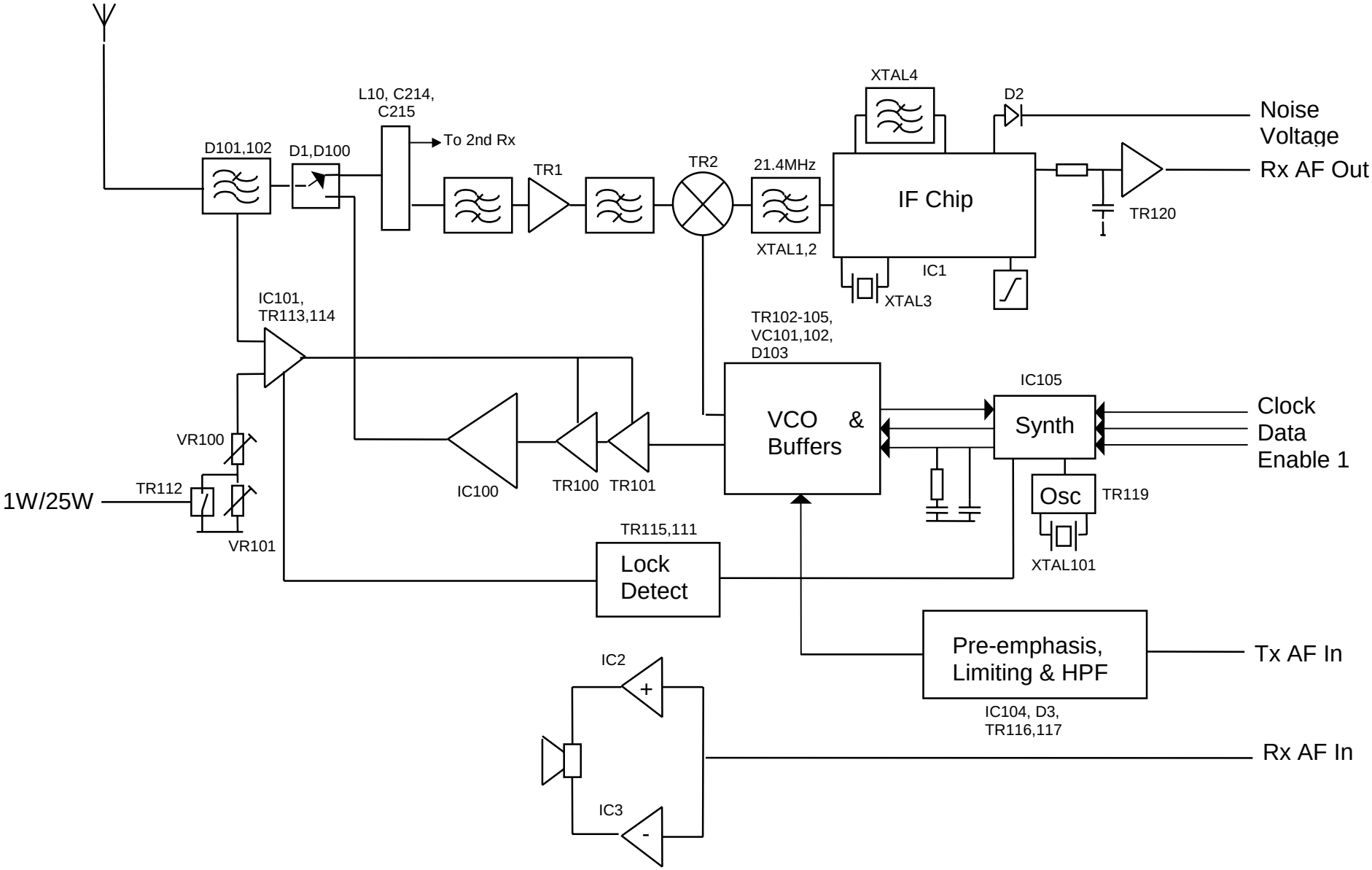
Transmitter. From the LO switch/buffer TR102, the transmit signal is amplified by controlled transistors TR101 and TR100, to drive the hybrid PA module IC100. This device is capable of generating the required 25Watts. The output is switched through PIN diode D100 before passing through the PA filter L1 to L4. L4 of this filter, with diodes D101 and D102 forms a simple forward and reverse power detector to provide power control and transmitter status indication on the front panel display. The power control signal is fed to differential amplifier IC101 along with the reference power signal from VR100 and VR101, used to set the hi and low powers. The output of this amplifier

forms a regulated supply with TR113 and TR114 to supply the PA drivers TR100 and TR101. Note that the reference input and supply for TR114 is fed from TR111 which is only turned on after the synthesiser is in lock.

Local Oscillator / Synthesiser. The main LO consists of TR105 connected as a Colpitts oscillator. Tuning is by L113 and varactor VC102. Band switching between Rx and Tx is by PIN diode D103. The output of this oscillator is buffered by a cascade pair formed by TR104 and TR103 in receive, and TR102 and TR104 in Transmit, the supply to TR102 and TR103 being switched between the two modes. The output is also buffered by TR118 to the input of the synthesiser, IC105. The reference frequency at 9.6MHz is generated by TR119 and controlled by XTAL101. C200, C115 and R157 form the main loop filter with additional suppression of the reference frequency given by R179 and C204. The synthesiser is controlled from the control panel via a 3 wire serial interface.

Modulator. Audio from the control panel is amplified by IC104b. The gain of this stage is configured by R169, R173 and C169 to give the signal pre-emphasis. The output of this stage is peak detected by D3 and detector TR116 to provide a gain control signal to TR117, to provide limiting of high level input signals. Temperature compensation of the limiter is provided by thermistor TH1. IC104a forms a high pass filter to meet the 14db/octave roll-off above 6kHz. The final output is fed to the modulation diode VC101 via gain control VR102, which is set to a maximum of 5kHz deviation.

Power Regulation and Switching. The 12Volt supply is switched on the front panel then feeds the audio amplifiers and regulators. The R.F. power module takes power before the switch to minimise voltage drops. Reverse polarity protection is provided by D104 and D105. A regulated 8V supply is provided by IC103 and 5V from IC107. The supply for receive and transmit circuits are switched by TR106 and TR110, controlled from the synthesiser via TR107 to TR109. IC105 controls the switching of PIN diode D103, ensuring that there a suitably high reverse bias across it in the OFF condition.



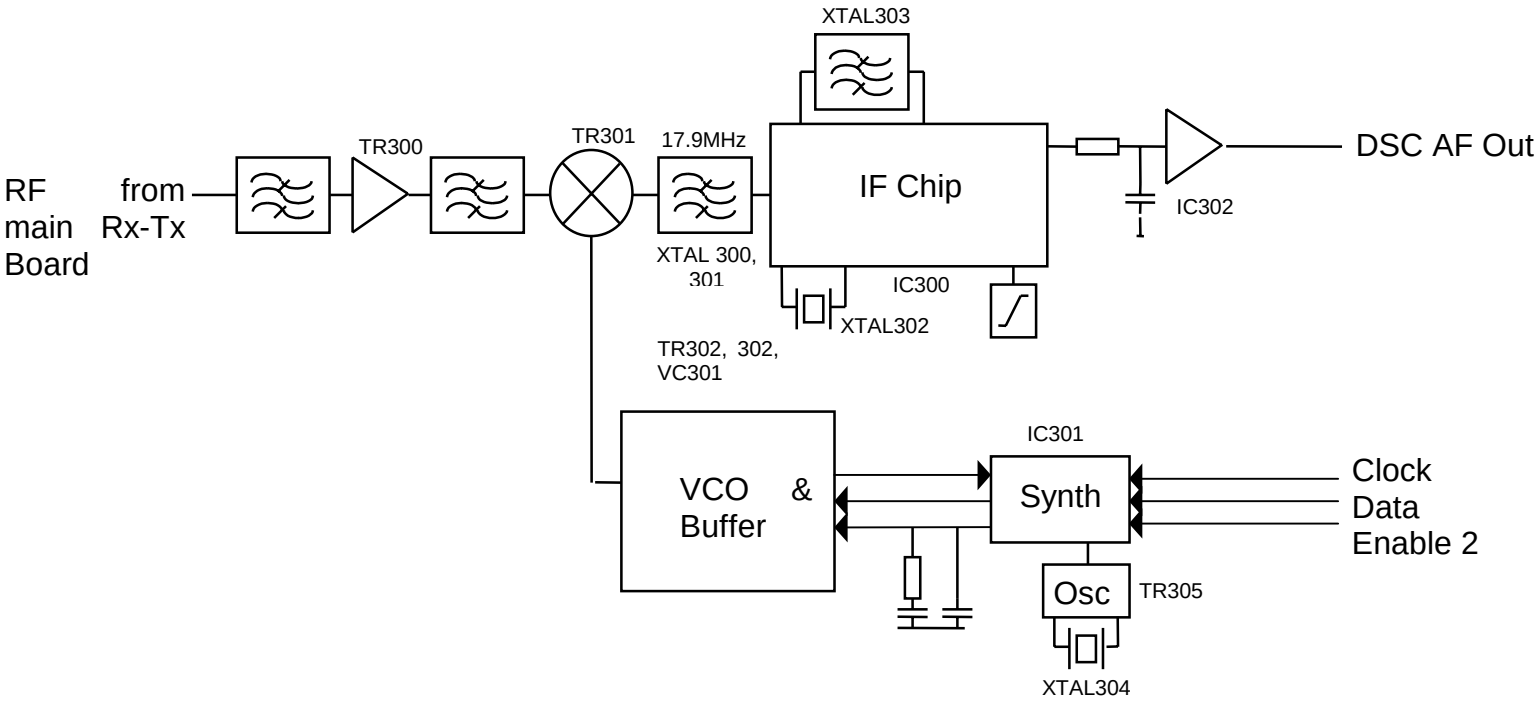
E02955 Rx - Tx Circuitry Block Diagram

E03211 Second Receiver PCB Assembly (AXIS RT1400 only)

The circuitry on this assembly is shown on drawing number E03209.

The second receiver is connected to the main receiver at the power splitter L10, C215, C214 and R205. The basic circuitry is exactly the same as the receiver section of the main receiver. L300 and L301 with associated capacitors form the input bandpass section, prior to the R.F. amplifier TR300. A second bandpass section is formed by L302 and L303, which couple into the mixer at the source of TR301. Low side injection from the local oscillator is fed into the gate. The output at 17.9MHz passes through the crystal filter XTAL 300 and XTAL 301 to the second IF stage, IC300. Demodulated audio is buffered by IC302a.

TR304 and XTAL304 form the reference oscillator for the synthesiser, IC301. Data from the front panel is fed from Clock, Data and Enable 2. C350, C355 and R345 form the basic loop filter to control the frequency of the local oscillator, TR303, by varactor VC301. The output of the local oscillator is buffered by TR302 before being coupled to the mixer through band bass filter L307 and L308.



E03209 Block Diagram

E02960 Control PCB Assembly.

The circuitry for this assembly is shown on drawing number E02958.

All the functions of the radio are controlled from this assembly by the microprocessor IC1. This microprocessor has it own clock controlled by XTAL1 at 4.096MHz. Reset generator IC5 ensures that the microprocessor starts up correctly, and resets under low voltage conditions. This microprocessor has an integral LCD interface driving the front panel display, LCD1. External controls consist of five push buttons, S1 to S5, rotary channel change switch CS1, and squelch control VR2. The level of illumination on the LCD and keypad is controlled by TR2 driving LED's LED1, LED5-9.

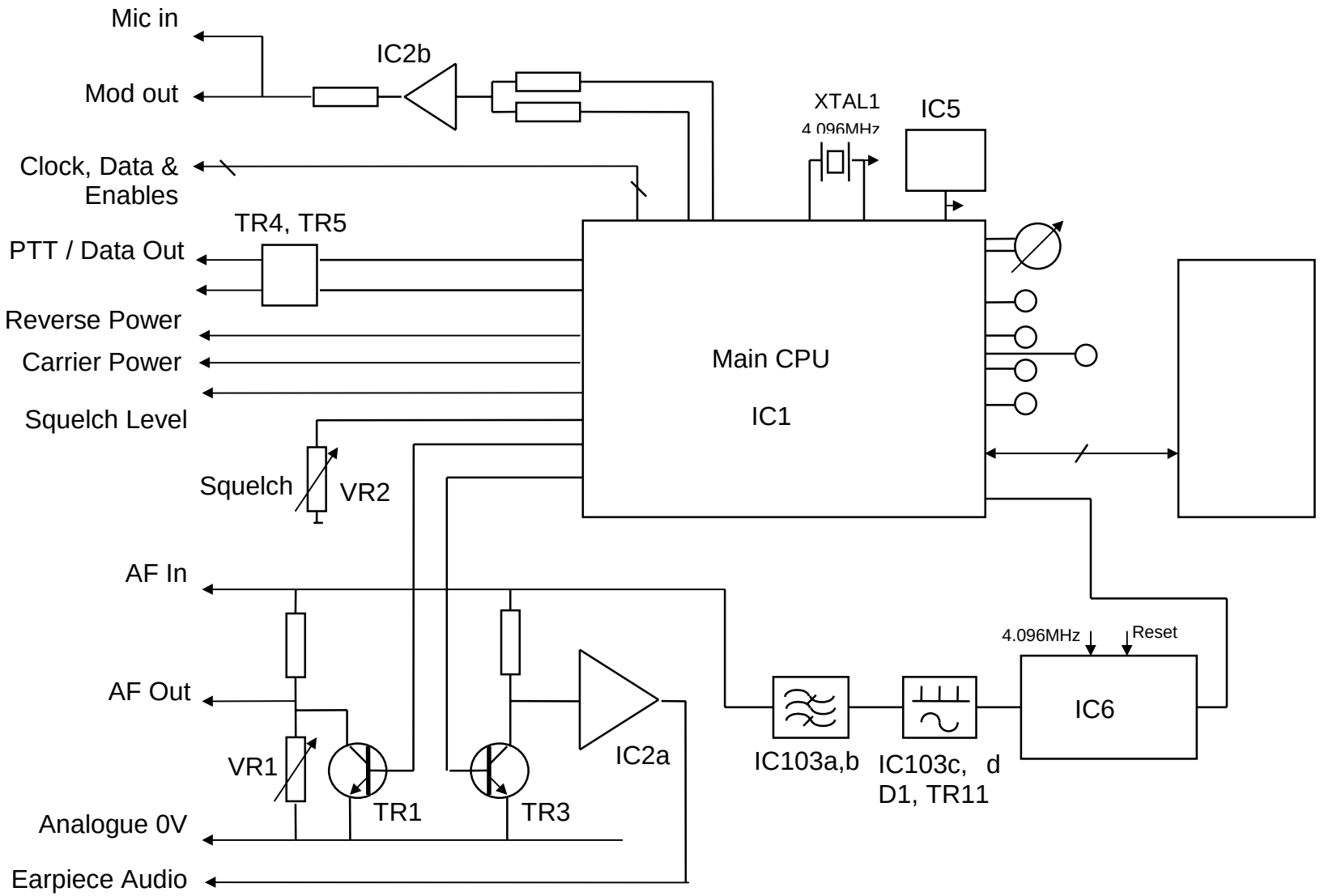
Configuration data and channel information is contained in the non volatile memory IC4. This interfaces to IC1 via a 4 wire serial interface shared with the synthesiser data to the Rx/Tx PCB assembly. Separate chip enables ensure that the data is routed correctly.

Volume control VR1 controls the level of audio in the loudspeaker. Amplifier IC2a boosts the level delivered to the handset earpiece. Individual mutes of the speaker and handset audio are provided by TR1and TR3 respectively, under control of the micro. This reads the voltages on the squelch control and noise input from the Rx/Tx PCB and mutes the audio as appropriate. Additionally the state of the handset on the cradle is detected from SKT1 to mute the speaker when the handset is off cradle (optional).

The handset interface is via connector SKT1. The microphone input is biased for use with Electret microphones and may be muted by TR6. The 12V output is current limited by TR7 and TR8. The cradle and PTT lines are additionally used for external data connections to a PC or third party accessories.
Additionally optional interfaces are provided for external programming and remote control (TR4 and TR5), ATIS generation (IC2b) and detection (IC3, IC6 and TR11) and alarm generation (TR9).

The ATIS signal is generated by the microprocessor, IC1, which produces a 2 bit (3 level) approximation of a sine wave at the correct frequency and baud rate. The two outputs are summed by R27, R43 and R30 before filtering by IC2b which forms a second order low pass filter. The output is then attenuated by R31 and R32 before summing into the microphone audio. Note that the microphone is muted by TR6 during transmission of the ATIS signal. The MMSI is held in the non volatile memory IC4 along with a control flag to enable ATIS generation.

The inclusion of IC6 allows the ATIS signal to be muted during reception. The received audio is filtered by IC3a and IC3b which are followed by a zero crossing detector formed by IC3c, IC3d, D1 and TR11. This signal is sent to a second microprocessor, IC6, which measures the period of each half cycle of the incoming signal. By counting the number of periods which might be an ATIS signal the micro can decide that ATIS is being received. When this decision is made, after about 10ms, IC6 sets an output to inform IC1 to mute the audio for 300ms. IC6 derives its clock from the main micro IC1 and the reset from IC5 via invertor TR10.



E02958 Circuit Block Diagram