COMPANY CONFIDENTIAL

Preliminary Datasheet

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Revision Note

BCM4356 Dual-Band 2x2 802.11ac and Bluetooth v4.1 Combo Module

Project Name	M.2 Type1216 BCM4356 WLAN + BT Combo Module
Foxconn Part No.	T77H566.01
Customer Model Name.	PK29S005P10

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1. Revision History

Date	Change Note	Author	REV Note
2014-07-25	Initial release(draft)	Robin Xu	0.1
2014-07-30	Add customer project code	Robin Xu	0.2
2014-08-21	1.Update the block diagram and support BTv4.1 in section2 2.Update the ME drawing in section3.1 3.Update the Recommended stencil aperture in setion3.4	Robin Xu	0.3
2014-11-14	Update WiFi Transmit Output Power	Ru-yan Li	0.4
2014-12-2	Add 3.7 RF port define	Ru-yan Li	0.5

2. Introduction

Project Name: M.2 Type 1216 BCM4356 WLAN+BT Combo Module
Project Number: T77H566.01

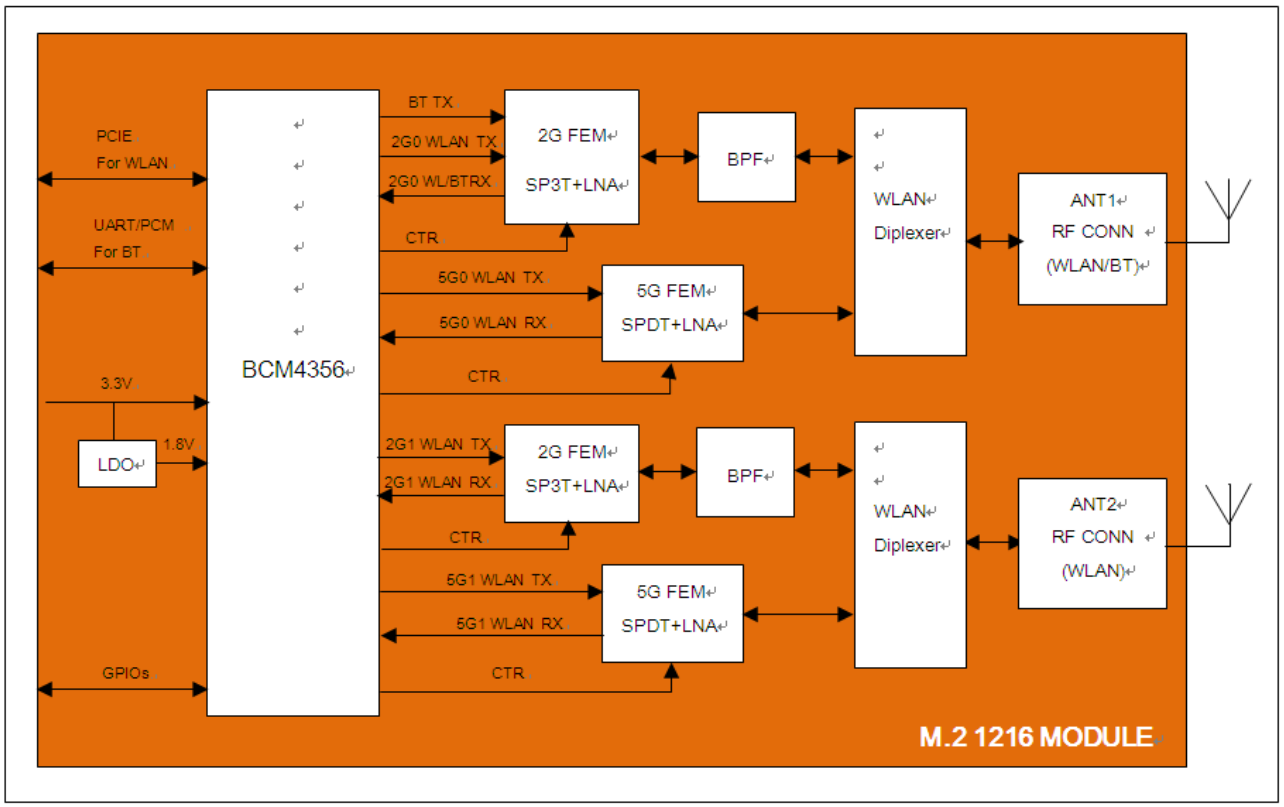
Form factor	M.2 Type 1216 LGA
Host Interface	WLAN: PCIe v2.0 BT: UART for data, PCM for audio
PCB	6-layer HDI design
RF connector	Two MHF-4 RF connectors on module

This documentation describes the engineering requirements specification of this M.2 1216 type module. WLAN is compliant with IEEE 802.11 a/b/g/n and 2x2 IEEE 802.11ac MAC/ baseband/radio, Bluetooth is compliant with Bluetooth v4.1+HS. This module takes advantage of the high throughput and extended range of Broadcom MIMO solution It is a confidential document of Foxconn.

* For b/g/n and a/b/g/n module, Foxconn HW/FW is the same, platform use different firmware and driver to enable or disable 5GHz 11ac function.

2.1 Hardware Architecture

The WLAN+BT combo module is designed base on BROADCOM BCM4356 chipset with external LNA for both 2.4G and 5GHz. The BCM4356 is a complete dual-band (2.4GHz and 5GHz) Wi-Fi 2X2 MIMO MAC/PHY/Radio System-on-a-Chip. This Wi-Fi single–chip device provides a high level of integration with dual-stream IEEE 802.11ac MAC/baseband/radio, Bluetooth v4.1 + HS. In IEEE802.11ac mode, the WLAN operation supports rates of MCS0-MCS9 (up to 256QAM) in 20MHz, 40MHz and 80MHz channels for data rates up to 866.7Mbps. In addition, all the rates specified in IEEE802.11a/b/g/n are supported. See the block diagram as below:



2.2 Features

This module supports the following features:

- IEEE 802.11a/b/g/n/ac dual-band 2x2 MIMO radio with virtual-simultaneous dual-band operation
- Bluetooth v4.1+EDR with integrated class1 PA
- Enhanced Bluetooth and WLAN coexistence performance
- WLAN PCIe module complies with PCI express base specification revision2.0 for x1 lane and power management base specification.
- Integrated ARMCR4™ processor with tightly coupled memory for complete WLAN subsystem functionality minimizing the need to wake up the applications processor for standard WLAN functions. This allows for further minimization of power consumption, while maintaining the ability to field upgrade with features,
- On-chip memory includes 768KB SRAM and 640KB ROM.
- OneDriver™ software architecture for easy migration from existing embedded WLAN and Bluetooth devices as well as future devices.
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
- Supports IEEE802.11ac/n beam forming.
- Bluetooth supports a high–speed UART interface(up to 4Mbps) and PCM for audio
- Bluetooth Smart Audio technology improves voice and music quality to headsets
- Bluetooth low power inquiry and page scan
- Bluetooth low energy(BLE) support
- Bluetooth Packet Loss Concealment(PLC)
- Bluetooth Wide Band Speech(WBS)
- GP/HF compliance

2.3 Standards Compliance

- Bluetooth 2.1+EDR
- Bluetooth 3.0+HS
- Bluetooth 4.1(Bluetooth Low Energy)
- IEEE802.11ac mandatory and optional requirements for 20MHz,40MHz and 80MHz channels
- IEEE802.11n
- IEEE802.11a
- IEEE802.11b
- IEEE802.11g
- IEEE802.11d
- IEEE802.11h
- IEEE802.11i
- Security
  - WEP
  - WPA/WPA2
  - WMM/WMM-PS(U-APSD)/WMM-SA
  - AES(Hardware Accelerator)
  - TKIP(Hardware Accelerator)
  - CKIP(SW support)
- Proprietary Protocols
  - CCXv2
  - CCXv3
  - CCXv4
  - CCXv5
- IEEE802.15.2 coexistence compliance-on silicon solution compliant with IEEE 3wire requirements

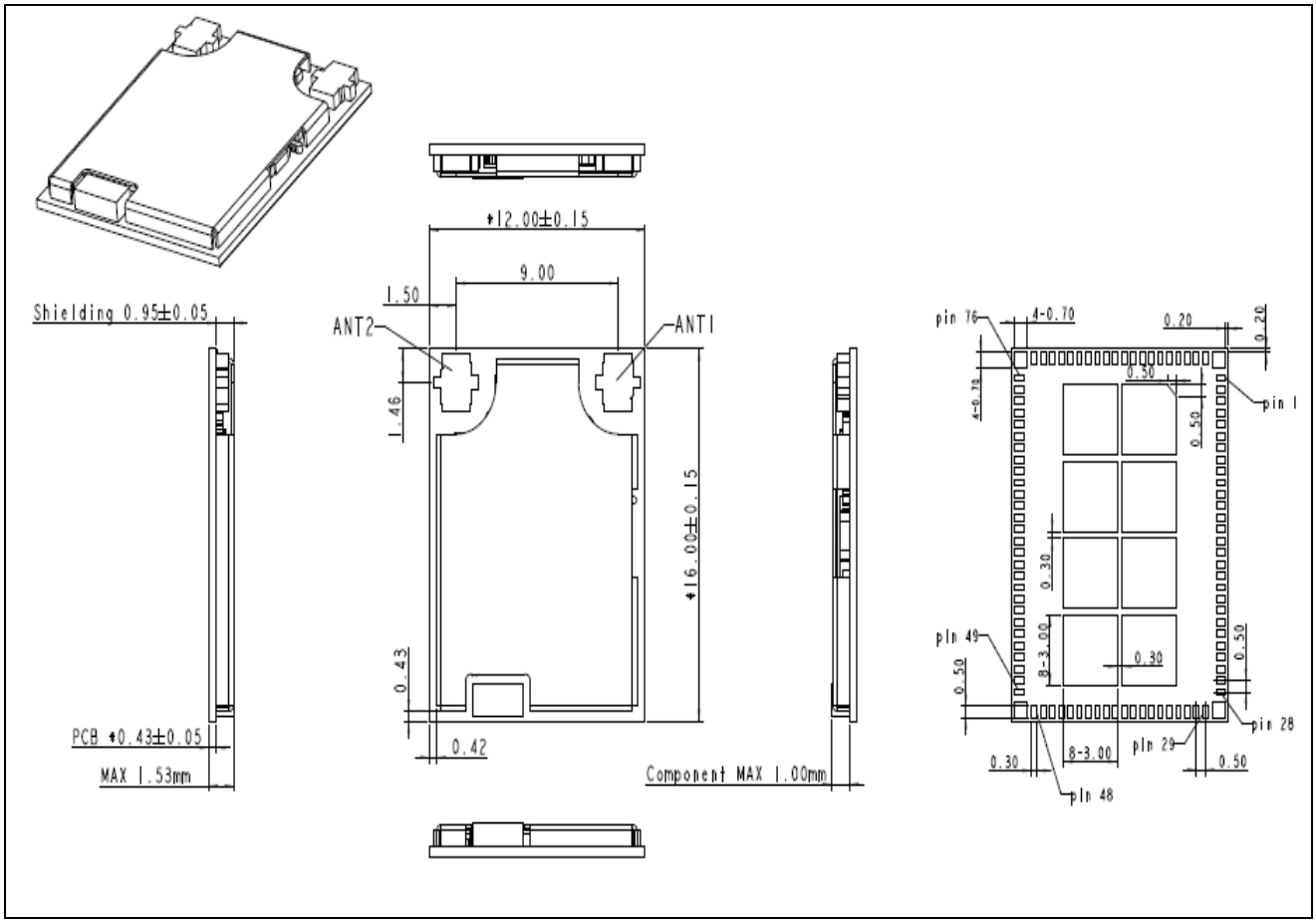
The module will the following future draft/standards:

- IEEE802.11r-Fast Roaming (between APs)
- IEEE802.11w-Secure Management Frames
- IEEE802.11 Extensions:
  - IEEE802.11e QoS Enhancements(In accordance with the WMM spec, QoS is already supported)
  - IEEE802.11h 5GHz Extensions
  - IEEE802.11i MAC Enhancements
  - IEEE802.11k Radio Resource Measurement

3. Mechanical Specification

3.1 Mechanical Drawing

Typical module dimension (W x L): 12mmx16mm. Max Z-height is 1.53mm.



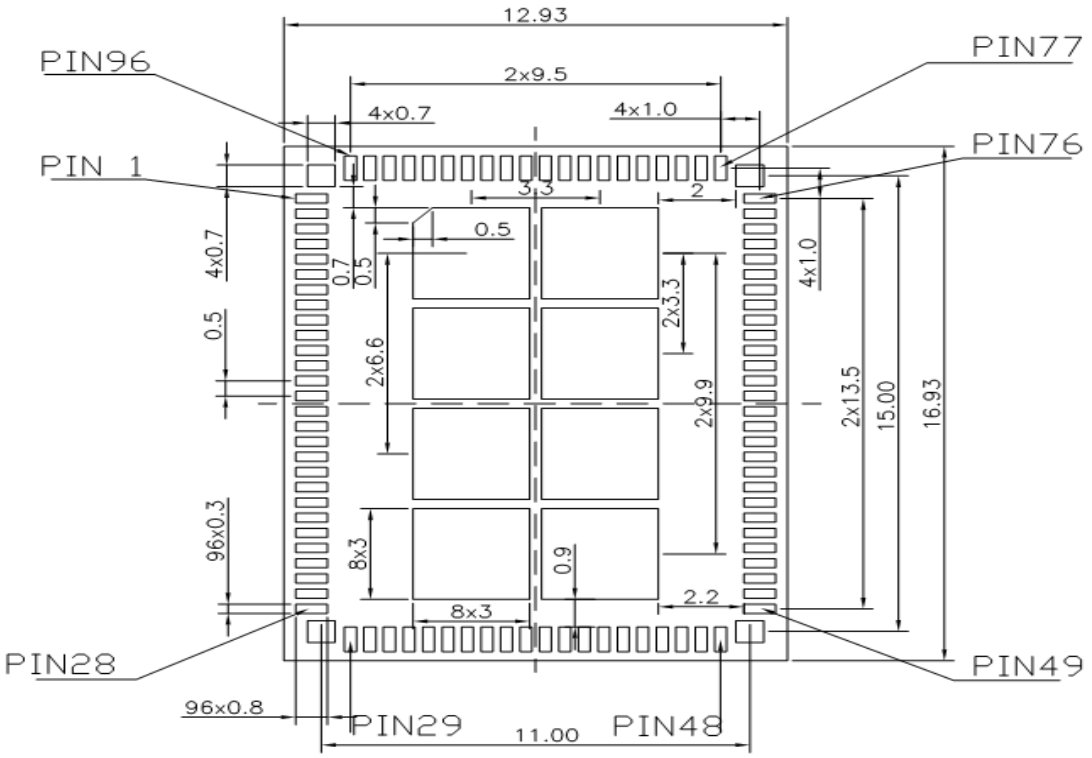
Unit:mm

3.2 PCB stack

6 Layers, HDI, thickness:0.43mm +/-0.05mm

Layer Name	Layer Type	Materials (um)	Finished (um)	Tolerance (um)
S/M	SolderMask		Min.10um	
FRONT	Copper(Base+Plating)	12	20	+10/-10
	Prepreg/1-0106 (0068)	68	58	+15/-15
L2	Copper(Base+Plating)	12	20	+10/-10
	Prepreg/1-0106 (0068)	68	58	+15/-15
L3	Copper(Base+Plating)	12	20	+10/-10
	Core	61	60	+13/-13
L4	Copper(Base+Plating)	12	20	+10/-10
	Prepreg/1-0106 (0068)	68	58	+15/-15
L5	Copper(Base+Plating)	12	20	+10/-10
	Prepreg/1-0106 (0068)	68	58	+15/-15
BACK	Copper(Base+Plating)	12	20	+10/-10
S/M	SolderMask		Min.10um	
	Finished Board Thickness		430	

3.3 Recommended LGA Land Pattern

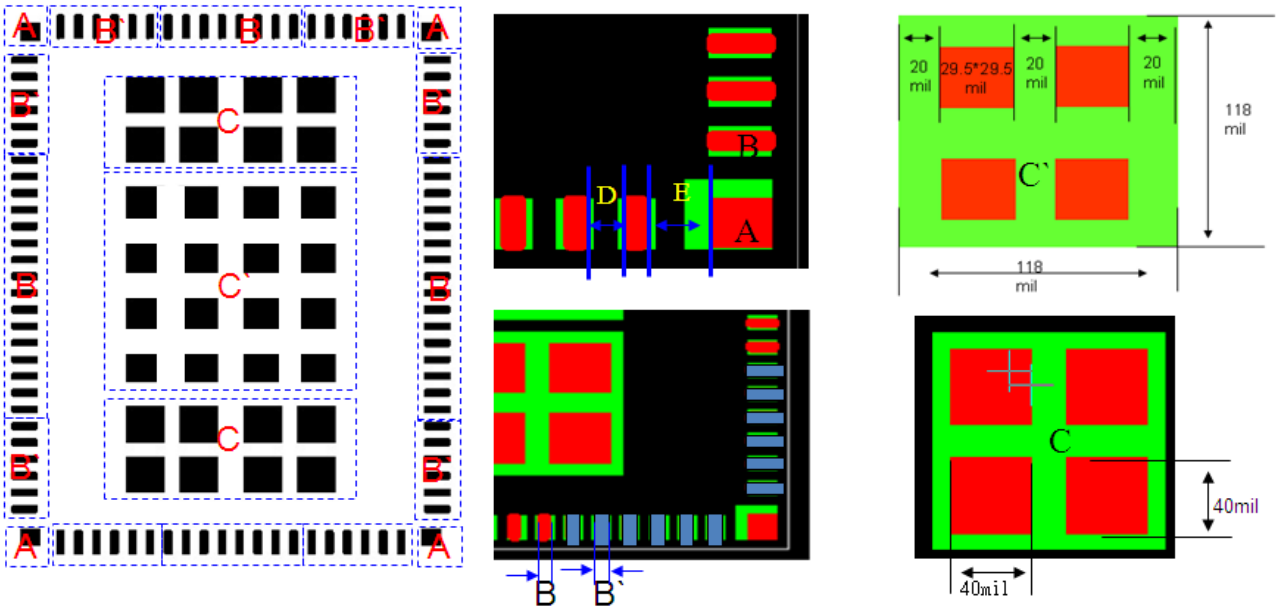


Unit: mm

TOP VIEW

Suggest use “solder-mask on pad” design for main-board to avoid the soldering short.

3.4 Recommended stencil aperture



Remark: Red→ stencil layer Green→ (pad layer)

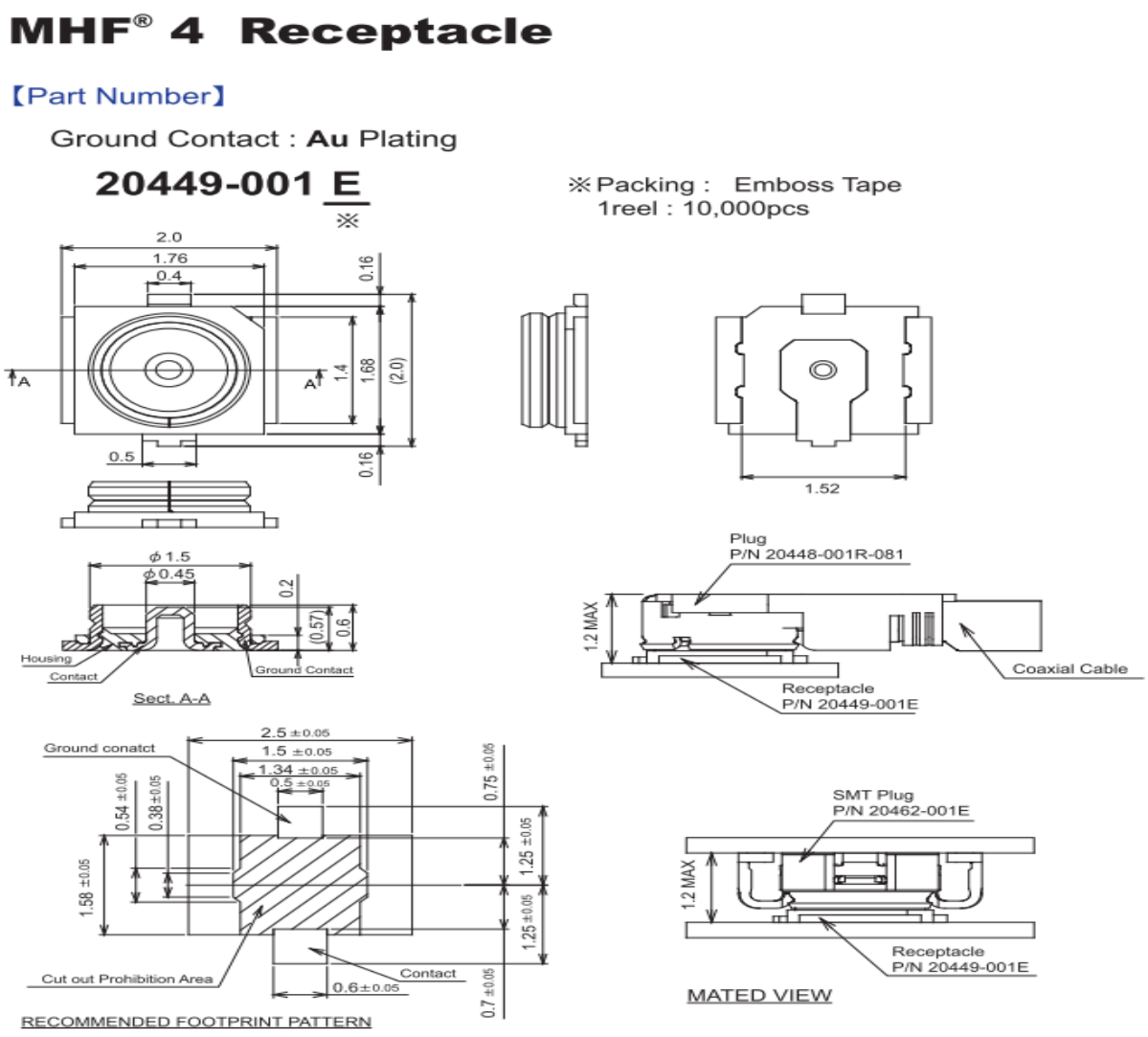
Below is recommendation about respectively defined apertures as A,B,B`,C and C`

- Stencil thickness=0.12mm
  A=24*24 mil^2 B=22*9 mil^2 B`=24*9 mil$^2$ C=40*40 mil$^2$ C`=29.5*29.5mil^2
- Define space between apertures as D and E
  D=11mil E=19.5mil

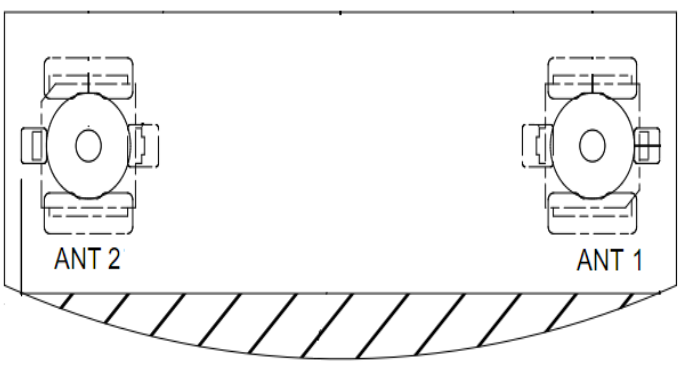
3.5 RF Connector Type

- The standard 2x2mm size RF receptacle connectors to be used in conjunction with the M.2 boards/modules
- Same RF Receptacle on module supports either 0.81mm or 1.13mm diameter cable Prefer to use 1.13mm diameter cable for lower cable loss
- 1.2mm max. mated height for low profile design

Example of IPEX RF connector
IPEX P/N: 20449-001E (MHF-4)



- **Antenna Placement**

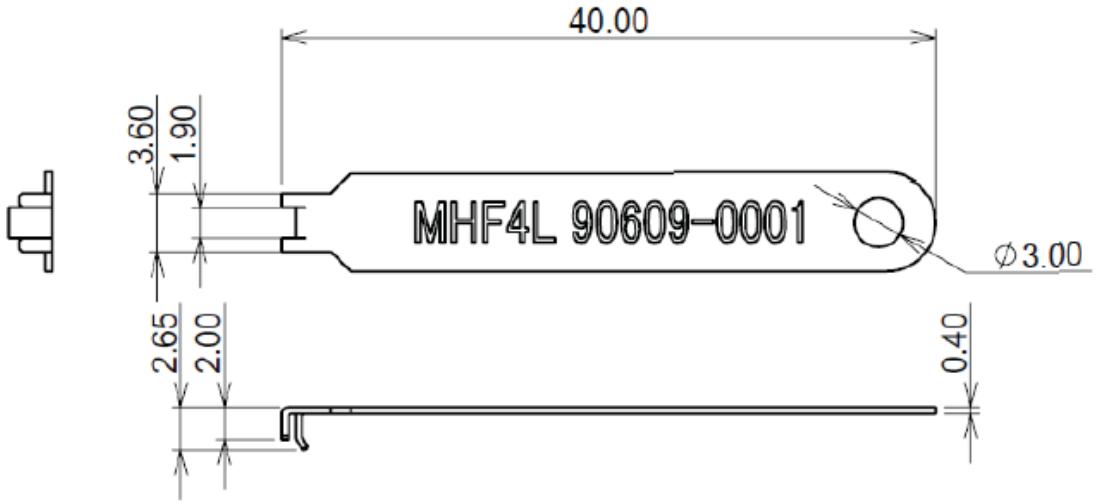


Antenna	Interface	Remark
ANT1	WLAN/BT	Main
ANT2	WLAN	AUX

3.6 RF cable assembly notice

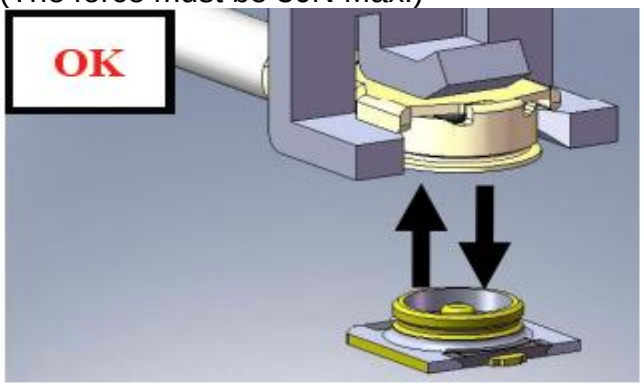
1> Mating/Unmating Jig

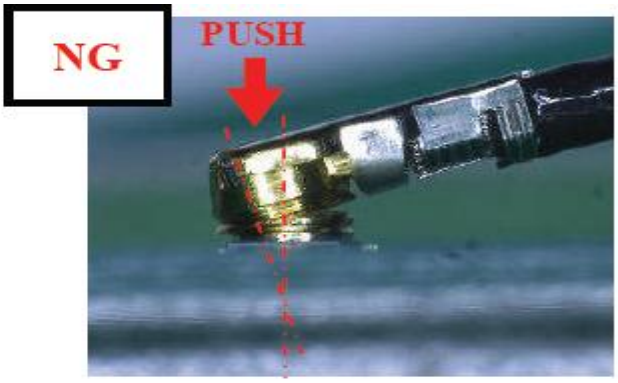
We recommend to use below Jig for mating/Unmating RF cable



2> Mating method of RF cable

Please push as gently as possible while mating plug with receptacle.
(The force must be 30N Max.)





3.7 RF port define

Main ANT for WiFi and BT, Aux ANT for WiFi.

4. LGA Pin-out Definition

4.1 Module pin-out definition

Top view

4.2 Pin definition

Pin No.	Pin Name	Type	Description	Voltage	Connecting
1-3, 7-16, 18,19,21, 22,25, 43-44,66, 67	NC	-	No connection	-	No
4,5,72,73	3.3V	Power	DC 3.3V power input	3.3V	Yes
24	BT_DEV_WAKE	I	Bluetooth device wake-up: Signal from the host to the BCM4356 indicating that the host requires attention. • Asserted: The Bluetooth device must wake-up or remain awake. • Deasserted: The Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.	1.8V	Yes
27	SUSCLK (32KHz)	I	Suspend Clock is a 32.768 kHz clock supply input that is provided by platform to enable the add-in card to enter reduce power consumption modes. SUSCLK will have a duty cycle that can be as low as 30% or as high as 70%. Accuracy will be up to 200ppm. See the detail spec in section6.	1.8V (Note1)	Yes
28	WLAN_RFDISABLE_L	I	Active low, debounced signal when applied by the system it will disable WLAN radio operation on the add-in cards that implement radio frequency applications. This signal is internal pull-up on the card by default.	1.8V (Note2)	No
29	PCIE_PME_L	OD	PCIe PME Wake. Open Drain with pull up on platform; Active Low	1.8V	Yes
30	PCIE_CLKREQ_L	OD	Clock Request is a reference clock request signal as defined by the PCIe Mini Card CEM specification; Also used by L1 PM Substates.	1.8V	Yes
31	PCIE_PERST_L	I	PE-Reset is a functional reset to the Add-In card as defined by the PCIe Mini Card CEM specification	1.8V	Yes
33	PCIE_REFCLKN	I	PCIe Reference Clock signals (100 MHz) defined by the PCIe2.0 specification.	-	Yes
34	PCIE_REFCLKP				
36	PCIE_TDN	O	PCIe TX differential signals defined by the PCIe2.0 specification	-	Yes
37	PCIE_TDP				
39	PCIE_RDN	I	PCIe RX differential signals defined by the PCIe2.0 specification. Add AC cap 0.1uF on PCIe signals of host side.	-	Yes
40	PCIE_RDP				
42	VIO	Power	Reserved for external 1.8V power source input. If don't need, MUST keep it floating or open	1.8V (Note3)	Option
45	WL_REG_ON	I	SDIO sideband GPIO pin to enable/disable (reset) the WiFi function. Platform firmware is required to assert/de-assert this pin on every boot (warm and cold). High active. See the detail sequence timing in section5.3.	1.8V	Yes
46	SDIO_WAKE_L	O	SDIO Host Wake. Note in band SDIO wake is not used for non-active modes, Active Low. Require pull up on the host side (recommended 15K to 100K)	1.8V	No

47	SDIO_DATA3	I/O	SDIO data line 3	1.8V	No
48	SDIO_DATA2	I/O	SDIO data line 2	1.8V	No
49	SDIO_DATA1	I/O	SDIO data line 1	1.8V	No
50	SDIO_DATA0	I/O	SDIO data line 0	1.8V	No
51	SDIO_CMD	I/O	SDIO Command line	1.8V	No
52	SDIO_CLK	I	SDIO clock input	1.8V	No
53	BT_UART_HOST_WAKE_L	O	UART sideband used to wake up host platform via BT device. Open Drain, Active Low. Require pull up on the host side (recommended 15K to 100K)	1.8V	Yes
54	BT_UART_CTS_L	I	UART Clear To Send connected to RTS on the platform.	1.8V	Yes
55	BT_UART_TXD	O	UART Transmit Data connected to RXD on the platform.	1.8V	Yes
56	BT_UART_RXD	I	UART Receive Data connected to TXD on the platform.	1.8V	Yes
57	BT_UART_RTS_L	O	UART Ready To Send connected to CTS on the platform.	1.8V	Yes
58	BT_PCM_SYNC	I/O	PCM synchronous data SYNC/ I2S Word Select.	1.8V	Yes
59	BT_PCM_IN	I	PCM synchronous data input/ I2S Serial Data IN.	1.8V	Yes
60	BT_PCM_OUT	O	PCM synchronous data output/ I2S Serial Data OUT	1.8V	Yes
61	BT_PCM_CLK	I/O	PCM Clock/ I2S Continuous Serial Clock (SCK)	1.8V	Yes
63	BT_REG_ON	I	Active high. Use GPIO pin to enable/disable the BT function.	1.8V	Yes
64	BT_LED_L	O	BT LED, open drain, active low signal. This signal is used to allow the add-in card to provide status indicators via LED devices that will be provided by the system.	1.8V	Option
65	WL_LED_L	O	WLAN LED, open drain, active low signal. This signal is used to allow the add-in card to provide status indicators via LED devices that will be provided by the system.	1.8V	Option
69	BT_USB_DN	I/O	USB Data ± Differential serial data interface compliant to the USB 2.0 Specification	-	No
70	BT_USB _DP				
6,17,20, 23,26,32, 35,38,41, 62,68,71, 74-108	GND	GND	Ground	0V	Yes

Note1: for pin27 SUSCLK(32KHz) signal, BCM4356 chipset is capable to tolerate 3.3V, but 1.8V input source is recommended.

Note2: for pin28 WLAN_RFDISABLE signal, it is provided for legacy wireless communications add-in cards.
It allows users to disable the add-in card's RF radio operation via a system-provided switch in order to meet public safety regulations or when otherwise desired. The wireless disable signals are active low signals that when asserted (driven low) by the system shall disable radio operation. All transients resulting from mechanical switches need to be de-bounced by system circuitry. It is anticipated that in the future the requirement for hardware wireless disable signals will be deprecated from use in favor of in-band mechanisms. If use SDIO interface, prefer to use pin45 to do software control to implement enable/disable the WiFi function. Default is 1.8V, and is capable to tolerate 3.3V.

Note3: for pin42 VIO, by default, MUST keep this pin floating or open.
If host platform can provide the external 1.8V power source as module IO voltage input, thus, the LDO inside module can be removed. It's just for customized design only

5. Product Specification

5.1 DC Electrical Specification

Absolute Maximum Ratings

These specifications indicate levels where permanent damage to the device can occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended can adversely affect long-term reliability of the device.

Rating	Symbol	Value	Unit
DC supply voltage for the device	3.3V	-0.5 to 3.9	V

Recommended Operating Condition

Element	Symbol	Value			Unit
		Minimum	Typical	Maximum	
DC supply voltage for the device	3.3V	3.15	3.3	3.45	V

Function operation is not guaranteed outside this limit, and operation outside this limit for extended periods can adversely affect long-term reliability of the device.

5.2 RF Characteristics(TBD)

All typical performance specification are measured at RF connector port based-on the room temperature(+25℃) and nominal supply voltages
The performance will be updated later based-on overall EDVT and regulatory testing..

WLAN	Standard	IEEE802.11a/b/g/n/ac
	Data Rate	**2.4GHz** 802.11b: 11, 5.5, 2, 1 Mbps; 802.11g: 54, 48, 36, 24, 18, 12, 9, 6 Mbps 802.11n: HT20 mode: up to 144.4Mbps **5GHz** 802.11a: 54, 48, 36, 24, 18, 12, 9, 6 Mbps 802.11n: HT20 mode: MCS0~7,up to 144.4Mbps HT40 mode: MCS0~7,up to 300Mbps 802.11ac VHT20: MCS0~8, up to 173.3Mbps 802.11ac VHT40: MCS0~9, up to 400Mbps 802.11ac VHT80: MCS0~9, up to 866.7Mbps
	Modulation Techniques	802.11b: CCK, DQPSK, DBPSK 802.11a/g: 64QAM,16QAM, QPSK, BPSK 802.11n: 64QAM,16QAM, QPSK, BPSK 802.11ac: 256QAM,64QAM,16QAM, QPSK, BPSK
	Frequency Range	2.4GHz~2.4835GHz 5.15GHz~5.845GHz
	Media Access Control	CSMA/CA with ACK

	Transmit Output Power Per Each Chain	**2.4GHz:** 11b 1~11Mbps: 16+/-1.5dBm 11g 6~54Mbps: 15+/-1.5dBm 11n HT20 MCS0~ MCS7: 14+/-1.5dBm **5GHz:** 11a 6~12Mbps: 15+/-1.5dBm 11a 18~54Mbps: 14+/-1.5dBm 11n/ac 20MHz MCS0~ MCS2: 15+/-1.5dBm 11n/ac 20MHz MCS3~ MCS7: 14+/-1.5dBm 11n/ac 40MHz MCS0~ MCS2: 15+/-1.5dBm 11n/ac 40MHz MCS3~ MCS6: 14+/-1.5dBm 11n/ac HT40 MCS7: 13+/-1.5dBm 11ac VHT20 MCS8: 11+/-1.5dBm 11ac VHT40 MCS8~ MCS9: 11+/-1.5dBm 11ac VHT80 MCS0~ MCS2: 14.5+/-1.5dBm 11ac VHT80 MCS3~ MCS6: 14+/-1.5dBm 11ac VHT80 MCS7: 12+/-1.5dBm 11ac VHT80 MCS8~MCS9: 10+/-1.5dBm
	Typical Minimum Receiver Sensitivity Per Each Chain	**2.4GHz**: 11b 1Mbps: -94dBm@PER<=8% 11b 11Mbps: -86dBm@PER<=8% 11g 6Mbps: -90dBm@PER<=10% 11g 54Mbps: -72dBm@PER<=10% 11n HT20 MCS0: -89dBm@PER<=10% 11n HT20 MCS7: -68dBm@PER<=10% **5GHz:** 11a 6Mbps: -90dBm@PER<=10% 11a 54Mbps: -72dBm@PER<=10% 11n HT20 MCS0: -90dBm@PER<=10% 11n HT20 MCS7: -69dBm@PER<=10% 11n HT40 MCS0: -86dBm@PER<=10% 11n HT40 MCS7: -67dBm@PER<=10% 11ac VHT20 MCS0,Nss1: -89dBm@PER<=10% 11ac VHT20 MCS8,Nss1: -66dBm@PER<=10% 11ac VHT40 MCS0,Nss1: -86dBm@PER<=10% 11ac VHT40 MCS9,Nss1: -62.5dBm@PER<=10% 11ac VHT80 MCS0,Nss1: -82dBm@PER<=10% 11ac VHT80 MCS9,Nss1: -58dBm@PER<=10%
BT	Radio Modulation Technology	FHSS
	Operating Frequency	2.402GHz ~ 2.4835GHz
	Channel Numbers	79 channels with 1MHz BW
	BDR Transmitter Output Power	Typical +9dBm for Class1 (TBD)
	BDR Power Control	2dB≤Power Control Step≤8dB
	BDR Initial Carrier Freq. Tolerance	≤ ± 75 kHz
	BDR Carrier Frequency Drift	Drift Rate/50us <±20kHz DH1: +/- 25kHz DH3: +/- 40kHz DH5: +/- 40kHz
	BDR Modulation Characteristics	140kHz ≤ Δf1avg ≤175kHz Δf2max ≥115kHz Δf2avg/Δf1avg ≥0.8
	BDR Maximum Receiver Signal	-20dBm@BER < 0.1% at 1Mbps
	BDR Multi-slot Sensitivity	-80dBm@BER < 0.1% at 1Mbps
	BDR Single Sensitivity	-80dBm@BER <= 0.1% at 1Mbps

	EDR Relative Power	P[GFSK]-4dB<P[DPSK]< P[GFSK]+1dB
	EDR Stability and Mod Accuracy	-75 kHz <ωi < 75 kHz -10kHz<ω0 <10kHz RMS DEVM<=0.13 for all 8DPSK @3Mbps Peak DEVM<=0.25 for all 8DPSK @3Mbps 99% DEVM<=0.2 for 99% 8DPSK @3Mbps
	BDR Frequency Range	FL>2.4GHz,FH<2.4835GHz
	EDR Sensitivity	-80dBm@BER <= 0.01% at 2Mbps -80dBm@BER <= 0.01% at 3Mbps
	BDR TX Output Spectrum -20dB Bandwidth	≤1MHz
	LE Output Power	<10dBm
	LE Modulation Characteristics	225kHz ≤ Δf1avg ≤275kHz; Δf2max ≥185kHz for at least 99.9% test packets; Δf2avg/Δf1avg ≥0.8
	LE Carrier frequency offset and drift	Carrier frequency offset: ±150kHz Carrier Drift: ≤50kHz Drift rate: ≤20kHz/50us
	LE Receiver Sensitivity	-70dBm@PER <= 30.8%

5.3 Power Up Sequence and Timing

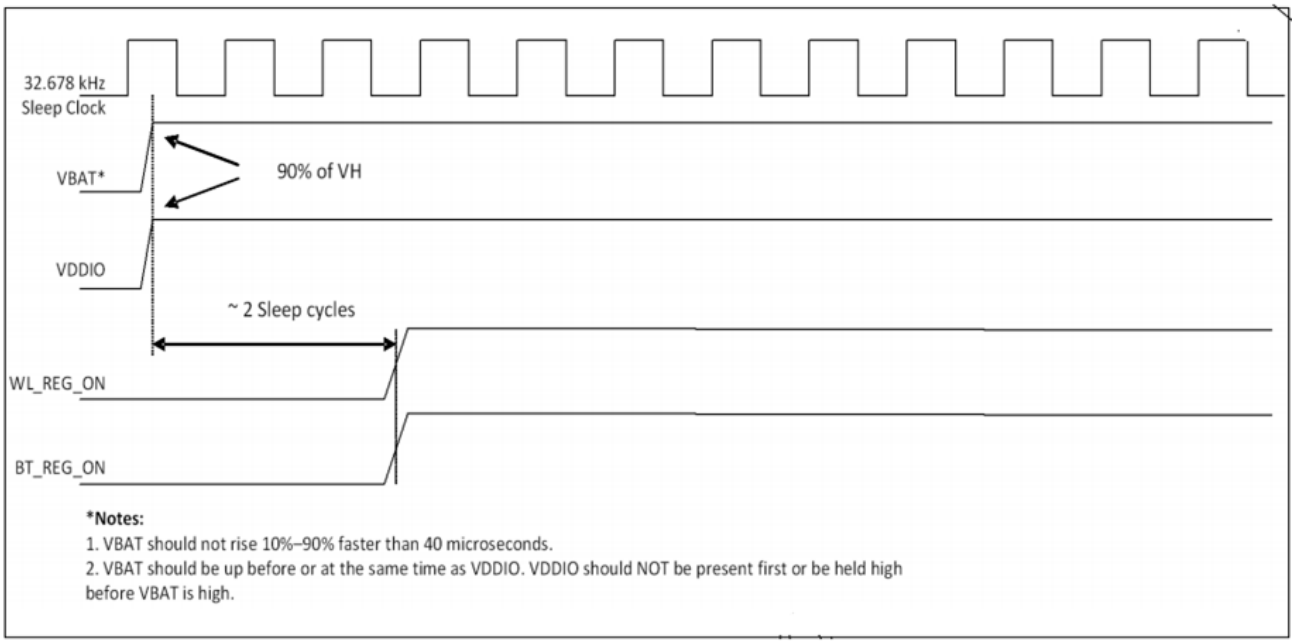
The BCM4356 has two signals WL_REG_ON [pin45] & BT_REG_ON [pin63] that allows the host to control the power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. Below timing diagram are provided to indicate proper sequencing of the signals for various operational states.

- **WL_REG_ON [pin45]**
  Used by the PMU to power up the WLAN section. It's also OR-gated with BT_REG_ON input to control the internal BCM4356 regulators. When this pin is high, the regulatory are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If both the BT_REG_ON and WLAN_REG_ON pins are low, the regulators are disable.

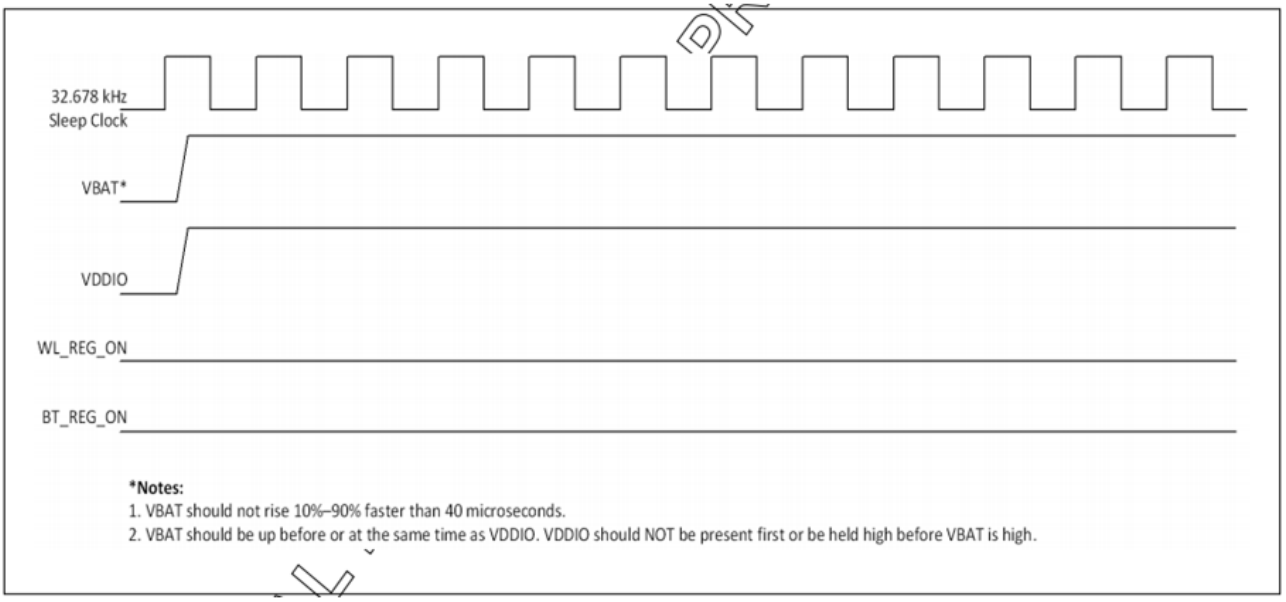
- **BT_REG_ON [pin63]**
  Used by the PMU(OR-gated with WL_REG_ON) to power up the internal BCM4356 regulators. If both the BT_REG_ON and WLAN_REG_ON pins are low, the regulators are disable. When this pin is high, the regulatory are enabled and the BT section is out of reset. When this pin is low, the BT section is in reset.

Remark: VBAT means DC input 3.3V in below timing diagram.

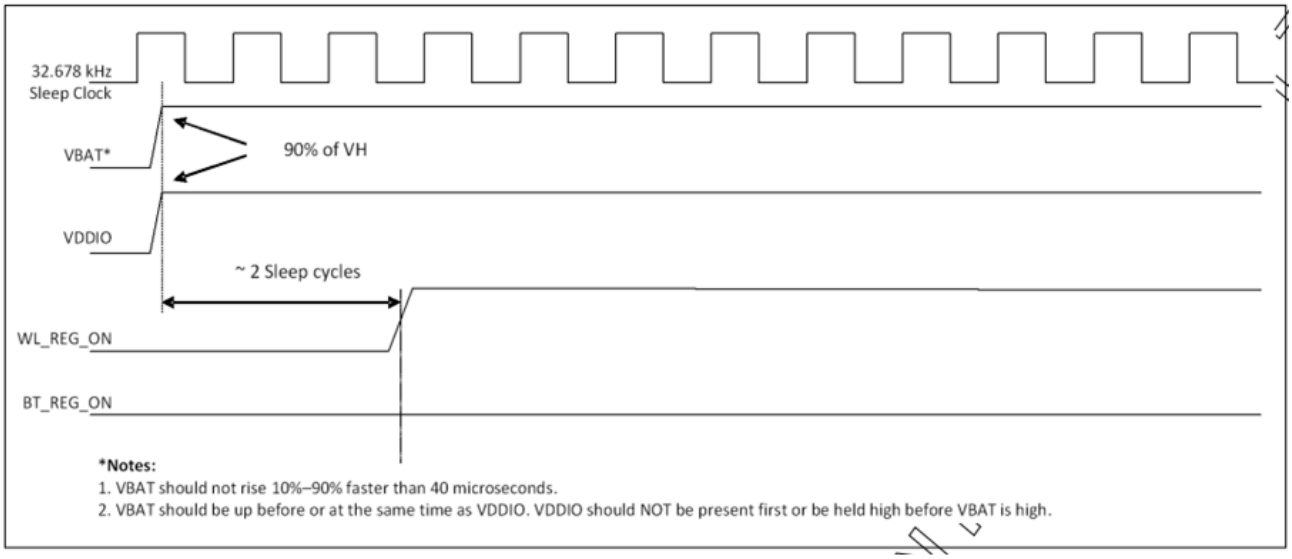
5.3.1 Control signal Timing (WLAN=ON, BT=ON)



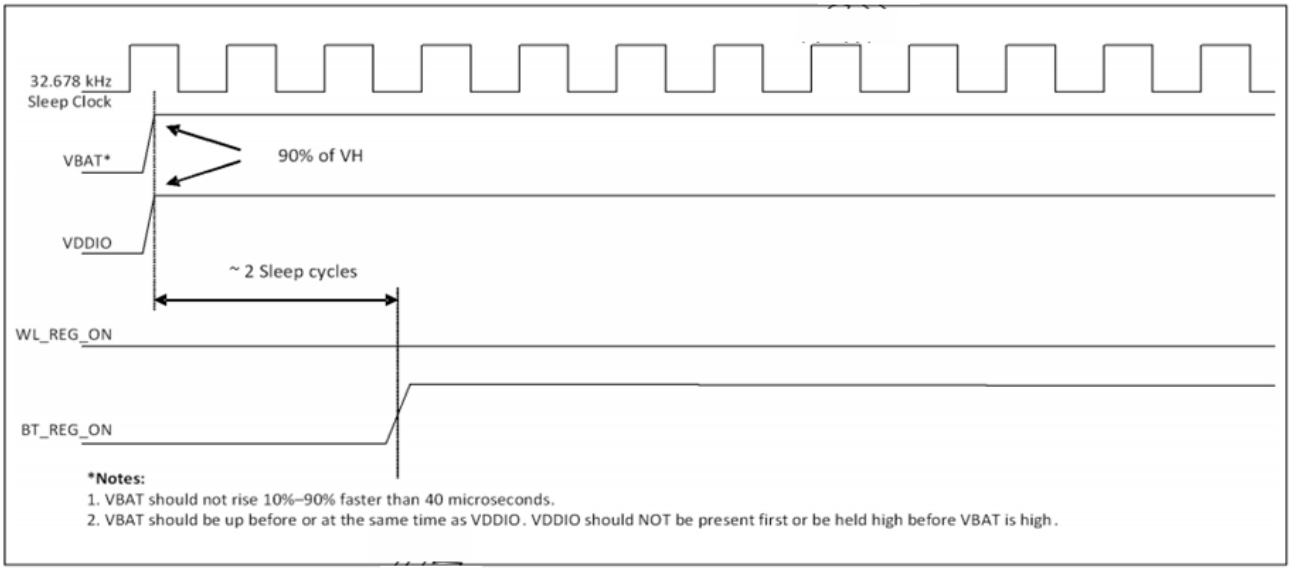
5.3.2 Control signal Timing (WLAN=OFF, BT=OFF)



5.3.3 Control signal Timing (WLAN=ON, BT=OFF)

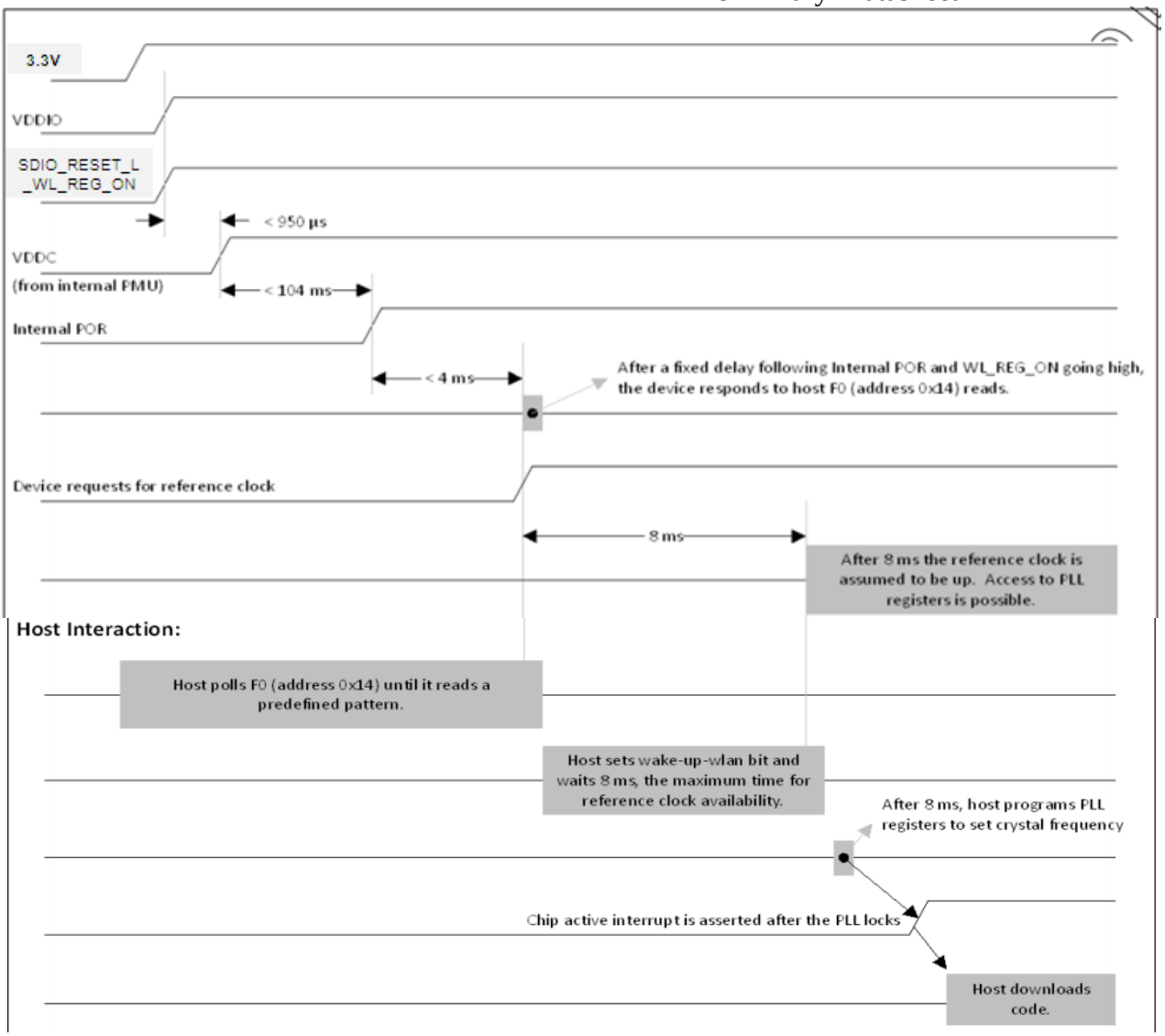


5.3.3 Control signal Timing (WLAN=OFF, BT=ON)



5.3.4 WLAN Boot Up Sequence

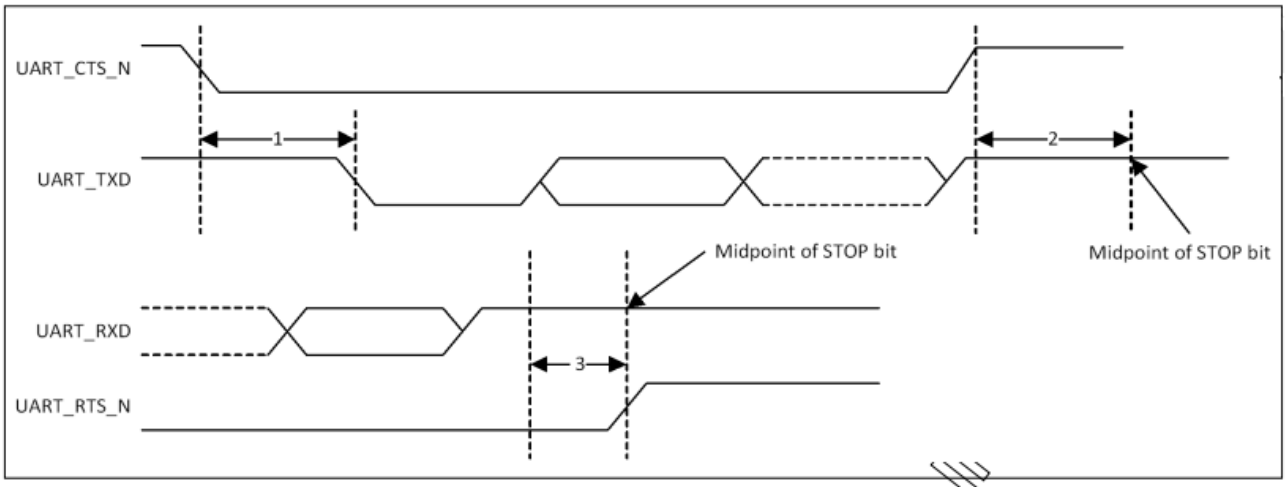
Below figure shows that the WLAN boot-up sequence from power-up to firmware download.



5.4 UART Host Interface Timing

The UART is a standard 4-wire interface(RX,TX,RTS and CTS) with adjustable baud rates from 9600bps to 4.0Mbps.

UART Timing



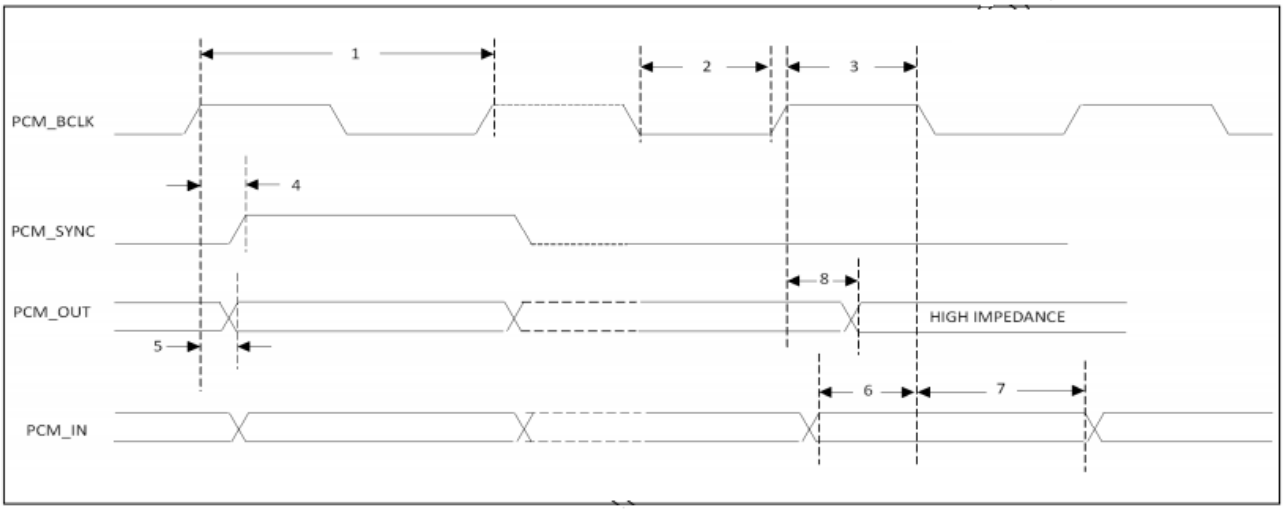
UART Timing Specifications

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	Delay time, UART_CTS_N low to UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	–	0.5	Bit periods

5.5 PCM Interface Timing

- Short Frame Sync, Master Mode

PCM Timing Diagram (Short Frame Sync, Master Mode)

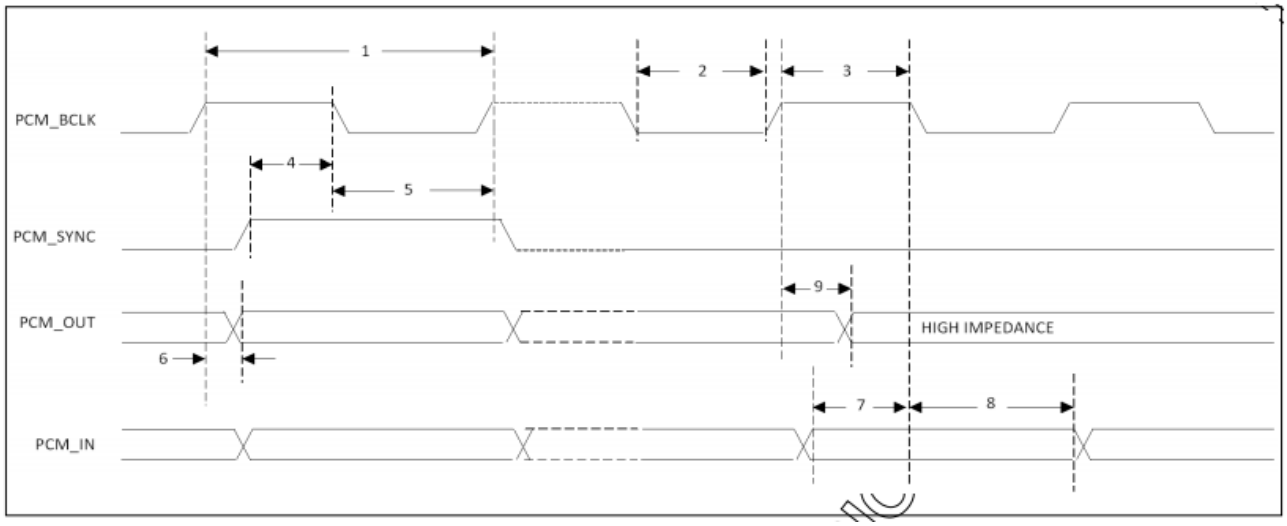


PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

- Short Frame Sync, Slave Mode

PCM Timing Diagram (Short Frame Sync, Slave Mode)

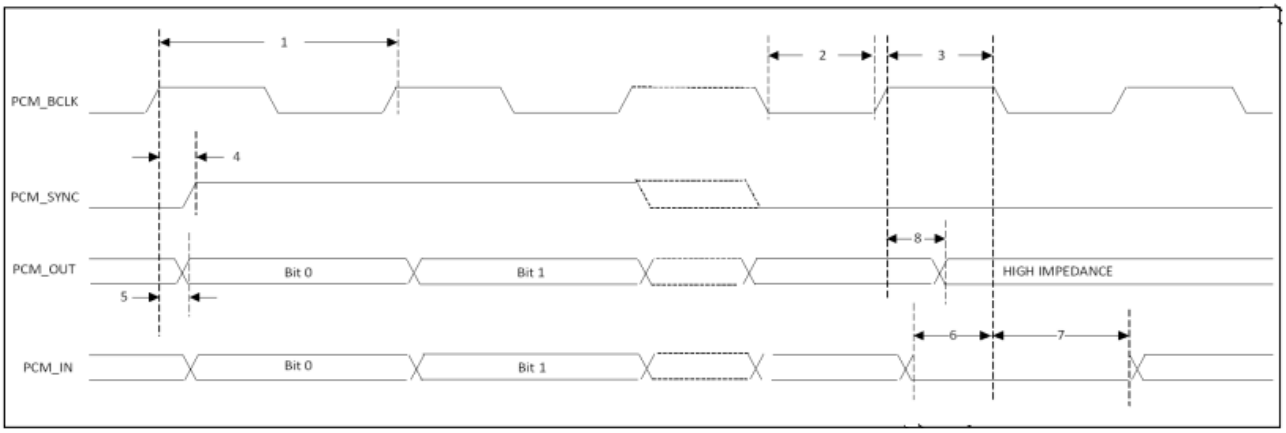


PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

- Long Frame Sync, Master Mode

PCM Timing Diagram (Long Frame Sync, Master Mode)

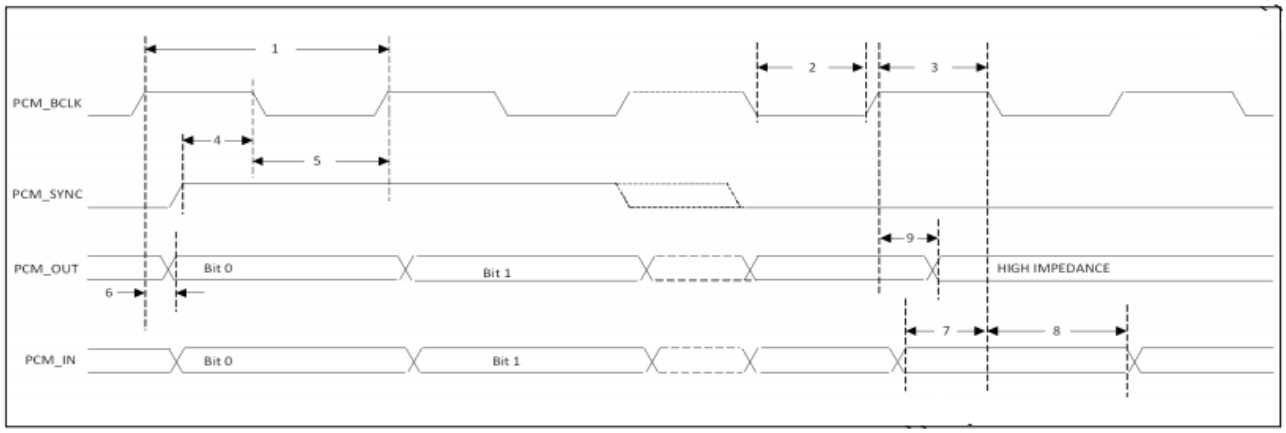


PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high-impedance	0	–	25	ns

- Long Frame Sync, Slave Mode

PCM Timing Diagram (Long Frame Sync, Slave Mode)

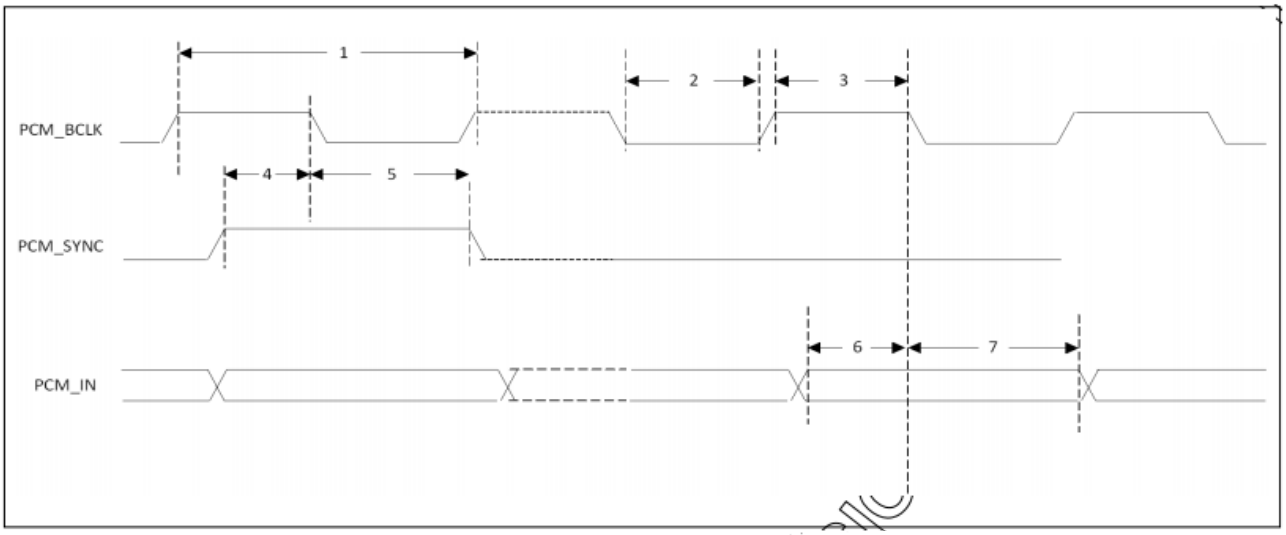


PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

- Receive Only, Short Frame Sync

PCM Burst Mode Timing (Receive Only, Short Frame Sync)

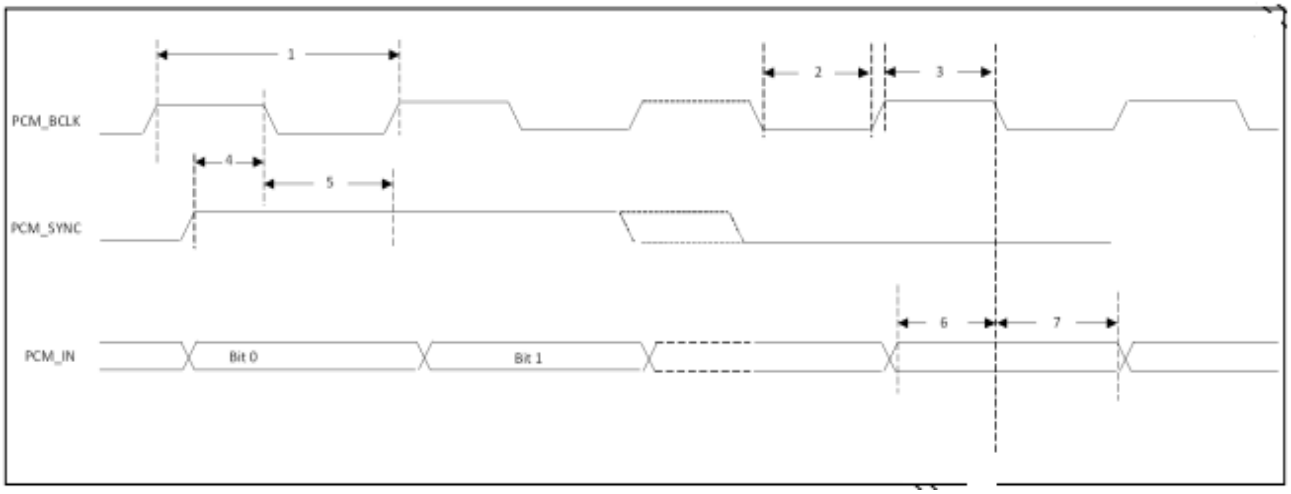


PCM Burst Mode (Receive Only, Short Frame Sync)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock LOW	20.8	–	–	ns
3	PCM bit clock HIGH	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

- Receive Only, Long Frame Sync

PCM Burst Mode Timing (Receive Only, Long Frame Sync)

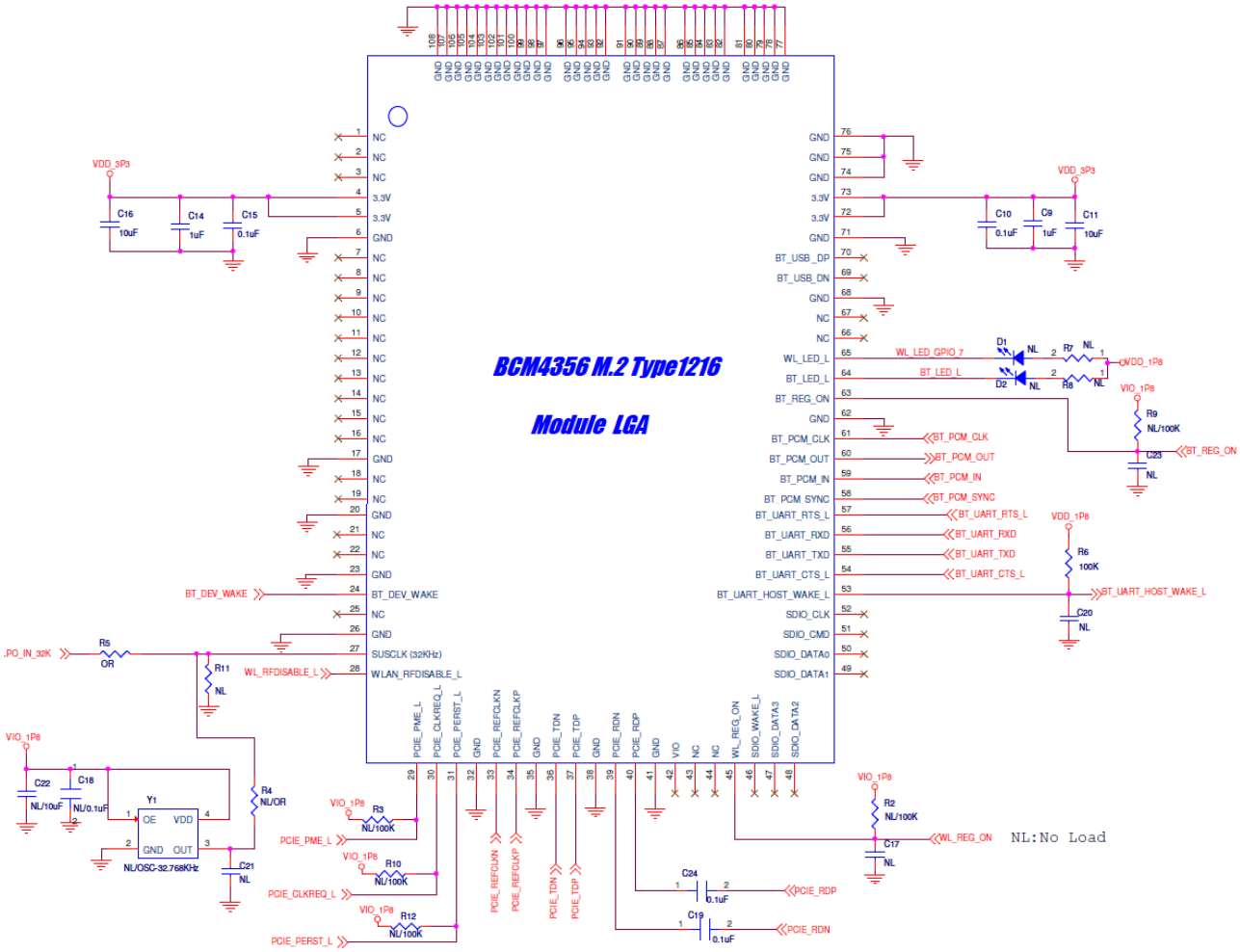


PCM Burst Mode (Receive Only, Long Frame Sync)

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock LOW	20.8	–	–	ns
3	PCM bit clock HIGH	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

6.Schematic Reference Design

Following is the evaluation board schematics of M.2 1216 BCM4356 module for reference.



- **Low Power Clock**

The BCM4356 module uses a secondary low frequency clock for low power mode timing. A precision external 32.768 KHz clock that meets the specifications listed in Table 3 is required by BCM4356.

Table 3: External 32.768K Low Power Oscillator Specifications

Parameter	Conditions/ Notes	Specification			Units
		Min	Typ	Max	
Nominal Input Frequency			32.768	-	KHz
Frequency Accuracy		-200		+200	ppm
Input signal amplitude		+0.2		+1.8	V, p-p
Duty cycle	Square waveor sine- wave	30	-	70	%
Clock jitter	300Hz-15KHz	-		5	ns
Clock jitter	During initial start-up			10,000	ppm

Below section describes the directionality of some of the interface signals incorporated in the various pinouts. Because some signals have directionality associated with them, their names and locations may be different between the Platform side and the Module side. The Module pinouts are described in Item2.5. The main differences between Platform-side pinouts and Module-side pinouts are shown in Figure 95~96 of M.2 spec.

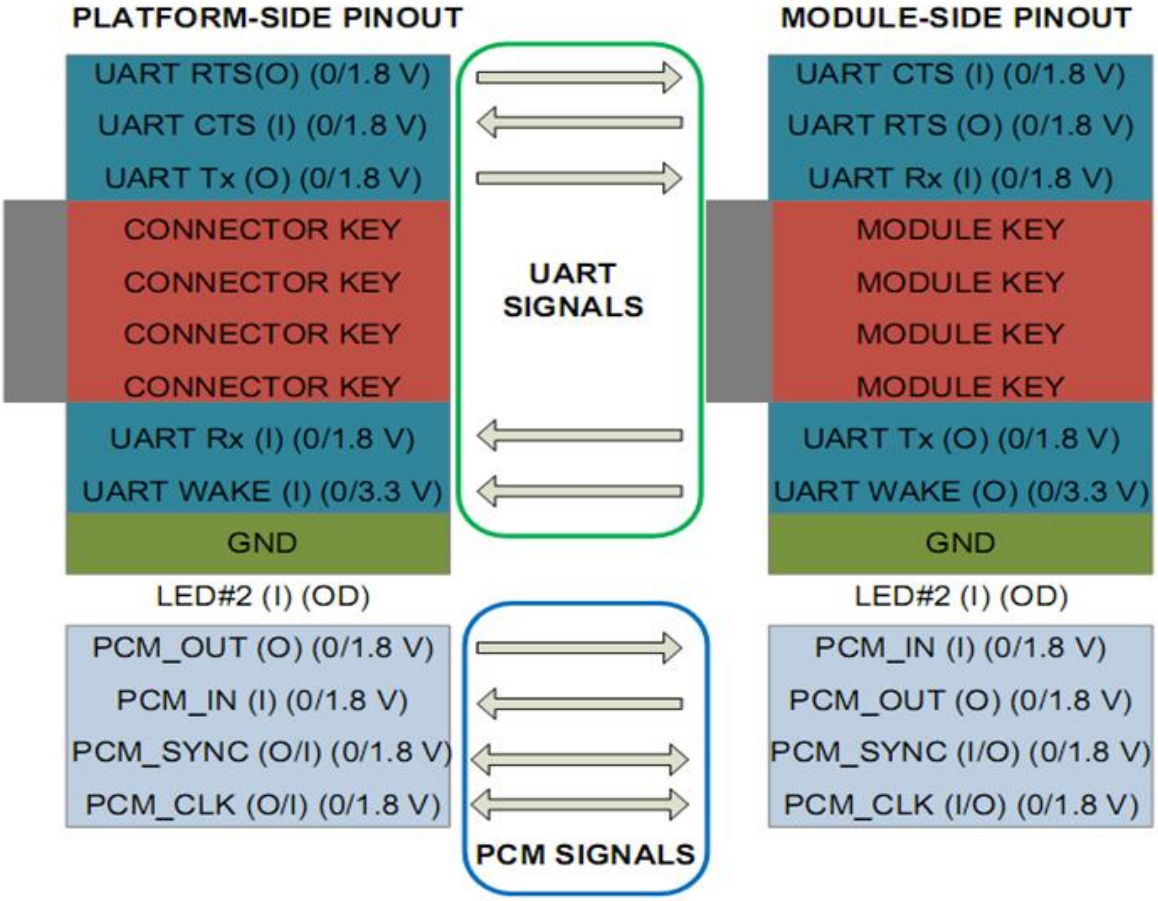


Figure 95: UART and PCM Signal Direction and Signal Name Changes

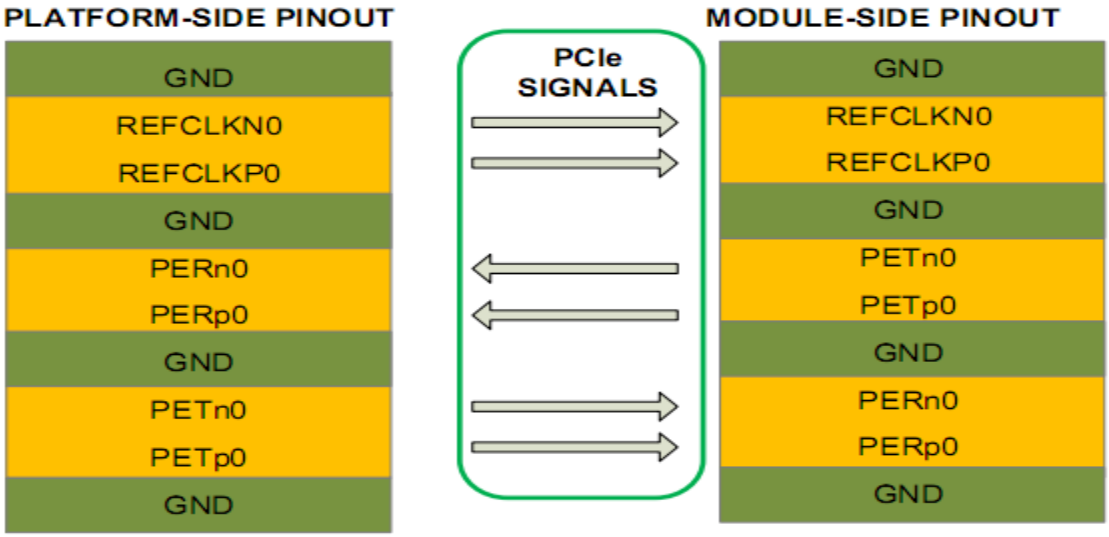


Figure 96. PCIe Signal Direction and Signal Name Changes

7. Software Requirement(TBD)

- Operating System Support
  - Windows 8
  - Windows Blue or later Android 4.3 and above

- WLAN Feature Support
  - WiFi Direct
  - WiFi Display
  - Wi-Fi Miracast (Intel will support WiDi with Miracast interoperability)

- WLAN Security Support
  - WPA/WPA2 Enterprise
  - CCX Lite or higher
  - WMM/AES/TKIP/CKIP

- WLAN Transmit Power Reduction
  - Software control to meet FCC SAR requirement
  - Capability to disable 5GHz operation

- Bluetooth Profile Support
  - Advanced Audio Distribution Profile(A2DP)
  - Basic Imaging Profile (BIP)
  - Basic Printing Profile(BPP)
  - General Audio/Video Distribution Profile (GAVDP)
  - Generic Object Profile(GOEP)
  - Hands-Free Profile(HFP)
  - Headset Profile(HSP)
  - Human Interface Device Profile(HID)[2.0/4.0]
  - Object Push Profile (OPP)
  - Service Port Profile(SPP)
  - Personal Area Network Profile(PAN)

- BLE (Bluetooth Low Energy) Support
  - Windows 8
  - Windows Blue or later

8. Regulatory(TBD)

The module shall pass below RF certification based-on customer requirement.

- USA : FCC P15B / FCC P15C / FCC P15E (FCC ID: TBD)
- Canada : IC RSS-210 (IC ID: TBD)
- Japan : TELEC
- EU : EN300328 V1.8.1 , EN301893 V1.6.1 , EN301489-1/-17 , EN 60950-1 2nd

9. Quality

The product quality must be followed-up by Foxconn factory quality control system.

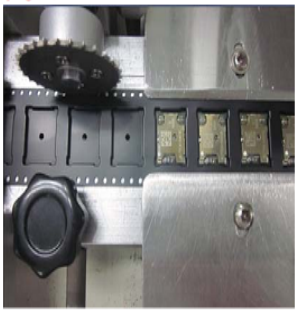
10. Package information

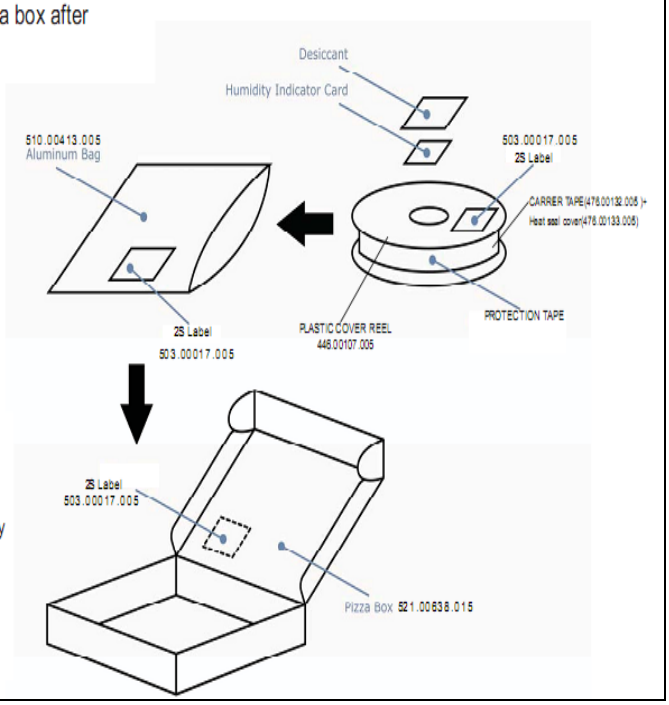
Below is M.2 1216 package information for reference only.

Packaging way:

Round at least a circle protect tape, and put the Humidity indicator and Drier into the Aluminum bag, then put into Pizza box after vacuum-packed,

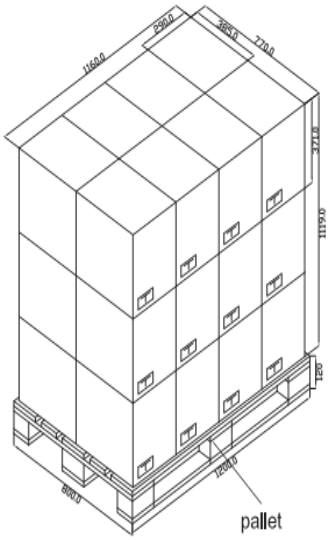
Reel Taping方向

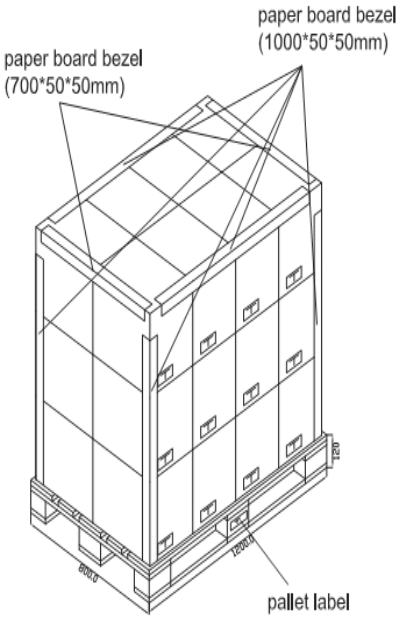




remark：
1, QA: After checked OK, please stamp on the label that stick on bag
2, if there is any unsure, inform engineer or PMC asap
3, less than two D/C for one Pizza box(OK for two D/C)
4, if there are too many MO to printing all,Can printing end 5 digit of every MO only.
5, can combine the different D/C production if needed, but need mark all D/C clear on the label
6, 1500pcs/ reel

Notes:
1. Carton manufacture size: 373*280*359mm
2. Outsize: 385*290*371mm
3. Qty: 1 pallet=4*2*3*1500*5pcs=180000pcs





11. Environmental Requirements and Specifications

11.1 Temperature

11.1.1 Operating Temperature Conditions
The product shall be capable of continuous reliable operation when operating in ambient temperature of 0 °C to +70°C.

11.1.2 Non-Operating Temperature Conditions
Neither subassemblies shall be damaged nor shall the operational performance be degraded when restored to the operating temperature when exposed to storage temperature in the range of -30°C to +85°C.

11.2 PCB bending

The PCB bending spec shall be keep planeness under 0.1mm for both Foxconn and end assembly customer.

11.3 Handling environment

ESD

There are semiconductors on the module, please handle the module under ESD protected and well-controlled environment (<100V).

Terminals Handling Notice

The product is mounted with motherboard through Land Grid Array. In order to prevent poor soldering, please do not touch LGA portion by hand.

Notes: As a rule, baking the components in accordance with condition mentioned above, because tape and real for packaging materials have no heat resistance, please bake the components moved into another container such as heat resistance trays.

Others

1. Please make sure to avoid mechanical shock and vibration for this module.
2. Please do not drop the module.
3. Please do not clean the module.

11.4 Storage Condition

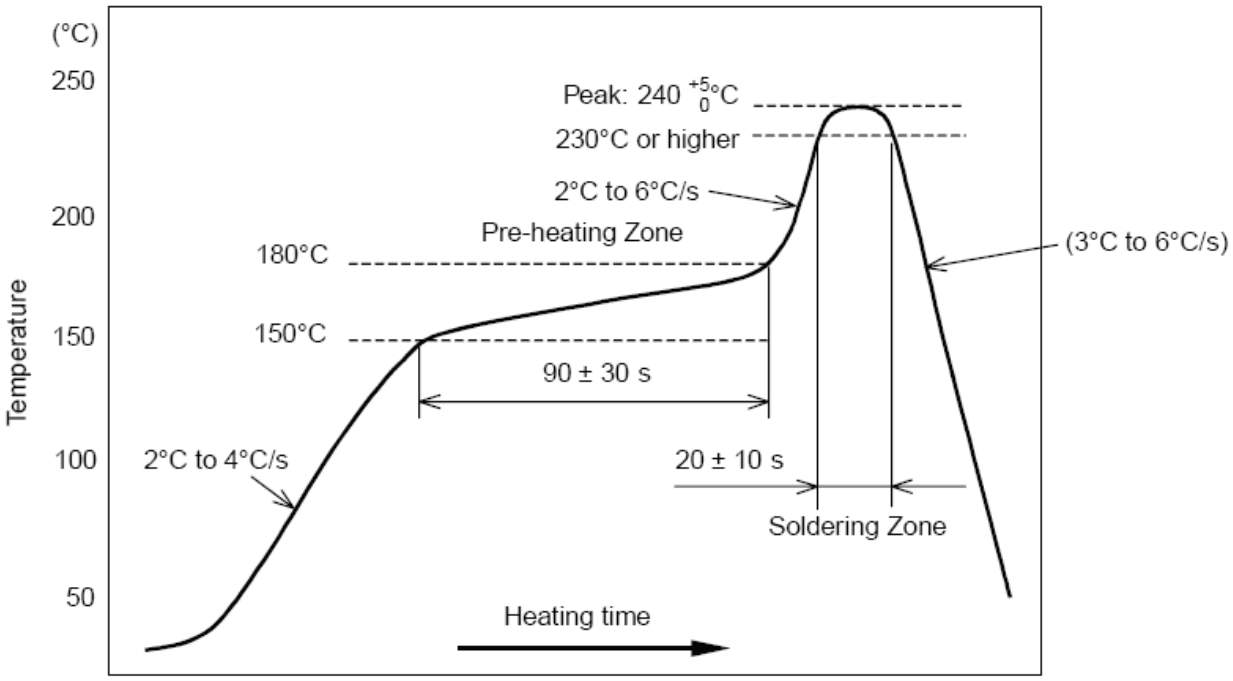
1. Moisture barrier bag must be stored under 40 ℃, humidity under 90% RH, when the moisture barrier bag is sealed by Foxconn.
2. The calculated shelf life for the dry packed product shall be a 12 months from the bag seal date.
3. If Moisture barrier bag is open, the component must be stored in an environment of <25±5℃ /10%RH
4. Please keep the module at 30℃/70% RH.

11.5 Baking Condition

If below two conditions happens:
a) Humidity indicator cards read >30%
b) Temp < 30 ℃, Humidity <70%RH, moisture barrier bag open over 96 hours
Products require baking before mounting
Baking condition: 125 ℃, 12-22 hours
Baking times: Max. 2 times

11.6 Soldering and reflow condition

1) Heating method
   Conventional Convection or IR/convection
2) Temperature measurement
   Thermocouple d=0.1mm ~ 0.2mm CA (K) or CC (T) at soldering portion or equivalent method.
3) Solder paste composition
   Sn/3.0Ag/0.5Cu
4) Allowable reflow soldering times: 2 times, based on the below reflow soldering profile
   Suggest reflow soldering one time for better reliability.
5) Temperature profile
   Reflow soldering shall be done according to the below temperature profile.
6) Peak temp: 245 degree C



Temperature profile for evaluation of solder heat resistance of a component (at solder joint)