Honeywell

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Technical Data and Theory of Operation

Technical Data

MCS-7200 System Description

The MCS-7200 avionics is made up of the SD-720, the HS-720 and the HP-720.

The SD-720 Satellite Data Unit supplies the digital and analog interface to all aircraft avionics, and implements all functionality associated with modulation/demodulation, error correction, channel rate/frequency selection, and RF translation for the system's seven baseband communication channels. The SDU's seven baseband channels support six simultaneous full-duplex circuit-mode voice connections and one packet-mode channel.

The HS-720 High Speed Data Unit incorporates the firmware necessary to support four narrowband (Swift64) channels, which provide simultaneous circuit-mode and/or packet-mode connectivity concurrently with the SDU's baseband channels at rates of 64 kbps (per single channel) or 256 kbps (four combined [bonded ISDN] channels) or two channels of up to 432 kbps (per single channel) SwiftBroadband functionality.

The HP-720 High Power Amplifier implements the linear power amplification of the SD-720 and HS-720 combined RF signals needed to assure their successful transmission from the aircraft to the satellite and to the ground network.

For more information refer to the System Description, Installation, and Maintenance Manual, A15-5111-010.

SD-720 Type Designation

The equipment has been designated by Honeywell International Inc. as an SD-720 Satellite Data Unit for use in a Multichannel SATCOM System, MCS-7200.

Service and Rule for Intended Operation

Aeronautical Mobile Satellite Service
Part 87, Subpart A

Type of Emission

G1W (A-QPSK)
G1D (A-BPSK)

Frequency Range [MHz]

1626.5 - 1660.5

Power Rating

60 Watts Maximum for MCS-7200 with 60 W HPA.
31.6 mW Maximum for the SD-720 alone.

Final Power Amplifier

The SDU final stage is an InGaP/GaAs HBT high linearity driver amplifier, TQP&M9103 (TriQuint / Qorvo).

Circuit Diagram

See attached schematics.

Tune-up Procedures

No field tuning is required. Tuning is done during manufacturing using subassembly test.

See Integrated Test Specifications.

Reference Oscillator

SC cut crystal ovenized oscillator manufactured by CQE.

An oven controlled high stability reference oscillator (Racal Part No. 81771-MBF located in the Satellite Data Unit) is used as the primary frequency reference for:

- Radio Frequency Module Local Oscillators and Synthesized Channel Local Oscillators
- Modem Sample Rate Clocks
- Voice Codec Bit Rate Clock

The crystal oscillator provides good stability versus temperature, power supply voltage and load variations. The output frequency is 10.08 MHz and has sufficient mechanical adjustment range to compensate for ten years of aging. The reference oscillator frequency is sent to the Radio Frequency Module (RFM) where it is buffered and routed to each Modem. The oscillator also outputs a logic signal directly coupled to the SDUs Main Processor Module to indicate the oven temperature stabilization.

Frequency Stabilization

The channel phase-locked-loop synthesizers and other phase-locked-loop oscillators are all referenced to the single reference oscillator.

Modulation Limiting

Not applicable.

Radiated Interference Suppression

The output of the High Power Amplifier in an operating system is fed into the transmit port of an LNA/Diplexer. This device provides greater than 80 dB rejection for out of band signals between 0 MHz to 1585 MHz and greater than 50 dB rejection between 1735 MHz and 12000 MHz. The transmitter chain in the SDU and in the HPA is also bandpass limited.

Modulation Methods

Aviation Binary Phase Shift Keying (A-BPSK)
Aviation Quaternary Phase Shift Keying (A-QPSK)

Carrier Modulation

The generation of a modulated carrier is achieved using digital signal processing techniques and is converted to an analog RF signal employing Digital to Analog conversion techniques. The SDU utilizes two kinds of signals as inputs for transmission, analog audio or digital data. The analog audio is digitized in the CODEC (Coder/ Decoder) assemblies. The digitized audio or the digital data is then scrambled, interleaved and Forward-Error-Corrected (FEC) before being inputted to the data "modulator".

Theory of Operation

The SD-720 is able to provide data and voice information simultaneously in full duplex mode. The power management and frequency selection in this system is controlled by the GES without user assistance.

The digital packet data to be transmitted is routed to the SD-720 main processor assembly, the analog voice to the six codec assemblies of the SD-720 and the digitized cabin voice is routed to the transcoder circuits of the SD-720.

The codec performs A/D and D/A conversion coding/decoding on the analog voice, while the transcoder executes coding/decoding functions. The coded data is passed to the processor module of the SD-720. After processing each channel of data or voice the information is forwarded to a modem assembly.

There are seven modems in the SD-720 and eight available channels in the RFM. Modems one through four can be connected to any of the RFM channels one through four. Modems five through seven can be connected to any of the RFM channels five through eight. There is one modem located on the main processor card and three modems on each of two Triple Transcoder Modem (TTCM) cards. The generation of the modulated RF signal begins in the modem assembly in the form of a fully digital complex baseband signal. This signal is then passed to the RFM where it is processed and converted into an analog IF signal. The RFM produces final frequency conversion to the operational L-band frequency region.

The Honeywell Multichannel Satcom System is compliant to AERONAUTICAL RADIO INC. (ARINC) CHARACTERISTIC 741 PART 2 paragraph 3.1.4 and 4.1.3. The digital modulator fulfills the functions of the modulator model presented on Figures 8b and 8c of Attachment 2x of ARINC 741 part 2.

ARINC 741 Part 2 Figure 8b - Modulator Model
ARINC 741 Part 2 Figure 8c - Data Encoder Model

Major Functions of the CODEC

- Digitize and encode the incoming cockpit or cabin audio, the Cabin Communication System (CCS), or PCM data using the voice coding algorithm specified by the British Telecom 9.6 kbit/sec Speech Codec for Aeronautical Mobile Satellite Communication.
- Receive encoded audio data arriving from the GES and convert it back to analog audio for routing to the cockpit, or to PCM data.
- Generate various call progress messages and tones.
- Decode Dual Tone Multi-Frequency (DTMF) tones as specified in CCITT Recommendations Q.11, Q.16 and Q.23, which have been generated by the telephone handset or a PBX and provide the information to the SDU Main Processor.
- Monitor and control the state of various interfaces.

Major Functions of the Modem

There are seven modems within the SD-720. Each modem receives and transmits Signaling Units and Circuit Mode Data Primary Fields to and from the Main Processor Module. Complex baseband I and Q signals are passed to and from the RFM. The receive channel of the Modem performs demodulation and decoding of complex baseband signals received and passed by the RFM. The transmit stages of the modem perform encoding and scrambling operations to provide a complex bandpass signal for the transmit section of the RFM. All inputs and outputs of the modem are in the digital domain.

Major functions of the Radio Frequency Module (RFM):

- Downconversion, filtering, and A/D conversion of received signals.
- AGC functions as commanded by the main processor.
- Passes baseband signals to the modem.
- Converts digital complex baseband signals into modulated IF signals.
- Upconverts IF signals to output RF frequency
- Adds Doppler correction to output frequency

The SDU contains one RFM. The RFM can process up to eight paired receive/transmit channels. The RFM has a “broadband” architecture whereby the entire receive band is processed by a single Analog-to-Digital Converter (ADC) and the entire transmit band is generated by a single Digital-to-Analog Converter (DAC).

Receiver RF/IF/ADC:

The L-band (1525-1559 MHz) signals from the Diplexer/LNA are routed to the receive port of the RFM. The signal is initially amplified by gain block U53. The signal then passes through a digital step attenuator which via main processor control compensates for variations in input signal level due to Diplexer/LNA gain and cable loss between the Diplexer/LNA and RFM. The digital step attenuator provides 28 dB of control. Next, the signal is bandpass filtered by FL2 and FL3 in order to further attenuate out-of-band interferers that are not completely attenuated by the Diplexer.

The signal is then mixed down in frequency from 1525 – 1559 MHz to 63.4 – 97.4 MHz in mixer U55. The fixed down-converter local oscillator frequency of 1461.600 MHz is generated by oscillator G2 and phase-locked loop frequency synthesizer U62. The down-converter frequency is derived from the 10.08 MHz reference oscillator with a multiplier of 145. The local oscillator signal is buffered by amplifier U59 and low-pass filtered before being applied to mixer U55.

The output of the mixer is the broadband IF ranging from 63.4 to 97.4 MHz. The IF is bandpass filtered by several discrete filters and SAW filter F1. The purpose of these filters is to attenuate any signals that are too close to the desired passband to be effectively filtered by the RF filters in order to prevent these signal from causing unwanted alias frequencies out of the ADC. Between the filters are amplifiers U51, U52 and U58 which prevent the signal level from dropping to the point that the noise figure is adversely affected due to filter losses and also to amplify the IF signal to a level that will not be affected by the Analog to Digital converter's noise figure.

The final filtered output from U58 is applied to an unbalanced-balanced transformer T4 to convert the single ended signal into a differential signal to input into ADC U63.

The sample clock frequency for the ADC is 107.52 MHz. This clock is generated by oscillator G3 and PLL frequency synthesizer U64. The output frequency is derived from the 10.08 MHz reference oscillator with a multiplier of 32/3.

In the ADC, the IF signal is under-sampled since the IF frequency is greater than Fsample/2. In terms of the ADC, the output frequency maps as follows:

RF	IF	ADC Output
1525 MHz ->	63.4 MHz ->	44.12 MHz
1559 MHz ->	97.4 MHz ->	10.12 MHz

The Analog to Digital conversion process causes a spectral inversion since the higher end of the RF band is mapped to the lower frequencies out of the ADC. This is compensated for in the FPGA.

The digital ADC output is fed to the FPGA where further filtering and individual channelization occurs. The individual FPGA outputs for each of the eight receive channels are buffered and routed to the modems in the SDU.

DAC/Transmit IF/Upconverter

The baseband digital transmit I and Q data for each of the eight channels is received from the modem, buffered and routed to the FPGA. This data contains the QPSK modulation at a sample rate of 84ksps. The FPGA takes the complex I/Q data for each of the eight channels and modulates it onto a single wideband digital carrier at the IF frequency. This IF frequency has been adjusted for any Doppler offset requested by the MPMM. The FPGA outputs I and Q data samples at 107.52 Msps to the DAC. By outputting I and Q data, an interpolating DAC can be used. An interpolating DAC internally increases the clock rate and shifts the desired signal to a higher frequency which simplifies the reconstruction filter (DAC output lowpass filter) and allows for a single conversion up to the L-Band transmit frequency.

The digital IF frequency range out of the FPGA is 6.98 MHz to 40.98 MHz. If a normal DAC was used, a single upconversion could not be implemented since the image out of the mixer at L-Band would only be 14 MHz from the desired signal and couldn't be filtered. But an interpolating DAC can perform a digital upconversion which is "perfect" and has no image frequency that has to be filtered. So while the digital input frequency range into the DAC is 6.98 to 40.98 MHz, the analog output frequency is 114.5 to 148.5 MHz. The DAC has interpolated by 4 (raised the clock frequency from 107.52 MHz to 430.08 MHz and shifted the IF signal up by Fs/4 or 107.52 MHz. Now the DAC reconstruction filter is easier to implement and so is the L-band filter since the mixer image at L-band will be 215 MHz away from the desired output.

The DAC clock is derived from the same oscillator that generates the ADC clock.

The fixed up-converter local oscillator frequency of 1512.000 MHz is generated by oscillator G1 and phase-locked loop frequency synthesizer U36. The up-converter frequency is derived from the 10.08 MHz reference oscillator with a multiplier of 150.

The IF frequency band of 114.5 to 148.5 MHz out of the DAC is lowpass filtered and amplified by gain block U43 prior to being applied to mixer U44. In U44, the signal is upconverted to the final transmit frequency band of 1626.5 to 1660.5 MHz.

The output of the mixer enters digital step attenuator U47. The purpose of U47 is to set the nominal transmit output power and provide temperature compensation in order to maintain a constant output power as device gains change with ambient temperature variations. The FPGA reads the board temperature from U42 and adjusts the attenuation of U47 accordingly.

The output of U47 is amplified by U46 and U45 and lowpass filtered prior to exiting the RFM on J3. The J3 output is routed to the HPA for further amplification prior to transmission.

RF Signal Path through HPA

HP-720 60W High Power Amplifier:

Input Frequency:	1626.5 MHz to 1660.5 MHz
Gain:	63 dB ± 3 dB with 0 dB back-off attenuation
Output Frequency:	1626.5 MHz to 1660.5 MHz
Output Power:	60 Watts operational (continuous)

The RF signals in the HPA are amplified and then connected to the diplexer and antenna subsystem.