

ENGINEERING SPECIFICATION		SECURITY NOTATION		SPEC NO. IT7026236		XA	
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TITLE INTEGRATED TEST SPECIFICATION FOR TRANSMITTER CCA 7026236-90X							
PREPARED BY: L. Rodriguez		DATE Apr. 5, 2002		APPROVED BY TECHNICAL MANAGER B. Brettner		DATE Apr. 5, 2002	
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FOR PAGE INDEX, SEE PAGE CR-2. REVISION RECORD FOLLOWS PAGE INDEX.							
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REV LTR	<u>TITLE:</u> INTEGRATED TEST SPECIFICATION FOR VDR TRANSMITTER CCA, PART NO. 7026236-902-903.				
	1. SCOPE This Integrated Test Specification establishes the manufacturing and operational requirements that the VDR TRANSMITTER CCA must meet to insure proper operation conditions. This specification also contains detailed test procedures that apply to the test equipment listed in paragraph 5. Appendix A provides final test report data sheets. Appendix B provides Pre-Test procedures to ensure CCA, as received from manufacturer, is operational. Note that this is only a convenience test that needs to be performed before final assembly of the Transmitter Module (i.e. before cover / heatsink / Power Transistors are installed, and before any other test in this document is run); and is intended for RED LABEL builds only. 2. REFERENCE DOCUMENTS TRANSMITTER CCA 7026236-902 or higher Top Level Drawing HRD Section for TRANSMITTER CCA/CPLD				
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REV LTR	3. GENERAL INFORMATION					
	All input signals shall be applied between the designated terminal and ground, unless otherwise stated. All output voltages shall be measured with respect to ground, unless otherwise noted.					
	3.1 <u>Standard Testing Environment</u>					
	Tests are to be performed as 25°C ± 10°C, 90 percent relative humidity maximum, and at an atmospheric pressure of 20 to 32 inches of mercury.					
	3.2 <u>Temperature Extremes</u>					
A power on warm-up period of 15 minutes is allowed following a 30 minute temperature stabilization period.						
3.3 <u>Burn-In</u>						
TBD						
3.4 <u>Low Speed Control Bus Overview</u>						
There is a four-wire bus connecting the CCAs to provide a control structure:						
• Clock (CONTROL-CLKX) • Transmit data (CONTROL-DX) • Address Sync (CONTROL-FSAX) • Receive data (CONTROL-DR).						
There is a three-wire transmit-control bus consisting of clock (CONTROL-CLKX), data (CONTROL-DX), and address sync (CONTROL-FSAX). This bus is used to transmit data from the Processor CCA to the Transmitter CCA.						
The control bus (a.k.a. low speed control bus) data structure consists of a thirty two-bit serial data stream. In the case of the transmit-control bus, the first eight bits together make an address that identifies a CCA and a location on that CCA to which the data is to be written. In the case of the receive-control bus, the address identifies the data source.						
The processor CCA controls bus timing on the control bus. The processor CCA transmits data to a CCA and only then does that CCA transmit data on the receive-control bus. Stated another way, the processor CCA interrogates each CCA and waits long enough for a reply. If there is a reply, the processor CCA exchanges data with that CCA, and then interrogates the next CCA.						
The serial clock rate for the control bus is 1.64 MHz (52.5 MHz/32).						
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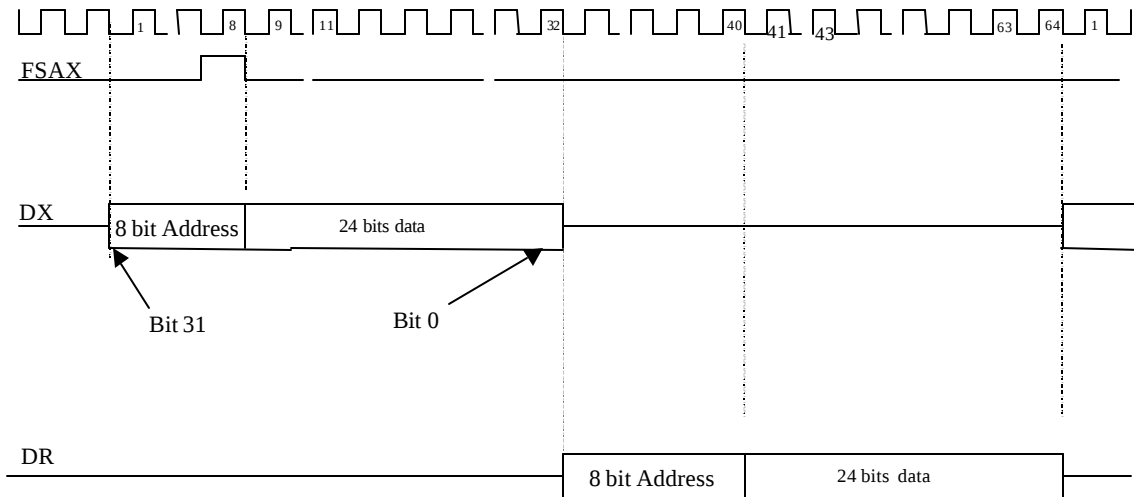


Table 1 lists the currently assigned message identifiers and the control bus communication between the Processor CCA and the Transmitter CPLD on the Transmitter CCA.

Table 1. Control Bus Message Protocol

MESSAGE IDENTIFIER		Transmit-Bus Message	Receive-Bus Message
Msb	lsb		
Device Address	CCA ID		
10000	001	Write Transmitter Control Register	Transmitter Control Register
01000	001	Request TX CPLD Version #	TX CPLD Version #
00100	001	Write TX Synthesizer Data	Echo Address
10100	001	Spare	Spare
X1100	001	Spare	Spare
00010	001	Spare	Spare
00110	001	Write TX Digital Pot	Echo Address
10110	001	Spare	Spare
X1110	001	Spare	Spare
Xxx01	001	Spare	Spare
00011	001	Write TX A/D Channel Number	TX A/D Channel Data
10011	001	Spare	Spare
X1011	001	Spare	Spare
X0111	001	Spare	Spare
01111	001	Spare	Spare
11111	001	Write TX Bias Control Word	Echo Address

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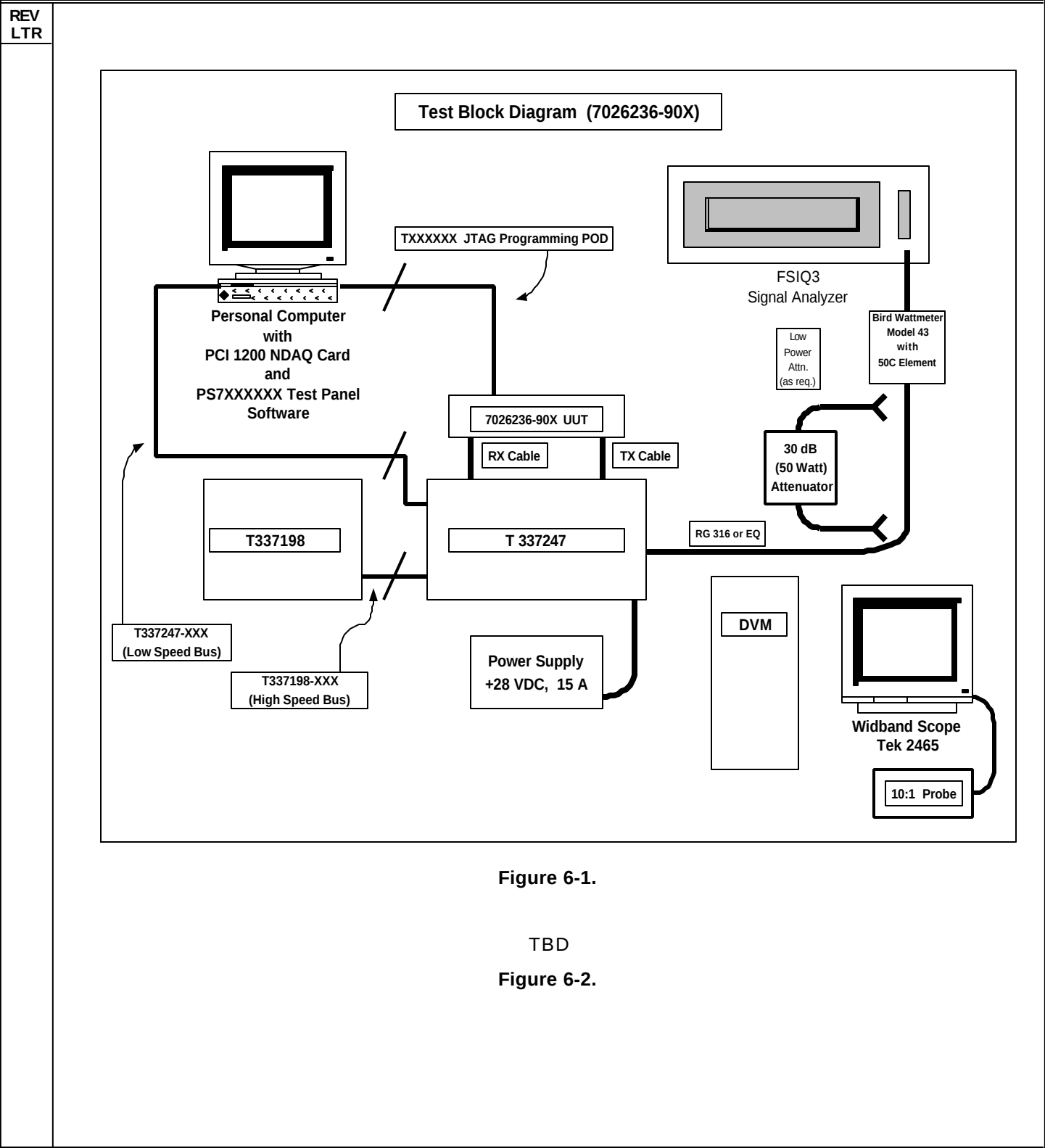
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	4. POWER AND SIGNAL REQUIREMENTS +28 VDC ± 1 VDC 5. RECOMMENDED TEST EQUIPMENT (OR EQUIVALENT) Personal Computer: IBM PC-AT compatible with National Instruments PCI 1200 PC Card. Power Supply: 28 VDC, 15 Amp, with output current and voltage metering; and over-current and over-voltage protection. Signal Analyzer: Rhode & Schwartz FSIQ 3. Power Meter: Bird Wattmeter, Model 43 with 50C element. Oscilloscope: Tektronix 2465 DVM: Fluke Attenuator: 30dB, 50Ω, 50W, (Return Loss > 22dB) Test Software: Windows VDR/VDL CCA Test Software (PS7XXXXXX).						
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REV LTR					
	6. TEST SETUP - Follow Figures 6-1 and 6-2. - Connect T337247 to PC (use T337247-XXX). - Connect T337198 to T337247 (use T337198-XXX and T337198-XXX). - Place CCA in T-fixture, T337247. - Connect J1 on T-fixture to P1 on UUT. - Connect +28 VDC +/- 1V to +28V input on T-fixture. Connect GND to RTN input on T-fixture. - Connect Xilinx Parallel cable III Pod (T7XXXXXX) and flying leads (T7XXXXXX-XXX) to UUT JTAG inputs (P2). - Power on FAN on T-fixture. - Power on T-fixture, T337247. - Reset T-fixture, T337247. - Power on UUT. - Load CPLD as specified on the top-level drawing using Xilinx Webpack Device Programmer software. - Disconnect Xilinx Parallel cable III Pod (T7XXXXXX) and flying leads (TXXXXXX-XXX) from UUT JTAG inputs (P2). - Power off T-fixture, T337247. - Start PC-based test software (PS7XXXXXX) which drives National Instrument PCI 1200 PC card to drive UUT Low Speed Control Bus (LSCB). - Select TRANSMITTER Test Panel. - Power on T-fixture, T337247. - Reset T-fixture, T337247. 6.1 <u>Voice Mode Setup</u> FSIQ 3 setup for AM / MODE 0 tests. If this setup has already been saved, recall 7026236-VOI and disregard the next step.				
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REV LTR	6.1.1 FSIQ 3 Setup for AM/MODE 0 Tests • PRESET Analyzer. • Select TRACE-> 1. • Set LEVEL->REF->REF LEVEL OFFSET-> +31dB • Set REF LEVEL-> +50dBm • Set FREQUENCY->CENTER-> 128MHz • Set FREQUENCY->SPAN-> 25kHz • Select DISPLAY->SPLIT SCREEN • Select SCREEN COUPLING->MODE COUPLED (Turns MODE COUPLING Off) • Select DISPLAY->ACTIVE SCREEN B • Select TRACE-> 2 • Select MODE->VECTOR ANALYZER->ANALOG DEMOD • Select MEAS RESULT->AM SIGNAL • Select MEAS RESULT->MODULATION SUMMARY • Set LEVEL->REF->REF LEVEL OFFSET-> +31dB • Set REF LEVEL-> +50dBm • Set FREQUENCY->CENTER-> 128MHz 6.2 <u>Data Mode Setup</u> FSIQ 3 setup for MODE2 tests. If this setup has already been saved, recall 7026236-DAT and disregard the next step. 6.2.1 FSIQ 3 Setup for MODE2 Tests TBD 6.3 <u>Setup Figures</u>								
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LTR	NO.	OPR LIMITS	C	TEST DESCRIPTION	SWITCH POS	C	WORK STEPS	
	1.0			Setup per section 6.1. (This step is only for –902 CCAs revXF or higher)			VOICE MODE SETUP (This step is only for –902 CCAs revXF or higher)	
	1.10			For 7026236-902 revXF or higher perform convenience pre-test in Appendix B.			Perform convenience Pre-Test per Appendix B.	
	2.0			Check CPLD version via Low Speed Control Bus (LSCB). Verify correct version received. Version is identified as bits 23 through 16 of the response word to 46XXXXXX ₁₆ .				Version = 03 ₁₆
	3.0			Check T-fixture Current Drain. The input current to the T-fixture with the UUT not powered shall read between xxx-xxxmA.	UUT PWR OFF		Turn off power to UUT. Read +28V current drain from power supply.	xxx-xxxmA
	4.0			Check UUT Initial Current Drain The input current to the UUT shall be between 300-500mA (400mA nom).	UUT PWR ON		Turn on power to UUT. Read +28V current drain from power supply.	
	4.10						Subtract T-fixture drain measured above from measurement.	300-500mA (400mA nom)
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LTR	NO.	OPR LIMITS	C	TEST DESCRIPTION	SWITCH POS	C	WORK STEPS	MFG LIMITS	
	5.0			Verify Synthesizer Lock Range Apply power to synthesizer section (enable LO-EN). Select COUPLE to FREQ. Select AM Mode.	LO ENABLE ON COUPLE TO FREQ ON AM ON		Select LO ENABLE box on test panel. Select COUPLE to FREQ box on test panel. Select AM radio button on test panel.		
	5.10			Select 25kHz VOICE Mode. Tune Synthesizer to 108MHz. Verify lock.	25kHz VOICE ON 108MHz		Select 25kHz VOICE radio button on test panel. Enter 108 on Active Frequency box. Press ENTER. Verify lock status on test panel.		LOCK (GREEN)
	5.20			Tune Synthesizer to 118MHz. Verify lock.	118MHz		Enter 118 on Active Frequency box. Press ENTER. Verify lock status on test panel.		LOCK (GREEN)
	5.30			Tune Synthesizer to 127.975MHz. Verify lock.	127.975MHz		Enter 127.975 on Active Frequency box. Press ENTER. Verify lock status on test panel.		LOCK (GREEN)
	5.40			Tune Synthesizer to 128MHz. Verify lock.	128MHz		Enter 128 on Active Frequency box. Press ENTER. Verify lock status on test panel.		LOCK (GREEN)
	5.50			Tune Synthesizer to 137MHz. Verify lock.	137MHz		Enter 137 on Active Frequency box. Press ENTER. Verify lock status on test panel.		LOCK (GREEN)
	5.60			Tune Synthesizer to 151.975MHz. Verify lock.	151.975MHz		Enter 151.975 on Active Frequency box. Press ENTER. Verify lock status on test panel.		LOCK (GREEN)
	5.70			Tune Synthesizer back to mid-range (128MHz).	128MHz		Enter 128 on Active Frequency box. Press ENTER. Verify lock status on test panel.		LOCK (GREEN)
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	6.0			Check Additional PLL Current Drain The additional current drain on the PLL shall be between 20-40mA (30mA nom).			Read +28V current drain from power supply.	
	6.10						Add T-fixture drain and UUT initial drain measured above in steps 3.0 and 4.0; subtract from measurement.	20-40mA (30mA nom)
	7.0			Check +5.2V Current Drain Apply power to +5.2V circuits (+5.2V-EN). The current drain on the +5.2V circuits shall be between 60-100mA (80mA nom).	5.2V ENABLE ON		Select 5.2V ENABLE check box on test panel. Read +28V current drain from power supply.	
	7.10						Add T-fixture drain, UUT initial drain, and PLL drain measured above in steps 3.0, 4.0, and 6.0; subtract from measurement	60-100mA (80mA nom)
	8.0			Check +5V-SW Current Drain Apply power to +5V-SW circuits (+5V-SW-EN#). The current drain on the +5V-SW circuits shall be between 40-70mA (55mA nom).	5V-SW-EN		Select 5V-SW-EN box on test panel. Read +28V current drain from power supply.	
	8.10						Add T-fixture drain, UUT initial drain, PLL drain, and +5.2V drain measured above in steps 3.0, 4.0, 6.0, and 7.0; subtract from measurement.	40-70mA (55mA nom)
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LTR	NO.	OPR LIMITS	C	TEST DESCRIPTION	SWITCH POS	C	WORK STEPS	MFG LIMITS
	9.0			Check +28V Monitor The +28V TX MONITOR display shall be between 27-29V (28V nom).			Read +28V TX MONITOR window.	27-29V (28V nom)
	10.0			Check Temperature Sensor The TEMPERATURE(C) display shall be between 20-30°C (25°C nom).			Read TEMPERATURE(C) window.	20-30°C (25°C nom)
	11.0			Adjust Driver Bias Adjust the Driver bias current to 0.75A.	DRIVER BIAS INITIALIZE		Select DRIVER BIAS INITIALIZE button on test panel. Adjust bias current using the slider bar while monitoring the DRIVER CURRENT window.	0.7-0.8A (0.75A nom)
					DRIVER BIAS COMPLETE		Once desired current has been set, select DRIVER BIAS COMPLETE button on test panel. Record DRIVER BIAS ADJUST value on Table in Appendix A.	
	12.0			Adjust Final Bias Adjust the Driver bias current to 1.5A.	FINAL BIAS INITIALIZE		Select FINAL BIAS INITIALIZE button on test panel. Adjust bias current using the slider bar while monitoring the FINAL CURRENT window.	1.45-1.55A (1.5A nom)
					FINAL BIAS COMPLETE		Once desired current has been set, de-select FINAL BIAS COMPLETE button on test panel. Record FINAL BIAS ADJUST value on Table in Appendix A.	
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LTR	NO.	OPR LIMITS	C	TEST DESCRIPTION	SWITCH POS	C	WORK STEPS	MFG LIMITS
	13.0			Check Buffer Current Drain De-select DRIVER BIAS and FINAL BIAS Apply power to the BUFFER circuit. (BUFFER ON). Press TRANSMIT button to enable bias. The current drain on the BUFFER circuit shall be between 400-550mA (475mA nom). Press TRANSMIT button to disable bias.	FINAL BIAS OFF DRIVER BIAS OFF GATE BIAS ENABLE BUFFER ON TRANSMIT ON Monitor PREDRIVER CURRENT TRANSMIT OFF BUFFER OFF		De-select FINAL BIAS ON box on test panel. De-select FINAL BIAS ON box on test panel. De-select GATE BIAS ENABLE box on test panel. Select BUFFER ON box on test panel. Enable TRANSMIT button on test panel. Read PREDRIVER CURRENT window. Disable TRANSMIT button on test panel. De-select BUFFER ON box on test panel.	400-550mA (475mA nom)
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LTR	NO.	OPR LIMITS	C	TEST DESCRIPTION	SWITCH POS	C	WORK STEPS	MFG LIMITS
	14.0			Check Pre Driver Current Drain Apply power to the PRE DRIVER circuit. (PRE DRIVER ON). Press TRANSMIT button to enable bias. The current drain on the PRE DRIVER circuit shall be between 400-550mA (475mA nom). Press TRANSMIT button to disable bias.	PRE DRIVER ON TRANSMIT ON Monitor PREDRIVER CURRENT TRANSMIT OFF PRE DRIVER OFF		Select PRE DRIVER ON box on test panel. Enable TRANSMIT button on test panel. Read PREDRIVER CURRENT window. Disable TRANSMIT button on test panel. De-select PRE DRIVER ON box on test panel.	400-550mA (475mA nom)
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REV	TEST	SPECIFICATION			PROCEDURE		SPECIFICATION	
LTR	NO.	OPR LIMITS	C	TEST DESCRIPTION	SWITCH POS	C	WORK STEPS	
	15.0			(This step is only for -903 CCAs or higher) Monitor Modulator Output Apply a 1kHz, 70% tone to the modulator input. Verify operation at Modulator output. Output power at J1 shall read -11dBm ± 3dB. SINAD shall be 36dB or greater. AM percentage shall be 70% ± 5%.	Use 70% EEPROMS. ALL POWER ON ENVELOPE LOOP OFF BUFFER ON PRE DRIVER ON FSIQ 3 TRACE 1 LEVEL-> REF-> REF LEVEL OFFSET-> 0dB LEVEL-> REF-> 0dBm		(This step is only for -903 CCAs or higher) Place EEPROMS marked 70% (T337198-XXX), on sockets in T337198 fixture. Select ALL POWER ON box on test panel. De-select ENVELOPE LOOP ON box on test panel. Select BUFFER ON box on test panel. Select PRE DRIVER ON box on test panel. On FSIQ 3, Select TRACE 1. Set LEVEL-> REF-> REF LEVEL OFFSET-> 0dB. Set LEVEL-> REF-> 0dBm.	
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REV	TEST	SPECIFICATION			PROCEDURE			SPECIFICATION
LTR	NO.	OPR LIMITS	C	TEST DESCRIPTION	SWITCH POS	C	WORK STEPS	MFG LIMITS
	15.10			<u>112MHz</u> Tune Synthesizer to 112MHz.	FSIQ 3 TRACE 2 LEVEL-> REF-> REF LEVEL OFFSET-> 0dB LEVEL-> REF-> 0dBm 112MHz FSIQ 3 FREQ-> CENTER-> 112MHz TRANSMIT ON TRANSMIT OFF		On FSIQ 3, Select TRACE 2. Set LEVEL-> REF-> REF LEVEL OFFSET-> 0dB. Set LEVEL-> REF-> 0dBm. ALL MEASUREMENTS DONE ON FSIQ 3. Enter 112 on Active Frequency box. Press ENTER. Verify lock status on test panel. On FSIQ 3, Set FREQUENCY-> CENTER-> 112MHz Enable TRANSMIT button on test panel. Measure Audio Frequency. Read output power at J1. Read SINAD at J1 Read AM%, +pk at J1 Read AM%, -pk at J1 Disable TRANSMIT button on test panel.	LOCK (GREEN) 990–1010Hz (1000Hz nom) -11dBm ± 3dB = 36dB 70% ± 5% 70% ± 5%
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REV	TEST	SPECIFICATION			PROCEDURE			SPECIFICATION
LTR	NO.	OPR LIMITS	C	TEST DESCRIPTION	SWITCH POS	C	WORK STEPS	MFG LIMITS
	15.20			<u>127.975MHz</u> Tune Synthesizer to 127.975MHz.	127.975MHz		Enter 127.975 on Active Frequency box. Press ENTER. Verify lock status on test panel. On FSIQ 3, Set FREQUENCY-> CENTER-> 127.975MHz Enable TRANSMIT button on test panel. Measure Audio Frequency. Read output power at J1. Read SINAD at J1 Read AM%, +pk at J1 Read AM%, -pk at J1 Disable TRANSMIT button on test panel.	LOCK (GREEN) 990–1010Hz (1000Hz nom) -11dBm ± 3dB = 36dB 70% ± 5% 70% ± 5%
	15.30			<u>128MHz</u> Tune Synthesizer to 128MHz.	128MHz		Enter 128 on Active Frequency box. Press ENTER. Verify lock status on test panel. On FSIQ 3, Set FREQUENCY-> CENTER-> 128MHz Enable TRANSMIT button on test panel. Measure Audio Frequency. Read output power at J1. Read SINAD at J1 Read AM%, +pk at J1 Read AM%, -pk at J1 Disable TRANSMIT button on test panel.	LOCK (GREEN) 990–1010Hz (1000Hz nom) -11dBm ± 3dB = 36dB 70% ± 5% 70% ± 5%

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REV	TEST	SPECIFICATION			PROCEDURE			SPECIFICATION
LTR	NO.	OPR LIMITS	C	TEST DESCRIPTION	SWITCH POS	C	WORK STEPS	MFG LIMITS
	15.40			<u>151.975MHz</u> Tune Synthesizer to 151.975MHz.	151.975MHz FSIQ 3 FREQ-> CENTER-> 151.975MHz TRANSMIT ON TRANSMIT OFF		Enter 151.975 on Active Frequency box. Press ENTER. Verify lock status on test panel. On FSIQ 3, Set FREQUENCY-> CENTER-> 151.975MHz Enable TRANSMIT button on test panel. Measure Audio Frequency. Read output power at J1. Read SINAD at J1 Read AM%, +pk at J1 Read AM%, -pk at J1 Disable TRANSMIT button on test panel.	LOCK (GREEN) 990–1010Hz (1000Hz nom) -11dBm ± 3dB = 36dB 70% ± 5% 70% ± 5%
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REV	TEST	SPECIFICATION			PROCEDURE			SPECIFICATION
LTR	NO.	OPR LIMITS	C	TEST DESCRIPTION	SWITCH POS	C	WORK STEPS	MFG LIMITS
	16.0			Adjust Output Power Level Apply a 1kHz, 70% tone to the modulator input and adjust the power output at J2 until it reads 18W.	Use 70% EEPROMS. ALL POWER ON GATE BIAS ENABLE ENVELOPE LOOP OFF ALL BIAS ON FSIQ 3 TRACE 1 LEVEL-> REF-> REF LEVEL OFFSET-> +31dB LEVEL-> REF-> +50dBm FSIQ 3 TRACE 2 LEVEL-> REF-> REF LEVEL OFFSET-> +31dB LEVEL-> REF-> +50dBm		Place EEPROMS marked 70% (T337198-XXX), on sockets in T337198 fixture. Select ALL POWER ON box on test panel. Select GATE BIAS ENABLE box on test panel. De-select ENVELOPE LOOP ON box on test panel. Select ALL BIAS ON box on test panel. On FSIQ 3, Select TRACE 1. Set LEVEL-> REF-> REF LEVEL OFFSET-> +31dB. Set LEVEL-> REF-> +50dBm. On FSIQ 3, Select TRACE 2. Set LEVEL-> REF-> REF LEVEL OFFSET-> +31dB. Set LEVEL-> REF-> +50dBm.	
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REV	TEST	SPECIFICATION			PROCEDURE			SPECIFICATION
LTR	NO.	OPR LIMITS	C	TEST DESCRIPTION	SWITCH POS	C	WORK STEPS	MFG LIMITS
	16.10			112MHz Tune Synthesizer to 112MHz.	112MHz		Connect 31dB ± 0.5dB of attenuation (includes cable, attenuator and any other losses) at J2 capable of handling 50W CW. POWER MEASUREMENTS DONE ON BIRD WATTMETER. ALL OTHER MEASUREMENTS DONE ON FSIQ 3.	
	16.11				FSIQ 3 FREQ-> CENTER-> 112MHz		Enter 112 on Active Frequency box. Press ENTER. Verify lock status on test panel. On FSIQ 3, Set FREQUENCY-> CENTER-> 112MHz	LOCK (GREEN)
	16.12				TRANSMIT ON		Enable TRANSMIT button on test panel. Measure Audio Frequency.	990–1010Hz (1000Hz nom)
				Wait for power amplifiers to cool down. Monitor TEMPERATURE© window until it reaches 40°C or lower.	TRANSMIT OFF		Adjust power output using the RF POWER ADJUST. Monitor output power at J2. Disable TRANSMIT button on test panel. Monitor TEMPERATURE© = 40°C window until it reaches desired level.	17-19W (18W nom)
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REV	TEST	SPECIFICATION				PROCEDURE		SPECIFICATION
LTR	NO.	OPR LIMITS	C	TEST DESCRIPTION	SWITCH POS	C	WORK STEPS	MFG LIMITS
				Enable ENVELOPE LOOP control and adjust output at J2 for 22W. SINAD shall be 34dB or greater. AM modulation percentage shall be 70% ± 5%. FM shall be <u>TBD</u> Hz or less.	ENVELOPE LOOP ON		Select ENVELOPE LOOP ON box on test panel.	
					TRANSMIT ON		Enable TRANSMIT button on test panel. Adjust output power at J2 using both FWD POWER ADJUST and RF POWER ADJUST simultaneously until the requirements below are met: Power Output: 22W	21-23W (22W nom)
	16.13							
	16.14						SINAD: = 34dB	= 34dB
	16.15						AM%, +pk: 70 ± 5%	70 ± 5%
	16.16						AM%, -pk: 70 ± 5%	70 ± 5%
	16.17						FM: = <u>TBD</u> Hz	= <u>TBD</u> Hz
					TRANSMIT OFF		Enable TRANSMIT button on test panel.	
					ENVELOPE LOOP OFF		De-select ENVELOPE LOOP ON box on test panel.	
				Record values on Table in Appendix A .			Record FWD POWER ADJUST and RF POWER ADJUST values on Table in Appendix A .	
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REV	TEST	SPECIFICATION			PROCEDURE			SPECIFICATION
LTR	NO.	OPR LIMITS	C	TEST DESCRIPTION	SWITCH POS	C	WORK STEPS	MFG LIMITS
	16.20			<u>118MHz</u> Tune Synthesizer to 118MHz.	118MHz		Enter 118 on Active Frequency box. Press ENTER. Verify lock status on test panel.	LOCK (GREEN)
	16.21			Repeat step 16.11.				
	16.22			Repeat step 16.12.				
	16.23			Repeat step 16.13.				
	16.24			Repeat step 16.14.				
	16.25			Repeat step 16.15.				
	16.26			Repeat step 16.16.				
	16.27			Repeat step 16.17.				
	16.30			<u>123MHz</u> Tune Synthesizer to 123MHz.	123MHz		Enter 123 on Active Frequency box. Press ENTER. Verify lock status on test panel.	LOCK (GREEN)
	16.31			Repeat step 16.11.				
	16.32			Repeat step 16.12.				
	16.33			Repeat step 16.13.				
	16.34			Repeat step 16.14.				
	16.35			Repeat step 16.15.				
	16.36			Repeat step 16.16.				
	16.37			Repeat step 16.17.				
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REV	TEST	SPECIFICATION			PROCEDURE		SPECIFICATION
LTR	NO.	OPR LIMITS	C	TEST DESCRIPTION	SWITCH POS	C	WORK STEPS
	16.40			<u>133MHz</u> Tune Synthesizer to 133MHz.	133MHz		Enter 133 on Active Frequency box. Press ENTER. Verify lock status on test panel.
					FSIQ 3		On FSIQ 3,
					FREQ->		Set FREQUENCY->
					CENTER->		CENTER-> 133MHz
					133MHz		
	16.41			Repeat step 16.11.			
	16.42			Repeat step 16.12.			
	16.43			Repeat step 16.13.			
	16.44			Repeat step 16.14.			
	16.45			Repeat step 16.15.			
	16.46			Repeat step 16.16.			
	16.47			Repeat step 16.17.			
				<u>138MHz</u>			
	16.50			Tune Synthesizer to 138MHz.	138MHz		Enter 138 on Active Frequency box. Press ENTER. Verify lock status on test panel.
					FSIQ 3		On FSIQ 3,
					FREQ->		Set FREQUENCY->
					CENTER->		CENTER-> 138MHz
					138MHz		
	16.51			Repeat step 16.11.			
	16.52			Repeat step 16.12.			
	16.53			Repeat step 16.13.			
	16.54			Repeat step 16.14.			
	16.55			Repeat step 16.15.			
	16.56			Repeat step 16.16.			
	16.57			Repeat step 16.17.			
				(extended frequency tests – 16.60 through 16.77) (for –902 only: extended frequency tests for reference only)			(extended frequency tests – 16.60 through 16.77) (for –902 only: extended frequency tests for reference only)
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REV	TEST	SPECIFICATION			PROCEDURE			SPECIFICATION
LTR	NO.	OPR LIMITS	C	TEST DESCRIPTION	SWITCH POS	C	WORK STEPS	MFG LIMITS
	16.60			145MHz Tune Synthesizer to 145MHz.	145MHz		Enter 145 on Active Frequency box. Press ENTER. Verify lock status on test panel.	LOCK (GREEN)
	16.61			Adjust the power output at J2 until it reads 15W.	FSIQ 3 FREQ-> CENTER-> 145MHz		On FSIQ 3, Set FREQUENCY-> CENTER-> 145MHz	
	16.62			Wait for power amplifiers to cool down. Monitor TEMPERATURE© window until it reaches 40°C or lower.	TRANSMIT ON		Enable TRANSMIT button on test panel. Measure Audio Frequency.	990–1010Hz (1000Hz nom)
				Enable ENVELOPE LOOP control and adjust output at J2 for 17W. SINAD shall be 30dB or greater. AM modulation percentage shall be 70% ± 5%. FM shall be TBD Hz or less.	TRANSMIT OFF		Adjust power output using the RF POWER ADJUST. Monitor output power at J2. Disable TRANSMIT button on test panel. Monitor TEMPERATURE© = 40°C window until it reaches desired level.	14-16W (15W nom)
					ENVELOPE LOOP ON		Select ENVELOPE LOOP ON box on test panel.	
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REV	TEST	SPECIFICATION			PROCEDURE			SPECIFICATION
LTR	NO.	OPR LIMITS	C	TEST DESCRIPTION	SWITCH POS	C	WORK STEPS	MFG LIMITS
	16.70			<u>151.975MHz</u> Tune Synthesizer to 151.975MHz.	151.975MHz		Enter 151.975 on Active Frequency box. Press ENTER. Verify lock status on test panel.	LOCK (GREEN)
	16.71			Repeat steps 16.61.	FSIQ 3 FREQ-> CENTER-> 151.975MHz		On FSIQ 3, Set FREQUENCY-> CENTER-> 151.975MHz	
	16.72			Repeat steps 16.62.				
	16.73			Repeat steps 16.63.				
	16.74			Repeat steps 16.64.				
	16.75			Repeat steps 16.65.				
	16.76			Repeat steps 16.66.				
	16.77			Repeat steps 16.67.				
	17.0			Power Off UUT Power off UUT and remove from Test Fixture.	UUT PWR OFF		Turn off power to UUT. Remove UUT from Test Fixture.	

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REV LTR	Appendix A Final Test Report PART NO. 7026236-_____SERIAL NO. _____ POWER UP VERIFICATION <table><tr><th>TEST NO.</th><th>DESC.</th><th>MEAS.</th><th>LIMIT-LOW</th><th>LIMIT-HIGH</th><th>UNIT</th></tr><tr><td>2.00</td><td>CPLD version</td><td></td><td>03h</td><td>---</td><td>0xh</td></tr><tr><td>3.00</td><td>T-fixture current</td><td></td><td>TBD</td><td>TBD</td><td>AMPS</td></tr><tr><td>4.00</td><td>UUT current measurement</td><td></td><td>---</td><td>---</td><td>AMPS</td></tr><tr><td>4.10</td><td>UUT initial current calculation</td><td></td><td>0.30</td><td>0.50</td><td>AMPS</td></tr><tr><td>5.10</td><td>108MHz Lock</td><td></td><td>---</td><td>---</td><td>CHECK</td></tr><tr><td>5.20</td><td>118MHz Lock</td><td></td><td>---</td><td>---</td><td>CHECK</td></tr><tr><td>5.30</td><td>127.975MHz Lock</td><td></td><td>---</td><td>---</td><td>CHECK</td></tr><tr><td>5.40</td><td>128MHz Lock</td><td></td><td>---</td><td>---</td><td>CHECK</td></tr><tr><td>5.50</td><td>137MHz Lock</td><td></td><td>---</td><td>---</td><td>CHECK</td></tr><tr><td>5.60</td><td>151.975MHz Lock</td><td></td><td>---</td><td>---</td><td>CHECK</td></tr><tr><td>5.70</td><td>128MHz Lock</td><td></td><td>---</td><td>---</td><td>CHECK</td></tr><tr><td>6.00</td><td>PLL current measurement</td><td></td><td>---</td><td>---</td><td>AMPS</td></tr><tr><td>6.10</td><td>PLL current calculation</td><td></td><td>0.02</td><td>0.04</td><td>AMPS</td></tr><tr><td>7.00</td><td>+5.2V current measurement</td><td></td><td>---</td><td>---</td><td>AMPS</td></tr><tr><td>7.10</td><td>+5.2V current calculation</td><td></td><td>0.06</td><td>0.10</td><td>AMPS</td></tr><tr><td>8.00</td><td>+5V-SW current measurement</td><td></td><td>---</td><td>---</td><td>AMPS</td></tr><tr><td>8.10</td><td>+5V-SW current calculation</td><td></td><td>0.04</td><td>0.07</td><td>AMPS</td></tr><tr><td>9.00</td><td>+28V Monitor</td><td></td><td>27</td><td>29</td><td>VOLTS</td></tr><tr><td>10.00</td><td>Temperature Monitor</td><td></td><td>20</td><td>30</td><td>°C</td></tr></table>						TEST NO.	DESC.	MEAS.	LIMIT-LOW	LIMIT-HIGH	UNIT	2.00	CPLD version		03h	---	0xh	3.00	T-fixture current		TBD	TBD	AMPS	4.00	UUT current measurement		---	---	AMPS	4.10	UUT initial current calculation		0.30	0.50	AMPS	5.10	108MHz Lock		---	---	CHECK	5.20	118MHz Lock		---	---	CHECK	5.30	127.975MHz Lock		---	---	CHECK	5.40	128MHz Lock		---	---	CHECK	5.50	137MHz Lock		---	---	CHECK	5.60	151.975MHz Lock		---	---	CHECK	5.70	128MHz Lock		---	---	CHECK	6.00	PLL current measurement		---	---	AMPS	6.10	PLL current calculation		0.02	0.04	AMPS	7.00	+5.2V current measurement		---	---	AMPS	7.10	+5.2V current calculation		0.06	0.10	AMPS	8.00	+5V-SW current measurement		---	---	AMPS	8.10	+5V-SW current calculation		0.04	0.07	AMPS	9.00	+28V Monitor		27	29	VOLTS	10.00	Temperature Monitor		20	30	°C
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10.00	Temperature Monitor		20	30	°C																																																																																																																									
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UNIT CALIBRATION <table><tr><td>TEST NO.</td><td>DESC.</td><td>MEAS.</td><td>LIMIT-LOW</td><td>LIMIT-HIGH</td><td>UNIT</td></tr><tr><td>11.00</td><td>Driver Bias Current</td><td></td><td>0.70</td><td>0.80</td><td>AMPS</td></tr><tr><td>11.00</td><td>Driver Bias Adjust</td><td></td><td>---</td><td>---</td><td></td></tr><tr><td>12.00</td><td>Final Bias Current</td><td></td><td>1.45</td><td>1.55</td><td>AMPS</td></tr><tr><td>12.00</td><td>Final Bias Adjust</td><td></td><td>---</td><td>---</td><td></td></tr><tr><td>13.00</td><td>Buffer Current</td><td></td><td>0.40</td><td>0.55</td><td>AMPS</td></tr><tr><td>14.00</td><td>Pre Driver Current</td><td></td><td>0.40</td><td>0.55</td><td>AMPS</td></tr></table>								TEST NO.	DESC.	MEAS.	LIMIT-LOW	LIMIT-HIGH	UNIT	11.00	Driver Bias Current		0.70	0.80	AMPS	11.00	Driver Bias Adjust		---	---		12.00	Final Bias Current		1.45	1.55	AMPS	12.00	Final Bias Adjust		---	---		13.00	Buffer Current		0.40	0.55	AMPS	14.00	Pre Driver Current		0.40	0.55	AMPS
TEST NO.	DESC.	MEAS.	LIMIT-LOW	LIMIT-HIGH	UNIT																																												
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	UNIT CALIBRATION									
	TEST NO.	DESC.	MEAS.	LIMIT-LOW	LIMIT-HIGH	UNIT				
	16.11	Audio Frequency @112MHz		990	1010	HZ				
	16.12	Power Output @112MHz		17	19	WATTS				
	16.13	Power Output @112MHz		21	23	WATTS				
	16.14	1kHz SINAD @112MHz		34	---	dB				
	16.15	AM%, +pk @112MHz		65	75	%				
	16.16	AM%, -pk @112MHz		65	75	%				
	16.17	FM @112MHz		---	TBD	HZ				
	16.21	Audio Frequency @118MHz		990	1010	HZ				
	16.22	Power Output @118MHz		17	19	WATTS				
	16.23	Power Output @118MHz		21	23	WATTS				
	16.24	1kHz SINAD @118MHz		34	---	dB				
	16.25	AM%, +pk @118MHz		65	75	%				
	16.26	AM%, -pk @118MHz		65	75	%				
	16.27	FM @118MHz		---	TBD	HZ				
	16.31	Audio Frequency @123MHz		990	1010	HZ				
	16.32	Power Output @123MHz		17	19	WATTS				
	16.33	Power Output @123MHz		21	23	WATTS				
	16.34	1kHz SINAD @123MHz		34	---	dB				
	16.35	AM%, +pk @123MHz		65	75	%				
	16.36	AM%, -pk @123MHz		65	75	%				
	16.37	FM @123MHz		---	TBD	HZ				
	16.41	Audio Frequency @133MHz		990	1010	HZ				
	16.42	Power Output @133MHz		17	19	WATTS				
	16.43	Power Output @133MHz		21	23	WATTS				
	16.44	1kHz SINAD @133MHz		34	---	dB				
	16.45	AM%, +pk @133MHz		65	75	%				
	16.46	AM%, -pk @133MHz		65	75	%				
	16.47	FM @133MHz		---	TBD	HZ				
	16.51	Audio Frequency @138MHz		990	1010	HZ				
	16.52	Power Output @138MHz		17	19	WATTS				
	16.53	Power Output @138MHz		21	23	WATTS				
	16.54	1kHz SINAD @138MHz		34	---	dB				
	16.55	AM%, +pk @138MHz		65	75	%				
	16.56	AM%, -pk @138MHz		65	75	%				
	16.57	FM @138MHz		---	TBD	HZ				

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REV LTR						
PART NO. 7026236-_____SERIAL NO. _____						
UNIT CALIBRATION						
TEST NO.	DESC.	MEAS.	LIMIT-LOW	LIMIT-HIGH	UNIT	
16.61	Audio Frequency @145MHz		990	1010	HZ	
16.62	Power Output @145MHz		14	16	WATTS	
16.63	Power Output @145MHz		16	18	WATTS	
16.64	1kHz SINAD @145MHz		30	---	dB	
16.65	AM%, +pk @145MHz		65	75	%	
16.66	AM%, -pk @145MHz		65	75	%	
16.67	FM @145MHz		---	TBD	HZ	
16.71	Audio Frequency @151.975MHz		990	1010	HZ	
16.72	Power Output @151.975MHz		14	16	WATTS	
16.73	Power Output @151.975MHz		16	18	WATTS	
16.74	1kHz SINAD @151.975MHz		30	---	dB	
16.75	AM%, +pk @151.975MHz		65	75	%	
16.76	AM%, -pk @151.975MHz		65	75	%	
16.77	FM @151.975MHz		---	TBD	HZ	
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REV LTR						
APPENDIX B CONVENIENCE PRE-TEST PROCEDURE (to be done before installing cover (7026228-2) or heatsink (7026215-902) to CCA)						
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REV LTR				
Appendix A Convenience Pre-Test Procedure (to be done before installing cover (7026228-2) or heatsink (7026215-902) to CCA) Set the Bench Power Supply DC Volts to 28 and the DC Current Limit to 2.5 Amps. 28VDC SW OFF (Power off on TEST STAND, Run SW in Center - Program) - Place a CCA insulator in the Test Stand cradle to prevent CCA from shorting to metal. - Place the UUT (236-902) CCA on the stand on insulator and connect P1 - Make sure RUN SW is in Program Position (Centered). - Turn on 28VDC Switch and observe the Test panel LEDS. Press Clear Trip if needed. - Remove the EMI Jumper on the end of the Test Panel. - Connect the JTAG Programming Cable to J2 on the TX CCA. - Use the Mouse Double-click to open the Xilinx JTAG Programmer ICON. - Select <u>FILE</u>, then <u>Initialize Chain</u> (Ctrl+I , Then double click ICON and Browse for file = VHFTX (3).jed .Select it.(Double Click) - Select <u>Operations</u>, Then <u>Program</u> and wait until it finishes. Click OK - Select <u>Operations</u>, then <u>Get Device Checksum</u>. When complete, it should return "4D57". Click OK. Close the Xilinx App. When done, DO NOT save. - Remove the J2 Programming Plug from P2. - Start the Digital Radio Card Test program. IF RX/TX Status is RED Click Transmit 2X to Clear. - Put RUN Switch up. Clear RED LED trips if any are lit. - Click Reinitialize. LO and 5.2V S/B enabled. ALL Status Buttons on CRT S/B GREEN=OK. - Set Freq. at 127.975 MHz. Clear trips if any are lit. All Test Stand LEDS S/B Green, too.... - Check(Ver = 003) & Check 8 Monitor Values for Nominal Values except 28VDC= ~ 1 VDC				
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REV LTR	Digital Pot Adjustments. 18. Click ALL POWER ON. (IN CW mode the Loop Enable will be OFF) 19. Click on Initialize FINAL Bias. Button Turns Blue. Using mouse pointer and left button, Slide Pot and with a DC Voltmeter read DC Volts at gate of Q4. DC Volts Should be adjustable from = 0 to about +5.2. Click Initialize again and the Complete Bar will illuminate Blue. 20. Click on Initialize DRIVER Bias. Button Turns Blue. Again, adjust slide pot and with a DC Voltmeter read DC Volts at gate of Q3. Should be adjustable from = 0 to about +5.2V. Click Initialize again and the Complete Bar will illuminate Blue. 21. Turn on 3rd Buffer, click TX ON and observe that DC current is now 430 to 450 ma higher 22. Turn off 3rd Buffer and turn on Pre-Driver. Click TX ON and observe 430 to 450 ma increase. 23. Click Transmit OFF. Turn OFF the Pre-Driver. 24. Adjust the RF Power Slider and read DC voltage at R82. Should change between Zero (0) and about +4V. Leave at a setting of 150. (About 2.1VDC Typical) 25. Adjust the FWD Power Slider and measure the DC Volt Change at R181 (bottom of CCA) or at U24-7 (top of CCA) Range about +5.2 to about 0.5VDC. Leave Pot at Zero (0)
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REV LTR	VCO Tests. 26. To Measure LoVCO Voltage at 108 MHz, Select VDB Button. (LoVCO will be enabled.). 27. Set TX Frequency to 108. Measure VCO Tuning Voltage at U40-1. (It is on the CCA Bottom near the metal VCO cover.) S/B about +1.80 V. +/- .5V Select 25KHz Button. 28. Set Freq. To 127.975 MHz. Measure VCO Tuning Voltage at U40-1, S/B 9.8 to 11.4 VDC. 29. To measure HiVCO Tuning Voltage, Set Freq to 128.05 MHz. Hi VCO will be enabled. Measure the VCO Tuning voltage at U40-1, S/B +1.9 to 2.5VDC. 30. Set Freq. To 151.975 MHz. Measure VCO Tuning Volts, S/B 9.0 to 11VDC 31. Set Freq. To 127.975 MHz, (LoVCO will be Enabled) RF Slider should be at 150 nominal. Modulator Tests. 32. With W/B O'Scope Measure VMOD. (top of CCA) at U2-8 and at U2-7, S/B 1 VPP on DC offset of ~1.0 VDC and identical at both points. 33. Click ☐ ALL Bias and Amps ON. Key Transmit With W/B (350MHZ) O'Scope and 10X Probe, measure Modulated RF at Q3 Gate. Should Be ~1 to 3VPP. A DC Offset will be present if the Driver Bias is not at Zero(0). Click ☒ Loop Enable ON, Signal Amplitude should Double At Least. Click Loop Enable OFF. 34. Select 128.05MHz. With O'Scope Measure Signal @ Q3 Gate. S/B 1-3 VPP Modulated RF. 35. CCA Pre-Tests are Complete. Turn off RUN Sw and then 28VDC Switch. Then Remove J1-P1. 36. Close DRCT program-No Save. Complete ITA Entry for CCA.= P-Test F.-OK.						
	<table border="1"> <tr> <td data-bbox="94 1822 570 1976" rowspan="2">  </td> <td colspan="2" data-bbox="570 1822 1528 1883">AW/CRITICAL NOTATION</td> </tr> <tr> <td data-bbox="570 1883 954 1976">SECURITY NOTATION</td> <td data-bbox="954 1883 1528 1976"> SUPPLEMENTS B-3 PAGE </td> </tr> </table>				AW/CRITICAL NOTATION		SECURITY NOTATION
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	SECURITY NOTATION	SUPPLEMENTS B-3 PAGE					