GLOCOM

DOCUMENT:	GL1.201.032-0-001-HRD
REVISION:	2.0
PROGRAM:	GCM-P46
DATE:	April 17, 2002

Aero-M4 MES Development Program

Core Aero-M4 MTU
Radio Module Hardware Specification

Issue 2.0

Glocom Corporation
Suite 300, 20010 Century Boulevard
Germantown, MD 20874

Glocom Corporation Proprietary
This document is proprietary to Glocom Corporation. Use or disclosure of this document or the information contained herein, for any purpose other than internal division use, is not permitted without prior authorization of Glocom Corporation.

Revision History

Design Document Name: Core Aero-M4 MTU Radio Module Hardware Specification			
Revision	**Description**	**Approval**	**Date**
DRAFT	Requirements Issue 1.0	G.E. Hosimer	May 8, 2000
1.0	Block diagram updated, Tables added. (Minheng Shan)	G.E. Hosimer	September 11, 2000
1.1	Pre-CDR reconciliation with schematics	G.E. Hosimer	October 17, 2000
1.2	Updated after Internal CDR	G.E. Hosimer	December 8, 2000
1.3	a) Change document number; From: GL1.201.032.002-HRD To: GL1.201.032-0-001-HRD b) Correct design document references in Section 1.4. c) Resolve various TBD's, TBR's, and TBA's throughout the body of the text.	G.E. Hosimer Minheng Shan	February 20, 2001
2.0	Update design detail information for FCC	G.E. Hosimer	April 17, 2002

Document Attributes:

File Name: HRD - RM 2.0
File Size: 955904 bytes

The use or disclosure of this information is subject to the restrictions on the title page.

Table of Contents

The use or disclosure of this information is subject to the restrictions on the title page.

The use or disclosure of this information is subject to the restrictions on the title page.

List of Figures

List of Tables

The use or disclosure of this information is subject to the restrictions on the title page.

1 Introduction

1.1 Purpose

The Core Aero-M4 Radio Module (RM) Hardware Specification, also referred to as the RM HRD (Hardware Requirements Document), is intended only for internal use at Glocom for product and design engineers in the design and application of the RM.

1.2 Scope

This document is a design specification detailing the hardware functions and parameters of the Aero-M4 Radio Module including information required for product application and the design of the module, and defines all the parameters necessary to interface with the DM software [4]. The overview section describes the Radio Module in terms of its origin, major functions, and general operation. The functional requirements section describes the RM functional elements in terms of the selected hardware implementation and basic operation. The interface section describes internal and external hardware interfaces and software interfaces including information for programming hardware elements. The performance section includes the parameters to which the RM design must adhere. The sections that include mechanical, environmental, manufacturing, installation, and maintenance describe additional hardware design requirements.

1.3 Conformance

This document conforms to [6] and [5].

1.4 References

The following references are related to the contents of this document.

[1] "Technical Requirements Document for the Functional Core Aero M4 MES Transceiver Unit (MTU)", GL1.201.032-0-000-TRD, Glocom Corporation.

[2] "ICD for the Functional Core Aero-M4 MTU", GL1.201.032-0-005-ICD, Glocom Corporation.

[3] "Core Aero-M4 MTU Digital Module Hardware Specification", GL1.201.032-0-011-HRD, Glocom Corporation.

[4] "Software Requirements Document for the Core Aero-M4 MTU", GL1.201.032-0-006-SRD, Glocom Corporation.

[5] "Design Control System Procedure", GCM-DGP-1001, Glocom Corporation.

[6] "Product Design Documentation", GCM-CGP-1011, Glocom Corporation.

[7] "LF to 2.5GHz TruPwr™ Detector", Data Sheet for AD8361, Analog Devices, 1999.

[8] "5-2000MHz Medium Power GaAs HBT Amplifier", Data Sheet for SXA-289, Stanford Micro Devices.

[9] "SXA/SXT-289 New Bias Scheme", Product Update, August 24, 2000, Stanford Micro Devices.

The use or disclosure of this information is subject to the restrictions on the title page.

[10] "Single- and 4-Channel, 9µs, 10-Bit ADCs with On-Chip Temperature Sensor", Data sheet for AD7816/17/18, Analog Devices, 2000.

[11] "DC-2000MHz, Cascadable SiGe HBT MMIC Amplifier", Product Description for SGA-2486, Stanford Micro Devices.

[12] "Mixer and IF Vector Modulator - PMB 2208 Specification", Version 1.2, Infineon Technologies, 1999.

[13] "Mixer and IF Vector Modulator - Application Note for PMB 2228", Version 1.1, Infineon Technologies, 1999.

[14] "DC-6GHz High Isolation SPDT GaAs MMIC Switch", Product Description for SSW-124, Stanford Micro Devices.

[15] "Low Noise Amplifier 1.5 - 1.6GHz", Data Sheet for MAAM12021, M/A-COM.

[16] "+2.5V to +5.5V, 230µA Dual Rail-to-Rail, Voltage Output 8-/10-/12-Bit DACs", Data Sheet for AD5302/12/22, Analog Devices, 1999.

[17] "Dual Sigma-Delta ADC with Auxiliary DAC", Data Sheet for AD7729, Analog Devices, 1998.

[18] "PLLatinum™ Low Power Frequency Synthesizer for RF Personal Communications", Data Sheet for LMX2306 and LMX2326, National Semiconductor, 2000.

[19] "CMOS, 125MHz Complete DDS Synthesizer", Data Sheet for AD9850, Analog Devices, 1999.

[20] "Filters for Communication Equipment", Specification, Section 7, Murata.

The use or disclosure of this information is subject to the restrictions on the title page.

1.5 Definitions of Terms and Acronyms

Table 1-1 lists the terms and acronyms used throughout this document.

Table 1-1 Definition of Terms and Acronyms

Term	Definition
ACSE	Access Control Signaling Equipment
ADC	Analog to Digital Converter
ANSI	American National Standards Institute
ATP	Acceptance Test Procedure
BER	Bit Error Rate
BITE	Built In Test Equipment
BPSK	Binary Phase Shift Keying
BRI	Basic Rate Interface (ISDN)
BSE	Bearer Services Equipment
BSU	Beam Steering Unit
CFS	Coarse Frequency Synthesizer
CPU	Central Processing Unit
CRC	Cyclical Redundancy Check
CU	Channel Unit
DAC	Digital to Analog Converter
DC	Direct Current
DDS	Direct Digital Synthesis
D/LNA	Diplexer-LNA
DM	Digital Module
DPLL	Digital PLL
DRD	Design Requirements Document
DSP	Digital Signal Processor
DVT	Design Verification Test
EEPROM	Electronically Erasable Programmable ROM
EIRP	Equivalent Isotropic Radiated Power
ESD	Electro-Static Discharge
FEC	Forward Error Correction
FLASH	Non-Volatile Re-programmable Memory
FPGA	Field Programmable Gate Array
FFS	Fine Frequency Synthesizer
G/T	Gain-to-Noise Temperature Ratio; the figure of merit
HPA	High Power Amplifier
HTRF	Host terminal RF Equipment
HTCE	Host Terminal Control Equipment
HSD	High Speed Data (≥64 Kbps)
HW	Hardware
ICE	In Circuit Emulator
IDU	In Door Unit
ITP	Integration and Test Plan
I/O	Input/Output
IEEE	Institute Electronic/Electrical Engineers
IF	Intermediate Frequency
IPDS	Inmarsat Packet Data Services
ISDN	Integrated Services Digital Network
IRQ	Interrupt Request
ITU	International Telecommunication Union
LAN	Local Area Network
LED	Light Emitting Diode
LES	Land Earth Station
LMT	Land Mobile (Class) Terminal
LNA	Low Noise Amplifier
LP	Link Processor
N_F	Noise Figure
NVRAM	See FLASH
MAC	Media Access Control (protocol)
M&C	Monitor and Control
MIPS	Million Instructions Per Second
MMI	Man Machine Interface
MTBF	Mean Time Between Failures
MTTR	Mean Time to Replace
MTU	MES Transceiver Unit
MUX	Multiplexer
O&M	Operations and Maintenance
ODU	Out Door Unit
PC	Personal Computer
PCM	Pulse Coded Modulation
PLL	Phase Locked Loop
POTS	Plain Old Telephone Service
PSC	Power Splitter/Combiner
QA	Quality Assurance
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RAM	Random Access Memory
RF	Radio Frequency
RM	Radio Module
ROM	Read Only Memory
RX	Receive
SNR	Signal-to-Noise Ratio
SN	Serial Number
SATCOM	Satellite Communications
SCC	Serial Communications Controller
SCPC	Single Carrier Per Channel
SDL	Specification and Description Language
SDRAM	Synchronous Dynamic RAM
SLIC	Subscriber Line Interface Circuit
SRD	Software Requirements Document
SU	Signaling Unit
SW	Software
TRD	Technical Requirements Document
TX	Transmit

The use or disclosure of this information is subject to the restrictions on the title page.

Term	Definition
UART	Universal Asynchronous Receiver Transmitter
V	Volt
V-A	Volt Ampere
V_{AC}	Voltage Alternating Current
V_{DC}	Voltage Direct Current
VSWR	Voltage Standing Wave Ratio
W	Watt

The use or disclosure of this information is subject to the restrictions on the title page.

2 Overview

The Radio Module component when combined with the Aero-M4 Digital Module [3] comprises the Aero-M4 MES Transceiver Unit (MTU) [1].

2.1 Radio Module Description

The Radio Module design is based on the Reference Designs ODU RF board and comprised of the two major sections as shown in Figure 2-1, the L-Band RF Section and the IF Section. In addition, the Radio Module design includes frequency synthesizers, filters, and up/down converters for the Tx and Rx paths respectively. The Radio Module interfaces with the Digital Module (see section 4.1.1), and HTRF equipment that includes a power splitter/combiner, LNA/Diplexer, and HPA.

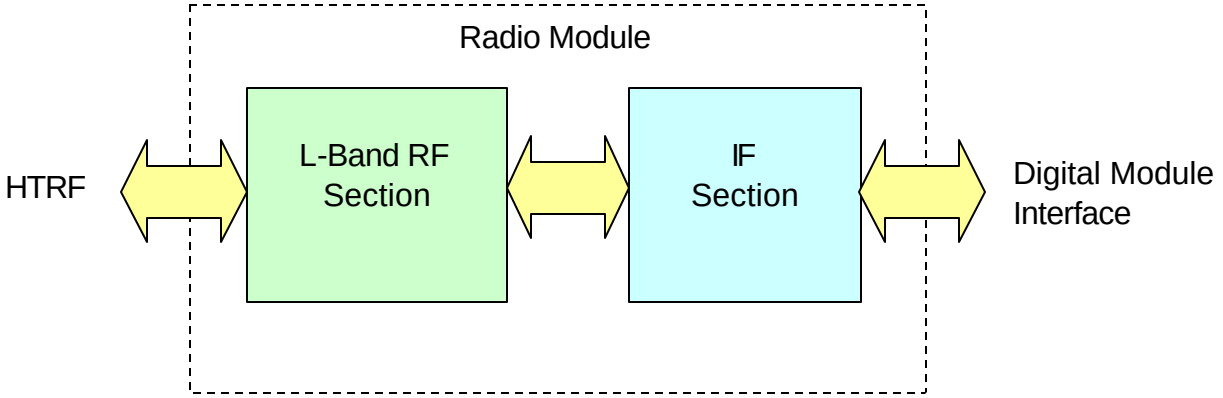

Figure 2-1 Major Functional Sections of the Radio Module.

2.1.1 General Architecture

The functional architecture of the Radio Module is the same, as that of the Reference Design with a few exceptions. Generally, the RM comprises four local oscillators implemented by four independently tunable frequency synthesizers, two for the receiver and two for the transmitter. From IF, Rx gain control amplifier adjusts the Rx signal amplitude before being applied the quadrature demodulator.

2.1.1.1 *RF Section*

The RF section comprises the TX and RX front-end circuitry. The TX front-end circuits include the final output power amplifier (TX PA), RF filters, coarse step frequency synthesizer (TXCFS), variable gain controlled amplifier, and the up-converter. The RX front-end circuits include the RX coarse step frequency synthesizer (RXCFS), the input power control, RX RF filters, AGC, and the down-converter. The RF section interfaces with the HTRF equipment at L-Band.

RX signal from the HTRF LNA, referred to as RXRF, is adjusted to the input level according to the configuration requirements of the HTRF equipment. The RXRF variable gain amplifier is set to static level during the initial system calibration upon at MTU installation and is available to assist the AGC amplifier during normal MTU operation to compensate for the additional dynamic range due to different installation configurations. The RXRF is down-converted to RXIF with the first LO from the RXCFS. The DM controls the variable gain amplifier, AGC, and RXCFS. This architecture down converts the input signal to a fixed IF band allowing the use of a narrow band SAW filter (with flat Group Delay

The use or disclosure of this information is subject to the restrictions on the title page.

performance and low insertion loss from 3~6dB) to suppress the maximum composite signal and provide 10 to 15dB dynamic range to the demodulator.

Each L-band modulated signal type is output to the HTRF HPA, referred to as the TXRF, the transmission power level is controlled according to the physical layer transmission requirements of the associated communications channel. The TXRF output signal power is measured using a power detector that provides measurement data to the DSP on the DM. The DSP power control algorithm closes the power control loop by adjusting the output power level according to the data stored in a gain curve compensation table that stores the unique characteristics of each RM assembly. Since temperature is an important operational parameter of the transmit power control algorithm the RM's temperature is monitored near the TX PA. The power control algorithm tests the temperature measurement against predetermined operating limits and if violated will indicate a hardware fault. When the TXRF is off, the DM puts the TX PA stage to 'sleep' to suppress any potential carrier leakage. Three cascaded SAW filters suppress the broadband noise of the modulator and other the lower noise floor devices like the mixer and TX amplifiers. Up-converting the TXIF using the TXCFS sets the TXRF frequency. The TXCFS is also controlled via the DM.

2.1.1.2 *IF Section*

The functions of the IF section include of the quadrature modulator, IF channel detector/demodulator, TX and RX fine step frequency synthesizers (TXFFS, RXFFS), and the TX and RX data converters that are controlled via the Digital Module interface.

RXIF signals from the RXRF front-end are translated to quadrature baseband signals RXI and RSQ, by the IF channel detector/demodulator at the selected IF channel frequency set by the RXFFS. Both RXI and RXQ are filtered and digitized by the RX data converter and provided to the DSP via the DM interface. DC offsets on RXI and RXQ are compensated for using bias adjustments that are controlled by the DM's DSP. The RXFFS is also controlled via the DM.

The TX data converter translates the TX digital baseband signals provided by the DM to analog TXI and TXQ for input to the quadrature modulator. The TXIF modulated output channel frequency is set by the TXFFS and provided to the TXRF front-end. The TXFFS is controlled via the DM to set the TX channel frequency and provide TX Doppler frequency compensation.

The use or disclosure of this information is subject to the restrictions on the title page.

2.2 Design Changes

The Radio Module design leverages the core RF circuitry from the Reference Designs ODU with changes that remove, add, and/or modify various functions and the impact of each of these design changes is listed in the last column summarized in Table 2-1.

Table 2-1 Summary of Design Changes comprising the Radio Module.

Gemini-128 Terminal	Aero-M4 Radio Module Changes	Design Impact
Reference oscillator w/10MHz PLL	External High Stability 10MHz OCXO	Add input buffer and distribution circuitry to provide signal to Digital Module.
HPA	Customer Provides external HPA	None
LNA/Diplexer	Customer Provides external LNA/Diplexer	None
Sleep Mode	Deleted	Disable former control lines to affected components.
Transmit frequency step size	1Hz Step added using DDS in the TXFFS for Doppler frequency control	DDS programming added to DSP SW and interface control circuit to FPGA.
DAC and ADC data converters	Move from ODU digital board to RM and delete AD5541 16bit DAC	Buffer the data signals on the Digital Module interface to assure drive capability and noise immunity.
Transmitter output dynamic range	Add TXRF front-end power amplifier	Provide increased output power to meet extended range and dynamic power control requirements
Power Detector	Move from ODU HPA output to RM PA output	Measures output signal from TX PA. TX path circuit variations over increased operating range compensated for by new correction tables in DSP SW.
Temperature Sensor	Move from ODU HPA case to RM	Limited operating range mapped to fault detection logic.
SELF TEST	RF Loopback added with TX output inhibit	TXCFS programming change to generate compatible receive frequency. Other signals added under SW control to configure loopback operation.
Receiver input dynamic range	Add 20dB variable attenuator or variable gain element	CGY-120 type used on TX side has known characteristics.
Environmental	Add TX/RX RF Input/Output Lightning Protection	Short circuit stub added.

The use or disclosure of this information is subject to the restrictions on the title page.

3 Functional Requirements

This section defines all the functional design requirements for the Aero-M4 Radio Module. A detailed functional block diagram of the RM is shown in Figure 3-1.

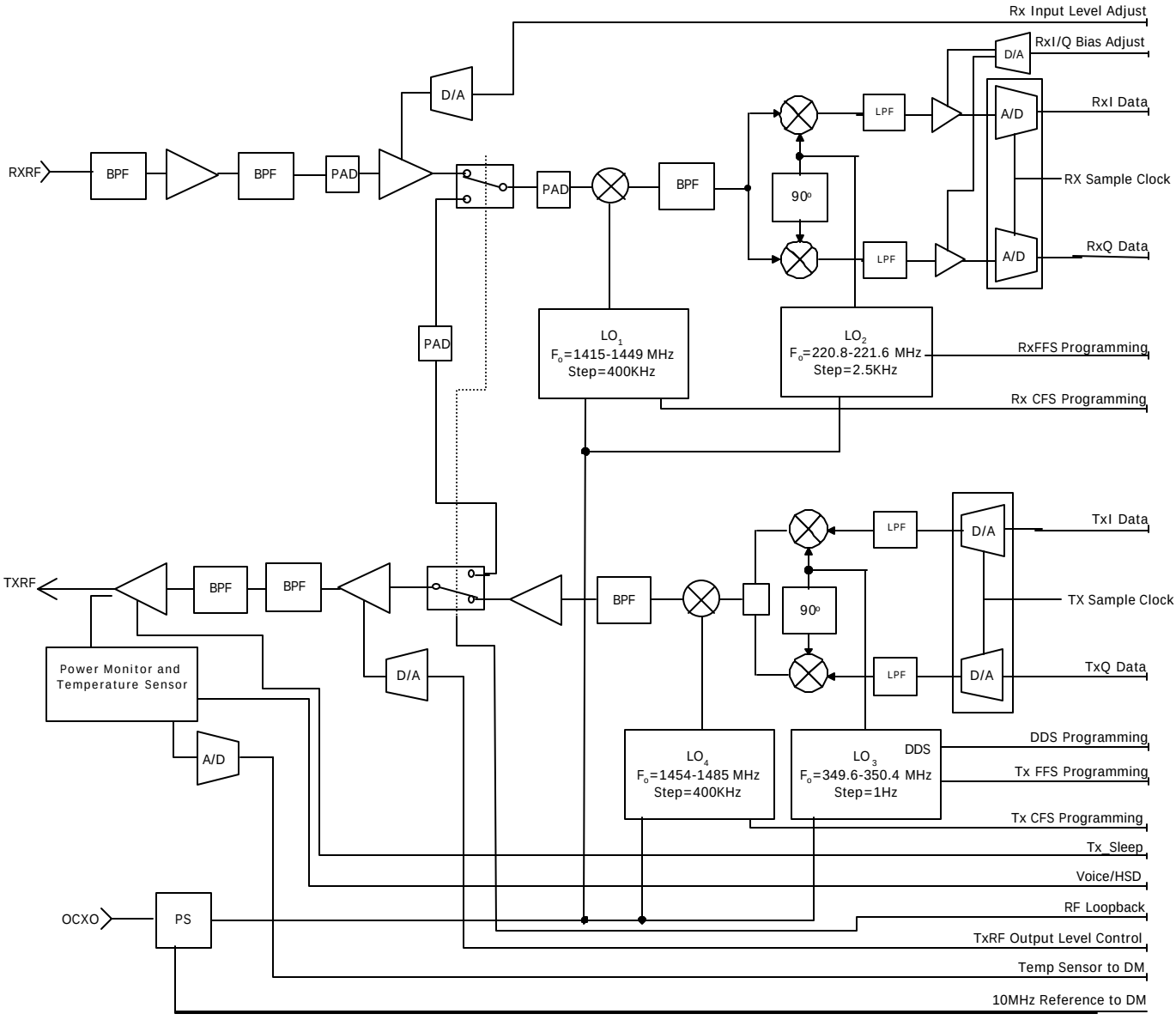

Figure 3-1 Detailed Block Diagram of Radio Module.

The use or disclosure of this information is subject to the restrictions on the title page.

3.1 Aero M4 Requirements

The new Aero M4 functions to be performed by the Radio Module are summarized in Table 3-1. These functions are in addition to the standard terminal functions performed by the baseline M4 terminal design.

Table 3-1 New Aero M4Functions Performed on the Radio Module.

Basic M4 Function	Aero M4 Software	Aero M4 Hardware
Baseband Analog Interface		Digital Interface
Power Control 2dB step	Dynamic Power Control, 0.5dB step	0.1dB step
	Doppler Compensation	DDS device - AD9850
Tx Power Control Range 6dB		Power Control Range 20dB
Tx Fine Synthesizer Step 2.5KHz		DDS control synthesizer, step size 1Hz.
		RF Loop Back

3.2 Hardware Requirements

The hardware requirements for the RM are described in this section for the major functional elements consisting of the RXRF Front-End, TXRF Front-End, IF detector, modulator, the DM interfaces, and the HTRF interface. The following sections describe the hardware requirements for these functional elements. The key components that comprise these RM functional elements are summarized in Table 3-2.

Table 3-2 Key Components of the Radio Module Design.

Function	Component Manufacturer	Description	Notes
LNA	MAAM12021	MA-Com LNA	
Rx VGA	CGY120	Siemens Variable Gain Amplifier	Replaced MAAM12021 but now obsolete - superceded by CGY-121
Down Converter	PMB2411	Siemens Single Chip Receiver	Included in demodulator chip
RX IF Filter	SAFU110.6	Murata SAW Filter	
Demodulator	PMB2411	Siemens Single Chip Receiver	
Rx Baseband LPF	OPA2340	Burr brown OPA	
Tx Baseband LPF	OPA2340	Burr brown OPA	Remove one gain stage and change component values.
Modulator	PMB2208	Siemens Modulator Chip	
Tx IF Filter - 175MHz	SAWTEK854622	SAWTEK SAW Filter	
Up Converter	CMY210	Siemens mixer	
Tx Fix Gain Block	SGA2486	Stanford Micro devices	
Tx VGA	CGY120	Siemens Variable Gain Amplifier	
Tx Output Amplifier	SXA-189	Stanford Micro devices	Replaced SGA6486
RF Switch	SSW-124	Stanford Micro devices	Obsolete - no substitute available
Synthesizer	LMX2306/2326	National Semiconductor	
TX/RX VCO	CLV1425/1455	Z-Com VCO	
Directional Coupler	DC16-73		
Rx RF Filter	DFC31R54		
Power Detector	AD8361	Analog Devices	
Switched Attenuator	AA103-72	Stanford Micro devices	

The use or disclosure of this information is subject to the restrictions on the title page.

3.2.1 Transmitter Description

The characteristics of the RM transmitter circuitry and any departures from the Reference Design are generally described in the following sections.

3.2.1.1 *TX RF Section*

The suppression of spurious radiation rests on a foundation of stable frequency generation, adequate filtering, careful component placement and circuit layout. Refer to Figure 3-1 for the following descriptions.

3.2.1.1.1 *TX Power Sensor*

A RF power sensor constantly monitors the TX output power. The AD8361 power sensor device measures TXRF output level through a 10dB directional coupler and a 0 or 10dB switched attenuator. With the useful range of the power sensor limited to 14dB ±0.25dB and the switched attenuator makes the total TX dynamic range 24dB. The detected voltage output is then converted by 10-bit ADC (Analog Devices AD7818) and made available to the DSP via the DM interface. Based on the detected power, DSP controls a TX variable gain amplifier and achieves the desired output power within ±0.5 dB. During normal operation the DSP power control algorithm adjusts the gain of the TX Variable Gain Amplifier to stabilize the TX output power level during the initial and dynamic power control operations. During HSD operation the attenuation setting is 10dB and for Voice/Signaling operation the attenuation is 0dB.

3.2.1.1.2 *TX Power Amplifier*

The TX PA is implemented using the SXA-189 device. When the transmitter is turned off or during RF loop back testing, the 7.5~8.0Vdc supply voltage is removed via control line from the DM interface. The output P_{1dB} compression point is 8dB greater than the desired maximum nominal output power level. Maximum nominal output power level is determined as +14dBm based on anticipated losses of downstream SATCOM equipment. This operating point provides more than enough linearity to meet the spectrum mask and peak power requirements when transmitting 16-QAM. For O-QPSK and BPSK signals the transmitter operates backed off by 11dB.

3.2.1.1.3 *TX RF Filter*

The RF filter is used to filter the image frequency from the up conversion mixer in order to meet spurious emissions requirements and to attenuate noise in the receive band. One filter device of the type in Table 3-3 is used at the output of the up-converter and two are cascaded after the TX Variable Gain Amplifier. The succession of these three identical ceramic band pass filters each centered at 1643.5 MHz has a bandwidth of 34 MHz and has a suppression of 30 dB or greater outside a band of ±75 MHz from the center.

Table 3-3 TX RF Filter Specification.

Requirement	Units	Specification
Manufacturer	-	Murata
Part number	-	DFC31R64P034BHA
F_C	MHz	1643.5
F_{BW}	MHz	34
IL	dB(max)	8
Ripple	dB(max)	0.7
Stop Band	dBc/MHz	30@±75
VSWR in F_{BW}	-	2

The use or disclosure of this information is subject to the restrictions on the title page.

3.2.1.1.4 *TX RF Switch*

A new device added to the design, the TXRF switch device SSW-124 is controlled jointly by the DM's LP and DSP depending on operating modes. The RF switch serves a dual purpose to provide isolation gain to meet carrier off requirements and to support an RF LOOPBACK BITE configuration. While in the BITE configuration, the RX frequency synthesizer is tuned to a special test frequency that falls within the TX RF band. More information about the BITE operation can be found in the maintenance facilities section of paragraph 9.1.1.

3.2.1.1.5 *TX Variable Gain Amplifier*

Referring now to Figure 3-2 the TXRF output power range is achieved using a voltage controlled variable gain RF amplifier (CGY120) with usable gain control range of 30dB that is controlled by signals from the DM interface. Calibration measures are necessary to assure linearity over temperature, frequency, and dynamic range. The calibration data are stored in look up tables in the DM's DSP memory. The operating linearity of this device, selected to operate over just a 6dB range in the Reference Design is being stretched to its limits due to its wide parameter variability over temperature, frequency and unit to unit. The CGY120 part is obsolete as of 2001 and in its place the CGY121 should be used.

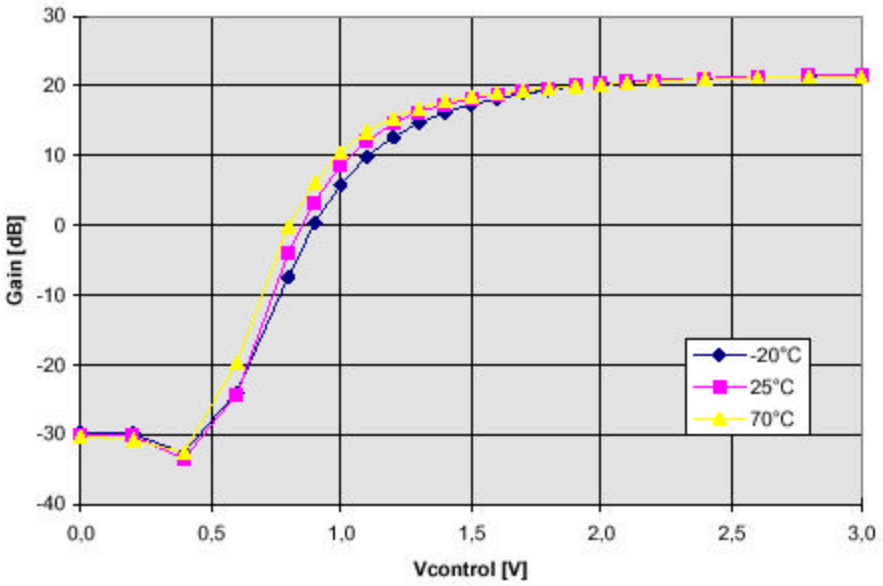

Figure 3-2 Measured VGA Gain Characteristics vs. Control Voltage

The use or disclosure of this information is subject to the restrictions on the title page.

3.2.1.1.6 *TX RF Amplifier*

A fixed gain RF amplifier is used just after the up converter using the SGA2486 device having the specifications shown in Table 3-4.

Table 3-4 TX RF Amplifier Specification

Parameter	Units	Specification
P_{1dB}	dBm	7.5
Gain	dB	17
Reverse Isolation	dB	23
Input VSWR		1.7:1
Output VSWR		1.3:1
IP_3	dBm	20
NF	dB	3.2
Power Supply	V	3.3V
	mA	20

3.2.1.1.7 *TX Operating Limits*

The DC voltages applied to and DC currents into these several elements of the transmit circuitry are summarized in Table 3-5 for normal operation over the output power range.

Table 3-5 TX Operating Power

Amplifier	DC voltage	DC current
SXA-289	7.5 V ~ 8.0 V	100 mA
CGY 120	3.4 V ~ 5.0 V	45 mA
SGA 2486	2.5 V	20 mA

3.2.1.1.8 *TX Coarse Step Frequency Synthesizer*

There are two frequency synthesizers in the transmitter: Tx coarse step frequency synthesizer and Tx fine step frequency synthesizer. Both synthesizers are phase-locked to a high-stability 10 MHz Oven Controlled Crystal Oscillator (OCXO). The main devices used in the frequency synthesizer circuit are listed in:

Table 3-6 TXCFS Components.

Device	Function	Notes
LMX2326	Frequency Synthesizer	
CLV1455	VCO	
SGA2486	Amplifier	

The frequency of the VCO, F_o, is determined by the ratio of the two dividers, N and R, in the synthesizer chip LMX2326 and the frequency of the reference source, F_i:

$$F_o = (N/R) * F_i$$

where F_i = 10 MHz, R = 25, and N = 3629 ~ 3714. The resulting frequencies are from 1451.6 MHz to 1485.6 MHz in 400 KHz steps. The VCO has extremely low phase noise and a loop filter is adjusted so that phase noise is well below the Inmarsat specifications.

The use or disclosure of this information is subject to the restrictions on the title page.

3.2.1.1.9 *Up Converter*

The up converter mixer noise will emerge in the frequency band 1559-1606MHz, where Inmarsat requires the noise emission to be < –105dBc/100kHz, if that mixers noise floor is too high. The vector modulator device PMB2208 provides an integrated up conversion mixer, The PMB2208's integrated mixer was considered for use as the up converter but has a high Noise Figure and inadequate linearity as the IP_3 output power at mixer output is only –22dBc. The Siemens CMY210 device includes a combination mixer/amplifier with a low output noise floor and a high input P_{-1dB} as specified in sufficient to use a 3-pole RF Filter characteristic.

Table 3-7 Up Converter Specification.

Requirement	Units	Specification
Manufacturer	-	Siemens
Part Number	-	CMY210
V_{dd}	V	3~6
I_{dd}	mA	7
Sleep Mode		N/A
F_{RF}	GHz	0.5~2.5
F_{LO}	GHz	0.5~2.5
F_{IF}	MHz	
LO level	dBm	0
Conversion Gain	dB	-5.5
N_F	dB(SSB)	5.5
IP3 intercept	dBm	25

3.2.1.2 *TX IF Section*

3.2.1.2.1 *TX IF Filter*

The output of the quadrature modulator at 175 MHz is filtered with the IF SAW filter specified in Table 3-8, which reduces the noise floor of the modulated carrier outside a band of ±1 MHz from the center frequency.

Table 3-8 TX IF Filter Specification.

Requirement	Units	Specification
Manufacturer		Murata
Part number		SAF175MA10T
Center Freq.	MHz	175
Band Width	MHz	0.8
Insertion Loss	dB(max)	3
Ripple	dB(max)	1.5
Stop Band	dBc/MHz	30@±1MHz

3.2.1.2.2 *Vector Modulator*

The vector modulator (PMB2208) converts baseband TXI/Q signals into a modulated single sideband carrier. Generally, the modulator provides –30dB Carrier and –40dB Sideband rejection. The N_F of the vector modulator is important, because of the QAM linearity requirement, forcing a back off level of at least 8dB from the P_{1dB} of the modulator output. According to the Inmarsat specification, the TX in-band N_F < -71dBc/100KHz thus requiring the modulator noise floor to be at least –79dBc/100KHz.

The use or disclosure of this information is subject to the restrictions on the title page.

The PMB2208 specification of includes a divide-by-two block in its LO input port that provides an accurate quadrature LO signal for the following two mixers, has superior carrier and SSB suppression values, a low input power level of about –10dBm, and low power consumption.

Table 3-9 Vector Modulator Specifications.

Requirements		Units	Specifications
Manufacturer			Siemens
Part Number			PMB2208
V_{dd}		V	2.7~4.5
I_{dd}		mA	12
Modulator	F_{IF}	MHz	100~275
	F_{LO}	MHz	2xIF
	F_{BB}	MHz	0~10
	Carrier Suppression	dBc@1V_{pp}	48
	SB suppression	dBc@1V_{pp}	-49
	P_{out}	dBm@1V_{pp}	-4
	LO level	dBm	-10
	N_F	dBc/Hz	-144
Up Converter	F_{RF}	GHz	0~2.5
	F_{LO}	GHz	0~2.5
	F_{IF}	MHz	0~2500
	LO level	dBm	0
	Conv. Gain	dB	3
	N_F	dB	8 (DSB)
	IP3 intercept	dBm	3

For equipment employing digital modulation techniques, a detailed description of the modulation system to be used, including the response characteristics (frequency, phase and amplitude) of any filters provided, and a description of the modulating wave train, shall be submitted for the maximum rated conditions under which the equipment will be operated. The transmitter may employ two different modulation schemes, BPSK at 3 K symbols per sec (Ksps), and 16-QAM at 33.6 Ksps.

3.2.1.2.2.1 *BPSK Modulation*

The 3 Ksps BPSK is generated in DSP. Its basic pulse is the square pulse at the output of DAC. Its higher order spectral components are suppressed by LPF_1 and LPF_2, which are 4-pole Butterworth filters with 3dB frequencies at 38KHz.

3.2.1.2.2.2 *16-QAM*

The I- and Q-channel signals of the 33.4 Ksps 16-QAM are generated in DSP. The symbols are filtered with commonly used **root-raised-cosine** filter with 3dB frequency of 16.7 KHz and a roll-off factor of 0.25. The filter is implemented as a Finite-Impulse-Response (FIR) filter with zero group delay in DSP. Stop-band starts at 21 KHz and is attenuated by 40 dB. The 4-pole Butterworth filters in the baseband further filter the outputs of the DAC to suppress harmonics.

3.2.1.2.3 *TX Fine Frequency Synthesizer*

The TXFFS tunes the frequency within the 400KHz of the coarse synthesizer step size. Inmarsat system channel spacing of 2.5KHz includes a 1.25KHz shift. The TXFFS provides the channel tuning function. Furthermore, to perform the Doppler Compensation function, the TXFFS includes a step size less than

The use or disclosure of this information is subject to the restrictions on the title page.

1Hz performed by a DDS device AD9850. With 32 bits of frequency tuning, its input clock is around 87.5MHz, and output of about 20MHz resulting in a step size less than 0.5Hz.

Table 3-10 TXFFS Components.

Device	Function	Notes
LMX2306	Frequency Synthesizer	
CLV1425	VCO	
AD9850	Direct Digital Synthesizer (DDS)	
MC12095	Divider (by 4)	

The frequency of the VCO is determined by the ratio of the two dividers, *N* and *R*, in the synthesizer chip LMX2306, the frequency of the reference source, F_i, and a 32-bit fractional number, $D \bullet 2^{-32}$:

$$F_o = 4 \times 4 \times (1/ D \bullet 2^{-32}) \times (N/R) \times F_i$$

Where F_i = 10 MHz is the reference clock and the other parameters, *N*, *R* and *D*, are chosen to minimize the discrete phase noise. The frequency of the VCO F_o, is in the range from 1398.4MHz to 1401.6MHz. The clock F_o, is first divided by 4 and then halved in the Modulator (PMB2208). The resultant clock has a range from 174.8 MHz to 175.2 MHz with a resolution better than 1Hz.

3.2.1.2.4 *Tx Baseband Filter*

The bandwidth of the modulated carrier baseband signals are limited by two LPFs and the TX baseband shaping filters implemented in executable DSP SW. The two LPFs are of 4-pole Butterworth design with 3dB frequency = 38KHz, one each on I-channel and Q-channel in the baseband, suppress the sampling clock and the harmonics out of the Digital-to-Analog Converters.

3.2.1.2.5 *TX Data Converter*

Refer to section 4.1.1.1.

The use or disclosure of this information is subject to the restrictions on the title page.

3.2.2 Receiver Description

The characteristics of the RM transmitter circuitry and any departures from the Reference Design are generally described in the following sections.

3.2.2.1 *RX RF Section*

The RX RF input signals to the RM are buffered by the HTRF equipment, the antenna, D/LNA, and PSC devices, even though, the RM RX RF path have been selected to experience minimal damage when subjected to abnormal input conditions of high power, lightening, etc. Through adequate filtering, careful component placement and circuit layout, the receiver is well isolated from its transmitter. Refer to Figure 3-1 for the following descriptions.

3.2.2.1.1 *RX RF Filter*

Although out-of-band noise and interference are suppressed by the diplexer, the D/LNA will amplify large amplitude signals and limit dynamic range of the receiver. Therefore, two RF filters are employed at the RX front end to improve the receivers' dynamic range, one at the RM input and the other just after the LNA.

Table 3-11 RX RF Filter Specifications.

Requirement	Units	Specification
Manufacturer		Murata
Part number		DFC31R54P034BHA
F_C	MHz	1542
F_{BW}	MHz	34
IL	dB(max)	3
Ripple	dB(max)	0.9
Stop Band	dBc/MHz	30@+/-85
VSWR	max	2

3.2.2.1.2 *RX Low Noise Amplifier*

This LNA block does not require a low noise figure as the RX RF signal is preceded by the external D/LNA. This device has a P_{1dB} compression point of +6dBm; a high enough gain and low enough noise figure to limit the noise contributions of subsequent RX gain stages. Key characteristics are shown in Table 3-12.

Table 3-12 LNA Specifications.

Requirement		Units	Specification
Manufacturer		-	M/A-COM
Part Number		-	MAAM12021
V_{dd}		V	4.5
I_{dd}		mA	8
LNA	F_{RF}	GHz	1.5 ~ 1.6
	N_F	dB	1.55 - 1.9
	Gain	dB	21
	P_{1dB}	dBm	6

3.2.2.1.3 *RX Variable Gain Amplifier*

This RX Variable Gain Amplifier (VGA) uses the same RF component (CGY120) as the TX Variable Gain Amplifier to cope with the wide dynamic range at the RX input to compensate for the operating and

The use or disclosure of this information is subject to the restrictions on the title page.

installation provisions and to preserve adequate linearity. Gain control is provided as described in sections 4.1.1.4 and 4.1.1.5. The gain vs. control voltage curve is shown in Figure 3-2.

3.2.2.1.4 *RX RF Switch*

As in the TX section, this is a new component added to the Reference Design. To invoke loop back the receiver down converter LO frequency can be tuned 101 MHz higher than normal to receive the loop back signal coming from TX section. The SPDT switch (SSW-224) is controlled via signals from DM interface. See the maintenance facilities described in paragraph 9.1.1.

3.2.2.1.5 *RX Coarse Step Frequency Synthesizer*

Like the TXCFS the RXCFS has a step size of 400KHz with a tuning range from 1414.4MHz to 1448.4MHz and provides an output signal level of about –4dBm. The method of frequency tuning is about the same as the TXCFS described in section 3.2.1.1.8 except for different values of *N* and *R*.

3.2.2.1.6 *Down Converter*

The down converter is part of the PMB2411 quadrature demodulator device and has the specifications defined by Table 3-13.

Table 3-13 Down Converter Specifications.

Requirements		Units	Specification
Manufacturer			Siemens
Part Number			PMB2411
V_{dd}		V	3.3
I_{dd}		mA	
Down Conv.	Conv. Gain	dB	10
	N_F	dB	13
	P_{1dB}	dBm	-14
	IIP3	dBm	-2
	F_{RF}	GHz	<2.5
	F_{IF}	MHz	40~460
	LO level	dBm	-4

3.2.2.1.7 *RX Image Filter*

This filter rejects of out-of-band interference and attenuates noise from the RX front end amplifier stages at the image frequency. The very tight Noise Figure specifications require the image noise from the Gain RX Block be <10dB relative attenuation easily achievable using a Murata 3 pole ceramic filter as specified in Table 3-14.

Table 3-14 RX Image Filter Specifications.

Parameter	Units	Value
Center Freq.	MHz	1542
Band Width	MHz	34
Insertion loss	dB(max)	3
Ripple	dB(max)	0.9
Stop Band	dBc@MHz	30@±85
VSWR	max	2
Impedance	ohm	50

The use or disclosure of this information is subject to the restrictions on the title page.

3.2.2.2 *RX IF Section*

3.2.2.2.1 *RX IF Filter*

The channel selectivity for the 16-QAM signal is established by the LPF after the down converter. Channel selection for the narrow band 2.5KHz signals are established in the executable DSP software as a digital filter. Therefore, the bandwidth of the IF filter is not very critical and only provides about 15dB suppression against the maxim composite signal.

Table 3-15 RX IF Filter Specifications.

Requirement	Units	Specification
Manufacturer		Murata
Part number		SAFU110.6MSA40T
F_C	MHz	110.592
F_{BW}	MHz	1.1
IL	dB(max)	4.5
Ripple	dB(max)	1
Stop Band	dBc/MHz	40

3.2.2.2.2 *RX IF Amplifier*

The RX IF Amplifier is part of the PMB2411 device and its gain is programmable via the DSP software.

3.2.2.2.3 *RX IF Detector - Quadrature Demodulator*

The IF Detector - Quadrature Demodulator device is the PMB2411 device by Siemens as shown in Table 3-16.

Table 3-16 RX IF Detector- Quadrature Demodulator Specifications.

Requirement	Units	Specification
Manufacturer	-	Siemens
Part Number	-	PMB2411
V_{dd}	V	3.3
I_{dd}	mA	
F_{IF} Range	MHz	40 ~ 460
F_{BB} Range	MHz	<550
F_{LO} Range	Hz	80 ~ 920
Gain	dB	18.9
V_{out}	Vpp	<2.5
LO Level	Vpp	-15
I/Q Amp. Balance	dB	1.7
I/Q Phase Accuracy	degrees	±3
Noise Figure	dB	12

3.2.2.2.4 *RX Fine Frequency Synthesizer*

Like the TXFFS the RXFFS has a step size of 5KHz with a frequency tuning range from 220.8 to 221.6MHz, two times the needed IF frequency and has an output power at about –15dBm. This signal frequency is divided by two inside the PMB2411 device.

3.2.2.2.5 *RX Baseband Filter*

The use or disclosure of this information is subject to the restrictions on the title page.

Because the receiver-matching filter is performed with DSP software, the RX baseband LPFs are 2-pole Butterworth characteristic used to suppress out-of-band spurious and alias frequency components.

3.2.2.2.6 *RX Data Converter*

Refer to section 4.1.1.2.

3.2.3 10MHz Reference Distribution

The 10MHz reference signal provided by the external OCXO is passed through a two-way power splitter and a four-way power splitter as illustrated in Figure 3-3.

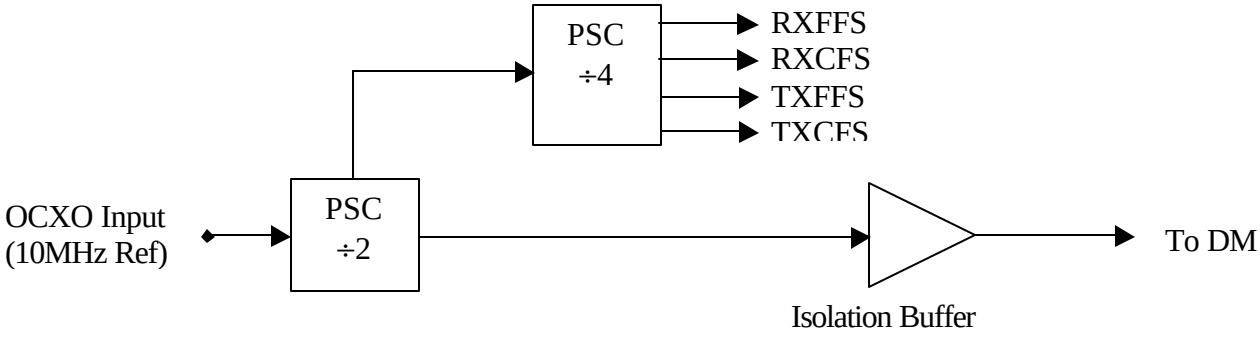

Figure 3-3 10MHz Reference Distribution.

3.2.4 Power Conditioning

The RM requires each voltage be subject to power conditioning to filter the power supply noise and help with isolation between noisy digital circuits and noise sensitive analog circuits. Voltage regulators and DC-DC converters are used according to the block diagram of Figure 3-4.

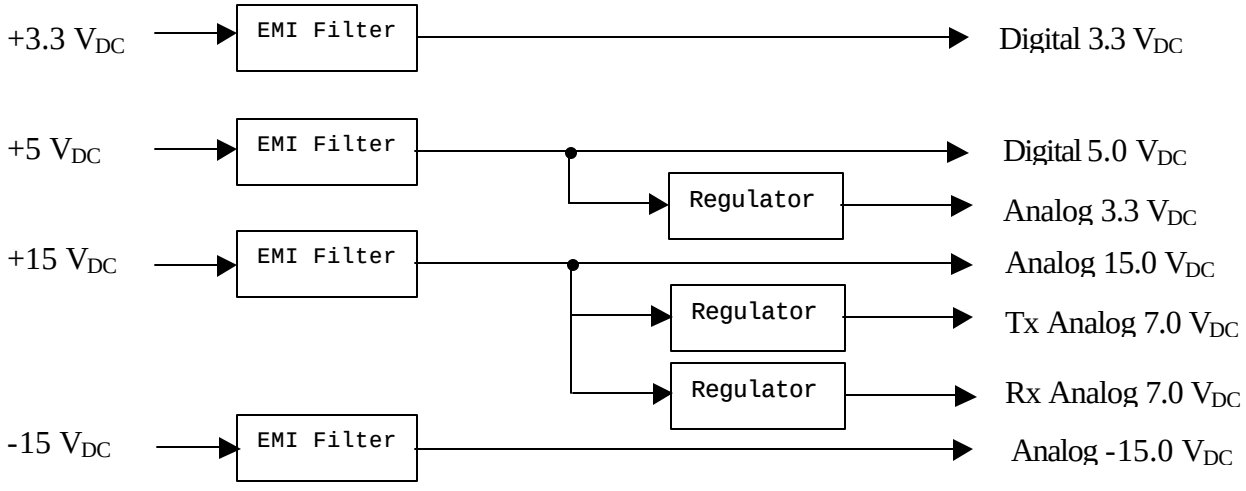

Figure 3-4 Power Conditioning Requirements.

3.3 Design Constraints

The RM design shall adhere to the following design constraints.

The use or disclosure of this information is subject to the restrictions on the title page.

3.3.1 Minimize Design Changes

Changes to the Reference Design, including physical component layouts, should be kept to an absolute minimum except where necessary to support new Aero M4 functional requirements, which may include component upgrades.

4 Interface Requirements

4.1 Hardware Interfaces

The following sections describe the functionality of the various RM hardware interfaces. Additional information on these interfaces can be found in references [2] and [3].

4.1.1 DM Interface

The DM interface is described in the following sections.

4.1.1.1 *TX Data Sample Interface*

The TX Data Interface is comprised of a DAC (AD5322) and its associated signals consisting of the clock (AD1_SCLK), serial data (AD1_DIN), frame (AD1_SYNC), and DAC load (AD1_LDAC) signals provided by the DM (see reference [3]). Data is docked to the device at a rate of 134.4KHz corresponding to the HSD mode or 96KHz to the VOICE and Signaling modes. See ref [16] for interface timing requirements.

4.1.1.2 *RX Data Sample Interface*

The RX Data Interface is comprised of a ADC device (AD7729). The AD7729 is a dual 15-bit Sigma-Delta ADC (with a 10-bit auxiliary D-to-A converter) accepts the RXI/Q signals from the quadrature demodulator and operates off a master clock of 48x sampling rate, or 6.4512 MHz sampling rate (48 x 134.4 KHz) for HSD mode, or 4.608 MHz (48 x 96KHz) in VOICE and Signaling modes. The ADC master clock is derived from the 64.512 MHz data rate clock reference on the DM. See ref [17] for interface timing requirements.

OPERATIONAL NOTE: During normal operation, carrier frequency offsets that result from the incoherent frequency conversion elements on the RM are compensated for by the executable DSP SW utilizing a polyphase filter technique while referenced to the received satellite channel data clock, which is synchronized the network clock in the LES.

4.1.1.3 *RX Bias Control Interface*

The demodulator chip encounters a differential DC-offset that must be compensated for to enhance the receivers performance. The chip provides a reference circuit as sample-&-hold function to provide some compensation. However, the Reference Design added two ADCs to compensate the residual DC offset for without compensation the RX I/Q signals would saturate the ADC. The RX Bias Interface provides this correction for DC bias voltage on the analog RXI and RXQ signal channels using the dual DAC AD5302. The DM provides the clock (AD4-SCLK), serial data (DATA), and frame (AD4_SYNC) signals (see reference [3]). See ref [16] for interface timing requirements.

The use or disclosure of this information is subject to the restrictions on the title page.

4.1.1.4 *Tx Power Control Interface*

The Power Control Interface provides two adjustments using another dual DAC AD5302 device for the TX output power. The DM provides the clock (AD5-SCLK), serial data (DATA), and frame (AD5_SYNC) signals (see reference [3]). The LDAC of this AD5302 is not required and thus connected to GND. See ref [16] for interface timing requirements.

4.1.1.5 *Rx Power Control Interface*

This AD5302 12-Bit DAC replaces the AD5541 DAC used to tune the Reference Design TCVCXO. For the DM it is used for the Rx Power Control. The DM provides the serial clock (AD3_SCLK), output data (DATA) and frame sync (AD3_SYNC) signals to the AD5302 device (see reference [3]). See ref [16] for interface timing requirements.

4.1.1.6 *Frequency Synthesizer Interface*

The four frequency synthesizers use the same LMX2306/2326 device type with a programming interface consisting of a common clock (SYN_CLK) and data (SYN_DATA) signals, individual load enable (SYN_LE1,2,3,4) signals, and individual status (SYN_ST1,2,3,4) signals all provided by the DM (see reference [3]). See ref [18] for interface timing requirements.

4.1.1.6.1 *DDS Interface (TX Doppler Correction)*

The DDS AD9850 device is used to provide Doppler frequency correction on the TX modulated carrier. The DM provides the serial clock (DDS_CLK), data (DDS_DATA), and frame sync (DDS_SYNC) signals (see reference [3]). See ref [19] for interface timing requirements.

4.1.1.7 *Temperature Sensor & Power Detector Interface*

The AD7418 device is a 10-bit Digital Temperature Sensor with an operating range from -55^{o}C to +125^{o}C. The single-ended analog input is used to sense the temperature near the TX PA, which dissipates the most power. The DM provides the serial clock (AD3_CLK) signal, the common data (DATA) signal, and the frame sync (AD3_SYNC) signal (see reference [3]). See ref [7] for interface timing requirements.

4.1.1.8 *Discrete Control Signals*

See reference [2].

4.1.2 HTRF Interface

For the RF Module, a short circuit RF stub will be added to the TX output and RX input to provide a short circuit path to ground to act as protection from transient effects such as indirect lightning. Refer to Section 7. Also, see reference [2] and the customer DRD.

5 Performance Requirements

The RM performances requirements are generally specified in section 5.0 of reference [1] are the requirements as those of the Reference Design.

The use or disclosure of this information is subject to the restrictions on the title page.

6 Mechanical Requirements

6.1 PCB Form Factor

The PCB mechanical form factor shall be per the requirements specified in the customers Design Requirements Document.

6.2 PCB Layout Standards

The PCB layout standards shall be per the requirements specified in the customers Design Requirements Document.

6.2.1 Signal Grounds

Analog signal return paths shall have low impedance paths connected to a common point (area) on the PCB away from the DM and RM digital interface.

6.3 External Interface Connectors

The external interface connectors shall be per the requirements specified in the customers Design Requirements Document.

7 Environmental Requirements

The environmental performance shall be per the requirements specified in the customers Design Requirements Document.

7.1 Shielding and Thermal Requirements

The RM employs the use of RF shielding according to the table below to help improve isolation between on-board circuit functions and external equipment.

8 Manufacturing Requirements

8.1 Manufacturability

The RM shall be manufactured in accordance with the requirements defined by the Program Management Plan and by customer Design Requirements (DRD), or in case of conflicting requirements, by the customer-defined requirements.

8.2 Testability

The RM PCB shall include test points according to their logical use for support of engineering level debug and testing, for use during production test, and for ongoing product maintenance. The following test points are available on the RM.

8.2.1 Reliability

The MTBF of the RM shall be per the requirements specified in the customers Design Requirements Document.

The use or disclosure of this information is subject to the restrictions on the title page.

9 Installation and Maintenance Requirements

9.1 Maintenance Facilities

An operations and maintenance manual is provided for the Aero-M4 MTU of which the DM is included.

9.1.1 Built In Test Equipment (BITE)

9.1.1.1 *RF Loop-Back*

When RR is configured for RF Loop Back, the Tx last stage power amplifier is shut down and the main path is terminated by the switch resistor. This make sure the RM meet the EMI or OFF state emission requirements. The loop back coupled signal from Tx RF signal is attenuated to the normal receive path input level. RF Loop-Back testing is part of the RF Module Diagnostic Self-Test features. The configuration can be employed during production test, burn-in test, or maintenance test.

9.1.1.2 *Frequency Synthesizer PLL Monitoring*

Lock detection circuits are built-in to the frequency synthesizer devices (see ref [18]) are summarized and made available to the DM interface where they are combined to a single status signal and provided to the LP which generates a visual alarm (board level LED) and made available to the HTCE when an out-of-lock condition is detected.

The use or disclosure of this information is subject to the restrictions on the title page.