SECTION 3
THEORY OF OPERATION

3.1 GENERAL

The RT-138 operational theory is presented in two sections. The first section is a basic presentation of module functions, while the second portion is a more detailed description of the operation of each module.

The radio is designed to provide multiple channel capability for VHF-FM communications in the 138.0000 to 173.9975 MHz band. The Transceiver is capable of being channeled to any 2.5 kHz increment in this band; 14,400 channels in all. An optional Guard Receiver allows monitoring a guard frequency while the Main Receiver is channeled to another frequency.

For pin assignment and other operational information on some of the integrated circuits used in the RT-138, see Section 7.3 of this manual.

3.2 COMPLETE OPERATIONAL BLOCK DIAGRAM

The RT-138, as shown in the block diagram (Figure 3.2-1), consists of five basic modules. These five modules are: Synthesizer Assembly, R/T Assembly, Audio Board, Guard Receiver Assembly, and a Power Supply. These modules plug into the Chassis Assembly which contains the interconnect wiring plus two voltage regulators that provide the +15 VDC for the radio.

The Synthesizer Module (A9) provides the first local oscillator injection for the Main Receiver and drive for the transmitter. All output channel frequencies are derived from a temperature controlled crystal reference oscillator that provides excellent stability. The Synthesizer contains an out-of-lock detection circuit that disables the transmitter power output if an unlocked condition exists. The Synthesizer is programmed by negative BCD codes applied to the tuning inputs and provides on-frequency operation for the transmitter or a 20 MHz offset for receiver L.O. injection, depending on the state of the PTT line.

The R/T Module (A7) contains the Main Receiver as well as a 10 watt transmitter. The T/R Relay switches the antenna between receive and transmit. Receive energy is divided equally between Main and Guard by a power splitter. The R/T Module contains RF, IF and detector circuits of the Main Receiver. Transmitter power stages are also located in the R/T Assembly.

3.2 COMPLETE OPERATIONAL BLOCK DIAGRAM (cont.)

The Audio Board (A3) contains the interfacing circuitry required to make the Main R/T and Synthesizer perform as a transceiver. The PTT control of the antenna relay, sidetone audio and modulation signal is provided by the Audio Board. Mic audio processing is performed by the Audio Board. The audio level control and squelch circuitry are also located on the Audio Board.

The Guard Receiver (A8) is optional. It is a single channel receiver without an audio power amplifier. The channel is crystal-controlled and the crystal frequency is tripled for low side local oscillator injection. The multiplier and preselector are aligned for a user specified channel. Any channel in the frequency band can be used. Noise squelch detection is incorporated in the module. Low level guard audio is fed to the Audio Board for further processing.

The Power Supply (A2) and the Regulator Assembly supply various DC voltages required by the RT-138. Primary voltage for the unit (15V) is distributed by two 15V dissipative regulators. Peripheral voltages needed in the system are generated by the FLEXCOMM Power Supply. Using 27.5V aircraft power as its input, the FLEXCOMM Power Supply delivers +5V, +28V and -28V used throughout the system.

3.3 SYNTHESIZER BLOCK DIAGRAM AND CIRCUIT THEORY

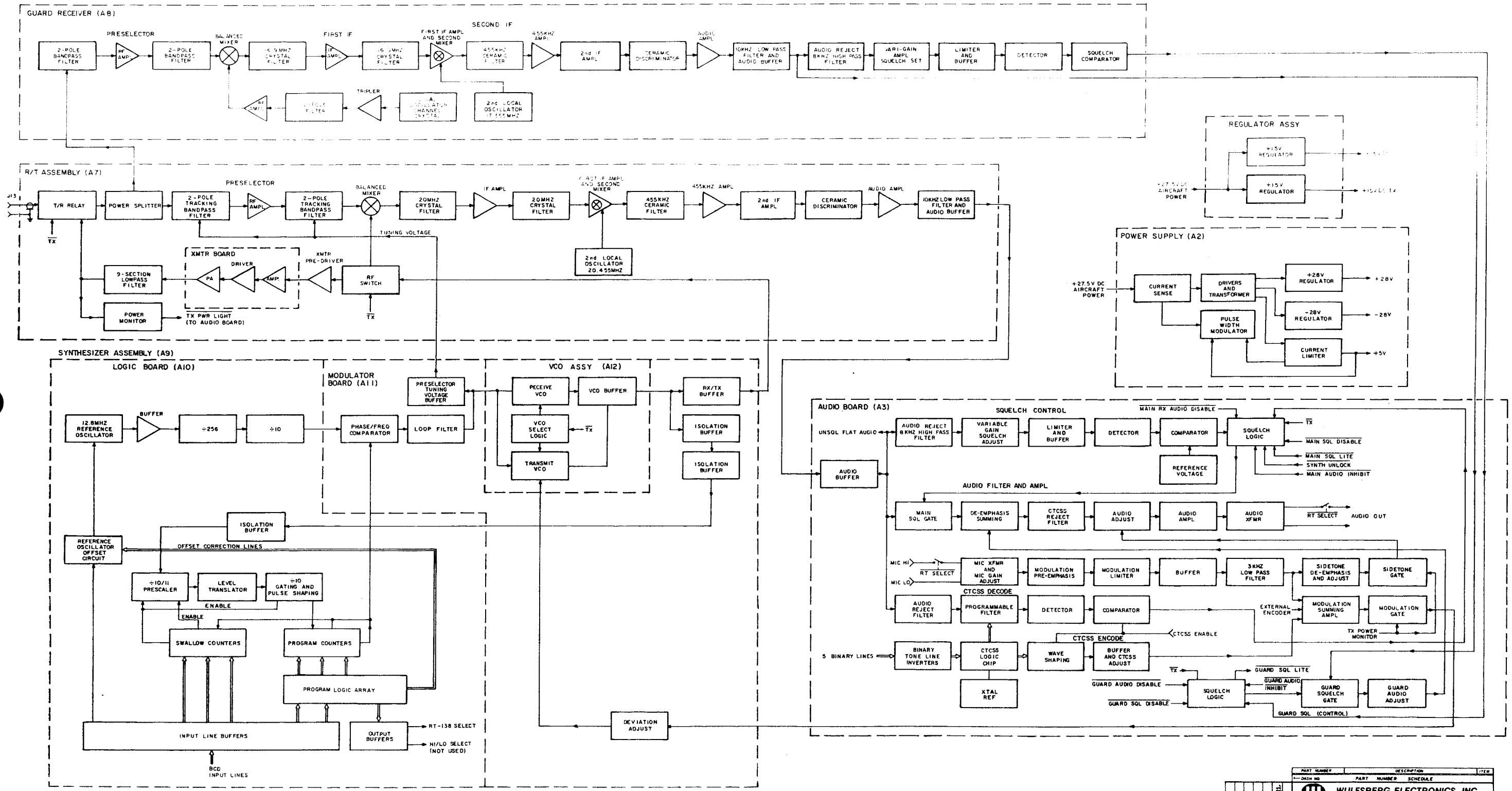
The Synthesizer Module consists of three sub-assemblies contained in an RF shielded box. See Figure 3.3-1 for the Synthesizer block diagram. The circuit blocks of the Synthesizer are:

Logic Board (A10)
Modulator Board (A11)
VCO Assembly (A12)

These three boards interconnect through the Chassis wiring to form a highly stable phase-locked RF generating system. Using one crystal (12.8 MHz) as a frequency reference, the Synthesizer is capable of tuning all 14,400 frequencies.

The Synthesizer is a plug-in module that generates outputs required for both receive and transmit modes of operation. For receive, the module functions are:

1. Synthesize the correct frequency and injection level for the R/T Assembly L.O. drive.
2. Generate the DC tuning voltage for the preselector.



RT-138 BLOCK DIAGRAM
FIGURE 3.2-1

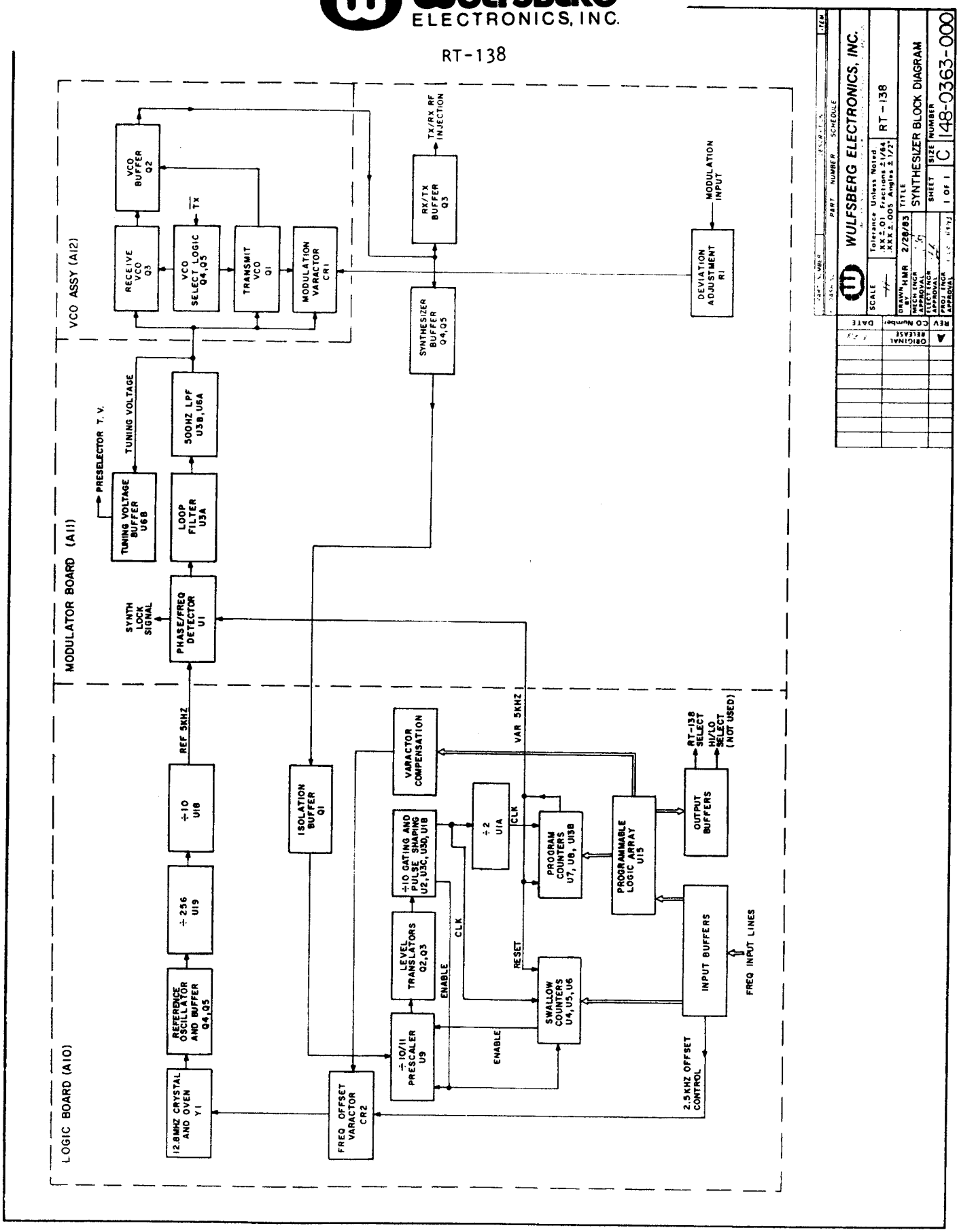
PART NUMBER	DESCRIPTION	ITEM
← DASH NO	PART NUMBER SCHEDULE	

WULFSBERG ELECTRONICS, INC.

SCALE	Tolerance Unless Noted .XX ±.01 Fractions ±1/64 .XXX ±.005 Angles ±1/2°
DRAWN BY HMR 8/82	TITLE RT-138 BLOCK DIAGRAM
MECH ENGR APPROVAL	
ELECT ENGR APPROVAL	SHEET 1 OF 1 / SIZE E / NUMBER 148-0327-000
PROJ ENGR APPROVAL	

ORIGINAL RELEASE — DATE 8-1-82 — REV A — CO Number

131-0016 REV C



RT-138 SYNTHESIZER BLOCK DIAGRAM
FIGURE 3.3-1

3.3 SYNTHESIZER BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

For transmit the functions are:

1. Synthesize the correct frequency RF injection level for the R/T Assembly transmitter.
2. Frequency modulate the RF injection.
3. Control the FM sensitivity across the frequency range of the system.

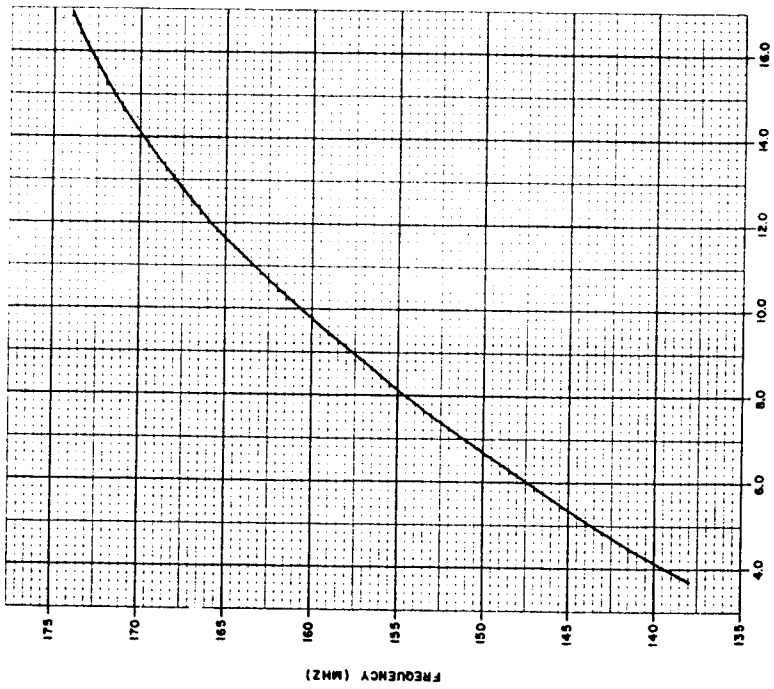
3.3.1 VOLTAGE CONTROLLED OSCILLATOR (A12)

This assembly features a rigid-mounted printed circuit contained in a shielded box. To prevent frequency instabilities caused by component vibration, the completed assembly is filled with an epoxy encapsulation material. Only variable tuning adjustments remain accessible.

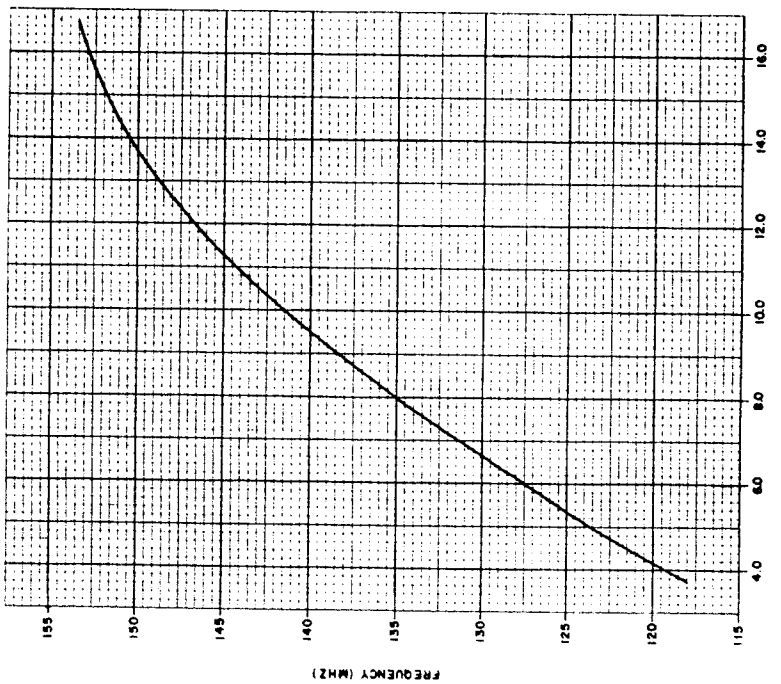
There are two independent oscillators plus a common buffer (A15Q2) housed within the VCO package. Only one VCO is functional at a time. Switch transistors (A12Q4 and A12Q5) select the desired oscillator. The VCO's and their frequency ranges are as tabulated.

VCO	F MIN	F MAX
TRANSMIT Q1	138.000 MHz	173.9975 MHz
RECEIVE Q3	118.000 MHz	153.9975 MHz

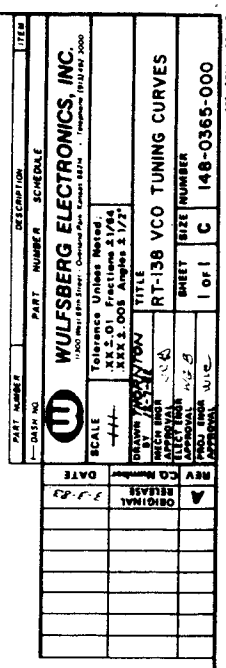
VCO frequencies are voltage controlled by varactor tuning of the oscillator LC circuits. A common tuning line from the Synthesizer Modulator controls both oscillators. Representative frequency versus voltage curves are shown in Figure 3.3.1-1.



TRANSMIT VCO TUNING VOLTAGE



RECEIVE VCO TUNING VOLTAGE



RT-138 TYPICAL RECEIVE AND TRANSMIT TUNING CURVES
FIGURE 3.3.1-1

3.3 SYNTHESIZER BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.3.1.1 RECEIVE VCO

In receive, A12Q3 is the selected oscillator. A high $\overline{TX}$ line turns on switch transistor (A12Q4) to activate the RECEIVE VCO. JFET A12Q3 is a self-biased device in a modified Colpitts configuration. Capacitors A12C26, A12C27 and A12C28 are the feedback control elements. These capacitors, along with variable padder A12C25 and varactor A12CR3, resonate with A12L8 to determine the oscillator frequency. Transmit and receive VCO's share a common drain network and a common buffer output (A12Q2).

3.3.1.2 TRANSMIT VCO

Transistor A12Q1 is selected for transmit operation by the VCO SELECT transistors. The TRANSMIT VCO design is similar to the receive except for modulation capability. The primary tuning varactor is A12CR2 and the modulation varactor is A12CR1. Corrected modulation bias voltage at A12C6 capacitor node is a combination of the main tuning voltage and an input from the fixed +10V supply. This summation of DC voltages maintains uniform modulation characteristics over the RT-138 frequency range.

3.3.1.3 VCO BUFFERED OUTPUT

The oscillator output is coupled through A12C19 to the base of output buffer stage A12Q2. Output from the buffer leaves the VCO Assembly at A12J15 pin 13.

3.3.2 SYNTHESIZER MODULATOR BOARD (A11)

In addition to the modulation adjustment, this board contains essential portions of the Synthesizer phase-lock loop. These are the RF buffers, the phase detection circuit and the loop filter circuit.

3.3.2.1 RF BUFFERS

The RF BUFFERS are part of the Modulator Board. The components are shielded by means of an RF fence with a removable top cover. Transistor A11Q3 is the RX-TX buffer which supplies RF energy to the R/T Assembly. Cascaded buffer transistors A11Q4 and A11Q5 complete the link between the VCO and the Logic Board prescaler.

3.3 SYNTHESIZER BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

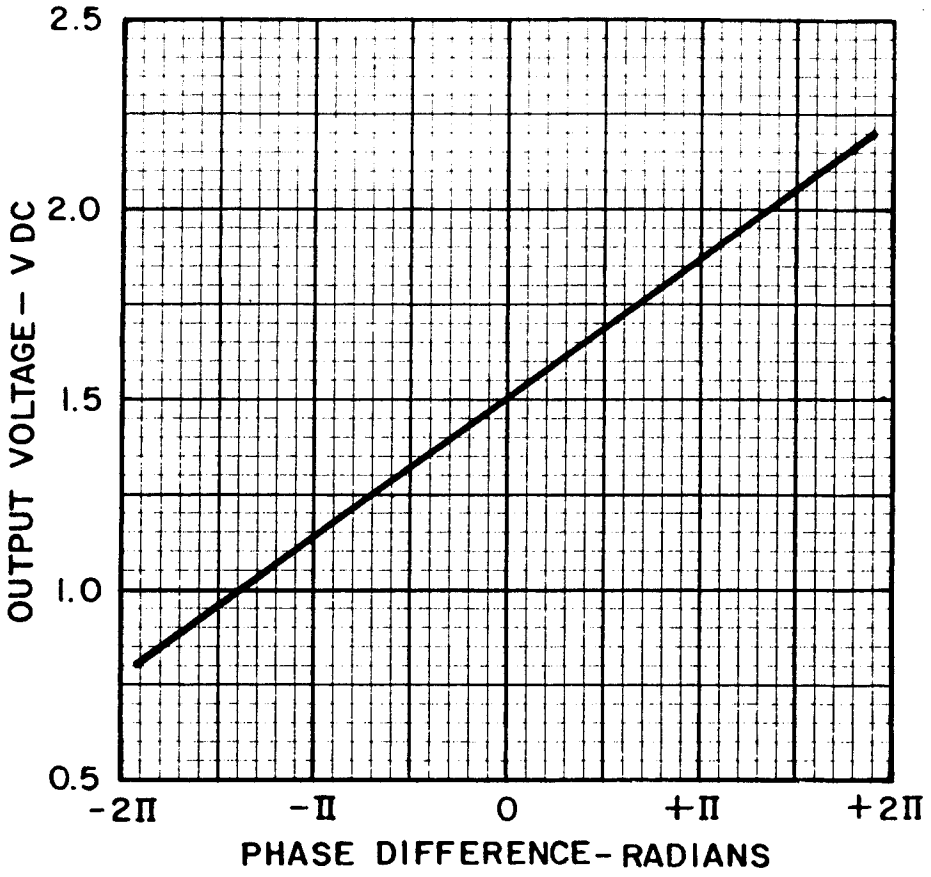
3.3.2.2 PHASE DETECTION/LOOP FILTERING CIRCUITRY

The complete Synthesizer is a closed-loop electronic servo system. In this servo, the VCO frequency is controlled by DC tuning voltage from the Modulator Board. The VCO frequency is divided by N on the Logic Board to become the variable phase 5 kHz input signal to phase detector A11U1. The variable phase is compared to a stable reference phase by detector A11U1. The detector generates an error correction to control the tuning voltage line. The filtered error correction always attempts to maintain the VCO frequency at an exact integer multiple of the 5 kHz reference frequency.

The phase detector and active loop filtering circuitry are both situated on the Modulator Board. Low pass filtering for the VCO tuning voltage is provided by A11U3 and A11U6A.

In the strictest sense, A11U1 is a Phase/Frequency Detector and a Charge Pump all contained in a single integrated circuit. Inputs to A11U1 are the two 5 kHz signals at A11P6, pins 2 and 4. The Phase/Frequency Detector output pins are 2 and 13 which are connected to the internal charge pump input pins 11 and 4. Common outputs, A11U1 pins 5 and 10, provide the up-down charge pump connection.

Reference divider A11R9 and A11R10 establishes a 1.5 VDC reference for the charge pump output. For $\pm$ phase differences of the 5 kHz signals, the output varies symmetrically about the reference voltage. Typical output is shown in Figure 3.3.3.2-1.



OUTPUT VOLTAGE VS PHASE DIFFERENCE
FIGURE 3.3.2.2-1

3.3 SYNTHESIZER BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.3.2.2 PHASE DETECTION/LOOP FILTERING CIRCUITRY (cont.)

During Synthesizer lock, pins 8 and 9 of speed-up switch A11U2C open. The DC error signal from phase detector pins 5 and 10 is applied through A11R11 and A11R12 to the inverting input of A11U3A. This amplifier is a second order active loop filter which acts much like an ordinary integrator. Components A11R11, A11R12, A11R14 and A11C14 are the primary elements determining the response times of the loop. Capacitors A11C12 and A11C13 attenuate higher frequencies than the active loop filter but have little effect on the basic loop response. They do provide significant rejection of 5 kHz to minimize these VCO sidebands.

The DC output of the loop filter is essentially the same as the VCO tuning voltage because of an opamp gain of unity. For AC signals, the active low pass has a filter cutoff of 500 Hz.

3.3.2.3 SYNTHESIZER SPEED UP AND LOCK OUTPUTS

Without loop speed up, channelling response times would be excessive. For large tuning voltage shifts, the loop filter cannot respond quickly. The voltage across A11C14 simply cannot change instantaneously; it must "ramp" slowly towards the new tuning voltage.

The time to find lock is greatly reduced with a speed up circuit activated by the phase detector. The condition of the phase detector is sensed by A11CR1 and A11CR2. When the Synthesizer is unlocked, square wave signals appear at the cathodes of these diodes. Rectification causes pin 13 of A11U2A to go negative releasing the ground which holds speed up switch A11U2C in an open state. Switch A11U2C closes, which reduces the ramp time of A11C14 by reducing its time constant. When lock is obtained, the square wave signals disappear and the loop filter reverts to its normal lock configuration with the speed up switch off.

The negative turn on signal of the speed up switch also controls the operation of A11Q1 and A11Q2. Assuming the unit is "on-line", RT-138 SELECT will be low pulling the anode of A11CR3 low. This low applied to A11R29 insures A11Q2 is biased off. When the speed up is activated, A11Q1 is turned on by A11U2B. Saturation of A11Q1 turns on A11Q2. SYNTH UNLOCK goes low sending the out-of-lock signal to the remainder of the unit.

3.3 SYNTHESIZER BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.3.2.3 SYNTHESIZER SPEED UP AND LOCK OUTPUTS (cont.)

If RT-138 SELECT is not activated, A11CR3 is off. Then, regardless of the Synthesizer's lock condition, A11Q2 is biased on and the SYNTH UNLOCK is kept low. This low inhibits both the transmitter RF and receiver audio.

3.3.2.4 MODULATION CIRCUITRY

FM modulation is impressed on the transmitter by applying a constant input to the input pins of the VCO. DEVIATION ADJUSTMENT A11R1 is simply an interface adjustment. For 3 kHz deviation, input to the Modulator Board is nominally 1.30 VRMS (1 kHz) while the output is adjusted to accommodate VCO sensitivity.

3.3.3 SYNTHESIZER LOGIC BOARD (A10)

Inputs to this board are VCO frequency, BCD channelling code in complemented form, and transmit/receive control ($\overline{TX}$). The outputs are two 5 kHz signals (reference and variable). The 5 kHz reference signal is obtained by dividing the 12.8 MHz by 2560. The variable 5 kHz is the VCO output divided by N (the integer programmed in by the BCD tuning). Phasing between these 5 kHz signals is detected on the Modulator Board to determine the tuning voltage and controlled frequency of the VCO.

3.3.3.1 REFERENCE OSCILLATOR AND FIXED DIVIDER

The crystal-controlled reference oscillator is A10Q5. To maintain frequency stability, A10Y1 is a 12.8 MHz quartz crystal mounted in a temperature-controlled oven.

To obtain 2.5 kHz channel spacing, the reference oscillator is frequency offset to pull the VCO the desired 2.5 kHz. Because the basic loop counts in 5 kHz steps, offset is required on 0.0025 and 0.0075 MHz channels. One wire ($\overline{0.0025}$ MHz) switches these channels. Without pull, A10R28 is switched low by logic gate A10U17C. For offset the ground is released to pull the oscillator. The switched resistor network (A10R31, A10R32 and A10R33) controls varactor sensitivity in coarse 10 MHz steps.

3.3 SYNTHESIZER BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.3.3.1 REFERENCE OSCILLATOR AND FIXED DIVIDER (cont.)

Output from the reference oscillator is coupled through A10C9 to the base of level shifter A10Q4, that switches between ground and +5V to provide a compatible logic input signal for A10U19 (a divide by 256 counter). Its output toggles A10U18 to divide by 10. The total counter division is 2560 with a resultant reference output of 5 kHz.

3.3.3.2 FREQUENCY CHANNELLING BUFFERS

The channel inputs are coded with BCD complements. Each input line is inverted to provide the positive logic BCD inputs used to parallel load the Synthesizer counters.

All frequency input lines are treated in the same manner, so only one input line will be discussed. The general operation applies equally to the other frequency select inputs. Consider the 0.01 MHz line. If the voltage at A10CR5 cathode is greater than 6 or 7 volts (or open), voltage divider action supplies a logic high to A10U11E pin 11. The inverters are 5V CMOS so that a logic high input signal is approximately 5 volts. Logic inversion on A10U11E pin 12 provides a "zero" to the jam input of counter A10U5. When a 0.01 MHz digit is desired, a logic "1" is presented to the counter.

3.3.3.3 DIVIDE BY N COUNTERS (GENERAL)

With a 5 kHz reference frequency, the ÷N integers vary between 27,600 and 34,799. A pulse-swallowing prescaler plus two program counters count the input frequency from the VCO. The program counters register the most significant counts; hundreds, tens and units MHz. The pulse-swallowing prescaler handles the high speed digits. It is capable of "swallowing" 001 to 999 counts.

The counters of the Logic Board are all "down-counters". They are preset to the desired integers and then count down to zero establishing a full count cycle. When the count cycle is completed, a reset pulse is generated to load, or preset, the counters to the desired integers. This load and count-down sequence occurs at the reference frequency or 5,000 times a second. The reset action generates a very narrow pulse - the variable 5 kHz output signal.

3.3 SYNTHESIZER BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.3.3.4 PULSE SWALLOWING PRESCALER

The prescaler is the circuitry between the RF injection input and the prescaled output at A10U1B pin 8. This circuitry consists of buffer A10Q1, variable modulus (÷ 10 or ÷ 11) ECL counter A10U9, level translators A10Q2 and A10Q3, flip-flops A10U2 and A10U1B, and the programmed swallow counters. The number of counts "swallowed" or gated out of the VCO pulse train is determined by the BCD code on the load inputs of the swallow counters.

3.4 MAIN R/T ASSEMBLY BLOCK DIAGRAM AND CIRCUIT THEORY

The R/T detailed block diagram is shown in Figure 3.4-1. In receive, the RF signal is passed through the Transmit/Receive Relay and Power Splitter to the Main Receiver preselector. The preselector features four-pole selectivity with an RF amplifier isolating two tuned pairs. The preselector output drives a double conversion superhetrodyne circuit with IF's of 20.0 MHz and 455 kHz. FM detection is accomplished by a 455 kHz ceramic discriminator.

The transmitter is a broadband design with a nominal output of 10 watts switched by the T/R Relay. The transmitter has an RF amplifier, a Class "C" driver, a Class "C" final P.A. and a filter to minimize harmonic content.

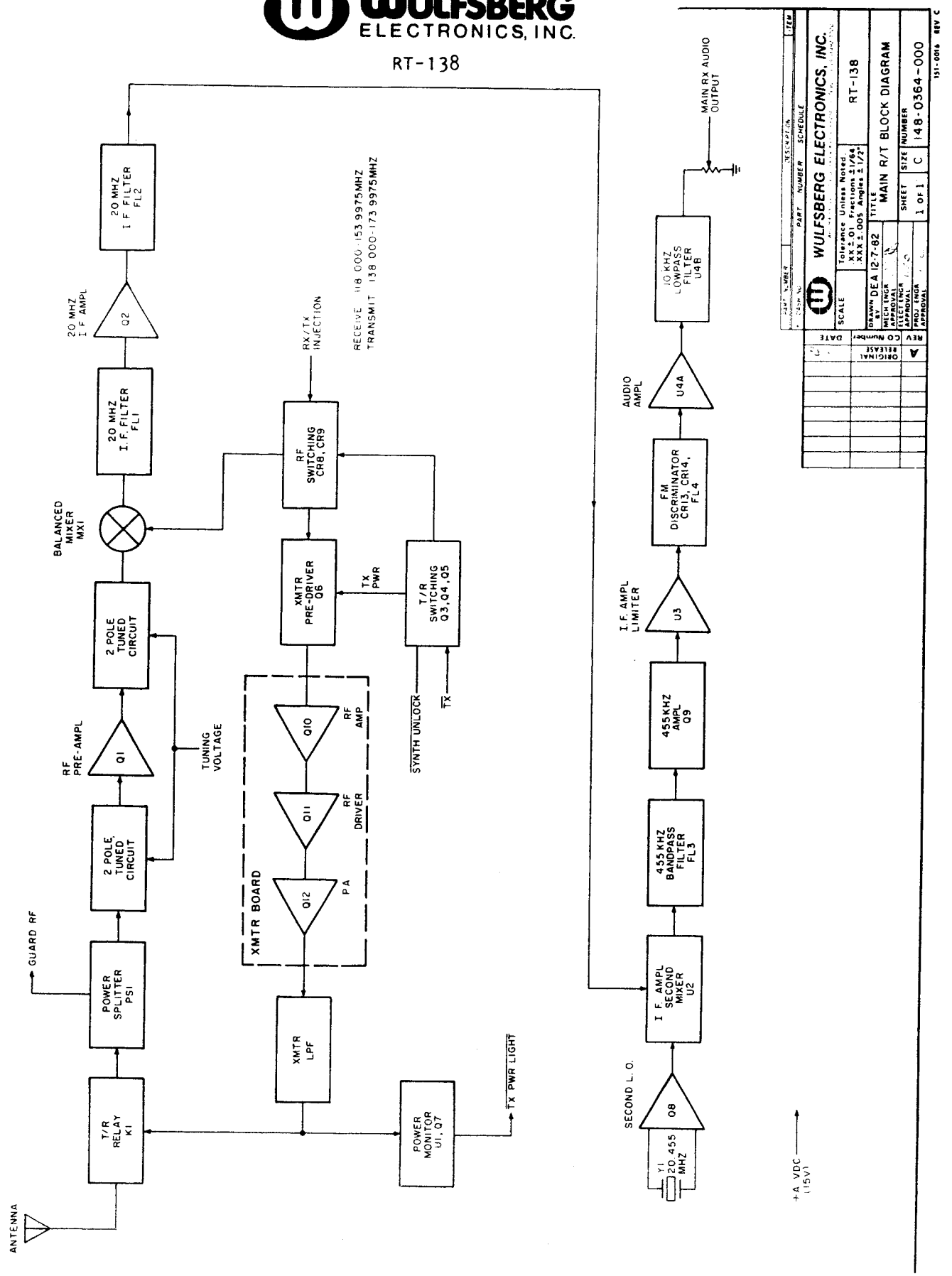
3.4.1 PRESELECTOR OPERATION

The primary function of the preselector is image rejection. Double-tuned resonant circuits are employed at the input and output of RF amplifier A7Q1. These circuits are broadly tuned to accept the desired frequency but highly attenuate the image at any selected channel. Tuning is accomplished by hyperabrupt varactor diodes with the DC tuning supplied by the Synthesizer.

A bipolar transistor (A7Q1) with excellent intermodulation characteristics, in conjunction with the input resonator, determines the overall receiver sensitivity. After amplification by A7Q1, the preselector output is fed to the receiver mixer for frequency conversion.

3.4.2 IF STRIP

The Main Receiver has a dual-conversion IF. The first IF is 20 MHz and the second IF is 455 kHz. Low side injection is applied to the first mixer through an RF switch diode. The second L.O. is 20.455 MHz to provide the 455 kHz second IF.



RT-138 R/T MODULE BLOCK DIAGRAM
FIGURE 3.4-1

3.4 MAIN R/T ASSEMBLY BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.4.2.1 FIRST IF AND MIXER (20.0 MHz)

The first mixer (A7MX1) is a doubly-balanced type whose output is primarily the sum and difference frequencies of the mixing process. The difference frequency is coupled through A7C33 to the input of A7FL1. Components A7C33, A7L15 and A7C34 match the mixer output impedance (typically 75 ohms) to the filter input impedance of 1.5 kohm.

Monolithic crystal filters A7FL1 and A7FL2 provide the 20 MHz selectivity of the IF strip. Each filter package provides four poles of IF selectivity. Input and output design impedances of this filter type are 1.5 kohms.

The 20 MHz filter output is AC coupled to Gate 1 of IF amplifier A7Q2. A voltage divider biases the gates to obtain maximum amplifier gain. Reactive components A7C35, A7C36, A7L16 and A7C38 tune the output of A7FL1. The drain circuit of A7Q2 is tuned by A7C43 providing the proper impedance for A7FL2.

This filter (A7FL2) is identical to the first filter and provides an additional four poles of 20.0 MHz selectivity. An "L" type step-down matching network matches the 1.5 kohm filter output to 220 ohms. The "L" is formed by A7L18 and A7C48. A fine adjust for the network is provided by A7C47.

3.4.2.2 IF AMP INTEGRATED CIRCUIT

A brief description of A7U2 (a multi-purpose integrated circuit designed for FM applications) follows. It has a three-stage limiting amplifier which is internally connected to a balanced product detector. The output of the product detector is emitter-follower buffered and appears at pin 1 of A7U4. Pin 9 of A7U4, monitored by a test point, is an attenuated version of the limiting amplifier output. It is attenuated 20 dB and terminated internally with 50 ohms.

The signal input of A7U2 is terminated by A7R44 and pin 6 is AC grounded by A7C70. The 20.0 MHz bandpassed signal input is amplified by the limiting amplifier and coupled to the product detector. The product detector serves as the second mixer of the IF.

3.4 MAIN R/T ASSEMBLY BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.4.2.3 SECOND LOCAL OSCILLATOR AND MIXER

A crystal-controlled Pierce oscillator (A7Q8) generates the Second L.O. frequency. The 20.455 MHz L.O. signal is coupled to the mixer input, pin 12 of A7U4. The 455 kHz difference is taken from A7U4 pin 1.

3.4.2.4 455 kHz IF AND FM DISCRIMINATOR

The mixer output of A7U2 is fed to A7FL3, a multi-element 455 kHz ceramic filter with equal input-output impedances of 1.0 kohm. This filter provides some adjacent channel selectivity plus spurious rejection.

The filter output is amplified by A7Q9 and then coupled to pin 4 of A7U3. Limited output from A7U3 drives a ceramic piezoelectric discriminator circuit through A7R55.

The discriminator circuit consists of A7FL4, hot-carrier diodes (A7CR13 and A7CR14) plus associated filter components. This combination of piezoelectric filtering and diode detectors produces the familiar "S" curve associated with FM detection. The curve is extremely linear for normal system deviation of $\pm$ 5 kHz.

3.4.3 RECEIVER AUDIO OUTPUT

Recovered discriminator audio is typically 100 mV peak-to-peak, and therefore, the primary function of A7U4A is audio amplification. The high impedance plus (+) input of A7U4A and A7R59 provides minimal discriminator loading. Voltage gain of A7U4A equals 16 which is controlled by A7R60 and A7R61. The low output impedance of A7U4A drives receiver output stage A7U4B.

The final opamp stage (A7U4B) is a low pass design whose response extends to 10 kHz before a frequency rolloff of 12 dB per octave occurs. The cascaded audio amplifiers reduce the 455 kHz component to an acceptable level before the audio leaves the R/T Assembly. Normalized audio from the R/T Assembly is adjusted to 0.50 VRMS by A7R68.

3.4.4 TRANSMIT/RECEIVER RF SWITCHING

Pin diodes A7CR8 and A7CR9 switch the TX/RX RF INJECTION to the MIXER or to the XMTR PREDRIVER input.

3.4 MAIN R/T ASSEMBLY BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.4.4 TRANSMIT/RECEIVER RF SWITCHING (cont.)

Within MX1, pins 7-8 are transformer primary connections which complete a DC path for the RX SWITCH diode. In receive, A7Q4 is off and the emitter follower output of A7Q3 goes to nearly 14 volts. Current flows through A7R21 and the mixer winding to turn on the RX SWITCH diode. The voltage drop across A7R20 is sufficient to keep the TX SWITCH back-biased during receive.

During transmit, the TX SWITCH diode becomes active. $\overline{TX}$ (A7P7 pin 14) is pulled low to energize the T/R relay; it also turns on A7Q4 and A7Q5 if the synthesizer loop is locked. The switched collector of A7Q5 closes the TX SWITCH and supplies power to the XMTR PRE-DRIVER (A7Q6). RF is amplified by A7Q6 to supply +12 dBm to the transmitter input.

3.4.5 TRANSMITTER SECTION

The transmitter chain is a three-transistor lineup located on the XMTR Board. It is a broadbanded VHF design providing 10 watts of saturated RF power. Active devices are A7Q10, A7Q11 and A7Q12.

3.4.5.1 XMTR BOARD

DC power is applied to all XMTR Board stages through Chassis mounted resistors. Remote mounted resistors distribute heat uniformly throughout the unit and also help stabilize Class "C" RF power stages by providing degenerate DC feedback.

The RF input is impedance transformed from 50 ohms (4:1 stepdown) by balun A7T2. Transistor A7Q10 is a Class "AB" RF stage whose temperature stability is maintained by A7CR16 and voltage feedback from the collector. Amplified power output is approximately one-half watt.

The base of A7Q11 is driven by a double-tuned interchange. Capacitor A7C98 is the mutual coupling element common with the A7Q10/A7Q11 tuned circuits. Bandpass characteristics are controlled by the mutual capacitance value.

The driver (A7Q11) is an intermediate level power device, capable of 2 to 3 watts of RF power operating Class "C". The interchange between the driver and the final is also double tuned with A7C105 being the mutual coupling element. The low impedance final output is matched to 50 ohms by output balun A7T3. A section of 50 ohm transmission line is tuned to resonance by A7C110 to couple the XMTR Board output to the LPF (Low Pass Filter).

3.4 MAIN R/T ASSEMBLY BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.4.5.2 LOW PASS FILTER (LPF)

The LPF is a nine-section elliptic filter design with ripples in both the pass and stop band responses. It is designed to pass transmit frequencies with low attenuation and to provide a large amount of harmonic suppression.

3.4.5.3 TRANSMIT POWER SENSOR AND MONITOR

Presence of RF is sensed by a detector consisting of diodes A7CR2 and A7CR3. When detected RF approaches the fixed voltage of comparator A7U1A pin 2, the comparator "trips" to turn on A7Q7 providing the $\overline{\text{TX PWR LIGHT}}$ function.

3.5 AUDIO BOARD BLOCK DIAGRAM AND CIRCUIT THEORY

The Audio Board is identical and interchangeable in all transceivers of the FLEXCOMM System. Only one transceiver of a FLEXCOMM system wired for multiple transceivers is actively used at a time. Control Unit tuning data indirectly controls MIC audio input and audio output switching of the desired transceiver. When the RT-138 is the only system transceiver, the MIC input-audio output switching is enabled for all valid RT-138 frequencies.

A block diagram of the audio circuitry is shown in Figure 3.5-1. Audio switching, audio response tailoring, Main Receiver squelch and Main Receiver tone encoding-decoding are the main functions of this board.

The circuitry blocks of the Audio Board are:

1. RT Select
2. Squelch logic and switching
3. Main Receiver squelch detection
4. Receiver audio processing
5. Transmit audio processing and switching
6. CTCSS tone encoding and decoding.

An understanding of these circuits will be aided by referencing the audio block diagram, the schematic diagram (Figure 5.1-7) and the following text.

3.5 AUDIO BOARD BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.5.1 RT SELECT CIRCUIT

$\overline{\text{RT SELECT}}$ is an active low input when the RT-138 Synthesizer recognizes the tuning wire inputs as a valid frequency. For other FLEXCOMM Transceivers, operated from the same Control Unit, $\overline{\text{RT SELECT}}$ will be high. Loading, due to paralleled input-output connections, is eliminated in a system hookup.

With $\overline{\text{RT SELECT}}$ low, emitter-follower A3Q11 is turned on and A3K1 is energized. One set of A3K1 contacts completes the MIC audio input circuit to A3T2 and another set of contacts completes the audio output circuit to A3T1.

3.5.2 MAIN RECEIVER SQUELCH LOGIC AND SWITCHING

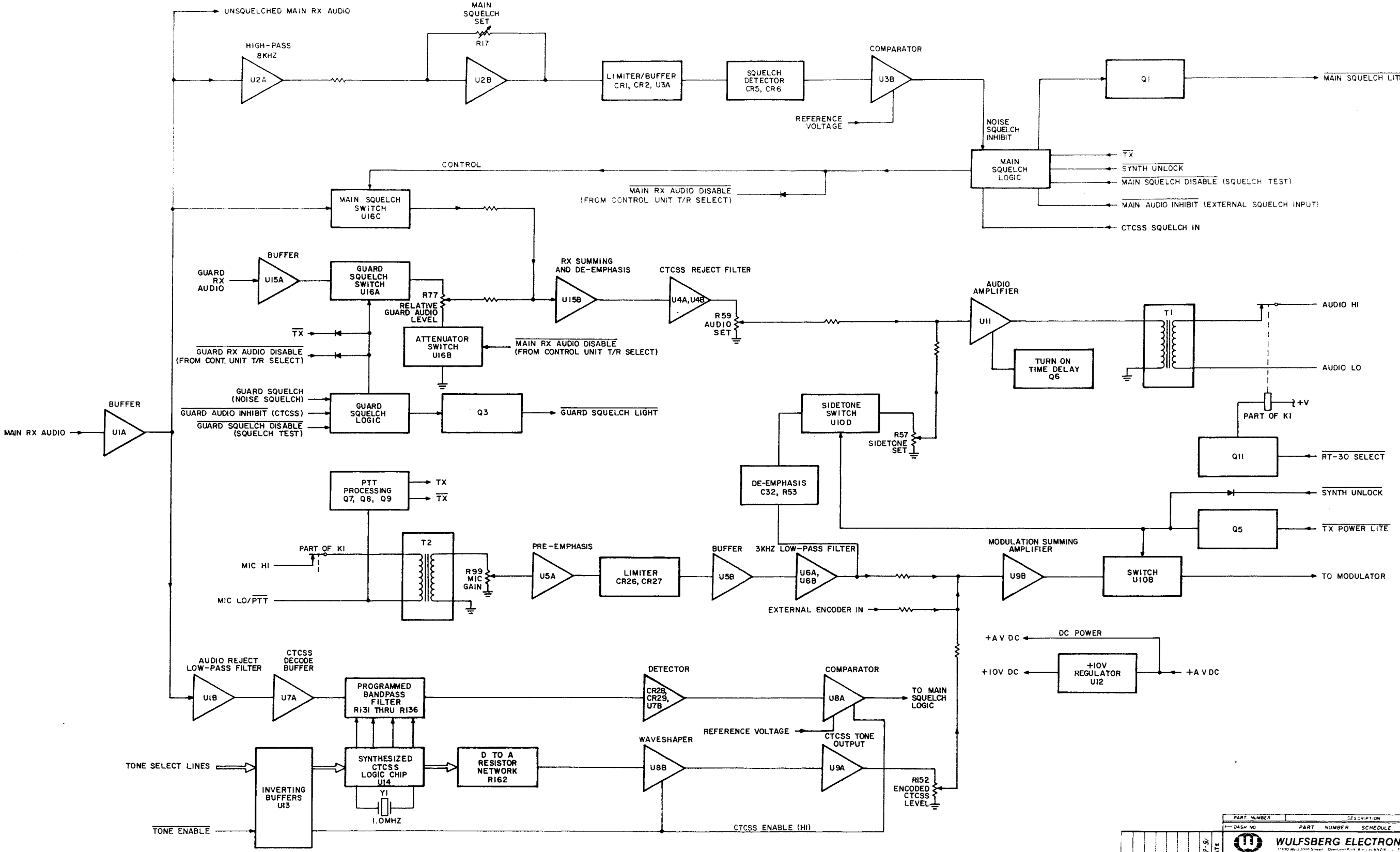
Figure 3.5.2-1 is a simplified diagram of the Main Receiver squelch logic components. It is used to explain squelch operation.

Main Receiver squelch logic has two outputs. One (A3Q1) is an open-collector transistor whose output turns on the main squelch LED. The other output is the controlling line of the Main Receiver squelch switch.

Unless the Control Unit SQ TEST switch is activated (low), squelch test transistor A3Q2 is turned off. With A3Q2 off, its collector acts as an open circuit and has no effect on the squelch logic. Squelch test operation is described in Section 3.5.2.4.

3.5.2.1 MAIN AUDIO GATE SQUELCH CONTROL

To close switch A3U16C, 10V DC is applied to pin 6 through a resistor string consisting of A3R34, A3R35 and A3R36. With no signal applied, rectified noise will cause A3U3B pin 7 output to be low. This low, or inhibit, effectively grounds the junction of A3R34 and A3R35. This causes A3R35 and A3R36 to act as a pull-down resistance on the control line, blocking the receiver audio signal. The same low from noise comparator A3U3B keeps A3Q1 turned off so that the main squelch LED is off.



AUDIO MODULE BLOCK DIAGRAM
FIGURE 3.5-1

3-21/22

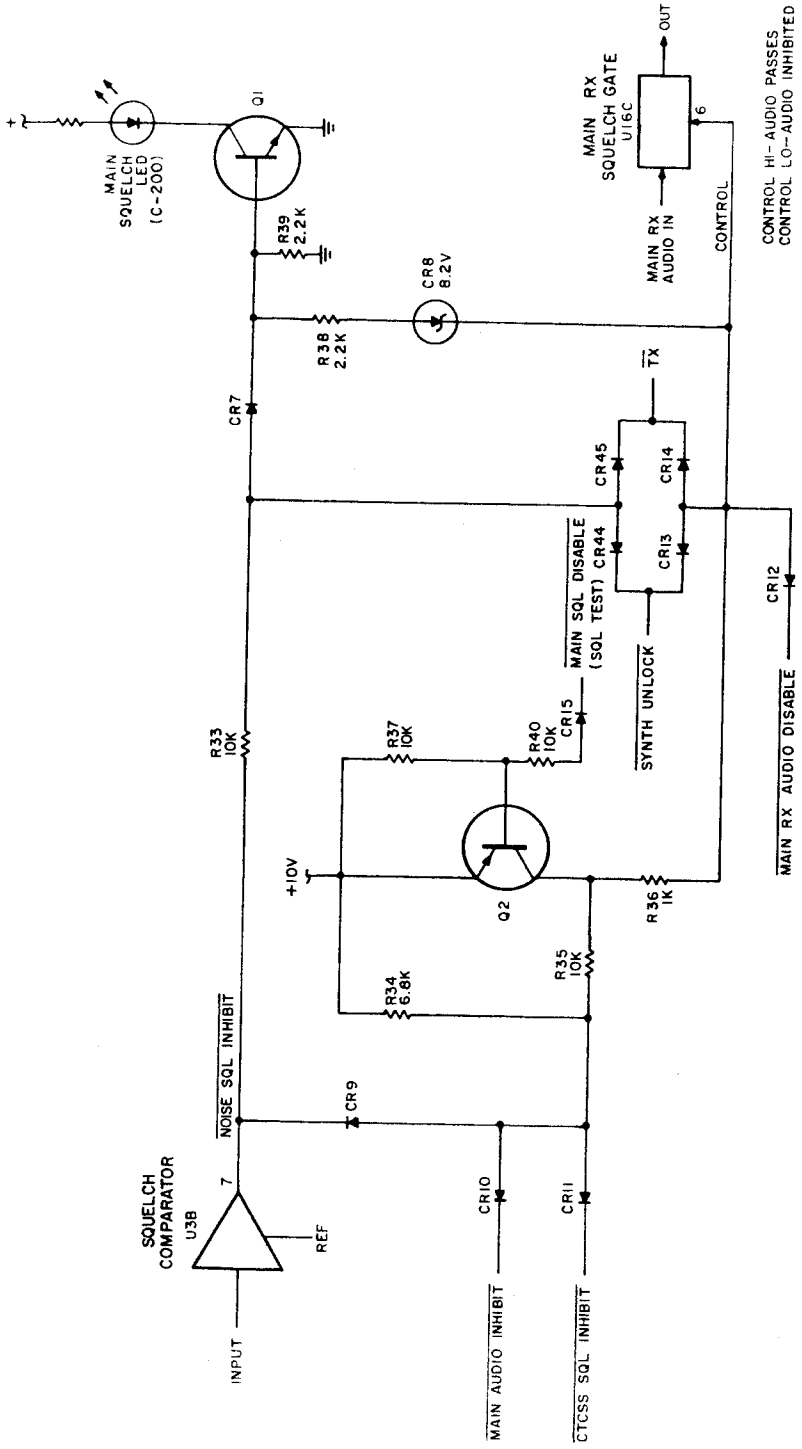
PART NUMBER	DESCRIPTION	ITEM
DASH NO	PART NUMBER SCHEDULE	

WULFSBERG ELECTRONICS, INC.

SCALE	Tolerance Unless Noted: .XX ±.01 Fractions ±1/64 .XXX ±.005 Angles ±1/2°		
DRAWN BY HMR 6/30/81	TITLE FLEXCOMM AUDIO BOARD BLOCK DIAGRAM		
MECH ENGR APPROVAL DE			
ELECT ENGR APPROVAL JHH	SHEET 1 OF 1	SIZE D	NUMBER 148-0272-000
PROJ ENGR APPROVAL WLC			

REV A — ORIGINAL RELEASE — C.O. Number — DATE 7-14-81

151-0016 REV C



WULFSBERG ELECTRONICS, INC.
SCALE —
Tolerance Unless Noted: XX ± .01 Fractions ± 1/64 XXX ± .005 Angles ± 1/2°
DRAWN HMR 7/2/81
MECH ENGR APPROVAL
ELECT ENGR APPROVAL
PROJ ENGR APPROVAL
TITLE FLEXCOMM MAIN RCVR SQUELCH LOGIC
SHEET 1 of 1
SIZE C
NUMBER 148-0277-000
REV A
ORIGINAL RELEASE 9-1-81
DATE

MAIN RECEIVER SQUELCH LOGIC SCHEMATIC
FIGURE 3.5.2-1

3.5 AUDIO BOARD BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.5.2.1 MAIN AUDIO GATE SQUELCH CONTROL (cont.)

For normal receiver operation, without tone squelch, all squelch logic input diodes will be back-biased or open circuited. Signal reception causes A3U3B pin 7 to go high. This removes the ground from the junction of A3R34 and A3R35 so that A3U16C pin 6 control line pulls up towards +10 VDC through A3R34, A3R35 and A3R36. Switch A3U16C closes passing Main Receiver audio to the audio amplifier stages. At the same time, A3U3B pin 7 applies a positive turn-on voltage for A3Q1 via A3R33 and A3CR7 so signal presence is indicated by the main squelch LED.

3.5.2.2 AUDIO SELECT: MAIN OR GUARD

$\overline{\text{MAIN RX AUDIO DISABLE}}$ at A3P3 pin 11 is activated by the Control Unit T/R SELECT switch. It will be low when the switch is in the GUARD position. Diode A3CR12 turns on and clamps A3U16C control input to a logic low level impeding the Main Receiver audio. This input does not affect the main squelch LED which will indicate signal through the A3R33-A3CR7 path.

3.5.2.3 SQUELCH OPERATION DURING TRANSMIT OR SYNTHESIZER UNLOCK

During Synthesizer unlock or transmit, Main Receiver audio and erroneous main squelch lighting are prevented by diode clamping. For an unlocked Synthesizer, $\overline{\text{SYNTH UNLOCK}}$ grounds the cathodes of A3CR13 and A3CR44. In transmit, $\overline{\text{TX}}$ grounds the cathodes of A3CR14 and A3CR45.

3.5.2.4. MANUAL SQUELCH TEST

Squelch testing is performed by grounding the cathode of A3CR15 causing A3Q2 to saturate, placing 10 VDC at the junction of A3R35 and A3R36. Resistor A3R35 acts as collector load and performs an isolating function. The collector voltage of A3Q2 is fed through A3R36 to A3U16C pin 6 and through A3CR8 to turn on A3Q1. The main squelch LED and audio switch (A3U16C) are both checked for operation. Should $\overline{\text{SYNTH UNLOCK}}$ or $\overline{\text{TX}}$ be low, both the squelch LED and switch A3U16C will be inoperative. For $\overline{\text{MAIN RX AUDIO DISABLE}}$, squelch testing is also disabled.

3.5 AUDIO BOARD BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.5.2.5 MAIN SQUELCH CONTROL LINE

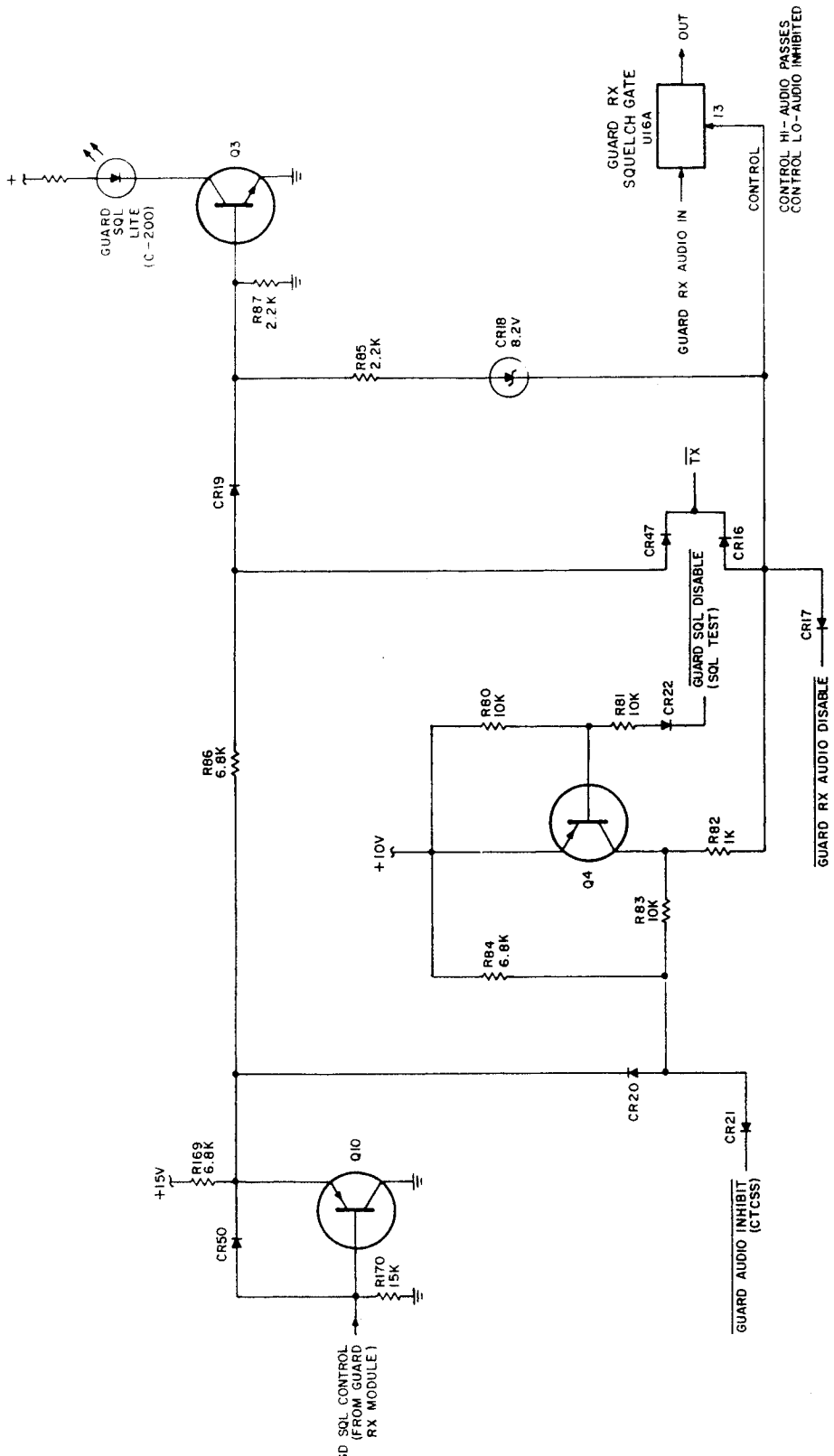
Besides the normal path to energize A3Q1, an alternate sneak path exists from A3U16C pin 6 to the base of A3Q1 through Zener diode A3CR8. This path is intended primarily for lighting the main squelch LED during the squelch test mode. The following explains why A3CR8 is a Zener diode. With normal signal reception, the main squelch gate control must be above a certain minimum DC level for "guaranteed-on" switch operation. The 8.2V Zener (A3CR8) insures the control voltage reaches at least 8.9 VDC before the Zener conducts. (This 8.9 VDC is equal to 0.7V E-B voltage of A3Q1 plus the Zener voltage). This allows the control line to exceed the threshold voltage required for predictable switch operation. If not held off by Zener action, the voltage dividing effect of A3R34, A3R35, A3R36 and A3R38 could lower the control voltage below the threshold level adversely affecting A3U16C switch "on" operation.

3.5.2.6 INTERNAL AND EXTERNAL CODED SQUELCH DECODER CONTROL

Diode A3CR10 is used for external decoder squelch control MAIN AUDIO INHIBIT and A3CR11 is the internal CTCSS squelch control. Diodes A3CR9, A3CR10, A3CR11, and pullup resistor A3R35 form a diode "AND" gate. In order for the junction of A3R34 and A3R35 to go high, all three inhibit inputs must be high. Therefore, any low "AND" gate input will open switch A3U16C. Although a low on either, or both, A3CR10 or A3CR11 cathodes will open the audio switch, these low inputs will not affect the main squelch LED. If an adequate signal is present, A3U3B pin 7 goes high applying a positive DC voltage via A3R33 and A3CR7 to the base of A3Q1. In the absence of a properly coded signal, audio is inhibited but the main squelch LED acts as a signal presence indicator.

3.5.3 GUARD RECEIVER SQUELCH LOGIC AND SWITCHING

The Guard Receiver squelch logic is similar to the main squelch logic. Figure 3.5.3-1 is a simplified diagram of the Guard Receiver squelch components.



WULFSBERG ELECTRONICS, INC.

DRAWN HMR 7/2/81	TITLE	FLEXCOMM				
MECH ENGR APPROVAL		GUARD RCVR SQUELCH LOGIC				
ELECT ENGR APPROVAL			SHEET 1 OF 1	SIZE C	NUMBER 148-0278-000	REV A
PROJ ENGR APPROVAL						

SCALE —

Tolerance Unless Noted.
.XX ± .01 Fractions ± 1/64
.XXX ± .005 Angles ± 1/2°

151-0016 REV C

GUARD RECEIVER SQUELCH LOGIC SCHEMATIC
FIGURE 3.5.3-1

3.5 AUDIO BOARD BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.5.3 GUARD RECEIVER SQUELCH LOGIC AND SWITCHING (cont.)

One of the differences between main and guard logic is A3Q10, whose primary purpose is to inhibit the guard squelch light and switch A3U16A if the Guard Receiver is not installed. Transistor A3Q10 is connected as an input follower. Without the Guard Receiver, base current to A3Q10 is supplied by A3R170. Input follower A3Q10 will be saturated thus placing A3CR20 cathode at nearly ground potential. When the Guard Receiver is installed, the cathode of A3CR20 will follow the noise squelch input developed by the Guard Receiver.

Unless the SQ TEST switch is activated (low), transistor A3Q4 is off. With A3Q4 off, its collector acts as an open circuit and has no effect on the squelch circuit outputs. See Section 3.5.3.4 for Guard SQ TEST theory.

To close switch A3U16A, 10 VDC is applied to A3U16A pin 13 through a resistor string consisting of A3R82, A3R83 and A3R84. With no signal applied to the Guard Receiver, rectified noise will cause a low input to A3Q10 at the base, thus saturating it and placing A3CR20 cathode at ground potential. This low effectively grounds the junction of A3R83 and A3R84. Then A3R82 and A3R83 act as a pull-down resistance for A3U16 pin 13 to block the guard audio signal. This same low keeps A3Q3 turned off so that the GUARD SQ LED is off.

For normal Guard Receiver operation, without tone squelch, all guard squelch logic input diodes will be back-biased or open-circuited. Signal reception causes the input to A3Q10, and then the cathode of A3CR20 to rise. This removes the inhibiting low from the junction of A3R83 and A3R84 so that A3U16A pin 13 pulls up towards +10V. Switch A3U16A closes passing guard audio to the common audio amplifier stages. At the same time, a positive turn-on voltage is applied to A3Q3 through A3R86 and A3CR19.

3.5.3.1 EXTERNAL CODED SQUELCH DECODER CONTROL

A two input "AND" gate is formed by A3CR20, A3CR21 and A3CR84. A low input on A3CR21 will inhibit audio but allows the guard squelch LED to act as a signal presence indicator.

3.5 AUDIO BOARD BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.5.3.2 AUDIO SELECT: MAIN OR GUARD

$\overline{\text{GUARD RX AUDIO DISABLE}}$ at A3CR17 cathode is grounded by placing the Control Unit T/R SELECT switch in the MAIN position. This turns on A3CR17 opening the Guard Receiver audio path. This low level does not affect the guard squelch LED which will function as a visual signal presence indicator.

3.5.3.3 SQUELCH OPERATION DURING TRANSMIT OR SYNTHESIZER UNLOCK

During the transmit function, Guard Receiver audio and possible erroneous squelch light tripping are prevented by diode clamping. In transmit, $\overline{\text{TX}}$ is low which grounds the cathodes of A3CR16 and A3CR47. $\overline{\text{SYNTH UNLOCK}}$ does not affect the guard audio gate because the Guard Receiver is independent of the Frequency Synthesizer.

3.5.3.4 MANUAL SQUELCH TEST

Squelch testing is performed when A3CR22 cathode is low. Transistor A3Q4 saturates placing +10 VDC at the junction of A3R82 and A3R83. The collector voltage of A3Q4 is fed through A3R82 to A3U16A pin 13 and through A3CR18 to turn on A3Q3. The guard squelch LED and audio switch (A3U16A) are both checked for operation. Should $\overline{\text{TX}}$ be a low during a SQ TEST switch closure, both the squelch LED and switch A3U16A will be inoperative. For $\overline{\text{GUARD RX AUDIO DISABLE}}$ low, the squelch test transistor cannot close A3U16A because of clamping by A3CR17. Therefore guard audio is blocked. Switch transistor A3Q3 will not turn on via A3CR18. Signal presence LED signalling, however, is still functional during SQ TEST through the A3R86-A3CR19 path.

3.5.4 MAIN RECEIVER SQUELCH DETECTION

The Main Receiver squelch is an integral part of the Audio Board. The active devices of this noise-activated circuit are A3U2 and A3U3. To derive the squelch trip signal, the Main Receiver signal is high-passed, clipped, average detected, and then compared to a fixed DC reference by a level comparator.

3.5 AUDIO BOARD BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.5.4 MAIN RECEIVER SQUELCH DETECTION (cont.)

A multiple-feedback active filter design, intended to reject audio components below 9 kHz, is provided by A3U2A. This design is a three-pole filter which has a rolloff characteristic of 18 dB/octave and a voltage gain of two. Capacitors A3C4, A3C5, A3C6 and resistors A3R9, A3R10 and A3R11 provide the frequency response-shaping feedback.

The high-passed audio (noise) from A3U2A pin 1 is fed to a variable gain stage through coupling capacitor A3C8. In this circuit, the output voltage can be varied from +20 dB gain to 20 dB of loss by main squelch setting potentiometer A3R17.

Diodes A3CR1 and A3CR2 plus A3R20 through A3R22 perform a limiting function to clip high-level random noise spikes. In the quiescient state both diodes are turned on with a trickle of current. The diodes will be near the turn-on knee of their diode characteristic curves, thus the anodes will be approximately 0.5 VDC above their cathodes. Anode voltage to A3CR1 and A3CR2 is 2.3 VDC and both cathodes are at 1.8 VDC. For low level AC signals, both diodes are on passing the unlimited signal to opamp U3A. A positive-going excursion of sufficient amplitude will eventually back-bias A3CR1 defining the positive clip point. Negative excursions are passed through A3CR1 until the level becomes low enough to turn off A3CR2. This circuit is a symmetrical clipper with an output of approximately 3 volts peak-to-peak.

Opamp A3U3A has a voltage gain of 3.3, but more importantly, it provides a low impedance driving source for the diode detector consisting of A3CR5 and A3CR6 plus DC filtering components A3C14 and A3R31. Voltage divider A3R27, A3CR3, A3CR4, and A3R28 sets a reference voltage of 3.2 VDC for the plus (+) input terminal of comparator A3U3B. During signal reception, 10 kHz noise and detected DC level decrease. With a strong enough signal, the detected level falls below the plus (+) terminal reference voltage, A3U3B senses this condition and its output slams the upper "rail" of the opamp. Resistors A3R29 and A3R32 provide hysteresis ensuring the comparator is insensitive to chatter.

The positive output level attained at A3U3B pin 7 is a function of the supply voltage of the opamp. If the supply voltage changes, the output of A3U3B pin 7 changes accordingly. To maintain hysteresis independent of the supply voltage, A3CR49 and A3R180 clamp the opamp output to 10.6 VDC. Therefore, the positive feedback (hysteresis) via A3R29 and A3R32 is immune to supply voltage changes.

3.5 AUDIO BOARD BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.5.5 RECEIVER AUDIO PROCESSING

Unsquelched audio from the Main and Guard Receivers is combined and processed to provide 100 milliwatt audio output capability.

Integrated circuit A3U1A is the Main Receiver inverting buffer with a gain of 1.18. With 0.5 VRMS input, A3U16A pin 1 output is 0.59 VRMS of unsquelched audio. This unsquelched signal is distributed to four places.

1. Connector A3P3 pin X
2. Main squelch circuitry
3. CTCSS decoder circuitry
4. Main squelch gating switch A3U16C

Unity gain buffering for the guard audio is provided by A3U15A. Its input level is 0.59 VRMS which is buffered and fed directly to guard squelch switch A3U16A.

Audio switches A3U16A and A3U16C are controlled by the squelch logic circuitry. A high on A3U16A pin 13 or A3U16C pin 6 closes the switch and a low opens the switch. The Main Receiver audio switch is A3U16C. Resistors A3R176 and A3R177 place both sides of switch A3U16C (pins 8 and 9) at the same DC level. Capacitor A3C2 is an AC ground which prevents audio coupling through the biasing resistors. When switching takes place, transients and pops are minimized since no DC level shift occurs. Biasing networks of this configuration are used for all audio switches and are easily identifiable.

With A3U16C closed, main audio is applied to the summing input (A3U15 pin 6) through A3R173. Guard audio is also fed to the summing input by A3R172 if switch A3U16A is closed.

Attenuator switch (A3U16B) is controlled by the T/R SELECT switch of the FLEXCOMM Control Unit. Similar audio output levels are maintained when either MAIN or GUARD are selected separately. Capability to adjust the Guard Receiver volume to less than the Main Receiver volume in the BOTH switch position is provided. In the Guard position, A3P3 pin 11 will be low due to conduction of A3CR48. Switch A3U16B opens so the undiminished guard audio is coupled through A3R172 into the summing input of A3U15B. For the BOTH position of the T/R SELECT switch, A3P3 pin 11 will be high and pullup resistor A3R73 will close the switch. With switch A3U16B closed, the low side of A3R77 is AC grounded supplying an attenuated guard signal from the wiper through summing resistor A3R172. Potentiometer A3R77 is adjustable to any desired attenuation relative to the main audio level.

3.5 AUDIO BOARD BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.5.5 RECEIVER AUDIO PROCESSING (cont.)

Besides performing the receiver audio summing, A3U15B deemphasizes the received signals. An RC circuit consisting of A3R175 and A3C79 attenuates A3U15B output frequencies at a 6 dB/octave rate from 300 Hz to 3 kHz.

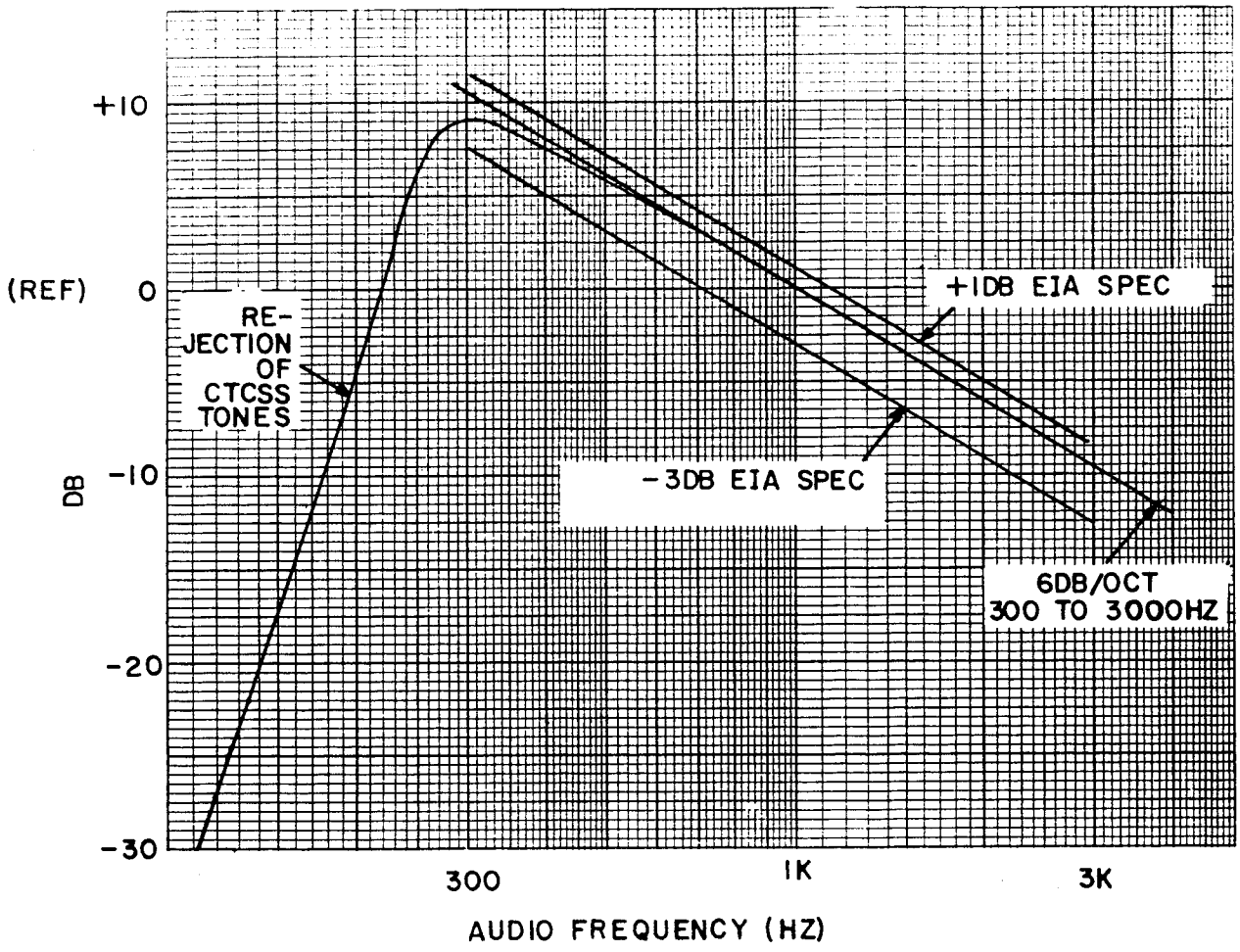
A very steep low frequency rolloff (30 dB/octave below 300 Hz) for signals from A3U15B is provided by A3U4A and A3U4B. This rolloff is primarily to reject CTCSS tones while passing audio frequencies.

The combined A3U4A and A3U4B amplifier is a MFB (multiple feedback) high-pass design with a voltage gain of 10 at pass frequencies of 300 Hz and up. It is a Chebychev design with a passband ripple of 0.1 dB. Below the pass frequency, attenuation is 30 dB per octave. Voltage divider A3R51-A3R52 (bypassed by A3C20) supplies the reference DC to operate A3U4A and A3U4B in a single-ended power supply configuration.

Output stage A3U11 is a fixed gain power amplifier block with a nominal voltage gain of 50 from input to output. Its response is essentially flat over the applicable frequency range of inputs. Combined receiver audio is coupled through A3C22 to audio level potentiometer A3R59. Isolation to prevent loading by the relatively low adjustment resistances is provided by A3R58 and A3R60. The amplified audio at pin 9 is fed to A3T1 primary through DC blocking capacitor A3C24 and resistor A3R65. The secondary of A3T1 transforms the impedance seen by the primary into 600 ohms on the secondary side. With A3K1 contacts closed, the 600 ohm output is connected directly to the audio output.

The combination of A3C25 and A3R64 is to suppress high frequency oscillation which can occur in A3U11. Transistor A3Q6 and associated circuitry provide a turn-on time delay for A3U11 to eliminate power amplifier transients from the speaker system. The delay time constant is determined by A3R63 and A3C26.

Because A3U11A has a flat frequency response, the cascaded amplifier response is influenced by CTCSS low-pass filtering and the deemphasis network of A3U15B. A typical overall audio response is shown in Figure 3.5.5-1.



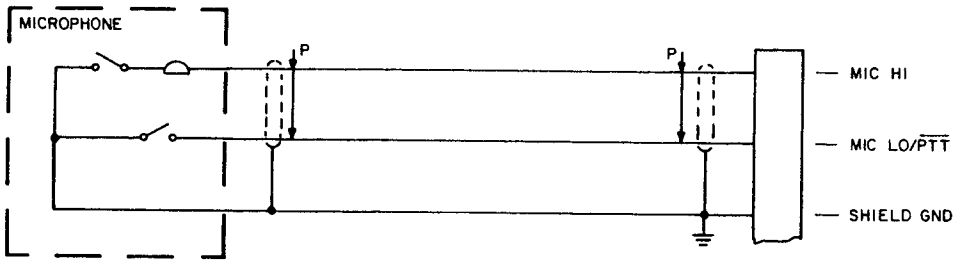
TYPICAL RECEIVER AUDIO RESPONSE
FIGURE 3.5.5-1

3.5 AUDIO BOARD BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.5.6 TRANSMIT AUDIO PROCESSING AND SWITCHING

Transmit audio processing includes limiting, frequency response shaping and signal routing functions. The input microphone audio is applied to A3P3 pins 4 and 5. The processed modulation output exits the Audio Board at A3P3 pin 8. Processed modulation is sampled and injected into the audio system as transmit sidetone.

The microphone wiring, external to the Audio Board, is similar to that shown in Figure 3.5.6-1. With this configuration, low-level mic audio is transferred to the audio input pins with a twisted-shielded pair for hum and noise rejection.



TYPICAL MICROPHONE WIRING DIAGRAM
FIGURE 3.5.6-1

Transformer A3T2 (DC blocked by A3C35) is the input for the transmit audio. The terminating load for the microphone element is A3R94. DC bias for the microphone element is also supplied through A3R94 with A3C40 completing the MIC LO return path for AC.

Both TX (high) and $\overline{TX}$ (low) are generated when $\overline{PTT}$ is grounded. With $\overline{PTT}$ grounded by the MIC key, A3Q7 is saturated supplying switched +15 VDC. The switched +15 VDC is used to power external encoders or devices. With $\overline{PTT}$ low, A3Q9 turns off applying turn-on bias to A3Q8 through A3CR43. Transistor A3Q8 saturates pulling $\overline{TX}$ low for the Synthesizer transmit logic. $\overline{TX}$ is also used by the squelch logic circuit to mute Main and Guard received audio.

3.5 AUDIO BOARD BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.5.6 TRANSMIT AUDIO PROCESSING AND SWITCHING (cont.)

The microphone input level from A3T2 is adjusted by A3R99 to control the signal amplitude fed to A3U5A. The preemphasis generated by A3U5A is a result of the opamp gain versus frequency response due to feedback components A3R103, A3R104 and A3C44.

The preemphasized output from A3U5A is coupled through A3C45 to a symmetrical diode limiter consisting of resistors A3R105 and A3R107 plus diodes A3CR26 and A3CR27. Operationally this limiter is the same as the main squelch limiter except the clipping level is 1.4 volts peak-to-peak.

Inverting buffer A3U5B is nearly a unity gain stage. The input resistance of A3R108 has minimal loading effect on the limiter circuit. The low output impedance of A3U5B effectively drives the low pass with a negligible effect on the calculated value of A3R112. This amplifier plus A3U6A and A3U6B are all referenced to the same voltage determined by divider A3R121, A3R166 and A3R122. A filter capacitor (A3C56) prevents interaction between the amplifying stages.

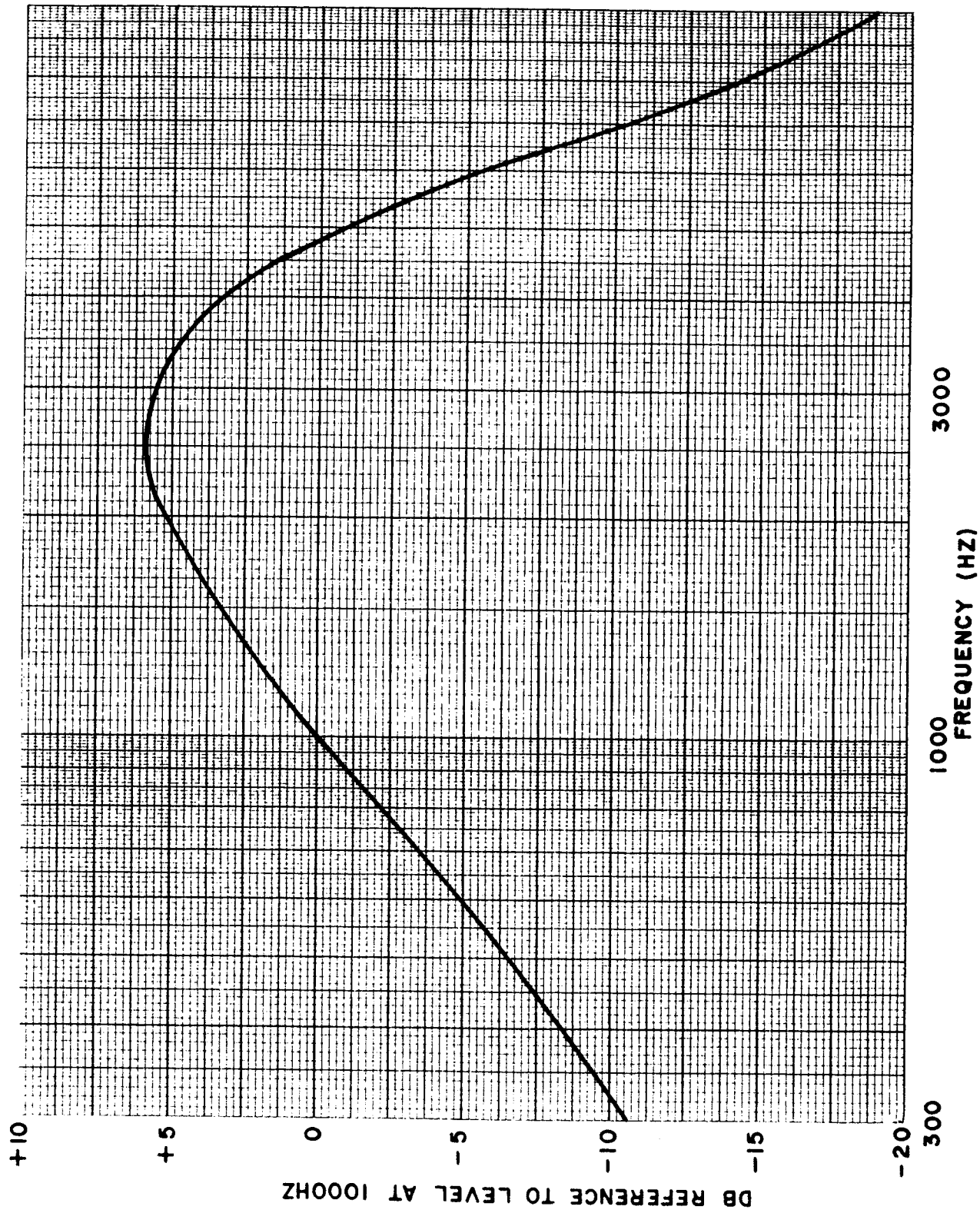
A steep high frequency rolloff is provided by A3U6A and A3U6B plus the associated RC feedback components. This rolloff is primarily to minimize transmitter frequency components in excess of 3 kHz.

The combined A3U6A and A3U6B amplifier is a MFB low pass design with a voltage gain of 4 at pass frequencies below 3 kHz. It is a Bessel design with attenuation of 24 dB/octave above the passband.

The final modulation stage (A3U9B) is a wideband summing amplifier for CTCSS tones plus voice modulation inputs. The summed output is coupled through closed switch A3U10B and A3C91 to modulate the transmitter. Overall response of the transmit audio processing is shown in Figure 3.5.6-2.

3.5.6.1 MODULATION GATING

In receive, A3Q5 is biased on by base current through A3R167 and A3R123. With the collector of A3Q5 saturated, switches A3U10B and A3U10D are both off, blocking audio. When $\overline{\text{PTT}}$ is keyed, the Synthesizer seeks a new lock frequency. During the unlock interval, A3CR46 cathode is low, ensuring A3U10B and A3U10D are held off. After frequency lock is achieved, SYNTH UNLOCK goes high which allows the R/T Assembly to transmit. The RF sensor of the R/T Assembly detects the presence of RF and pulls the TX power monitor low.



TRANSMIT AUDIO PROCESSING
FIGURE 3.5.6-2

3.5 AUDIO BOARD BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.5.6.1 MODULATION GATING (cont.)

Transistor A3Q5 is turned off allowing the control inputs of switches A3U10B and A3U10D to rise to 10 VDC. Switches A3U10B and A3U10D are then closed and A3U10D passes de-emphasized modulation to the sidetone input of audio amplifier A3U11. The deemphasis network is formed by A3R53 and A3C32. Simultaneously A3U10B completes the circuit to the modulation output.

3.5.7 CTCSS TONE ENCODING AND DECODING

Custom LSI chip (Large Scale Integration) A3U14 is designed for the purpose of encoding and decoding any one of 32 EIA tones. A 1.0 MHz quartz crystal (A3Y1) determines the frequency of a clock oscillator within A3U14.

PROGRAMMING CODE
(FOR CTCSS PRODUCTS)

TONE NO.	FREQ.	CODE	PIN 10	PIN 11	PIN 12	PIN 13	PIN 14
1	67.0	XZ	0	0	0	0	0
2	71.9	XA	0	0	0	0	1
3	74.4	WA	0	0	0	1	0
4	77.0	XB	0	0	0	1	1
5	79.7	SP	0	0	1	0	0
6	82.5	YZ	0	0	1	0	1
7	85.4	YA	0	0	1	1	0
8	88.5	YB	0	0	1	1	1
9	91.5	ZZ	0	1	0	0	0
10	94.8	ZA	0	1	0	0	1
11	97.4	ZB	0	1	0	1	0
12	100.0	1Z	0	1	0	1	1
13	103.5	1A	0	1	1	0	0
14	107.2	1B	0	1	1	0	1
15	110.9	2Z	0	1	1	1	0
16	114.8	2A	0	1	1	1	1
17	118.8	2B	1	0	0	0	0
18	123.0	3Z	1	0	0	0	1
19	127.3	3A	1	0	0	1	0
20	131.8	3B	1	0	0	1	1
21	136.5	4Z	1	0	1	0	0
22	141.3	4A	1	0	1	0	1
23	146.2	4B	1	0	1	1	0
24	151.4	5Z	1	0	1	1	1
25	156.7	5A	1	1	0	0	0
26	162.2	5B	1	1	0	0	1
27	167.9	6Z	1	1	0	1	0
28	173.8	6A	1	1	0	1	1
29	179.9	6B	1	1	1	0	0
30	186.2	7Z	1	1	1	0	1
31	192.8	7A	1	1	1	1	0
32	203.5	M1	1	1	1	1	1

(LOGIC ONE IS 10VDC)

3.5 AUDIO BOARD BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.5.7 CTCSS TONE ENCODING AND DECODING (cont.)

The 1.0 MHz output of the crystal oscillator is internally divided and synthesized to provide precise timing signals for the encode and decode circuitry external to the chip.

The frequency select code on pins 10 through 14 of A3U14 determines the sub-audible tone frequency to be synthesized or decoded. The tone select input lines are active lows which are inverted by A3U13 buffers. The logic levels at A3U14 input pins are +10V logic levels as shown in the preceeding table. Pin 14 is the least significant bit (LSB) and pin 10 is the most significant bit (MSB) of the code.

The Custom LSI chip can simultaneously encode and decode whenever power is applied to the Audio Board. Diodes A3CR32 and A3CR33 inhibit the external encode and decode circuitry unless the $\overline{\text{TONE ENABLE}}$ is low. When the CTCSS tone is desired, the $\overline{\text{TONE ENABLE}}$ is inverted by buffer A3U13. This inverted output (+10V) back biases the diodes so A3U8A and A3U8B are free to operate.

3.5.7.1 CTCSS ENCODING

Consider the tone encode function of A3U14. Pins 6, 7, 8, and 9 are the outputs of a four-stage binary up-down counter which is clocked at a multiple of the desired encode frequency. Pin 6 is the MSB and pin 9 is the LSB of the binary counter. An R-2R ladder, such as A3R162, is a conventional method for converting digital outputs to analog signals with an amplitude proportional to the binary count. The counter goes through a complete up-down count cycle for each cycle of the encoded frequency so a stair-stepped triangular wave is generated at pin 6 of the ladder. The output of the ladder is filtered and shaped by A3C65 and diode clipped in opamp stage A3U8B. The encoder output stage (A3U9A) is level adjusted by A3R152. A high-frequency rolloff for the encoded output is provided by A3R151 and A3C70. Frequency accuracy is within $\pm$ 0.1 Hz of the selected EIA tone.

3.5.7.2 CTCSS DECODING

The following concerns the CTCSS tone decoder. Unsquelched Main Receiver audio from buffer A3U1A pin 1 is direct coupled through resistors to the plus (+) input of A3U1B. Direct coupling establishes a DC reference voltage for A3U1B (a multiple feedback low pass filter). The output at A3U1B pin 7 is capacitively coupled into limiting amplifier A3U7A.

3.5 AUDIO BOARD BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.5.7.2 CTCSS DECODING (cont.)

A voltage divider (A3R131 and A3R132) attenuates the square waved output presenting a smaller version of the square wave to the digital filter input.

The digital filter network is composed of A3R133 and A3R134 and "charge-trapping" capacitors A3C74 through A3C77 which are driven by pins 15, 16, 17 and 18 of A3U14. These pins act as switches to ground that open and close at the CTCSS rate. A definite pattern of switch closures is generated by A3U14. See Figure 3.5.7-1.

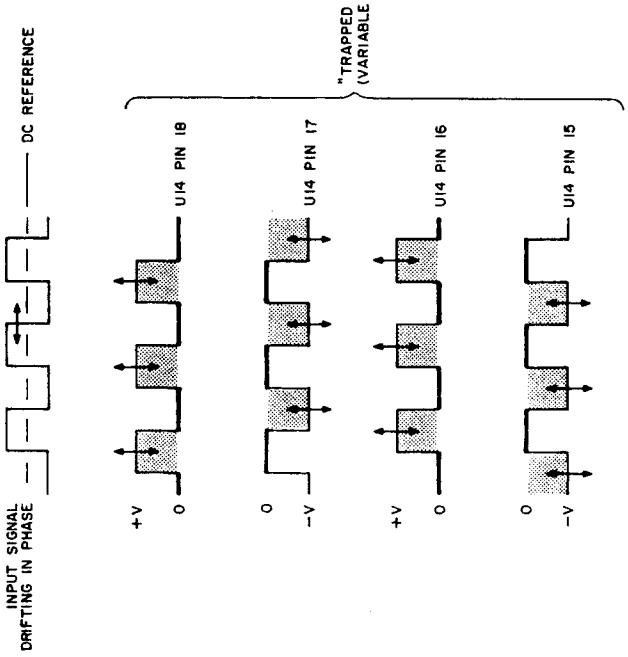
The switch closures are indicated by the presence of a dark line. The portion of the cycle with the two-headed arrow indicates the DC level trapped by the capacitors. The instantaneous DC levels depend on the phase relationship of the signal input with respect to the digitized inputs. Also shown is a decoded digital filter output for a synchronized tone frequency of 203.5 Hz. The "trapped charge" waveshapes appear only when the sub-audible signal is within the passband of the programmed frequency (typically $\pm$ 1.5 Hz bandwidth).

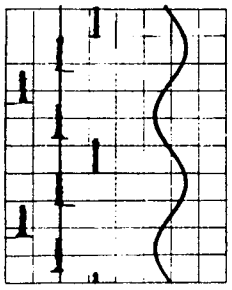
The charge time constant for each capacitor is essentially the RC product of 100 kohm and 1 uf. If the frequency difference between the received input tone and the digitized signals exceeds $\pm$ 1.5 Hz, the commutating capacitors cannot follow the DC level shifts because of their time constants. Then the synchronous adding effect at A3U7B pin 5 is lost and the filter has no AC output.

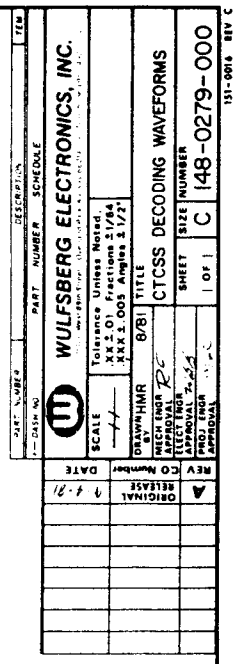
With the correct CTCSS tone frequency present, the low level output is amplified and rectified by A3U7B to provide a detected DC level which is compared by A3U8A to a fixed reference obtained from a voltage divider. If the DC exceeds the reference, comparator output A3U8A pin 1 switches high to remove the main squelch inhibit at A3CR11.

3.6 GUARD RECEIVER BLOCK DIAGRAM AND CIRCUIT THEORY

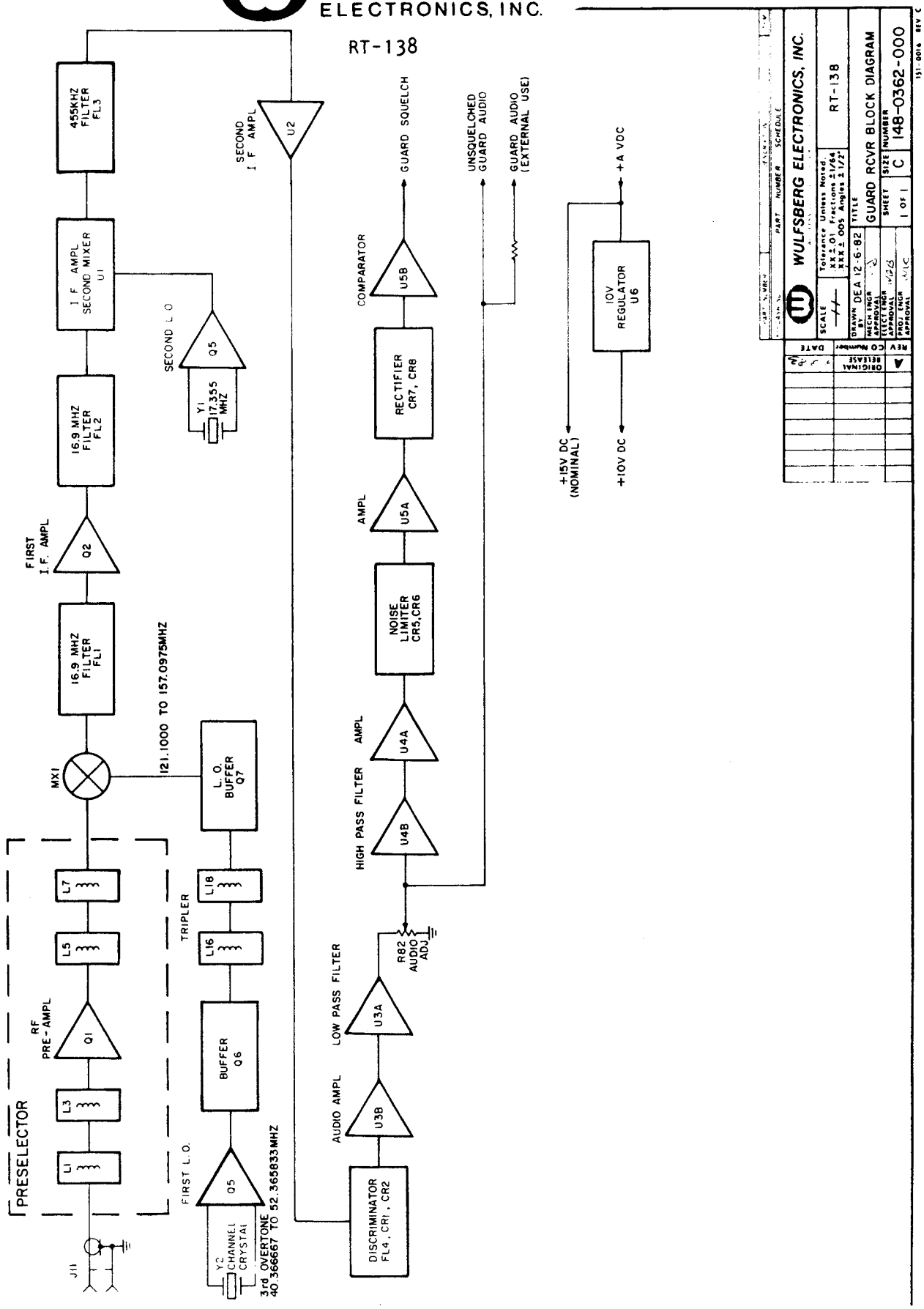
The RT-138 Guard Receiver is a self-contained single channel dual conversion superhetrodyne receiver. The block diagram is shown in Figure 3.6-1. The Guard Receiver design is similar to that of the Main Receiver.







CTCSS DECODING WAVEFORMS
FIGURE 3.5.7-1



GUARD RECEIVER BLOCK DIAGRAM
FIGURE 3.6-1

3.6 GUARD RECEIVER BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

The preselector features a four-pole filter with an RF preamp between each pole pair. These circuits are broadly tuned to accept the desired frequency but attenuate the image frequency.

The design has a first intermediate frequency (IF) of 16.9 MHz and a second IF of 455 kHz. FM detection is accomplished by a 455 kHz ceramic discriminator.

Crystal oscillator A8Q5 determines the channel frequency for the receiver. The third overtone crystal frequency is tripled to provide low side receiver L.O. injection.

3.6.1 PRESELECTOR

The first preselector section couples the RF signal to the RF preamp (A8Q1). The first tuned stage consists of A8L1 and A8C1 and is inductively coupled to the second tank section (A8L3 and A8C2). The output is coupled by A8C3 to RF preamp A8Q1.

The RF preamp is a bipolar transistor with excellent inter-modulation characteristics. Device current is determined by A8R1 and A8R2. Power is applied through A8R4 and decoupled by A8C5 and A8C6. The collector output is coupled to the second set of preselector filters by A8C7.

The second filter set provides an impedance match to the balanced mixer (A8MX1). A preselector test point is provided by A8TP1.

3.6.2 LOCAL OSCILLATOR AND TRIPLER

The local oscillator (A8Q5) consists of a modified Colpitts oscillator using a third overtone crystal. Feedback capacitors are A8C44 and A8C43. Components A8L12 and A8L13 suppress fundamental mode operation of the crystal. Supply voltage for the oscillator is +10 VDC regulated by Zener diode A8VR1.

A buffer stage (A8Q6) follows the oscillator and is biased by A8R35, A8R36 and A8CR4. Operating current is set by A8R37. The output, rich in third harmonic, is coupled by A8C50 to a double-tuned circuit resonated to the third harmonic.

Buffer A8Q7 provides power gain for the tripled signal. The transistor operating current is set by A8R42. The device's collector impedance is matched through a 4:1 impedance transforming balun (A8T1) and coupled to mixer A8MX1. A test point is provided by A8TP2.

3.6 GUARD RECEIVER BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.6.3 BALANCED MIXER AND FIRST IF

The receive signal and the local oscillator injection are both combined at A8MX1 (doubly balanced mixer) yielding a difference signal of 16.9 MHz. This IF signal is matched by A8C10, A8L8 and A8C11 into the first monolithic crystal filter (A8FL1). The filter output is matched to IF amp A8Q3 by components A8C12, A8C13, A8L9 and A8C15.

The first IF amplifier consists of A8Q2 and its associated circuitry. Gate bias voltages are generated by a divider consisting of A8R6, A8R7 and A8R8. Gate No. 2 bias is decoupled by A8C14 and A8C16. Drain supply is fed through a decoupling network consisting of A8R9, A8R11, A8C86 and RF choke A8L10.

The 16.9 MHz signal is matched into the last monolithic crystal filter by A8C20, A8L10 and A8C91. The filter output is matched to the following stage by A8C21, A8L11 and A8C86.

3.6.4 SECOND L.O., MIXER AND IF

Transistor A8Q3 is a crystal-controlled Pierce operating at 17.355 MHz. The L.O. signal is DC blocked and coupled by an RC network to mixer pin 12 of A8U1. The 455 kHz difference is taken from pin 1 of A8U1.

The mixer output of A8U1 is resistively matched to A8FL3. This filter provides some adjacent channel selectivity plus spurious response rejection. The filter output feeds gain stage A8Q4. The transistor is biased by A8R21 and A8R22 then coupled into A8U2 by A8C33.

The three-stage limiting amplifier of A8U2 drives a ceramic piezoelectric discriminator (A8FL4).

3.6.5 DISCRIMINATOR AND AUDIO AMPLIFIER

The discriminator circuit consists of A8FL4, hot-carrier diodes A8CR1 and A8CR2 plus associated filtering components. This combination of piezoelectric filtering and diode detectors produces the familiar "S" curve associated with FM detection. The curve is extremely linear for normal system deviations of $\pm$ 5 kHz.

3.6 GUARD RECEIVER BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.6.5 DISCRIMINATOR AND AUDIO AMPLIFIER (cont.)

Recovered discriminator audio is typically 100 mV peak-to-peak, and therefore the primary function of A8U3B is audio amplification. The high impedance noninverting plus (+) input of A8U3B and A8R46 provide minimal discriminator loading. Voltage gain of A8U3B is determined by resistors A8R48 and A8R47. The low output impedance of A8U3B effectively drives receiver output stage A8U3A.

The final audio output stage (A8U3A) is a low pass filter design with flat audio response extending to 10 kHz. Beyond 10 kHz, the frequency rolloff is 12 dB/octave. The cascaded audio amplifiers reduce the unwanted 455 kHz component to an acceptable level. Level control A8R82 is adjusted for 0.60 VRMS output with 3 kHz modulation.

3.6.6 SQUELCH

The Guard Receiver contains its own noise squelch. The active devices of the noise activated circuit are A8U4 and A8U5. To derive the squelch trip signal, the detected audio is clipped, average detected, and then compared to a fixed DC reference by a level detector.

Adjusted audio is coupled to A8U4B, a multiple feedback active filter designed to reject audio components below 8 kHz. This design is a three-pole filter which has a rolloff characteristic of 18 dB/octave and a voltage gain of two. Capacitors A8C69, A8C70, A8C71 and resistors A8R55, A8R56 and A8R57 provide the frequency response shaping feedback.

The high-passed audio (noise) from A8U4B is fed to a variable gain stage (A8U4A) through coupling capacitor A8C72. In this circuit, the output voltage can be varied from 20 dB gain to 20 dB loss by A8R61.

Diodes A8CR5 and A8CR6 plus resistors A8R67, A8R64 and A8R68 perform a limiting function to clip high-level random noise spikes. This circuit provides symmetrical clipping with an output of nearly 3 volts peak-to-peak.

Opamp A8U5A provides a low impedance driving source for the diode detector consisting of A8CR7 and A8CR8, plus DC filtering components A8C77 and A8R77. Voltage divider A8R73, A8CR9, A8R90 and A8R74 set a reference voltage of 3.4 VDC for the non-inverting plus (+) input terminal of comparator A8U5B. During signal reception, 10 kHz noise and detected DC level decrease. With a strong signal, the detected level falls below the plus (+) terminal reference voltage, A8U5B senses this condition and its output jumps to the upper "rail" of the opamp. Resistors A8R75 and A8R76 provide hysteresis, which insures the comparator is insensitive to chatter.

3.6 GUARD RECEIVER BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.6.6 SQUELCH (cont.)

The positive output level attained at A8U5B pin 7 is a function of the opamp and its supply voltage. To maintain hysteresis independent of the supply voltage, A8CR10 and A8R79 clamp the output level for the hysteresis circuit to 10.6 VDC. Therefore, the positive feedback (hysteresis) via A8R75 and A8R76 is immune to supply voltage changes.

3.6.7 10 VDC REGULATOR

The Guard Receiver assembly contains its own "on-board" voltage regulator (A8U6). The +15 VDC supply voltage is filtered by A8C79 and applied to A8U6. Voltage divider A8R80 and A8R81 program the 8V regulator to provide 10 VDC for the squelch circuit.

3.7 POWER SUPPLY BLOCK DIAGRAM AND CIRCUIT THEORY

The Power Supply block diagram is shown in Figure 3.7-1. This supply uses a regulating Pulse Width Modulator (PWM) to convert 27.5 VDC aircraft power into three regulated output voltages, +28 VDC, -28 VDC and +5 VDC. The design provides current limiting for the 5 volt supply and for the entire supply. Integrated circuit regulators are used to regulate the +28 and -28 VDC output. The regulators are internally current limited.

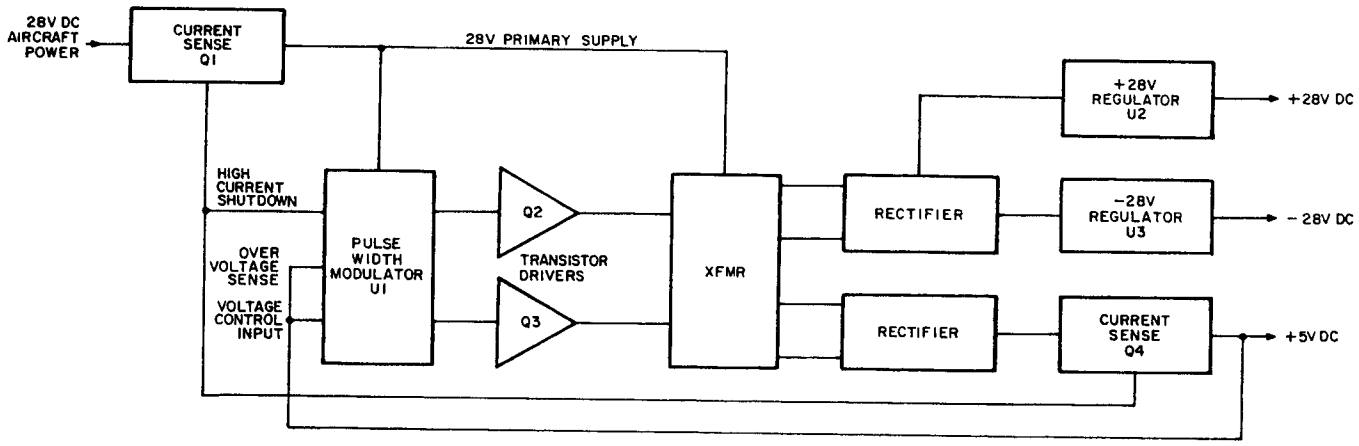
3.7.1 PULSE WIDTH MODULATOR

The manufacturer's block diagram for the Pulse Width Modulator is shown in Figure 3.7-2.

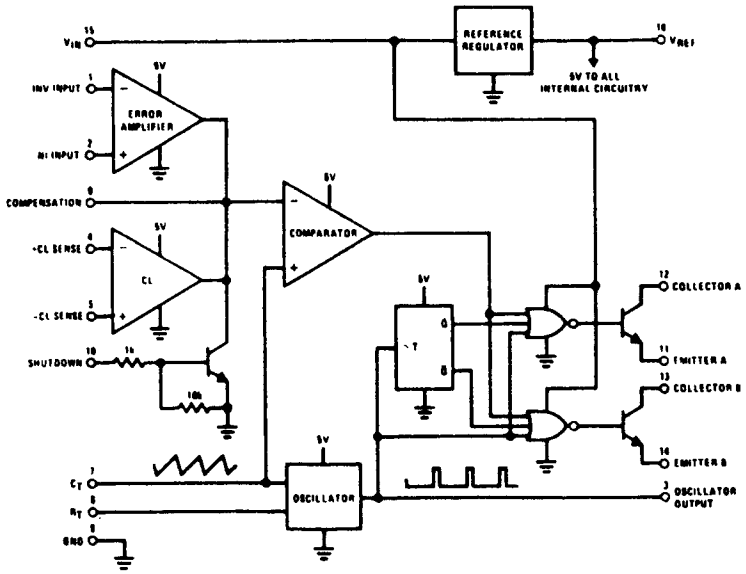
The on-chip oscillator frequency is determined by external components connected to pins 6 and 7. The sawtooth waveform from the oscillator establishes a toggle point for the comparator. The oscillator also drives the T flip-flop so the output transistors are driven 180^{o} apart. The OR gates allow the internal comparator to gate the flip-flop outputs, resulting in a varying duty cycle to the output transistors.

Comparator pin 4 is used as an over-voltage sensor. When pin 4 goes above ground, the comparator output goes high and disables the outputs through the comparator and OR gate.

The shutdown pin (10) is used when either current limiter reaches an over current condition.



POWER SUPPLY BLOCK DIAGRAM
FIGURE 3.7-1



PULSE WIDTH MODULATOR BLOCK DIAGRAM
FIGURE 3.7-2

3.7 POWER SUPPLY BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.7.1 PULSE WIDTH MODULATOR (cont.)

The error amplifier compares a reference voltage to a variable voltage on pins 1 and 2. The error amplifier output varies the non-inverting input to the comparator to change the pulse width. When the device is regulating properly, the voltages on pins 1 and 2 will be equal.

3.7.2 POWER SUPPLY CIRCUIT THEORY

The detailed circuit theory understanding will be aided by referring to the Power Supply schematic, Figure 5.1-5.

The open collector outputs of the PWM are pulled up by resistors A2R26 and A2R27. These two outputs, (180^{o} apart) are coupled to the bases of Darlington drive transistors A2Q2 and A2Q3 through A2C8 and A2C9.

Transformer A2T1 steps up the voltage to the secondary windings 4, 5 and 6 and steps down the voltage at windings 1, 2 and 3. The center tapped full wave bridge rectifier (A2CR6, A2CR7, A2CR8 and A2CR9) provides both the positive and negative supply voltages.

3.7.3 +28 VDC AND -28 VDC REGULATORS

Positive voltage from the bridge is filtered by A2C14 and A2C15 and regulated by A2U2. The output voltage is determined by voltage divider A2R17 and A2R18.

Negative voltage is filtered by A2C17 and A2C18 and regulated by A2U3. The output voltage is determined by divider A2R19 and A2R20.

3.7.4 5 VDC REGULATOR

Pins 1 through 3 of A2T1 supply push-push square waves to drive the 5V switcher. Inductor A2L2 is the energy storage choke and A2CR10 is the flyback diode associated with the switching supply. The 5V output is divided by A2R10 , A2R28 and A2R9 and coupled to the PWM error amplifier on pin 1. The PWM 5V reference is divided by A2R6 and A2R7 to provide a 2.5V reference on pin 2. In normal operation pins 1 and 2 will be equal. Resistor A2R28 is used to adjust the +5 VDC output to 5 $\pm$ 0.1 VDC.

3.7 POWER SUPPLY BLOCK DIAGRAM AND CIRCUIT THEORY (cont.)

3.7.5 OVER VOLTAGE PROTECTION

Should the 5V line exceed 6.2V, Zener diode A2CR11 will conduct forcing PWM pin 4 above ground to drive the PWM to a shorter pulse width. Diode A2CR12 keeps this pin from exceeding 0.6V.

3.7.6 CURRENT LIMITING

The 5V line current is sensed by A2Q4. When the current through A2R21 exceeds 2A, the collector output of A2Q4 turns on A2Q1. Transistor A2Q1 will also turn on when the total power supply current exceeds 2A. In either current limit condition, PWM pin 10 is pulled up, which shuts down the supply.

3.7.7 POWER-UP CIRCUIT

A power-up circuit is provided by A2C10, A1CR1, A2R11 and A2CR3. This circuit prevents the Power Supply outputs from going over-voltage when power is first applied.

3.8 +15 VDC REGULATORS

The Chassis contains two series regulators to convert 27.5 VDC aircraft power to +15 VDC. These regulators are located inside a cover on the Rear Panel of the unit.