2GHZ Two Watt IF/RF MODULE
PS1454_OBR_2W_IF_RF.doc

PS-1454 Rev 3 14 Jan 2003 3:48pm Revise CX72300 to use 18 bit mode
Rev-2 7 Nov 2002 Revised charge Pump Formula, Page 5, Relax Phase Noise
Rev-1 13 Nov 2001

RF requirements: Jim Riddle
IF/ Microcontroller requirements: Scott Dennison

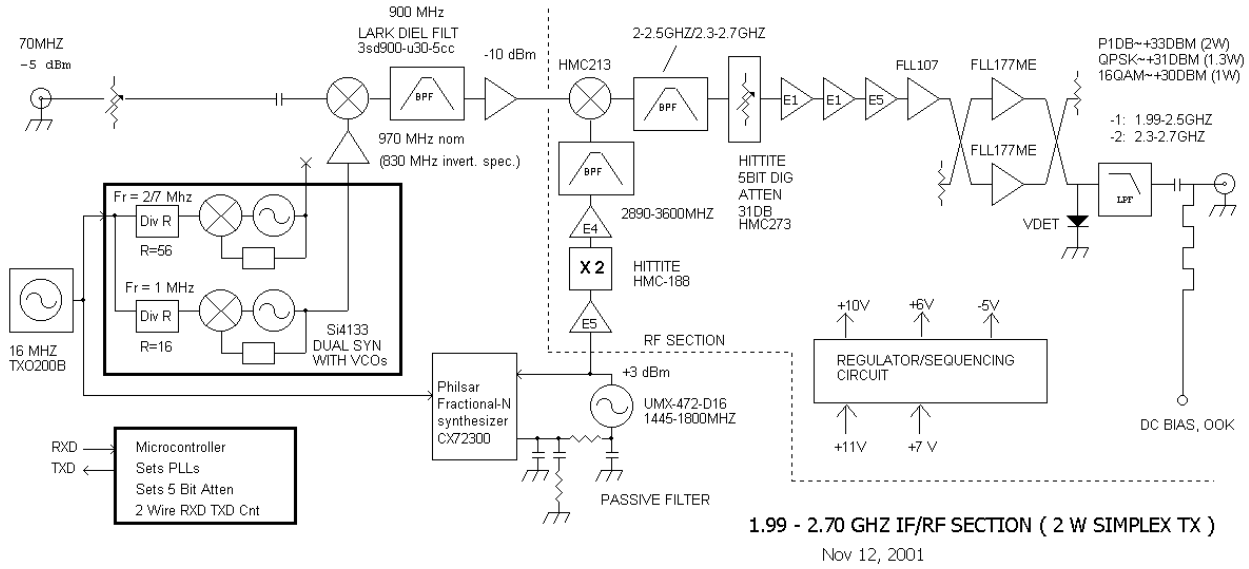

Figure One Block Diagram

Figure One shows the block diagram of the IF/RF assembly. The 70 MHz input can be analog or digital. It is upconverted to 900 MHz IF, filtered, then reconverted to an output frequency between 1.99 to 2.7 GHz. The output passes through a step attenuator and a power amplifier. The step attenuator is set to provide the proper linearity for each modulation type and is adjusted across the tuning band.

1.0 ELECTICAL SPECIFICATIONS:

1.1 Frequency Range:	1.99-2.5GHz/2.3-2.7GHz
1.2 Power Output	Psat= +33dBm Typ. P(QPSK)= +31dBm Typ. P(16QAM)= +30dBm Typ.
1.3 LO Input:	1.45-1.8GHz @ +3dBm Typ. (HSLO)
1.4 IF Input:	Frequency 70 MHz +/- 15 Mhz Impedance 75 ohms

Return Loss	24 dB
Connector	MMCX, (50 ohm version)

1.5 Internal IF:	900MHz @ -10dBm
1.6 Signals In/Out:	2GHz; 50 ohm (SMA) "OOK" Tone (-20dBm) (Feedthru) +10 to + 48VDC @ 6A max. (Feedthru)
1.7 DC Input:	+11V @ 1A max. +7V @ .45A max.
1.8 Power Monitor:	
1.8.1 DC Voltage for Psat:	+.8V to +1.2V
1.8.2 DC Voltage for no RF:	<100mV
1.8.3 DC Load Resistance:	10K ohm
1.9 Variable Pout:	Adjustable, 30 dB in 1dB steps from P1dB
1.10 Harmonics:	<-46dBc (Psat=+33dBm)
1.10.1 Spurious	
1.10.1.1 In-Band:	<-45dBc
1.10.1.2 Out-of-Band:	<-46dBc (Psat= +33dBm)

1.11 **DC Connector:**

8 pin 2mm connector (AMP 173981-8)

J8-1	TXD	Serial Word to Microcontroller	
J8-2	RXD	Serial Word from Microcontroller	
J8-3	+7VDC	450 ma Max	(150 ma IF section) (300 ma RF section)
J8-4	+7 V RTN		
J8-5	+11 V RTN		
J8-6	+11 V RTN		
J8-7	+11 V }	1 A	(RF Section)
J8-7	+11 V }		

1.12 Reference Crystal

1.12.1 Frequency	16 MHz

1.12.2 Stability +/- 2 ppm

1.13 Overall Unit

1.13.1 Frequency Stability
IF in Transmit out +/- 10 KHz

1.13.2 Phase Noise

Foffset	dBc/Hz
100 Hz	-68
1 KHz	-72
10 KHz	-82
100 KHz	-103
1 MHz	-120

2.0 ENVIRONMENTAL SPECIFICATIONS:

2.1 Operating Temp. Range: -30deg C to +70deg C case temp.

3.0 PHYSICAL SPECIFICATIONS:

3.1 RF Output:	SMA female
3.2 Vbias Tee/OOK:	Capacitive feedthru (47pF)
3.3 GND:	Solder lug
3.4 IF Input	MMCX female (50 ohm type) 75 ohm
3.5 DC Connector	8 pin 2mm header AMP 173981-8
3.6 Test Connector	16 pin SULLINS PPPN162GFNS

4.0 Microcontroller functions:

The serial control word enables all the functions, RF switches and an attenuator. Lock detect status and power amp detector voltages are returned on the serial data line. Bill Brown and his software department will determine the protocol for these RXD and TXD lines.

Whenever the module is powered on, the RF power amplifier must be disabled until all the oscillators have locked up. The unit shall reset to the last set of programmed frequencies and switch settings. A test tune algorithm will be developed to sweep the sources across the entire band and learn the 5 bit attenuator settings. It is expected that we will copy the Code Runner approach. The test tune algorithm will be available to the factory but not the end user.

4.1 Microwave Attenuator

A 5 bit digital attenuator precedes the RF power amplifier. The function is to back off the signal levels to achieve the needed amount of signal linearity. Some gain adjustment is also used

to compensate for amplitude ripples in the amplifier. The attenuator steps from 0 dBr to 31 dBr in 1 dB steps. The polarity of the control line is active low, with 5 volts at high.

4.2 ADC inputs

Three lines are sampled by input Analog to Digital Converters (ADC): The RF power detect, UHF lock detect and RF lock detect. The value of the RF power detector, and the status of the lock detect lines (locked/unlocked) is sent back to the external controller

4.3 LED outputs

The microcontroller samples the Si4133 lock detect (U_LOCK) and the CX72300 lock detect (R_LOCK) , then enables the corresponding LEDs.

U_LOCK	lock	< 0.5 V
	Unlock	> 1.5 V
U_LOCKED	locked	= output low
	Unlocked	= open drain
R_LOCK	lock	> 2.0 V
	Unlock	< 1.0 V
R_LOCKED	locked	= output low
	Unlocked	= open drain

4.4 UHF synthesizer

The UHF local oscillator is generated with a Silicon Labs Si4133 UHF synthesizer. This device has two on board VCOs, integrated loop filters and phase lock loops. The RF frequency is set to a nominal 970 MHz. 830 MHz may be selected if the spectrum is inverted. The RF reference divider is set to 16 in each case for a phase detector frequency of 1 MHz. The IF section is powered down.

4.4.1 Si 4133 parameters:

AUXSEL =	011	= Lock detect
IFDIV =	xx	= IF VCO Divider
LPWR =	0	= "< 500 ohms"
XPDM =	0	= Ref Amp Pwr Dwn at D=0
AUTOPBD =	0	= Software controlled Pwr Dn
AUTOKP =	0	= Kp gain set by software

Write to RF2 register (RF1 not used):

PDAB =	1	= Reference Amp on
PDIB =	0	= IF synthesizer on
PDRB =	1	= RF synthesizer on

KP2 =	00	= RF2 Phase Detect. Gain = 1
NRF2 =	970	= Output Freq = 970 MHz
RRF2 =	16	= Phase detector freq = 1MHz
KPI =	xx	= IF Phase Detector Gain = ½
NIF =	xx	= IF VCO Freq = 633 1/7 MHz
		(divided by 8 output = 79 1/7 MHz)
RIF =	xx	= Phase detector freq = 2/7 MHz

4.5 Microwave synthesizer

4.5.1 CX 72300 parameters:

A Skyworks (Philsar/Conexant) CX72300 synthesizer is used to tune the microwave VCO. The VCO is followed by a frequency doubler and the output frequency is 900 MHz above the transmitted frequency.

We only use the main synthesizer. The auxiliary synthesizer is powered down. Direct Modulation, Frequency Power Steering and Modulation Data are not used. The CX72300 RF synthesizer will tune 1445 to 1800 MHz. The preferred mode of 18 bit resolution can be used to meet any future 2 GHz frequency plan.

The frequency step size, with a reference frequency of 16 MHz and 18 bit mode, will be 122.0703125 Hz (16MHz x 2 / 2^18).

The VCO frequency is calculated from:

4.5.2 Fvco = (Ftransmitter + 900 MHz) / 2

Example: If Radio transmits at 2500 MHz, Set VCO frequency to 1700 MHz.

The charge pump gain is calculated with a formula to compensate for the VCO tuning sensitivity.

The Main phase detector gain is calculated from:

4.5.3 PDg = INT [(Fvco /1800) x 31]

The gain is 25 at Fvco = 1445 MHz, and 31 at 1800 MHz.

Note that the phase detector gain was calculated to compensate the tuning curve of UMX-472-D16, a low noise VCO from Universal Microwave. If a new VCO is substituted, a new charge pump equation should be derived. The procedure to calculate this equation is as follows. The VCO is set to the highest frequency and the charge pump gain set to maximum. The high end of the VCO has the lowest tuning sensitivity in MHz/Volt. A passive loop filter is designed for optimum performance for this combination. A typical open loop bandwidth is in the 3 to 5 KHz range. The goal is to then maintain a constant open loop gain at all frequency settings; this will ensure that the loop has proper phase and gain margin and will remain stable. When this is met, the phase noise also remains relatively constant.

From classical feedback theory the open loop gain of the circuit is:

$$G(s)H(s) = \frac{Kp\ Kv}{sN} \cdot F(s)$$

Where Kp is the phase detector gain, Kv is the VCO "gain", F(s) is the transfer function of the loop filter, s is the Laplace integator and N is the division ratio Fvco/Fdet.

Kp is made proportion to N/ Kv to ensure G(s)H(s) remains constant.

4.5.4 CX 72300 example:

For an example, to get a transmitter frequency of 2300.25 MHz set the Philsar CX72300 at 1600.125 MHz. (2 x 1600.125 – 900 MHz).

Fvco = 1600.125 MHz (Fout = Fvco X 2)
Fdiv_ref = 16 MHz

Nfrac = Nfractional = Fvco / Fdiv_ref = 100.0078125

Nint = ROUND[Nfract] = 100 ← Rev 3
Note: ROUND rounds the number to the nearest integer

The Main Divider Register is programmed with the integer portion of Nfrac – 32.

Nreg = Nint – 32 = 68 ← send to Main Divider Register

The dividend is calculated by multiplying the remainder by 262144 (2^18):

Dividend = ROUND((Nfrac – Nint) x 262144) ← Send to Main Dividend MSB and LSB Registers. ← Rev 3

Note that this is a 18 bit signed value that can range from –131072 to +131071.

All the Auxiliary registers are unused and should be in a power down state.

Main Reference Frequency Divider Index	=	0	= Div by 1
Main Phase Detector Gain	=	31	= Max gain (see formula for PDg above)
Main Pwr Steer/Lock Det En	=	0	= Lock Det on
Aux Phase Det Gain	=	not used	
Aux Pwr Steer/Lock Det En	=	not used	

4.5.5 Description of Pins on Microcontroller:

Pin #	Name	Function	
1	MOSI	input program chip	(Programming pins attach
2	MISO	input program chip	to 6 pin 2mm Molex conn.)
3	SCLK	input program chip	
4	RESET	input program chip	(normally pulled high)
5	VCC	+5V	
6	GND	GND	
7	XTL2	Crystal Out, 7.368MHz	
8	XTL1	Crystal In, 7.368MHz	
9	RXD	Received Data from external serial controller	
10	TXD	Transmitted Data to external serial controller ***Specifications to be described by Bill Brown and his Software Department.***	
11	UDAT	UHF Data to Si4133; see data sheets for Si4133	
12	UCLK	UHF Clk to Si4133	
13	UENB	UHF Enable to Si4133	
14	R_LOCKED	RF synthesizer lock detect	
15	U_LOCKED	UHF synthesizer lock detect RF/UHF: low = locked, hi = unlocked	
16	PA_EN	Enable Power Amp	low = disable, active high = ON
17	VCC	+5V	
18	GND	GND	
19	ATT1	Attenuator 1dB Bit	low = 1 dB, active high = 0 dB
20	ATT2	Attenuator 2dB Bit	low = 2 dB, active high = 0 dB
21	ATT4	Attenuator 4dB Bit	low = 4 dB, active high = 0 dB
22	ATT8	Attenuator 8dB Bit	low = 8 dB, active high = 0 dB
23	ATT16	Attenuator 16dB Bit	low = 16 dB, active high = 0 dB
24	RDAT	RF Data to CX72300; see data sheets for CX72300	
25	RCLK	RF Clk to CX72300	
26	RENB	RF Enable to CX72300	
27	VCC	+5V	
28	AGND	GND	
29	AREF	+3.00 V +/- 1 percent	
30-34	UNUSED	Maybe next time.	

35	U_LOCK	UHF lock detect from Si4133; ADC input Lock < 0.5 VDC Unlocked > 1.5 VDC Read level and enable LED. Report back status.

Pin #	Name	Function
36	R_LOCK	Lock > 2 VDC Unlocked < 1 VDC Read level and enable LED. Report back
37	PWR_DET_A	RF power amp detector voltage; ADC input Full Power nominally 1VDC
38	VCC	+5V
39	GND	GND
40-44	UNUSED	Not Connected

4.6 Test Connector

To test and troubleshoot the IF/RF assembly with a microcontroller, a multipin 2mm header is provided on the underside of the assembly. The lines are attached to override the logic states of the microcontroller. The synthesizer lines are 3 volt logic, the attenuator lines are 5 volt logic.

J10-1	Not Connected	
J10-2	GND	
J10-3	UCLK	Si4133 CLK
J10-4	UDAT	Si4133 DATA
J10-5	2DB	2dB BIT
J10-6	UENB	Si4133 ENABLE
J10-7	8DB	8dB BIT
J10-8	16DB	16dB BIT
J10-9	1DB	1dB BIT
J10-10	4DB	4dB BIT
J10-11	RDAT	CX72300 DATA
J10-12	RENB	CX72300 ENABLE
J10-13	RCLK	CX72300 CLK
J10-14	PWR_DET	Sample of RF Detector
J10-15	GND	
J10-16	PA_ENB	Power Amp Enable; Open = Enable Short = Off