SAU-1900E CIRCUIT DESCRIPTION & THEORY OF OPERATION

Product Description: SAU-1900E Wireless Local Loop

The function of the SAU-1900E is to provide a wire-free interface between a Telephone Service Provider and the telephone wiring in a home or business. Up to 4 Telephones (or equivalent telephone-like loads) may be connected through up to 1000 Feet (~300 meters) of wire to the SAU-1900E to support a single-line (single phone number) telephone service. The SAU-1900E interfaces to the Public Switched Telephone Network (PSTN) via the 1900 MHz CDMA Cellular Phone Interface per IS-98A.

The SAU-1900E provides all features associated with a standard 'Plain Old Telephone System' (POTS), plus Enhanced Features including the following:

Telephone Battery Voltage (-60 to -68VDC),
Telephone RINGING Voltages (40 Vrms minimum),
Call Progress Signaling (Dial Tone, Stutter Tone, Receiver Off-Hook, Busy Signal, etc.)
Caller-ID Signaling per GR-30-CORE,
Call Waiting,
Cancel Call Waiting,
3-Way Calling,
Call Forwarding, and
Cancel Call Forwarding.

An ***optional*** expanded feature of the SAU-1900E is the ability to add an analog modem to the telephone line. This allows for the addition of an analog fax machine or a personal computer equipped with a modem.

The following major functional blocks accomplish these features of the SAU-1900E:

a. Subscriber Loop Interface Circuit
b. 12V Battery Management
c. Caller-ID FSK Generator
d. Interface Circuitry
e. DC/DC Power Supply
f. CDMA RF and Baseband Interface
  f.1. Receiver
  f.2. Transmitter
  f.3. Synthesizer
  f.4. Baseband ASIC
  f.5. Mobile Station Modem
g. MDL-1 Fax/Data (***Optional***)

SAU-1900E CIRCUIT DESCRIPTION & THEORY OF OPERATION

SUBSCRIBER LOOP INTERFACE CIRCUIT (SLIC):

The Subscriber Loop Interface Circuit (SLIC) provides the means to transfer the voice-band audio signals between the CDMA board and the Telephone line. It also uses the output of the DC Power supply to provide telephone line power and power for ringing telephone extensions. All of these functions are accomplished via a single IC (U501) with external components selected to establish the desired operating parameters. A more detailed description follows:

Operating Modes:

The SAU controller (located on the CDMA board) establishes the following operating modes by setting the GPIO (and/or GPIO_Expansion) lines to an appropriate state.

1. **Low Power Scan**: In this state, the SAU controller configures the DC/DC converter to supply a –65VDC to the Battery Input pins of U501. All other internal circuits, except for the off-hook detector, are turned off to conserve power. The SAU will be placed in this state when U501 indicates that all attached telephone-like loads are in an On-Hook (high DC impedance) condition.
2. **Powerup, Forward**: This is the normal condition when at least one phone is Off-Hook and a conversation is either in-progress or in the process of being established. The DC/DC power supply is configured for -24 Vdc (rather than -65 Vdc) to conserve power (for increased talk-time on battery power) and to reduce heat dissipation in U501. While in this mode, the SLIC acts as a DC Current Source to provide a 30 mA loop current for powering the telephone. In this state the SLIC IC converts AC Loop Current Signals from a telephone into AC Voltage Signals for transmission to the CDMA CODEC. In addition it operates as a signal amplifier for transmitting voice band analog signals received from the CDMA CODEC to the low impedance telephone receiver.
3. **Powerup, Reverse:** Same as the state listed above, except the Tip and Ring voltage polarities are reversed from normal {normally Tip is more positive than the Ring line}. This state is infrequently used, typically for signaling equipment other than telephones, which may also be attached to a telephone line. Normal telephone operation is unaffected by Tip/Ring polarity.
4. **Ring State:** When configured for this mode, and with the DC/DC power supply configured to provide -65 Vdc, the SLIC can apply a 20 Hz, 40-55 Vrms Ring signal to alert a telephone user of an in-coming call. In addition, U501 will monitor the ring current to determine when the phone is taken off-hook so that the SAU controller can terminate the ring signal and the Powerup Forward state can be established.

Contrary to standard wireline ringing signals, wherein a Telephone Central Office supplies a 90 Vrms ringing signal which is superimposed upon a battery voltage of -48 Vdc, the SAU-1900E produces the ring signal by reversing the tip/ring voltage at a 20 Hz rate. Wave shape is controlled to produce a balanced trapezoidal waveform with a peak-to-peak swing of approximately 120 Vpp and a RMS voltage between 40 Vrms and 55 Vrms. This waveform is sufficient to ring all telephone types (including older phones with electromechanical ringers) under short loop length (< 100 meters) applications. In addition, up to 4 Ringer Equivalent Network (REN) loads may be simultaneously attached while still providing the minimum 40 Vrms ringing signal.

5. **Disconnect State:** During this mode of operation, the SLIC is put into a low power mode and the Tip/Ring lines put into a high impedance condition (> 100K Ohms). This state is applied for approximately 800 mSec after receipt of a far-end disconnect message to signal telephone answering machines (and other, similar equipment) to stop recording and to go into an On-Hook condition.

Satisfactory audio performance relies upon the ability of this circuit to provide an electrical interface to a telephone which adequately emulates that provided by standard whirling telephone networks. The key

features that must be controlled are AC Termination Impedance, Transmit Gain (Telephone Microphone Output to Codec Input direction), Receive Gain (Codec Output to Telephone Speaker direction), and Hybrid Balance.

AC Impedance: The SAU is designed to apply a typical telephone network AC load to an attached telephone. Ideally, the SAU will present an impedance which can be modeled as a 270 Ohm resistor in series with a parallel combination of a 750 Ohm resistor and a 0.15uF capacitor (270 + 750‖0.15uF). This will result in a frequency dependant impedance characteristic which simulates a medium length PSTN network cable and which has been shown to work well with real telephone devices in providing good audio quality.

The desired AC impedance is established by converting the AC *current* signals generated by the Telephone Microphone circuitry into an AC *voltage* signal and feeding back a controlled portion of this voltage signal back to the Tip/Ring line. By changing the magnitude of the feedback signal with respect to frequency, the desired AC impedance can be generated. U501 performs the initial current-to-voltage conversion by providing an AC Voltage signal at U501-3 (VITR) which is proportional to the AC current flowing through the Tip and Ring lines. Amplifier U503, with the RC feedback network comprised of R525, R526, R527, and C521 provide a frequency dependent feedback signal which is injected into U501-5 (RCVN) via voltage divider circuit R508, and R529 and DC blocking capacitor C509.

U501 then amplifies the AC voltage signal at pin 5 (RCVN) and applies the resulting signal across the Tip and Ring pins of the telephone line.

Transmit Gain: This is a measure of the ratio of the signal power supplied by a telephone to that arriving at the CDMA CODEC Input pin. For simplification, all measurements are made assuming the SLIC impedance is 600 Ohms (across all frequencies). {For example, if the Tip/Ring AC signal voltage is 500mVrms - the signal power is determined to be 0.417 mW (or -3.80 dBm). Similarly, if the signal voltage received at the Codec Pins is determined to be 250 mVrms, the signal power is determined to be -9.80 dBm and the Transmit Gain is determined to be -9.80 - (-3.80) = -6.0 dB}

The magnitude of the Transmit Gain is set by the circuitry which establishes the AC Impedance (and hence the Tip/Ring AC voltage), by R509, and by the Codec Gain Setting Resistor (R63: 10K Ohms) on the CDMA board. Typical values for Transmit Gain in the SAU are -6 to -9 dB.

The actual magnitude of the audio or voice signal received at the other end of the telephone network will be determined by multiple factors. The specific impedance characteristics of the telephone attached to the SAU. The transmit gain in the SAU. Any amplification or attenuation applied to the signal in the cellular domain. The impedance characteristics of the far end telephone and of the intervening telephone network.

Receiver Gain: This is a measure of the ratio of the signal power supplied by the CDMA CODEC Output pin to that injected into the Tip/Ring wire pair. As above, all measurements are made assuming a load impedance of 600 Ohms (across all frequencies). {For example, if the Codec output AC signal voltage is 500mVrms - the signal power is determined to be 0.417 mW (or -3.80 dBm). Similarly, if the signal voltage supplied across the Tip/Ring wire pair is determined to be 250 mVrms, the signal power is determined to be -9.80 dBm. And the Receiver Gain is determined to be: -9.80 - (-3.80) = -6.0 dB}

The magnitude of the Receiver Gain is set by the receiver buffer amplifier U503B. The gain network comprised of R520, R521, R522, R523, R533, R534, R535, and R540. The divider network comprised of R511 and R529. The gain supplied by U501, the AC impedance of the telephone network and the attached load. Typical values for the Receiver Gain in the SAU are -2 dB to +2 dB.

As for the Transmit Gain discussion above, the actual signal levels received at the telephone speaker are dependent upon many factors beyond direct control of the SAU.

Hybrid Balance: This is a measure of how well the subscriber loop interface circuit provides matching impedance to an attached telephone load. A good impedance match will minimize the reflection of signals injected by the CDMA CODEC into the SLIC circuitry. Poor hybrid balance will result in excessive echoes heard by the person connected at the far-end of a telephone link (e.g. the far end party hears echoes of their own voice). Echoes are more noticeable (and thus, undesirable) in the presence of networks which have time lags greater than 100 mSec. Most digital cellular networks will have time lags significantly larger than 100 mSec.

The Hybrid Balance is directly affected by the magnitude of Transmit Gain, Receiver Gain, and the Hybrid Matching Network provided by R510, R555, and C535. Typical values for the attenuation provided by the Hybrid balance circuitry in the SAU are -35dB to -40 dB at 1000 Hz and with a 600 Ohm AC load across the Tip/Ring wire pair.

In a real application, the actual values for the Transmit Gain and Receiver Gain are strongly affected by the AC impedance characteristics of the attached telephone. The SAU circuit design, however, is optimized around a nominal telephone AC impedance of 600 Ohms. This means the magnitude of signal echoes heard at the far-end of the telephone link could vary significantly from installation to installation if no other means of echo cancellation were provided. In the SAU, however, real echo performance has been significantly improved by the providing additional of echo cancellation in the digital domain of the DSP-based Vocoder (located in the CDMA board).

12V Battery Management

The purpose of this functional block is to perform the following tasks:

a. Automatically disconnect the Battery from the circuit load when its voltage level falls below 9.5 Volts so that the battery will not be damaged due to over-discharge.

   This function is accomplished by the following components (not listed in signal order): D802, D805, Q805, Q806, Q808, R814, R816, R820, and R821. Zener Diode D805 (8.2 Vdc), diode D802 (forward drop ~0.6 Vdc), and Q808 together establish the dropout voltage for the circuit. Once the Battery voltage is insufficient to maintain Q808 in a conducting condition (VBAT approximately 9.5 VDC) the base-to-emitter voltage at Q806 will fall to zero and Q806 will turn off. This will result in the gate voltage at power switch Q805 to rise to the battery voltage and turn off the current flow to the circuit load.

   Normal operation will be restored upon the application of System Power (+16 to +30.4 Vdc) or by installing a battery with sufficient charge remaining for operating the SAU. {Note: it is fairly trivial to demonstrate that the SAU will power up when System Power is applied, how this is accomplished when a fresh battery is installed is less obvious. The presence of capacitor C814, resistors R819, R815, R816 and transistor Q806 support the latter event. After C814 has been fully discharged (e.g. following removal of a discharged battery) installation of a fresh battery will cause a charging current to flow through C814. This charging current will temporarily turn on transistor Q806 to allow switch Q805 to conduct. Once Q805 is conducting, and as long as the battery voltage is sufficiently high, power will be applied to the emitter of Q808 which will, in turn keep Q806 (and thus Q805) in the ON state. At this point the WLL will remain operational until the battery voltage level again drops to 9.5 Vdc.}

b. Apply a temperature dependent float voltage to the Battery when AC power is available.

   Battery charging current is supplied via the parallel connection of series pass transistors Q801, Q802 and Q803 through a current limiting resistor R803. The float voltage (measured at the junction of D807 and C804) is nominally 13.8 Vdc at room temperature (25 °C). Voltage accuracy is assured using a precision DC Voltage Regulator (U802) as the voltage reference for the DC Voltage Control loop formed by Op Amp U801, D801, Q801, Q802, Q803, D807, TH801, and R804 through R806. Under nominal conditions of temperature and supply voltage, this circuit will restore a fully discharged battery to approximately 85% of capacity after a 24 hour charging period.

   The float voltage is changed by approximately -26 mVdc / °C using Thermistor TH801 and resistor network R803 through R806.

c. Provide a DC signal voltage to the SAU-1900E ADC which is proportional to the Input System Power voltage so that the controller will know when normal power is no longer available and that the unit is operating from the Battery.

This is accomplished using a simple voltage divider comprised of R824 (10K) and R825 (1K). The output of this divider is connected to the Analog MUX (U20) on the CDMA board.

d. Provide a DC signal voltage to the SAU-1900E ADC which is proportional to the Battery Voltage so that the controller can determine if the battery is approaching the end of its useful charge when it is operating from Battery Power.

   This is accomplished using a simple voltage divider comprised of R801 (1M) and R802 (200K). The output of this divider is connected to the Analog MUX (U20) on the CDMA board.

e. Provide a DC signal voltage to the SAU-1900E ADC which is proportional to the Battery Temperature so that the SAU-1900E controller can monitor the environmental conditions and ensure that the Battery is not charged or operated outside its specification limits (-15 °C to +50 °C).

   The output of the precision DC Voltage Regulator (U802) is applied to R901, R902, and Thermistor TH901 to provide a signal proportional to the Battery Temperature. The Thermistor TH901 is mounted on the MAIN board in close proximity to the Battery compartment in order to maximize the temperature measurement accuracy.

f. Provide a means for the SAU-1900E controller to Enable/Disable Battery charging and operation in response to the environmental conditions (Battery Temperature and/or Battery Voltage).

   Applying +5 VDC to the base of transistor Q804 can disable the battery charging circuit. Turning Q804 ON will drop the voltage reference at U801 pin 2 from 5.0 Vdc to approximately 3 Vdc. In response to this change, the output of U801 will increase and the charging voltage at the collectors of transistors Q801 through Q803will decrease to approximately 8 VDC ceasing the battery charging function.

   The output of the battery can be disconnected from the circuit by applying +5 Vdc to D803. This action will turn Q807 ON, resulting in transistor Q806 turning OFF. Once Q806 is no longer conducting, the gate of the Analog Switch Q805 will float to the battery voltage and the switch will go into a high impedance state. If normal system power is not available, the battery path will remain disabled and the SAU will be powered down.

   Upon application of normal system power (+16 Vdc to +30.4 Vdc), Q808 will turn ON and force Q806 into a conducting state, thus re-enabling the battery power path.

g. Switch between Battery Power and AC/DC adapter power without interrupting a conversation in-progress.

   Dual Diode D802 is used to feed power to the SAU from either the Battery or the AC/DC adapter power. The source with the highest voltage will supply power to the circuitry. Since the AC/DC adapter has been selected to yield a minimum of 15.2 Vdc under worst case loading and AC voltage conditions, while the maximum battery voltage will be 14.5 Vdc (under minimum temperature conditions), the AC/DC adapter power will provide power whenever AC power is available. When AC power is lost, D802 will smoothly transfer circuit load to the Battery path.

Caller-ID GENERATOR:

The Caller-ID Generator circuit is used to produce a sequential series of tones on the telephone Tip/Ring lines which encode the Time, Date, and Calling Party Number in accordance with the guidelines established in Bellcore Document GR-30-CORE (LSSGR: Voice band Data Transmission Interface Section 6.6). The heart of this generator is a standalone microcontroller (U701), which is normally in a low-power idle state and is only awakened by the SAU processor to perform its task during an incoming call.

The signal produced by the Caller-ID Generator is a continuous phase binary frequency-shift-key (FSK) signal that represents a binary 0 as a 2200 Hz sinusoid and a binary 1 as a 1200 Hz sinusoid. The transmission rate of the data transmitted on the Tip/Ring wire pair is 1200 baud. The generator produces

the desired frequencies using a simple 8-bit D/A circuit formed by the summation of the data at the digital output pins PC0 through PC7. These signals are fed into a low pass filter/amplifier circuit comprised of U702A and U702B to smooth out the discontinuities inherent with digital waveform synthesis. By sequentially programming the data at ports PC0 through PC7 the microcontroller can produce the necessary sinusoidal signals.

Upon the occurrence of an incoming call, the SAU processor will apply the first Ring-burst to the Tip/Ring wire pair. It then wakes up the Caller-ID Generator by applying a Logic 0 to U701-2 (IRQ). After a brief interval (less than 10 mSec) the crystal oscillator X701 will turn on and U701 will 'wake-up'. Once sufficient time has passed to ensure that the microcontroller is active and the tip/ring voltage is stable (approximately 500 mSec) the SAU processor will Serially transmit the Time, Date, Calling Part Name (if available) and Calling Party Number (if available) to the Caller-ID generator at 38400 Baud. All data transfers from the SAU processor to the Caller-ID microcontroller are asynchronous and no handshaking is performed (meaning the microcontroller does not acknowledge receipt of the data).

Once the microcontroller has received all necessary data (as determined by comparing the number of received bytes to the expected number of bytes provided at the beginning of the data transfer) it will begin modulating output pins PC0 through PC7 in order to generate the required FSK data sequence. For a typical set of caller-id data, the microcontroller will complete its data transfer in less than 1 second.

The SAU controller will disable the Caller-ID generator (by applying a logic '1' to U702-2 (IRQ) upon either of the following. Detection that a phone has been taken Off-Hook or when the time to generate the next Ring Burst arrives (4 seconds after completion of the previous Ring burst).

The FSK data is injected into the SLIC receive path via the low pass filter output U702B-7 at R533. Component values have been selected to ensure that the signal level will be adequate at the Tip/Ring wire pair to satisfy the signal level requirements of caller-id receivers (e.g. greater than -30 dBm (30mVrms into a 900 Ohm Load) at the receiver input). Typical FSK data signal levels will fall between -18 and -15 dBm at CLID receiver.

INTERFACE CIRCUITRY

Integration of the various functional blocks is accomplished by the interface circuitry in the SAU. The various tasks accomplished by this section are as follows:

a. Logic level translation between the 3.3 V logic in the CDMA circuitry and the 5 V logic on the SLIC, DC/DC Power Supply, Battery Management, and Caller-ID Generator circuitry

   Conversion of Logic Output signals from 3.3 V logic to 5 V logic is accomplished via U904 which is a dedicated logic level converter IC. This circuit accepts output signals GPIO_0, GPIO_2, GPIO_3, GPIO_4, Serial output MSM_TXD and CTS from the CDMA Processor and converts these to 5V logic.

   Conversion of 5V Logic Input signal MSM_RXD to a level suitable for injection onto the CDMA Card (<3.3 Vpk) by the resistor divider comprised of R910 and R911. The 5Vpk Off_Hook_Int signal from the SLIC circuitry is also stepped down to 3Vpk via the resistor divider circuit comprised of R907 and R908. The remaining 5V logic input signals are tied the MSM pins Keyin_0, Keyin_1, Keyin_2, Keyin_3, and GPIO_5 via the open collector outputs of Q905 through Q909 which invert the applied logic level. In the later instance the CDMA circuitry provides the pull-up resistors to its local logic reference of 3.3Vdc.

b. Input/output (I/O) Port Logic Expansion.

   The original quantity of output control lines available from the CDMA circuit was insufficient to accomplish the necessary control tasks. This limitation was overcome by using a Serial-to-Parallel port expander circuit (IC's U901 and U902). This circuit utilizes three (3) of the existing output lines as Clock, Data, and Strobe signals to produce a total of sixteen (16) new output signals for an improvement of thirteen data lines. Each bit can be individual set under software control without

affecting the other bits at a rate of 10000 times per second (or better) which is more than sufficient to perform necessary hardware tasks in the SAU.

c. Dual Tone Multi Frequency (DTMF) detection and decoding

Detection of telephone key press events is necessary for call origination over the cellular interface, as well as for collection of dial strings for conference calling. A dedicated DTMF detection IC (U905) w provides a Data valid strobe, as well as a 4 Bit representation of the decoded data to the SAU controller.

The DTMF Detection circuit is normally unpowered. When the SLIC circuit detects an Off Hook condition, it's output signal (Off_Hook_Int) is used to turn on transistor Q910 which provides power to the DTMF circuitry. This approach was used to reduce power consumption in the SAU in thereby improve Battery Standby time.

DC/DC Power Supply

Theory of Operation for SAU-1900E DC-DC Converter Power Supply Board, Maxon America Board #610-040-0006, Rev. 3

Overview:

The DC-DC Converter Power Supply Board provides power the SAU-1900E system, including the CDMA and MDL-1 daughter boards, as well as power for the Subscriber Loop Interface Circuit (SLIC) section, Caller-ID section, and all other Main board sections.

The DC-DC converter board receives power from the battery management circuit of the Main board. This battery management circuit receives power from two sources: 1. A 12V sealed lead-acid battery or 2. An AC-DC linear transformer. These two voltage inputs provide a voltage in the range of +9.5VDC to +30.4VDC, which is used as the input power to the DC-DC converter board.

The DC-DC converter board consists of four major sections:

1. Main board Connector
2. Primary +5V supply (+5V)
3. Primary -24V or -65V supply (VBAT (-24V/-65V)).
4. LED display (IN_SERVICE, BATT_SIGN, and MALFUNCTION).

The purpose of the of the +5V supply is to provide power to the following SAU sections:

1. The CDMA daughter board.
2. The MDL-1 daughter board.
3. SLIC.
4. Caller-ID.
5. General-purpose input/output (GPIO) expansion circuits.

6. Drive power for the LED's.

The purpose of the VBAT (-24V/-65V) supply is to provide power for the SLIC circuit to manage a telephone line interface circuit, primarily to ring the telephone(s), detect off/on hook conditions, and to power the telephone(s) while in conversation.

Finally, the LED section provides the status of the SAU-1900E. The IN_SERVICE indicates if the SAU-1900E is in communication with a CDMA cellular base station. The BATT_SIGN simply shows if the battery management circuit is charging the 12V lead-acid battery. The MALFUNCTION LED shows if the primary power supply fuse has been blown.

System Specifications:

Operating Temperature: -20°C to +60°C

Power input at startup with full load: 9.5VDC-30.4VDC supply with a surge output power of at least 28.5 watts (i.e. at 9.5V, must be capable of sourceing at least 3.00A, and at 30.4V, must be capable of sourcing at least 0.94A).

Power input at startup with no load: 9.5VDC-30.4VDC supply with a surge output power of at least 20 watts (i.e. at 9.5V, must be capable of sourcing at least 2.10A, and at 30.4V, must be capable of sourcing at least 0.66A).

Continuous power input with full load: 9.5VDC-30.4VDC supply with an output power of at least 15 watts (i.e. at 9.5V, must be capable of sourcing at least 1.60A, and at 30.4V, must be capable of sourcing at least 0.50A).
Overview:

The SAU-1900E power supply board shall consist of two power supplies to provide external power. One is a +5VDC@3.5A supply, which is constantly on. The second is a supply that can be switched on and off, and be switched between -24VDC@50mA (see below) and -65VDC@100mA (see below). Input voltage is from +9.5VDC to +34VDC.

+5V Output:

Output Voltage: +5VDC ±5% (+4.75VDC to +5.25VDC) under all loads
Minimum Current Output: 0mA
Maximum Current Output: 1.45A
Maximum permissible ripple: $50mV_{PK-PK}$

-24V Output:

Output Voltage: -24VDC ±5% (-22.8VDC to -25.2VDC) under all loads and during voltage switching
Minimum Current Output: 0mA
Maximum Current Output: 50mA
Maximum permissible ripple: $350mV_{PK-PK}$

-65V Output:

Output Voltage: -65VDC ±5% (-61.75VDC to -68.25VDC) under all loads and during voltage switching
Minimum Current Output: 0mA
Maximum Current Output: 100mA
Maximum permissible ripple: $350mV_{PK-PK}$

EMI/EMC:

The power supply shall emit as little EMI as possible. The power supply shall perform to all above specifications above while being subjected to the maximum allowable EMI as permitted by FCC Part 15, CE mark approvals, etc.

-24V/-65V On/Off Control Line:

Expected Levels: 0V to turn the supply off, +3.3V or +5.0V to turn the supply on.
Absolute Minimum Drive Level: -10VDC
Absolute Maximum Drive Level: +10VDC

-24V/-65V Select Line:

Expected levels: 0V to supply -24VDC, +3.3V or +5.0V to supply -65VDC.
Absolute minimum drive level: -10VDC
Absolute maximum drive level: +10VDC

IN_SERVICE LED Input:

Expected Input: +5VDC current limited with a 220Ω resistor.
Maximum power dissipation of LED: 60mW
Maximum current through LED: 20mA

IN_SERVICE LED Light Output:

Green @ 0.9mcd minimum, 2.6mcd typical @ I_F = 10mA

BATT_SIGN LED Input:

Expected Input: +5VDC current limited with a 220Ω resistor.
Maximum power dissipation of LED: 60mW
Maximum current through LED: 20mA

BATT_SIGN LED Light Output:

Green @ 0.9mcd minimum, 2.6mcd typical @ I_F = 10mA

MALFUNC LED Input:

Expected Input: +9.5VDC to +30.4VDC with constant current source of 9-11mA.
Maximum power dissipation of LED: 60mW
Maximum current through LED: 20mA

MALFUNC LED Light Output: Red @ 1.70mcd minimum, 5.0mcd typical @ I_F = 10mA

Specific Theory of Operation for the SAU-1900E DC-DC Converter Board:

Main board Connector

Overview:

The Main board connector provides a means of transferring power back and forth between the Main board and DC-DC converter board. It also has some control lines from the Main board to control the DC-DC converter board, as well as some lines to drive the on board LED's.

Specifics:

1. Pins 1 and 2 of CON601 (CON601.1 and CON601.2) are used to bring power from the Main board to the DC-DC converter board. It should have a voltage range of around +9.5V to +30.4V.
2. Pins 3 and 6 of CON601 (CON601.3 and CON601.6) provide a common ground path between the Main board and the DC-DC converter board.
3. Pins 4 and 5 of CON601 (CON601.4-5) provide +5V power at a maximum of 1.45A to the Main board.
4. Pins 8 and 9 of CON601 (CON601.8-9) provide either -24V at a maximum of 50mA or -65V at a maximum of 100mA to the Main board, based on the logic lines of DCDC_0 or DCDC_1.
5. DCDC_0 is a logic line on pin 11 of CON601 (CON601.11) that is generated by the Main board. When it is at logic low, the -24V/-65V supply is turned off. When it is at logic high, the -24V/-65V supply is turned on.
6. DCDC_1 is a logic line on pin 12 of CON601 (CON601.12) that is generated by the Main board. When it is at logic low, the -24V/-65V supply is selected to output -24V. When it is at logic high, the -24V/-65V supply is selected to output -65V.
7. IN_SERVICE is a current source generated from the Main board to drive D606. It is on pin 13 of CON601 (CON601.13).
8. BATT_SIGN is a current source generated from the Main board to drive D605. It is on pin 14 of CON601 (CON601.14).
9. MALFUNCTION is a current source generated from the Main board to drive D604. It is on pin 15 of CON601 (CON601.15).

Primary +5V supply (+5V)

Overview:

The primary +5V supply is a switching power regulator, a Maxim Integrated Products MAX797. It is capable of driving up to 5A at a nominal +5V output, with a 9.5V to 30.4V input. It is approximately 95% efficient.

Specifics:

1. U601 is a switching step down controller that maintains a nominal +5VDC by means of an internal comparator to control the duty cycles of the external MOSFET switches Q601 and Q602. When Q601 is on power is supplied to the load and inductor L601. R601 sets the output current limit when this limit is reached or the comparator senses that the output is becoming larger than the regulated voltage Q601 is turned off and Q602 is turned on. D602 rectifies the resulting voltage and allows L601 to supply the

load. R601 sets the output current limit, if the limit is met Q602 is turned off, if the comparator senses the output falling below the regulated voltage Q602 is turned off and Q601 is turned on again.
2. C606 and D601 form a capacitor charge circuit that supplies the enhancement mode gate voltage for Q601.
3. C601 controls the ramp up to full current limit (controls current inrush).
4. C602, C603, C608, C620 are high frequency bypass capacitors.
5. C604, C605, C609, C610, C619 are low ESR ripple filter capacitors.
6. C607 is an energy storage capacitor for the internal voltage regulator.
7. L602, L603 are ferrite beads for EMI protection.
8. F601 protect the circuit from external loads of greater than 3A.

Primary -24V or -65V supply (VBAT (-24V/-65V))

Overview:

The primary –24V or –65V supply is an inverting switching power regulator, using a Maxim Integrated Products MAX774. This supply has a single output that can be turned off and on or switched between –24V and –65V. It is approximately 80% efficient.

Specifics:

1. U601 has an internal voltage comparator that senses when the output voltage is below the reference voltage and switches on the external MOSFET switch Q603. When Q603 is on energy is stored in the transformers T601 secondary, Q601 is on for a period of time determined by either an internal one-shot multi-vibrator, or R602 which sets the input current level switch. When Q603 is turned off the stored energy in T601 secondary is forced through T601's primary and rectified by D603 and is supplied to the load and the feedback circuit.
2. C612, C613, Q604, R603, R604, R605, R607 form the feedback circuit that controls the output voltage level. A logic 1 voltage level on control line DCDC_1 sets a –65VDC, logic 0 sets a –24VDC. R607 ensures logic 0 level to protect the SLIC circuitry in the absence of control level on DCDC_1.
3. Q605 R606 form the shut down circuit for U602. Logic 1 level on control line DCDC_0 turns the –24V/-65VDC circuit on, logic 0 level turns the circuit off. R606 ensures the circuit is off to protect the SLIC circuitry in the absence of a control level on DCDC_0.
4. C614, C615, C616, C617 are low ESR ripple filter capacitors.
5. C618, C621 are high frequency bypass capacitors.
6. L604, L605 are ferrite beads for EMI protection.
7. F602 protects the supply from external loads of greater than 500mA.

LED display (IN_SERVICE, BATT_SIGN, and MALFUNCTION)

Overview:

There are three LED's on the DC-DC converter board that act as a man-machine interface.

Specifics:

1. D605 and D606 are connected in a similar fashion. Each LED is driven by a current source to turn the LED on.
2. D604 is illuminated only when the system fuse is blown. It is fed by a constant current source.

SAU-1900E
CDMA BOARD Theory of Operation

RF Section (Receiver):

Front-end: Signals received at the antenna in the frequency band 1930-1990MHz are passed to a duplexor (DUP1) and low noise amplifier Q6. The duplexor provides 35dB of rejection to the transmitted RF energy (1850-1910 MHz) while passing the desired receive signal in its pass band with 4dB of loss. The Low Noise Amplifier (LNA) circuit consists of transistor Q6, bias, and LC matching circuits providing approximately 20dB of gain at a Noise Figure of 1.0dB.
A Band pass Filter is provided for the Rx frequency band by FL3 (a Surface Acoustic Wave –SAW- device) which immediately follows the LNA. It has 3dB loss for pass band and 30dB rejection for out of band signals such as the transmit frequency.
The result is a signal within the RX pass band is amplified approximately 14dB gain and a 70Db rejection on out of band signals.

Down-Converter: The received signal out of front-end is fed to an active double balanced Mixer (U14) which provides the first down converter function. It down converts the Rx signal from FL3 with the UHF local oscillator (at approx. 1719 to 1780 MHz.) to produce the CDMA_RX (+/-) IF signal at 210.38 MHz.

RX IF Amplifier: The IF signal is applied to a SAW Band pass filter FL1, which provides the main channel selectivity, before being passed to the IF amplifier U8. This amplifier has an AGC gain control input which is driven from the Baseband Processor to maintain the IF output signal at approximately 5mVrms.

RF Section (Transmitter):

TX IF Amplifier: The Transmitter IF signal is generated by the Baseband circuitry at a frequency of 130.38 MHz at a fixed level of -20 dBm and is supplied to the input of the TX AGC amplifier U2. The gain of U2 is varied by means of the TX_AGC_ADJ signal under control of the Baseband Processor in order to maintain a constant RF level output. This amplifier provides a dynamic range of 90dB, allowing the gain to be varied from a level of -50dB to +40dB.

Up Converter: The output of U2 is passed through a impedance converter which converts the 500 ohms output impedance of U2 to the 12 ohms input impedance of U3 up converter

The signal from U2 (130.38MHz) is combined with the TX_LO (1719 to 1780Mhz) in the U3 up converter and converted from the TX IF frequency to the RF TX frequency (1850 to 1910 MHz). The signal is then passed through FL4 TX SAW band pass filter to reduce image products of up converter.

The filter (FL2) which follows the up converter suppresses the sum products from the up converter by 20 dB and suppresses the TX_LO (in the range of 1719 to 1780Mhz) signal by 20 dB

The up converted and filtered TX signal from FL4 TX SAW BPF, is fed to a gain block on U2 and is amplified by 14dB. Then passed through FL2 TX SAW BPF to suppress any out of band signals including TX_LO and image products of the up converter. FL2 TX SAW BPF provides 2dB loss in the pass band (1850 to 1910Mhz) and 20 dB loss on out of band.

The TX signal out of FL2 is fed to U4 TX Power Amplifier.

The Power Amplifier amplifies the signal by 28 dB while maintaining a better level on the CDMA 3rd IMD product than that specified in IS-98A.

The output of the Power Amplifier is taken via isolator IS2 to the transmit port of the duplex filter. This isolator serves to provide stable load impedance to the power amplifier regardless of duplexor load impedance or antenna termination. IS2 also serves to provide reverse isolation against other external interfering signals, which could cause generation of unwanted modulation products.

A detector circuit fed through R83 to duel diode D7. This accomplishes power level detection at the output of the transmitter. This circuit, with its pair of forward biased diodes provides self-temperature compensation.

The ceramic duplexor DUP1 provides 42dB (minimum) rejection of transmit generated noise across the receive band, 30dB rejection at second harmonic frequencies and third harmonic frequencies.

RF Section (Synthesizer):

The UHF local oscillator synthesizer is composed of four major components. These components are:
1) The Frequency Reference TCX1, which is a voltage controlled, temperature compensated crystal oscillator.
2) The Voltage Controlled Oscillator (VCO1) which generates the UHF LO directly (i.e. 1719 to 1780 MHz).
3) The Synthesizer itself (U6).
4) The VHF Voltage Controlled Oscillator on U12, Baseband ASIC.

In operation, the 19.68 MHz reference is divided within the synthesizer IC to provide a 30 kHz reference signal for the phase comparator section (internal to U6). A sample of the output from VCO1 is fed back to the 'FIN1' pin on the U6 where it is also divided to provide the feedback input to the phase comparator. The phase comparator output (pin 'DO1') is fed to the voltage control pin on VCO1 via a passive RC loop filter (loop bandwidth is approximately 500 Hz).

By changing the division ratios used by the synthesizer IC the UHF Local Oscillator frequency may be changed. This action is controlled by the Mobile Station Modem via a 3 line serial interface (Data, Clock, and Latch Enable).

For the VHF Voltage Controlled Oscillator, an VCO signal from Baseband ASIC fed in to 'FIN2' pin on the U6 and controlled by 2nd phase comparator output (Pin 'DO2') to maintain stable 420.76 MHz of 2nd Rx Local signal.

The voltage 'fine tune' control pin to the VCTCXO (TRK_LO_ADJ) is controlled by the Mobile Station Modem to follow the frequency of the Base Station's Pilot signal. A Lock Detect output is also provided, this is combined with another Lock Detect output signal from Baseband ASIC (U12) and fed in to Mobile Station Modem (U11). The Mobile Station Modem (U11) uses this Lock Detect output signal to shutdown the transmitter if an out-of-lock situation is detected.

Baseband Section (Baseband ASIC):

The Baseband ASIC (U12) is the main component used to interface the RF and Digital sections of the CDMA WLL. It performs the following major functions:

1.) Final down conversion of the RX IF signal into I and Q (phase quadrature) paths.
2.) Channel filtering, performed by 630 kHz low pass filters in the I and Q paths.
3.) Analog to Digital conversion of the RX I and Q paths (4bit wide digital I and Q outputs) with an automatic DC offset compensation provided by the MSM device.
4.) Digital to Analog conversion of the TX IF signal (digital I/Q inputs, 130 MHz output to the transmitter RF circuitry).

5.) Analog to Digital Input (multiplexed via U20) to provide measurements of Battery Temperature, Battery Voltage, System Power Voltage, RF PA detect voltage, and a Precision Reference Voltage.
6.) Synthesizer Lock Detect input (used to shutdown the transmitter on detection of an out-of-lock condition).
7.) Divider for the 19.68 MHz TCXO reference, providing reference signals TCXO/4 and CHIPX8.

In receive operation, the final down conversion from 210.38 MHz RX IF to Baseband I and Q channels is performed in the Baseband ASIC using two mixers with 210.38 MHz local oscillators in phase quadrature. These local oscillator signals are derived from a single reference at 420.76 MHz using the principle of a Div-by-2 circuit combined with an Exclusive-Or device. The 420.76 MHz signal is produced by a phase locked loop, with the VCO active device being contained in the Baseband ASIC, an external tank circuit, and an external fixed frequency synthesizer device (U6).

In transmit operation, the final up conversion of the TX Baseband signals to 130 MHz TX IF is performed in the Baseband ASIC using two mixers with 130.38 MHz local oscillators in phase quadrature. These local oscillator signals are derived from a single reference at 260.76 MHz, this oscillator signal is produced in a manner similar to the oscillator used in the receive section with the exception being that the only external component required is the tank circuit. All other components, including the PLL and synthesizer, are internal to the Baseband ASIC.

Baseband Section (Mobile Station Modem (MSM)):

The MSM (IC11) is a highly integrated ASIC which performs the majority of the digital control and data management tasks in the CDMA WLL. The following functional components (or tasks) make up this device:

1.) CDMA Core: This section includes data bus interfaces to the A-to-D and D-to-A converters in the Baseband ASIC for RX and TX I/Q data. It also performs CDMA coding, decoding, Pilot Acquisition, Data Interleaving (and de-interleaving), RX AGC control, TX AGC control, and Frequency Control.

2.) Microprocessor Core: (including external interfaces for FLASH, SRAM, and serial EEPROM memory devices).

3.) Vocoder Core: This section performs Voice Processing for both TX and RX signal paths. Supports 8 Kbits/sec and 13.3 Kbits/sec Variable Rate data compression/de-compression of the 64 Kbits/sec PCM Voice data stream (to/from the Voice CODEC (U16)).

4.) General I/O Interface: Provided for DTMF digit collection/ Line Card Control / and Sonic Alerts.

5.) Serial I/O Data Port: For support of external Test and Maintenance activities, as well as support for Digital Serial data devices.

The MSM is provided with its own 27 MHz clock, using crystal X1, with is divided by 2 and used as the main clock source for both the MSM and the Baseband ASIC.

MDL-1 FAX/DATA BOARD

Theory of operation for MDL-1 board, Maxon America, Inc. Board # 610-060-0019 rev0.

Overview:

The MDL-1 board contains a fax/data modem and a serial interface circuit. Combined with the other circuits of the SAU-1900E they allow for the modulation and demodulation of fax/data signals. This allows for the addition of a near end fax/data terminal such as a G3 analog fax machine or a personal computer equipped with a modem.

The MDL-1 board also contains RAM IC's employed as data buffers. These Buffers allow the SAU-1900E to de-couple the data transfer speed available from the digital cellular air interface from the variety of DTE transfer speeds or from the available serial data line speed.

The MDL-1 Board consists of five major sections:

1. Main Board connector.
2. Serial Interface circuit.
3. Fax/Data Modem.
4. Data Buffers.
5. LED Display

1. MAIN BOARD CONNECTOR:

Overview:

The Main Board Connector provides the power for the MDL-1 Board. It is also provides for data transfer back and forth between the Main Board and MDL-1 Board.

Specifics:

1. FAX_TXA is an analog signal on pin 1 of CON1 (CON1.1) that is provided by the modem's transmit outputs.
2. FAX_RXA is an analog signal on pin 2 of CON1 (CON1.2) that is provided by the main board for the modem's receive input.
3. Pins 3, 13, 15 of CON1 (CON1.3, 13, 15) provide a common ground path between the MDL-1 and the Main boards.
4. MSM_TXD (5V) is a digital signal on pin 4 of CON1 (CON1.4) that is provided by the Main board for the modem's digital receive input.
5. FAX_TXD is a digital signal on pin 5 of CON1 (CON1.5) that is provided by the MDL-1 board for the modem's digital transmit output.
6. RFR (FAX) is a digital signal on pin 6 of CON1 (CON1.6) that is provided by the MDL-1 board for mode control of the MSM (Mobile Station Monitor) IC's Ready to Receive signal.

7. CTS (5V) is a digital signal on pin 7 of CON1 (CON1.7) that is provided by the Main board for mode control of the Serial interface circuitry's Clear to Send signal.
8. OFF_HOOK_INT_5V is a digital signal on pin 8 of CON1 (CON1.8) that is provided by the Main board for detection of the phones hook status.
9. G_EXP_08, G_EXP_09, GPIO_6 are digital signals on pins 9, 10, and 11 of CON1 (CON1.9, 10, 11) that are provided by the Main board for future product enhancements. Not in use in the current circuit.
10. BOOT is a digital signal on pin 12 of CON1 (CON1.12) that is provided for programming U8 EPROM and is not connected on the Main board.
11. Pins 14 and 16 of CON1 (CON1.14, 16) provide +5VDC power for the MDL-1 board.

2. SERIAL INTERFACE:

Overview:

The serial interface circuitry provides the control circuitry for the transfer of the data between the SAU-1900E's digital cellular air signals and the analog modem circuitry.

Specifics:

Micro-Controller U15, ROM IC U8, voltage sensor U6, NAND-GATE IC U7, switching diode D1, Transistor Switches Q2 and Q3, along with their associated pull-up resistors and high frequency by-pass filter capacitors form the Serial interface and control circuitry for the MDL-1 board.

3. FAX/DATA MODEM:

Overview:

The Fax/Data modem provides the means of converting the analog data signals that appear on the SAU-1900E's Tell-line interface into digital data for transmission over the SAU-1900E's CDMA cellular air link. The reverse is also true it converts the digital signals received over the SAU-1900E's CDMA cellular air link are converted to analog data and placed on the SAU-1900E's Tell-line interface.

Specifics:

1. Fax/Data modem IC U10, ROM IC's U11 and U5, their associated pull-up resistors and high frequency by-pass filter capacitors form the main functional block of the Fax/Data circuitry.
2. Op-amp IC's U1, U2, U3, U4, transistor switch Q1 and analog switch IC U13 along with their associated resistors and capacitors form a filter circuit for the special control tones of CNG and CED. These tones are then provide to the Serial interface circuitry.

4. DATA BUFFERS:

Overview:

Due to the varying speeds at which data is transferred between the various formats in the SAU-1900E extra RAM is provided. These RAM IC's act as data buffers. This allows the Serial interface circuit to control the data transfers with out any loss of data.

Specifics:

1. RAM IC U9 acts as a data buffer for the Serial interface circuit.
2. RAM IC' U12 acts as a data buffer for the Fax/Data modem circuit.

5. LED INDICATORS:

Overview:

There are three LED indicators that act as a man machine interface.

Specifics:

1. All three indicators function in the same manner. They are driven by the Micro-Controller to turn them on.
2. LED D2 is current limited by R65 and indicates the SLEEP/ACTIVE State of the MDL-1 board.
3. LED D3 is current limited by R67 and indicates if the SAU-1900E is the active link.
4. LED D4 is current limited by R66 and indicates if the analog Fax link is the active link.