

Bluetooth Wireless Headset Product Specification

Product ID : ABH-204

Bluetooth Wireless Headset

1. General Specification

(1) General

This product enables convenient cord-free communication with mobile phone(CDMA/GSM/GPRS) and Bluetooth device that are compliant with Bluetooth Version 1.1 or higher. It is a highly integrated Bluetooth headset for world wide ISM band(2.4GHz). It has designed with low power consumption and most of functions can controlled by microprocessor. It will minimize your exposure to radio frequency(RF) from your mobile.

(2) Specifications

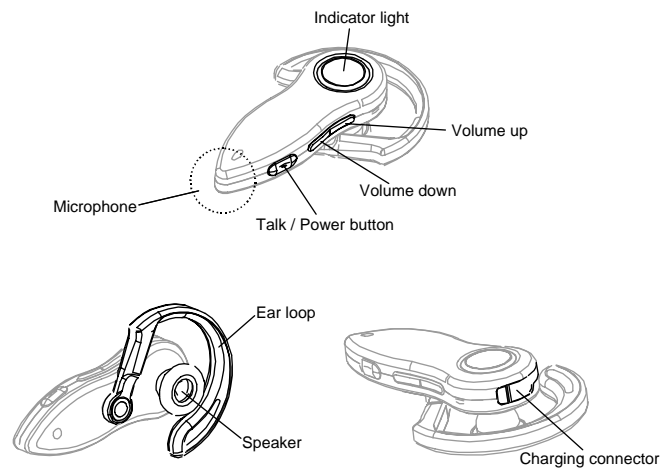
- Bluetooth™ Qualified** : Version 1.1 Compliant(Class2)
- Radio Frequency Range** : 2.402~2.480 GHz
- Transmit Power** : Typical 2dBm(1.6mW)
- Receive Sensitivity** : -78dBm
- Service Distance** : Up to 10 meters (30feet) at open field
- Security** : 56 bit encryption
- Profile** : Headset Profile
- Operating Temperature** : -10~55°C
- Dimension** : 68.5 x 26 x 25.3(L x W x H)
- Weight** : 19grams
- Charging Time** : 3 hours for 90% capacity
- Talk Time** : Up to 5hrs
- Standby Time** : Up to 150 hrs

(3) Power

- Battery** : 180mAh rechargeable Lithium Polymer
 - Charger** : DC 5V, 100mA AC adaptor (100~240V)
 - Charging Current** : 100mA
 - Battery Current (Operating mode)** : <30mA
 - Battery Current(standby mode)** : <1mA
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Bluetooth Wireless Headset

2. General Information



(1) Name of Operating Parts

Indicator light : LED displays status of the Headset. Active, Standby and Off mode.

Talk / Power Button : Controls a lot of functions of the Headset including Headset ON and OFF, as well as pairing the headset.

Volume Up/Down : Adjusts the loudness of the sound level that you hear.

Charging Connector : Socket for charging the headset battery.

Microphone : For outgoing audio.

Speaker : For including audio.

3. Operation Description

1) General Description

It supports Class2 and Class3 radio transmission without the need for an external Power amplifier. Fully integrated synthesizer without external VCO varactor diode, resonator or loop filter. It has designed for use in voice application such as hands-free kits. It has designed with low power consumption and most of can be controlled by microprocessor.

2) Radio Architecture

(1) Transmitter Architecture

-The Transmitter uses a conventional IQ modulator, as Figure 2.1 Shows. The Baseband Bluetooth signal is generated digitally and modulated in accordance with the Gaussian Frequency Shift Keying(GFSK) modulation scheme employed in Bluetooth. An additional frequency offset of to $\pm 1\text{MHz}$ can be added to the digital baseband signal.

-The baseband signal is up-converted in the in-phase and quadrature (IQ) modulator to 2.4GHz. An RF amplifier then boosts the signal level and drivers differential TX_A and TX_B.

-A conventional PLL synthesizer provides the local oscillator drive to the IQ modulator. The synthesizer produces signals at around 1.2GHz, which are then doubled to 2.4GHz. The 2.4GHz signal passes through a 90° phase splitter to provide the IQ driver to the modulator. The loop filter components for the synthesizer are internal to the chip.

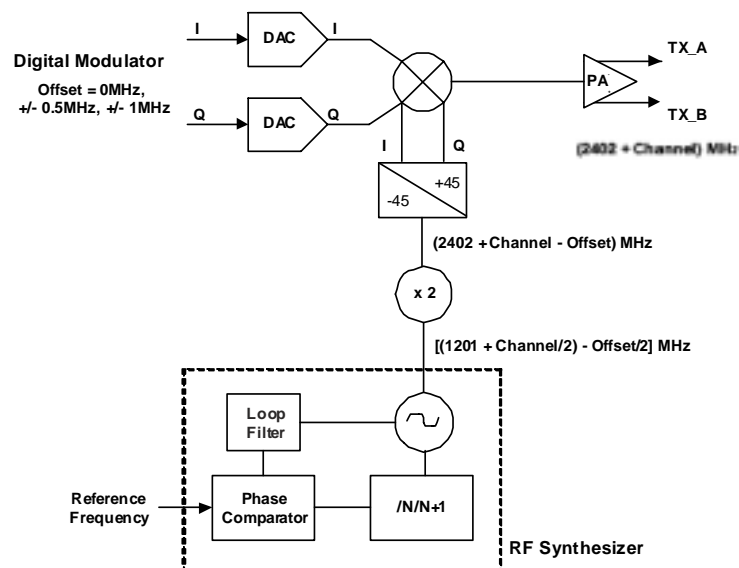


Figure 2.1 : Overview of Transmitter Architecture

(2) Receiver Architecture

-Figure 2.2 shows a receiver of a double conversion design, which uses the same synthesizer as the transmitter. The RF switch enables the use of inputs from either the differential or signal-ended receive ports. The differential ports are the same TX_A and TX_B ports utilized by the transmitter. Single-ended inputs used the RF_IN port.

-Both differential and single-ended inputs are amplified by a low noise amplifier (LNA) and

passed to an IQ mixer where the signal is then down-converted to a first intermediate frequency (IF) of 1.5MHz. This signal is amplified and filtered before undergoing a second quadrature mix to 2.5MHz. The 2.5MHz signal is further amplified and filtered. The signal is limited, sampled and then digitally demodulated. The 2.5MHz IF block also provides received signal strength indication(RSSI).

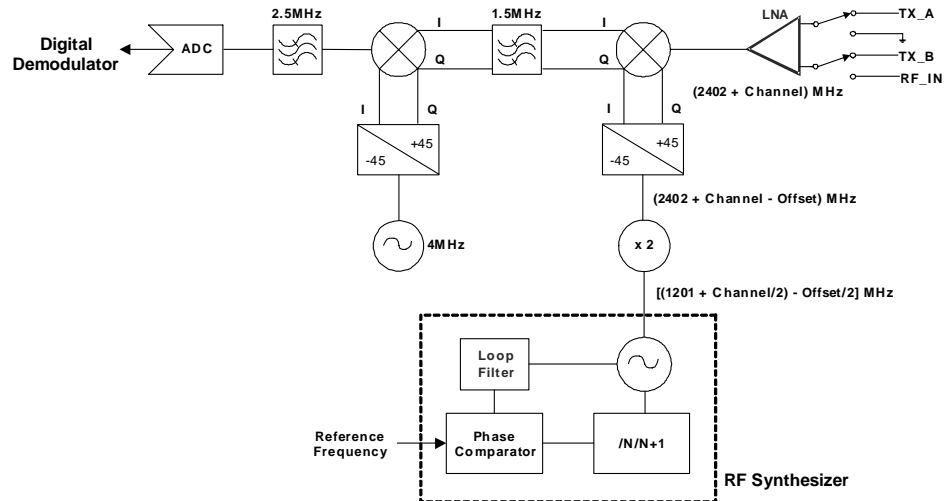


Figure 2.2 : Overview of Receiver Architecture