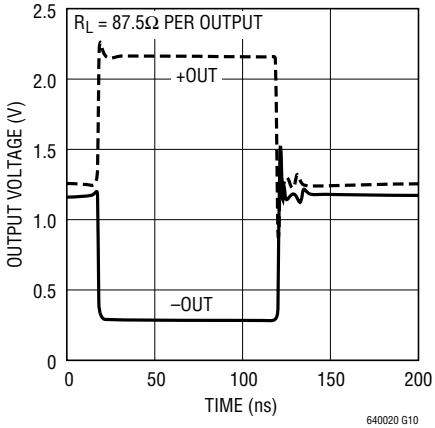
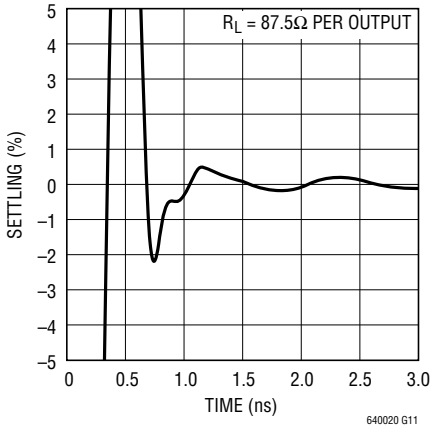
TYPICAL PERFORMANCE CHARACTERISTICS

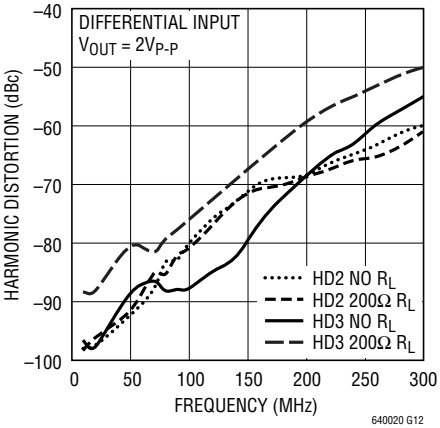
Overdrive Recovery Time



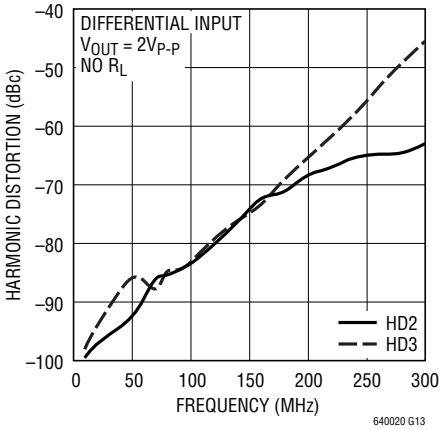
1% Settling Time for 2V Output Step



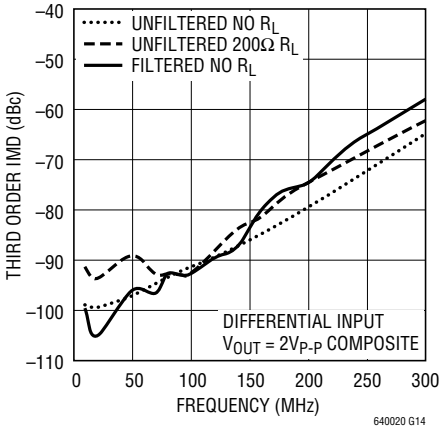
Harmonic Distortion (Unfiltered) vs Frequency



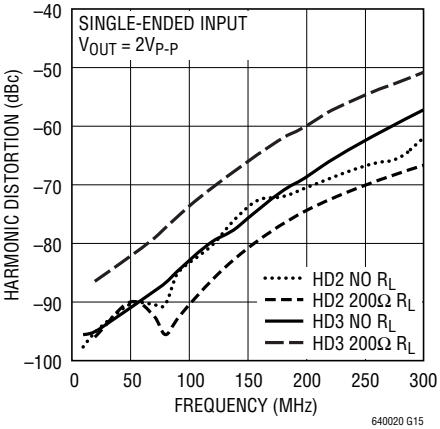
Harmonic Distortion (Filtered) vs Frequency



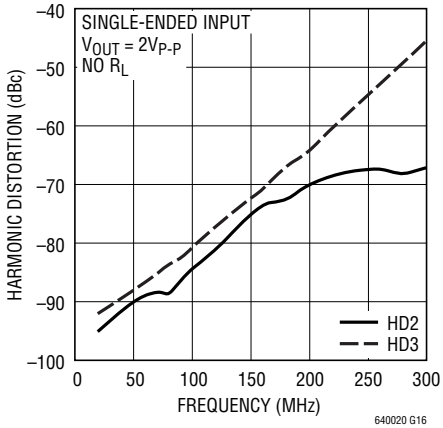
Third Order Intermodulation Distortion vs Frequency



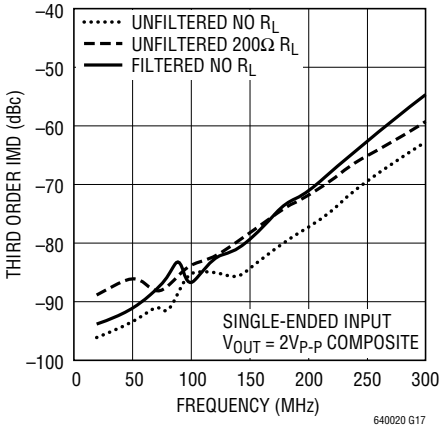
Harmonic Distortion (Unfiltered) vs Frequency



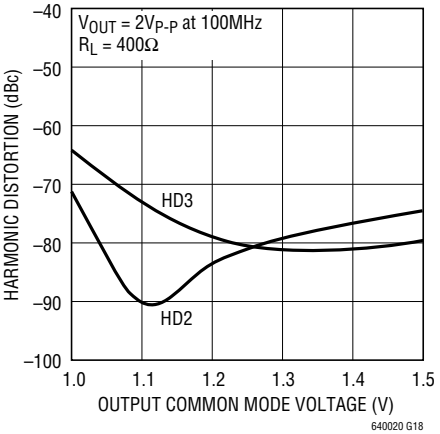
Harmonic Distortion (Filtered) vs Frequency



Third Order Intermodulation Distortion vs Frequency

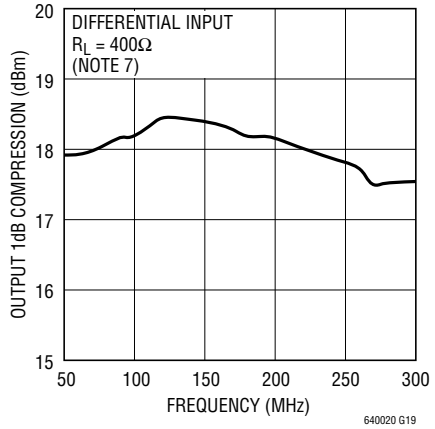


Harmonic Distortion vs Output Common Mode Voltage (Unfiltered Outputs)

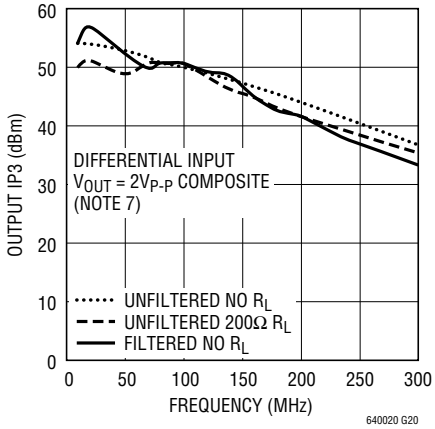


TYPICAL PERFORMANCE CHARACTERISTICS

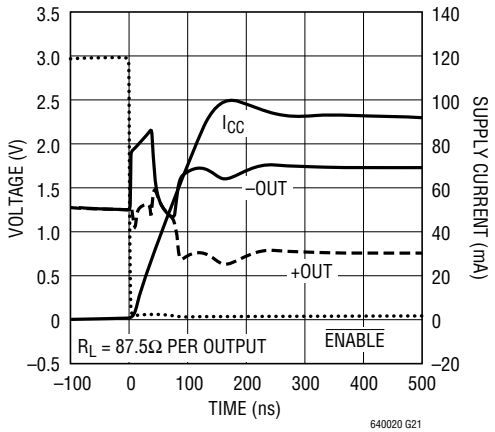
Output 1dB Compression Point vs Frequency



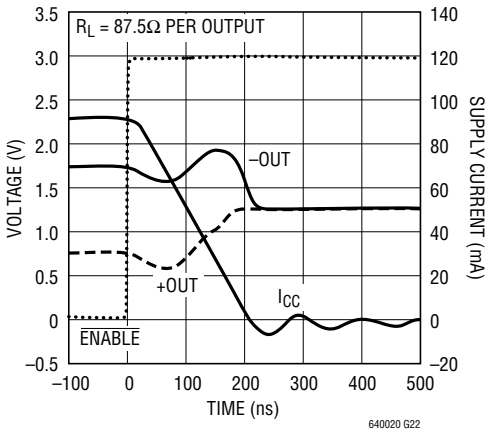
Output Third Order Intercept vs Frequency



Turn-On Time



Turn-Off Time



PIN FUNCTIONS

V^+ (Pins 1, 3, 10): Positive Power Supply (Normally tied to 3V or 3.3V). All three pins must be tied to the same voltage. Bypass each pin with 1000pF and 0.1µF capacitors as close to the pins as possible.

V_{OCM} (Pin 2): This pin sets the output common mode voltage. A 0.1µF external bypass capacitor is recommended.

V^- (Pins 4, 9, 12, 17): Negative Power Supply (GND). All four pins must be connected to same voltage/ground.

–OUT, +OUT (Pins 5, 8): Unfiltered Outputs. These pins have series resistors, R_{OUT} 12.5Ω.

–OUTF, +OUTF (Pins 6, 7): Filtered Outputs. These pins have 50Ω series resistors and a 2.7pF shunt capacitor.

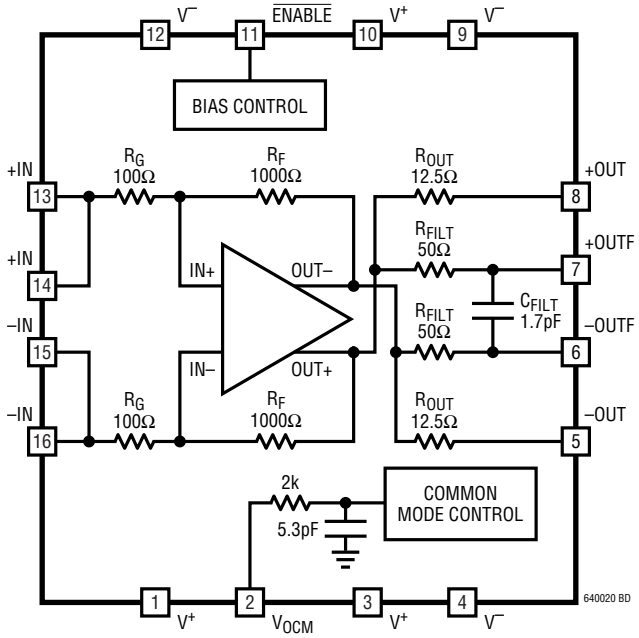
$\overline{\text{ENABLE}}$ (Pin 11): This pin is a logic input referenced to V_{EE}. If low, the part is enabled. If high, the part is disabled and draws approximately 1mA supply current.

+IN (Pins 13, 14): Positive Input. Pins 13 and 14 are internally shorted together.

–IN (Pins 15, 16): Negative Input. Pins 15 and 16 are internally shorted together.

Exposed Pad (Pin 17): V^-. The Exposed Pad must be connected to same voltage/ground as pins 4, 9, 12.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Circuit Operation

The LTC6400 is a low noise and low distortion fully differential op amp/ADC driver with:

- Operation from DC to 1.8GHz (–3dB bandwidth)
- Fixed gain of 10V/V (20dB)
- Differential input impedance 200Ω
- Differential output impedance 25Ω
- On-Chip 590MHz output filter

The LTC6400 is composed of a fully differential amplifier with on chip feedback and output common mode voltage control circuitry. Differential gain and input impedance are set by 100Ω/1000Ω resistors in the feedback network. Small output resistors of 12.5Ω improve the circuit stability over various load conditions. They also provide a possible external filtering option, which is often desirable when the load is an ADC.

Filter resistors of 50Ω are available for additional filtering. Lowpass/bandpass filters are easily implemented with just a couple of external components. Moreover, they offer single-ended 50Ω matching in wideband applications and no external resistor is needed.

The LTC6400-20 is very flexible in terms of I/O coupling. It can be AC- or DC-coupled at the inputs, the outputs or both. Due to the internal connection between input and output, users are advised to keep input common mode voltage between 1V and 1.6V for proper operation. If the inputs are AC-coupled, the input common mode voltage is automatically biased close to V_{OCM} and thus no external circuitry is needed for bias. The LTC6400-20 provides an output common mode voltage set by V_{OCM}, which allows driving an ADC directly without external components such as a transformer or AC coupling capacitors. The input signal can be either single-ended or differential with only minor differences in distortion performance.

Input Impedance and Matching

The differential input impedance of the LTC6400-20 is 200Ω. If a 200Ω source impedance is unavailable, then the differential inputs may need to be terminated to a lower value impedance, e.g. 50Ω, in order to provide an impedance match for the source. Several choices are available. One approach is to use a differential shunt resistor (Figure 1). Another approach is to employ a wide band transformer (Figure 2). Both methods provide a wide band impedance match. The termination resistor or the transformer must be placed close to the input pins in order to minimize the reflection due to input mismatch. Alternatively, one could apply a narrowband impedance match at the inputs of the LTC6400-20 for frequency selection and/or noise reduction.

Referring to Figure 3, LTC6400-20 can be easily configured for single-ended input and differential output without a balun. The signal is fed to one of the inputs through a matching network while the other input is connected to the same matching network and a source resistor. Because the return ratios of the two feedback paths are equal, the two outputs have the same gain and thus symmetrical

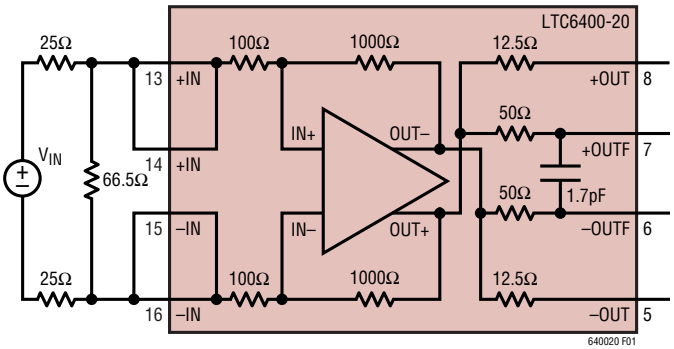


Figure 1. Input Termination for Differential 50Ω Input Impedance Using Shunt Resistor

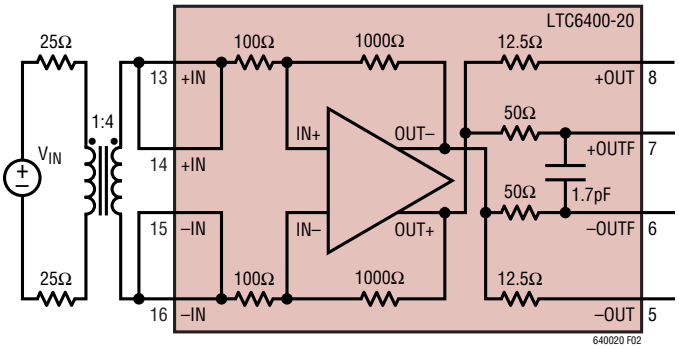


Figure 2. Input Termination for Differential 50Ω Input Impedance Using a 1:4 Balun

APPLICATIONS INFORMATION

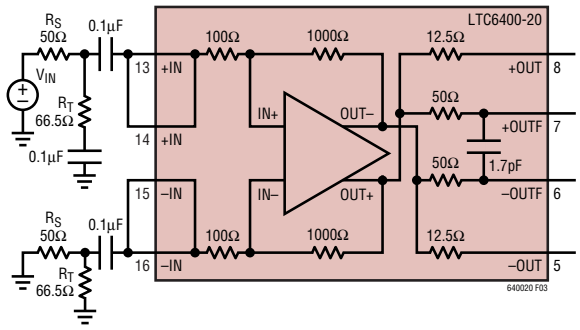


Figure 3. Input Termination for Single-Ended 50Ω Input Impedance

swing. In general, the single-ended input impedance and termination resistor R_T are determined by the combination of R_S, R_G and R_F. For example, when R_S is 50Ω, it is found that the single-ended input impedance is 202Ω and R_T is 66.5Ω in order to match to a 50Ω source impedance.

The LTC6400-20 is unconditionally stable. However, the overall differential gain is affected by both source impedance and load impedance as shown in Figure 4:

$$A_V = \left|\frac{V_{OUT}}{V_{IN}}\right| = \frac{2000}{R_S + 200} \bullet \frac{R_L}{25 + R_L}$$

The noise performance of the LTC6400-20 also depends upon the source impedance and termination. For example, an input 1:4 balun transformer in Figure 2 improves SNR by adding 6dB of voltage gain at the inputs. A trade-off between gain and noise is obvious when constant noise figure circle and constant gain circle are plotted within the same input Smith Chart, based on which users can choose the optimal source impedance for a given gain and noise requirement.

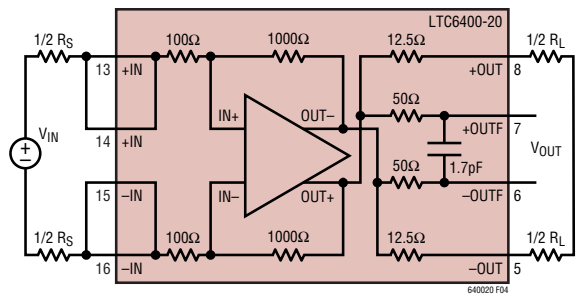


Figure 4. Calculate Differential Gain

Output Match and Filter

The LTC6400-20 can drive an ADC directly without external output impedance matching. Alternatively, the differential output impedance of 25Ω can be matched to higher value impedance, e.g. 50Ω, by series resistors or an LC network.

The internal low pass filter outputs at +OUTF/–OUTF have a –3dB bandwidth of 590MHz. External capacitors can reduce the low pass filter bandwidth as shown in Figure 5. A bandpass filter is easily implemented with only a few components as shown in Figure 6. Three 39pF capacitors and a 16nH inductor create a bandpass filter with 165MHz center frequency, –3dB frequencies at 138MHz and 200MHz.

Output Common Mode Adjustment

The output common mode voltage is set by the V_{OCM} pin, which is a high impedance input. The output common mode voltage is capable of tracking V_{OCM} in a range from 1V to

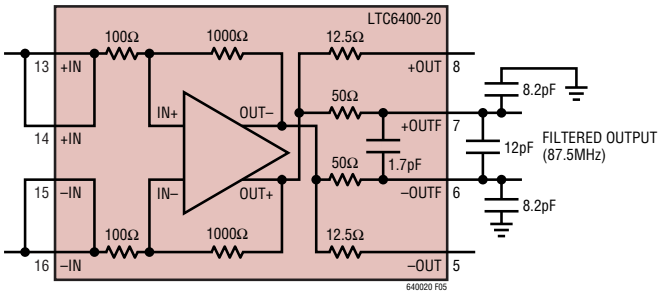


Figure 5. LTC6400-20 Internal Filter Topology Modified for Low Filter Bandwidth (Three External Capacitors)

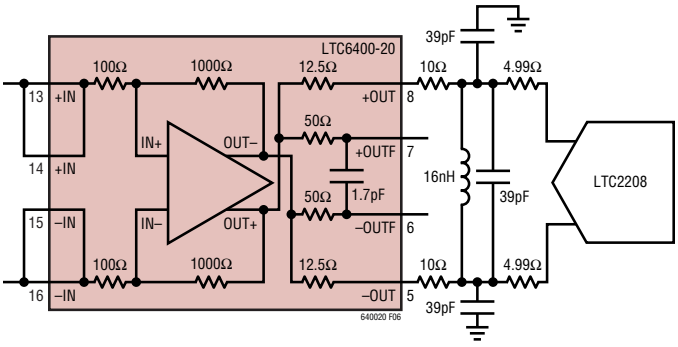


Figure 6. LTC6400-20 Internal Filter Topology Modified for Bandpass Filtering (Three External Capacitors, One External Inductor)

APPLICATIONS INFORMATION

1.6V. The bandwidth of V_{OCM} control is typically 15MHz, which is dominated by a low pass filter connected to the V_{OCM} pin and is aimed to reduce common mode noise generation at the outputs. The internal common mode feedback loop has a –3dB bandwidth around 300MHz, allowing fast common mode rejection at the outputs of the LTC6400-20. The V_{OCM} pin should be tied to a DC bias voltage with a 0.1µF bypass capacitor. When interfacing with A/D converters such as the LT22xx families, the V_{OCM} pin can be connected to the V_{CM} pin of the ADC.

Driving A/D Converters

The LTC6400-20 has been specifically designed to interface directly with high speed A/D converters. In Figure 7, an example schematic shows the LTC6400-20 with a single-ended input driving the LTC2208, which is a 16-bit, 130Msps ADC. Two external 10Ω resistors help eliminate potential resonance associated with stray capacitance of PCB traces and bond wires of either the ADC input or the driver output. V_{OCM} of the LTC6400-20 is connected to V_{CM} of the LTC2208 V_{CM} pin at 1.25V. Alternatively, a single-ended input signal can be converted to differential signal via a balun and fed to the input of the LTC6400-20. The balun also converts input impedance to match 50Ω source impedance.

Figure 8 summarizes the spurious free dynamic range (SFDR) for IMD3 of the whole system in Figure 7.

Test Circuits

Due to the fully-differential design of the LTC6400 and its usefulness in applications with differing characteristic

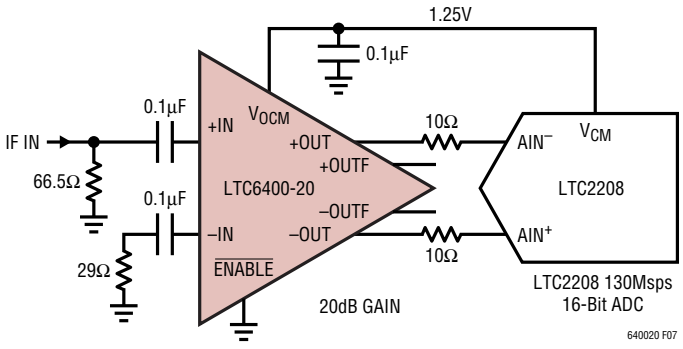


Figure 7. Single-Ended Input to LTC6400-20 and LTC2208

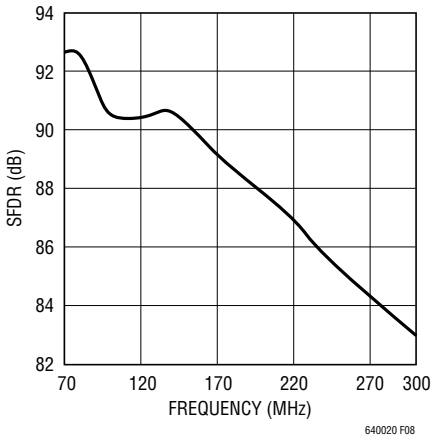
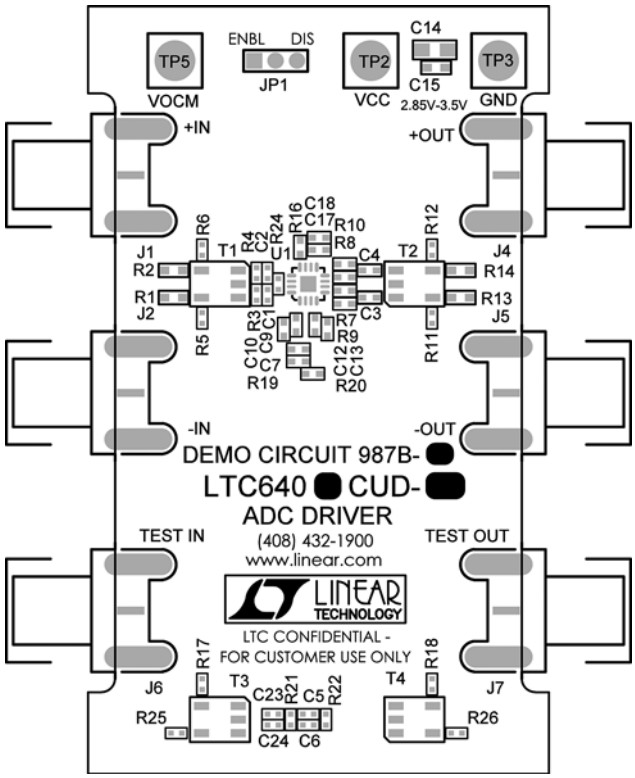


Figure 8. SFDR for the Combination of LTC6400-20 and LTC2208

specifications, two test circuits are used to generate the information in this datasheet. Test Circuit A is DC987B, a two-port demonstration circuit for the LTC6400 family. The schematic and silkscreen are shown below. This circuit includes input and output transformers (baluns) for single-ended-to-differential conversion and impedance transformation, allowing direct hook-up to a 2-port

Top Silkscreen



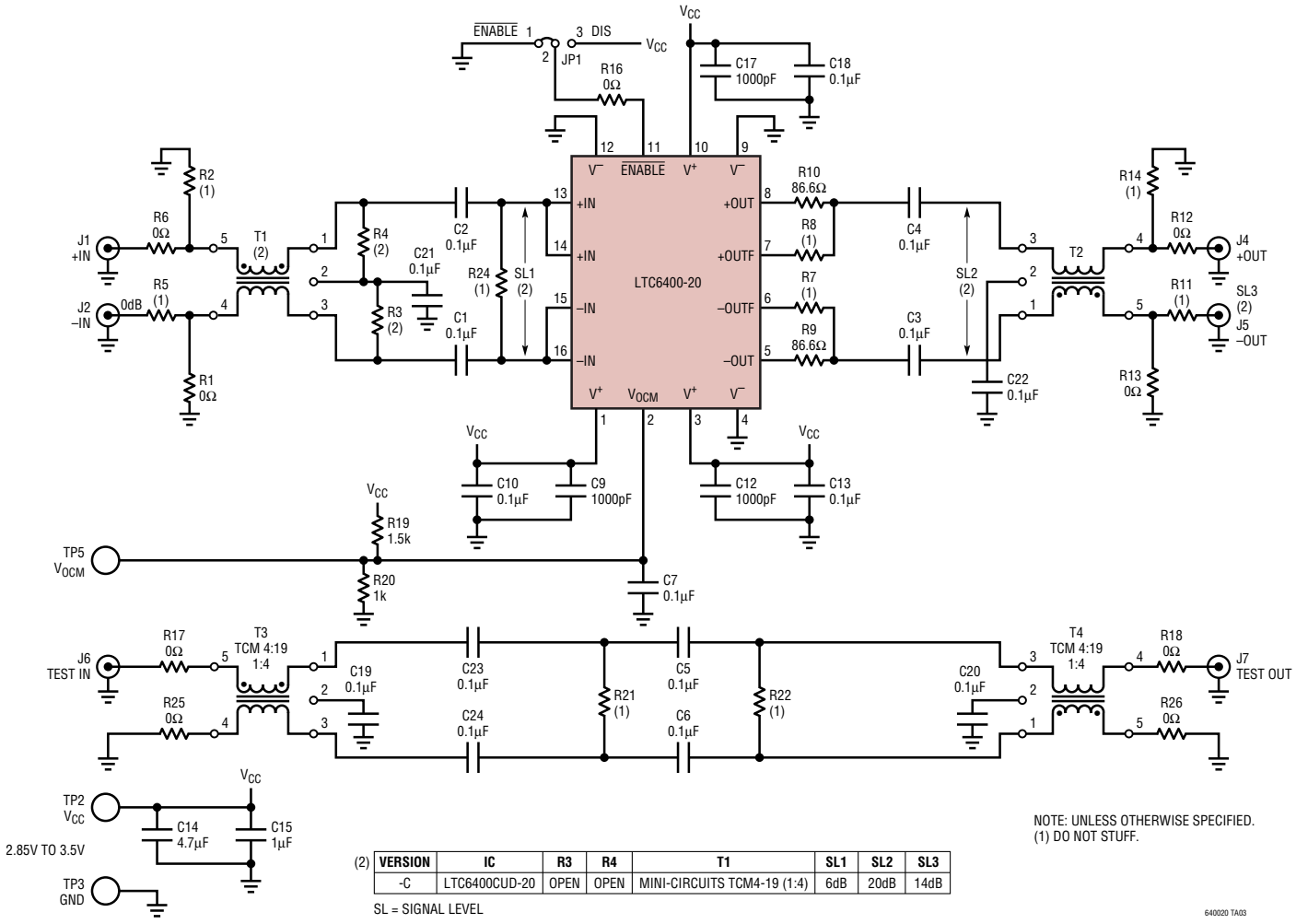
APPLICATIONS INFORMATION

network analyzer. There are also series resistors at the output to present the LTC6400 with a 375Ω differential load, optimizing distortion performance. Due to the input and output transformers, the –3dB bandwidth is reduced from 1.8GHz to approximately 1.3GHz.

Test Circuit B uses a 4-port network analyzer to measure S-parameters and gain/phase response. This removes the effects of the wideband baluns and associated circuitry, for true picture of the >1GHz S-parameters and AC characteristics.

TYPICAL APPLICATIONS

Demo Circuit 987B Schematic (Test Circuit A)



NOTE: UNLESS OTHERWISE SPECIFIED.
(1) DO NOT STUFF.

(2)

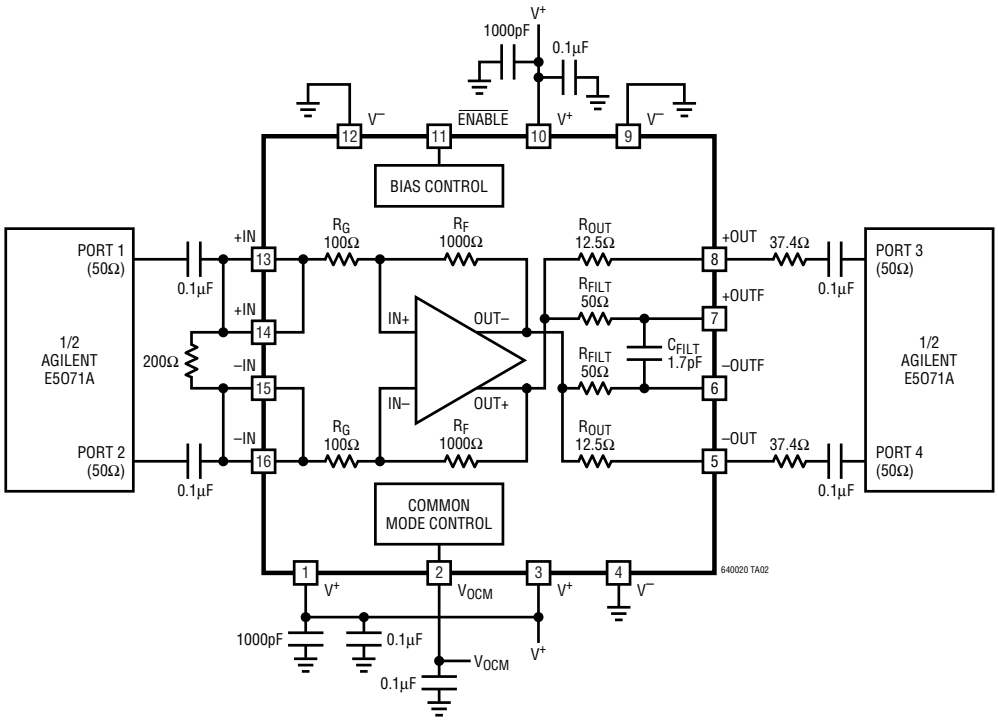
VERSION	IC	R3	R4	T1	SL1	SL2	SL3
-C	LTC6400CUD-20	OPEN	OPEN	MINI-CIRCUITS TCM4-19 (1:4)	6dB	20dB	14dB

SL = SIGNAL LEVEL

640020 TA03

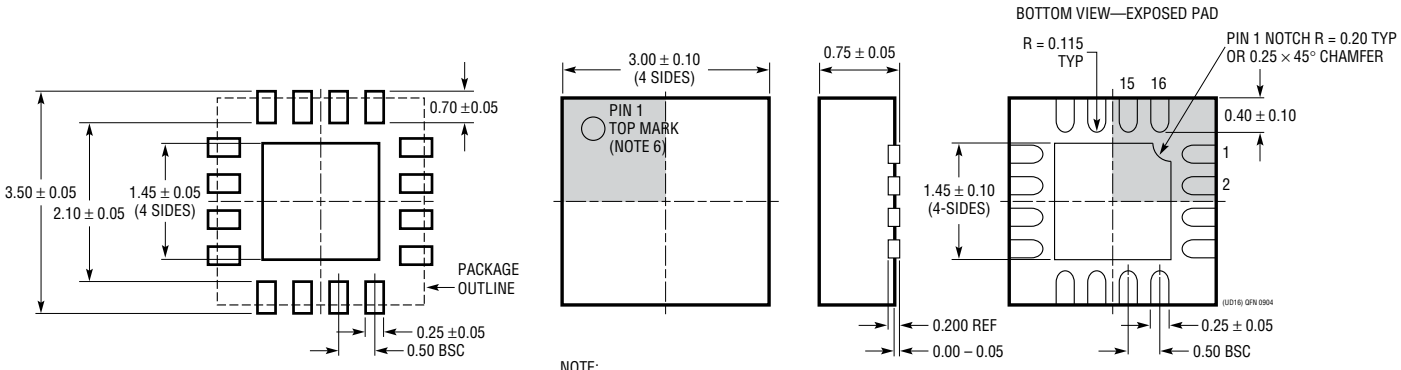
TYPICAL APPLICATIONS

Test Circuit B, 4-Port Analysis



PACKAGE DESCRIPTION

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691)



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
High-Speed Differential Amplifiers/Differential Op Amps		
LT®1993-2	800MHz Differential Amplifier/ADC Driver	A_V = 2V/V, OIP3 = 38dBm at 70MHz
LT1993-4	900MHz Differential Amplifier/ADC Driver	A_V = 4V/V, OIP3 = 40dBm at 70MHz
LT1993-10	700MHz Differential Amplifier/ADC Driver	A_V = 2V/V, OIP3 = 40dBm at 70MHz
LT1994	Low Noise, Low Distortion Differential Op Amp	16-Bit SNR and SFDR at 1MHz, Rail-to-Rail Outputs
LT5514	Ultralow Distortion IF Amplifier/ADC Driver with Digitally Controlled Gain	OIP3 = 47dBm at 100MHz, Gain Control Range 10.5dB to 33dB
LT5524	Low Distortion IF Amplifier/ADC Driver with Digitally Controlled Gain	OIP3 = 40dBm at 100MHz, Gain Control Range 4.5dB to 37dB
LTC6401-20	1.3GHz Low Noise, Low Distortion, Differential ADC Driver	A_V = 20dB, 50mA Supply Current, IMD_3 = –74dBc at 140MHz
LT6402-6	300MHz Differential Amplifier/ADC Driver	A_V = 6dB, Distortion < –80dBc at 25MHz
LT6402-12	300MHz Differential Amplifier/ADC Driver	A_V = 12dB, Distortion < –80dBc at 25MHz
LT6402-20	300MHz Differential Amplifier/ADC Driver	A_V = 20dB, Distortion < –80dBc at 25MHz
LTC6406	3GHz Rail-to-Rail Input Differential Op Amp	1.6nV/$\sqrt{Hz}$ Noise, –72dBc Distortion at 50MHz, 18mA
LT6411	Low Power Differential ADC Driver/Dual Selectable Gain Amplifier	16mA Supply Current, IMD3 = –83dBc at 70MHz, A_V = 1, –1 or 2
High-Speed Single-Ended Output Op Amps		
LT1812/LT1813/ LT1814	High Slew Rate Low Cost Single/Dual/Quad Op Amps	8nV/$\sqrt{Hz}$ Noise, 750V/µs, 3mA Supply Current
LT1815/LT1816/ LT1817	Very High Slew Rate Low Cost Single/Dual/Quad Op Amps	6nV/$\sqrt{Hz}$ Noise, 1500V/µs, 6.5mA Supply Current
LT1818/LT1819	Ultra High Slew Rate Low Cost Single/Dual Op Amps	6nV/$\sqrt{Hz}$ Noise, 2500V/µs, 9mA Supply Current
LT6200/LT6201	Rail-to-Rail Input and Output Low Noise Single/Dual Op Amps	0.95nV/$\sqrt{Hz}$ Noise, 165MHz GBW, Distortion = –80dBc at 1MHz
LT6202/LT6203/ LT6204	Rail-to-Rail Input and Output Low Noise Single/Dual/Quad Op Amps	1.9nV/$\sqrt{Hz}$ Noise, 3mA Supply Current, 100MHz GBW
LT6230/LT6231/ LT6232	Rail-to-Rail Output Low Noise Single/Dual/Quad Op Amps	1.1nV/$\sqrt{Hz}$ Noise, 3.5mA Supply Current, 215MHz GBW
LT6233/LT6234/ LT6235	Rail-to-Rail Output Low Noise Single/Dual/Quad Op Amps	1.9nV/$\sqrt{Hz}$ Noise, 1.2mA Supply Current, 60MHz GBW
Integrated Filters		
LTC1562-2	Very Low Noise, 8th Order Filter Building Block	Lowpass and Bandpass Filters up to 300kHz
LT1568	Very Low Noise, 4th Order Filter Building Block	Lowpass and Bandpass Filters up to 10MHz
LTC1569-7	Linear Phase, Tunable 10th Order Lowpass Filter	Single-Resistor Programmable Cut-Off to 300kHz
LT6600-2.5	Very Low Noise Differential 2.5MHz Lowpass Filter	SNR = 86dB at 3V Supply, 4th Order Filter
LT6600-5	Very Low Noise Differential 5MHz Lowpass Filter	SNR = 82dB at 3V Supply, 4th Order Filter
LT6600-10	Very Low Noise Differential 10MHz Lowpass Filter	SNR = 82dB at 3V Supply, 4th Order Filter
LT6600-15	Very Low Noise Differential 15MHz Lowpass Filter	SNR = 76dB at 3V Supply, 4th Order Filter
LT6600-20	Very Low Noise Differential 20MHz Lowpass Filter	SNR = 76dB at 3V Supply, 4th Order Filter

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1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT 0707 • PRINTED IN USA

1.3GHz Low Noise, Low Distortion Differential ADC Driver for 140MHz IF

FEATURES

- 1.3GHz –3dB Bandwidth
- Fixed Gain of 10V/V (20dB)
- –93dBc IMD_3 at 70MHz (Equivalent OIP_3 = 50.5dBm)
- –74dBc IMD_3 at 140MHz (Equivalent OIP_3 = 41dBm)
- 1nV/√Hz Internal Op Amp Noise
- 2.1nV/√Hz Total Input Noise
- 6.2dB Noise Figure
- Differential Inputs and Outputs
- 200Ω Input Impedance
- 2.85V to 3.5V Supply Voltage
- 50mA Supply Current (150mW)
- 1V to 1.6V Output Common Mode Voltage, Adjustable
- DC- or AC-Coupled Operation
- Max Differential Output Swing $4.4V_{P-P}$
- Small 16-Lead 3mm × 3mm × 0.75mm QFN Package

APPLICATIONS

- Differential ADC Driver
- Differential Driver/Receiver
- Single Ended to Differential Conversion
- IF Sampling Receivers
- SAW Filter Interfacing

DESCRIPTION

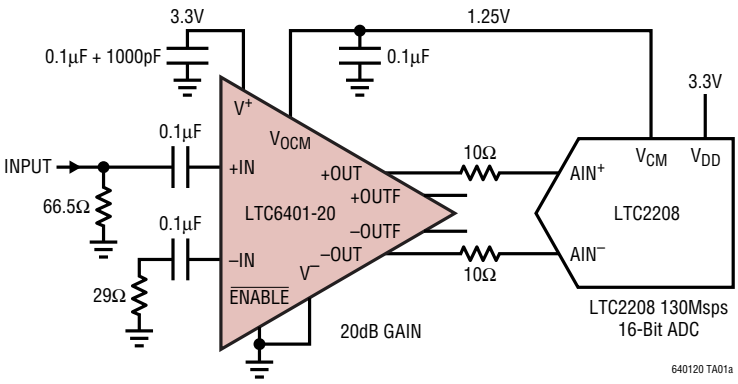
The LTC®6401-20 is a high-speed differential amplifier targeted at processing signals from DC to 140MHz. The part has been specifically designed to drive 12-, 14- and 16-bit ADCs with low noise and low distortion, but can also be used as a general-purpose broadband gain block.

The LTC6401-20 is easy to use, with minimal support circuitry required. The output common mode voltage is set using an external pin, independent of the inputs, which eliminates the need for transformers or AC-coupling capacitors in many applications. The gain is internally fixed at 20dB (10V/V).

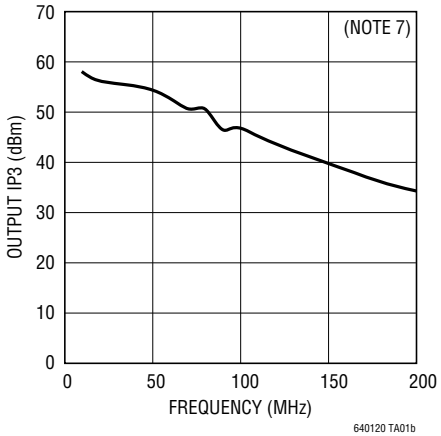
The LTC6401-20 saves space and power compared to alternative solutions using IF gain blocks and transformers. The LTC6401-20 is packaged in a compact 16-lead 3mm × 3mm QFN package and operates over the –40°C to 85°C temperature range.

TYPICAL APPLICATION

Single-Ended to Differential ADC Driver



Equivalent Output IP3 vs Frequency

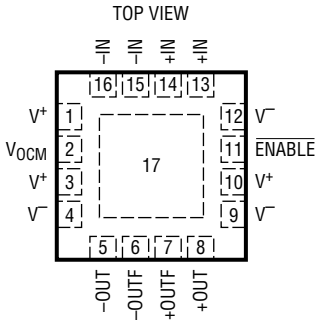


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage ($V^+ – V^–$).....3.6V
Input Current (Note 2).....±10mA
Operating Temperature Range
(Note 3) ..... –40°C to 85°C
Specified Temperature Range
(Note 4) ..... –40°C to 85°C
Storage Temperature Range..... –65°C to 150°C
Maximum Junction Temperature..... 150°C

PIN CONFIGURATION



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 68°C/W, θ_{JC} = 4.2°C/W
EXPOSED PAD (PIN 17) IS $V^–$, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6401CUD-20#PBF	LTC6401CUD-20#TRPBF	LCDB	16-Lead (3mm × 3mm) Plastic QFN	0°C to 70°C
LTC6401IUD-20#PBF	LTC6401IUD-20#TRPBF	LCDB	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

LTC6400 AND LTC6401 SELECTOR GUIDE

Please check each datasheet for complete details.

PART NUMBER	GAIN (dB)	GAIN (V/V)	Z_{IN} (DIFFERENTIAL) (Ω)	I_{CC} (mA)
LTC6400-20	20	10	200	90
LTC6401-20	20	10	200	50

In addition to the LTC6401 family of amplifiers, a lower distortion LTC6400 family is available. The LTC6400 is pin compatible to the LTC6401, and has the same low noise performance. The low distortion of the LTC6400 comes at the expense of higher power consumption. Please refer to the separate LTC6400 data sheets for complete details. Other gain versions from 8dB to 26dB will follow.

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, +IN = –IN = V_{OCM} = 1.25V, $\overline{ENABLE}$ = 0V, No R_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input/Output Characteristic							
G_{DIFF}	Gain	V_{IN} = ±100mV Differential	●	19.4	20	20.6	dB
G_{TEMP}	Gain Temperature Drift	V_{IN} = ±100mV Differential	●		1		mdB/°C
$V_{SWINGMIN}$	Output Swing Low	Each Output, V_{IN} = ±400mV Differential	●		90	170	mV
$V_{SWINGMAX}$	Output Swing High	Each Output, V_{IN} = ±400mV Differential	●	2.3	2.44		V
$V_{OUTDIFFMAX}$	Maximum Differential Output Swing	1dB Compressed			4.4		V_{P-P}
I_{OUT}	Output Current Drive	Single-Ended	●	10			mA
V_{OS}	Input Offset Voltage	Differential	●	–2		2	mV
TCV_{OS}	Input Offset Voltage Drift	Differential	●		1.4		µV/°C
I_{VRMIN}	Input Common Mode Voltage Range, MIN					1	V
I_{VRMAX}	Input Common Mode Voltage Range, MAX			1.6			V
R_{INDIFF}	Input Resistance	Differential	●	170	200	230	Ω
C_{INDIFF}	Input Capacitance	Differential, Includes Parasitic			1		pF
$R_{OUTDIFF}$	Output Resistance	Differential	●	18	25	32	Ω
$R_{OUTFDIFF}$	Filtered Output Resistance	Differential	●	85	100	115	Ω
$C_{OUTFDIFF}$	Filtered Output Capacitance	Differential, Includes Parasitic			2.7		pF
CMRR	Common Mode Rejection Ratio	Input Common Mode Voltage 1.1V to 1.4V	●	45	66		dB
Output Common Mode Voltage Control							
G_{CM}	Common Mode Gain	V_{OCM} = 1V to 1.6V			1		V/V
V_{OCMMIN}	Output Common Mode Range, MIN		 ●			1 1.1	V V
V_{OCMMAX}	Output Common Mode Range, MAX		 ●	1.6 1.5			V V
V_{OSCM}	Common Mode Offset Voltage	V_{OCM} = 1.1V to 1.5V	●	–15		15	mV
TCV_{OSCM}	Common Mode Offset Voltage Drift		●		6		µV/°C
IV_{OCM}	V_{OCM} Input Current		●		5	15	µA
$\overline{ENABLE}$ Pin							
V_{IL}	$\overline{ENABLE}$ Input Low Voltage		●			0.8	V
V_{IH}	$\overline{ENABLE}$ Input High Voltage		●	2.4			V
I_{IL}	$\overline{ENABLE}$ Input Low Current	$\overline{ENABLE}$ = 0.8V	●			±0.5	µA
I_{IH}	$\overline{ENABLE}$ Input High Current	$\overline{ENABLE}$ = 2.4V	●		1.2	3	µA
Power Supply							
V_S	Operating Supply Range		●	2.85	3	3.5	V
I_S	Supply Current	$\overline{ENABLE}$ = 0.8V	●	38	50	62	mA
I_{SHDN}	Shutdown Supply Current	$\overline{ENABLE}$ = 2.4V	●		1	3	mA
PSRR	Power Supply Rejection Ratio (Differential Outputs)	2.85V to 3.5V	●	55	84		dB

AC ELECTRICAL CHARACTERISTICS

Specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, +IN and –IN floating, V_{OCM} = 1.25V, $\overline{ENABLE}$ = 0V, No R_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
–3dBBW	–3dB Bandwidth	200mV$_{P-P,OUT}$ (Note 6)		1.25		GHz
0.1dBBW	Bandwidth for 0.1dB Flatness	200mV$_{P-P,OUT}$ (Note 6)		130		MHz
0.5dBBW	Bandwidth for 0.5dB Flatness	200mV$_{P-P,OUT}$ (Note 6)		250		MHz
1/f	1/f Noise Corner			12.5		kHz
SR	Slew Rate	Differential (Note 6)		4500		V/µs
$t_{S1\%}$	1% Settling Time	2V$_{P-P,OUT}$ (Note 6)		2		ns
t_{OVDR}	Output Overdrive Recovery Time	1.9V$_{P-P,OUT}$ (Note 6)		7		ns
t_{ON}	Turn-On Time	+OUT, –OUT Within 10% of Final Values		78		ns
t_{OFF}	Turn-Off Time	I_{CC} Falls to 10% of Nominal		146		ns
–3dBBW$_{CM}$	Common Mode Small Signal –3dB BW	0.1V$_{P-P}$ at V_{OCM}, Measured Single-Ended at Output (Note 6)		15		MHz
10MHz Input Signal						
HD$_{2,10M}$/HD$_{3,10M}$	Second/Third Order Harmonic Distortion	2V$_{P-P,OUT}$, R_L = 400Ω		–122/–92		dBc
		2V$_{P-P,OUT}$, No R_L		–110/–103		dBc
		2V$_{P-P,OUTFILT}$, No R_L		–113/–102		dBc
IMD$_{3,10M}$	Third-Order Intermodulation (f1 = 9.5MHz f2 = 10.5MHz)	2V$_{P-P,OUT}$ Composite, R_L = 400Ω		–96		dBc
		2V$_{P-P,OUT}$ Composite, No R_L		–108		dBc
		2V$_{P-P,OUTFILT}$ Composite, No R_L		–105		dBc
OIP$_{3,10M}$	Third-Order Output Intercept Point (f1 = 9.5MHz f2 = 10.5MHz)	2V$_{P-P,OUT}$ Composite, No R_L (Note 7)		58		dBm
$P_{1dB,10M}$	1dB Compression Point	R_L = 375Ω (Notes 5, 7)		17.3		dBm
NF_{10M}	Noise Figure	R_L = 375Ω (Note 5)		6.2		dB
$e_{IN,10M}$	Input Referred Voltage Noise Density	Includes Resistors (Short Inputs)		2.1		nV/√Hz
$e_{ON,10M}$	Output Referred Voltage Noise Density	Includes Resistors (Short Inputs)		21		nV/√Hz
70MHz Input Signal						
HD$_{2,70M}$/HD$_{3,70M}$	Second/Third Order Harmonic Distortion	2V$_{P-P,OUT}$, R_L = 400Ω		–91/–80		dBc
		2V$_{P-P,OUT}$, No R_L		–95/–88		dBc
		2V$_{P-P,OUTFILT}$, No R_L		–95/–88		dBc
IMD$_{3,70M}$	Third-Order Intermodulation (f1 = 69.5MHz f2 = 70.5MHz)	2V$_{P-P,OUT}$ Composite, R_L = 400Ω		–88		dBc
		2V$_{P-P,OUT}$ Composite, No R_L		–93		dBc
		2V$_{P-P,OUTFILT}$ Composite, No R_L		–92		dBc
OIP$_{3,70M}$	Third-Order Output Intercept Point (f1 = 69.5MHz f2 = 70.5MHz)	2V$_{P-P,OUT}$ Composite, No R_L (Note 7)		50.5		dBm
$P_{1dB,70M}$	1dB Compression Point	R_L = 375Ω (Notes 5, 7)		17.3		dBm
NF_{70M}	Noise Figure	R_L = 375Ω (Note 5)		6.1		dB
$e_{IN,70M}$	Input Referred Voltage Noise Density	Includes Resistors (Short Inputs)		2.1		nV/√Hz
$e_{ON,70M}$	Output Referred Voltage Noise Density	Includes Resistors (Short Inputs)		21		nV/√Hz
140MHz Input Signal						
HD$_{2,140M}$/HD$_{3,140M}$	Second/Third Order Harmonic Distortion	2V$_{P-P,OUT}$, R_L = 400Ω		–80/–57		dBc
		2V$_{P-P,OUT}$, No R_L		–81/–60		dBc
		2V$_{P-P,OUTFILT}$, No R_L		–80/–65		dBc

AC ELECTRICAL CHARACTERISTICS

Specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, +IN and –IN floating, V_{OCM} = 1.25V, $\overline{ENABLE}$ = 0V, No R_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$IMD_{3,140M}$	Third-Order Intermodulation (f1 = 139.5MHz f2 = 140.5MHz)	$2V_{P-P,OUT}$ Composite, R_L = 400Ω		–71		dBc
		$2V_{P-P,OUT}$ Composite, No R_L		–74		dBc
		$2V_{P-P,OUTFILT}$ Composite, No R_L		–72		dBc
$OIP_{3,140M}$	Third-Order Output Intercept Point (f1 = 139.5MHz f2 = 140.5MHz)	$2V_{P-P,OUT}$ Composite, No R_L (Note 7)		41		dBm
$P_{1dB,140M}$	1dB Compression Point	R_L = 375Ω (Notes 5, 7)		18		dBm
NF_{140M}	Noise Figure	R_L = 375Ω (Note 5)		6.4		dB
$e_{IN,140M}$	Input Referred Voltage Noise Density	Includes Resistors (Short Inputs)		2.1		nV/√Hz
$e_{ON,140M}$	Output Referred Voltage Noise Density	Includes Resistors (Short Inputs)		22		nV/√Hz
$IMD_{3,130M/150M}$	Third-Order Intermodulation (f1 = 130MHz f2 = 150MHz) Measure at 170MHz	$2V_{P-P,OUT}$ Composite, R_L = 375Ω (Note 5)	–61	–69		dBc

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Input pins (+IN, –IN) are protected by steering diodes to either supply. If the inputs go beyond either supply rail, the input current should be limited to less than 10mA.

Note 3: The LTC6401C and LTC6401I are guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 4: The LTC6401C is guaranteed to meet specified performance from 0°C to 70°C. It is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LTC6401I is guaranteed to meet specified performance from –40°C to 85°C.

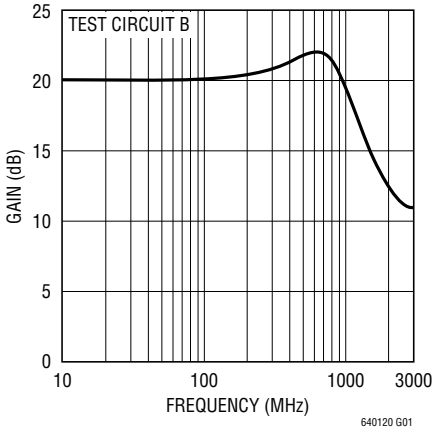
Note 5: Input and output baluns used. See Test Circuit A.

Note 6: Measured using Test Circuit B.

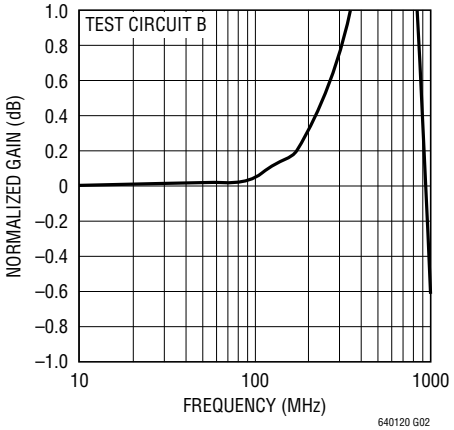
Note 7: Since the LTC6401-20 is a feedback amplifier with low output impedance, a resistive load is not required when driving an AD converter. Therefore, typical output power is very small. In order to compare the LTC6401-20 with amplifiers that require 50Ω output load, the LTC6401-20 output voltage swing driving a given R_L is converted to OIP_3 and P_{1dB} as if it were driving a 50Ω load. Using this modified convention, $2V_{P-P}$ is by definition equal to 10dBm, regardless of the actual R_L.

TYPICAL PERFORMANCE CHARACTERISTICS

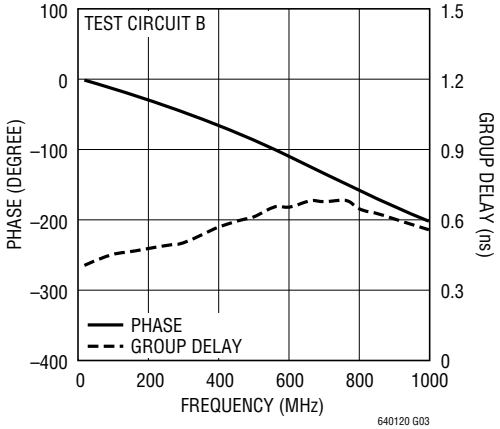
Frequency Response



Gain 0.1dB Flatness

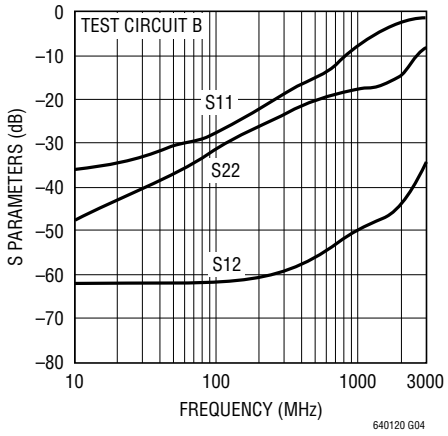


S21 Phase and Group Delay vs Frequency

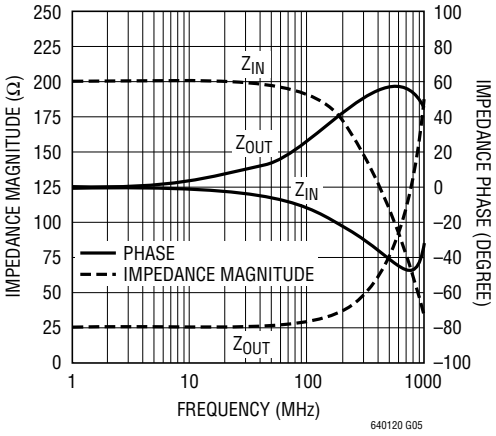


TYPICAL PERFORMANCE CHARACTERISTICS

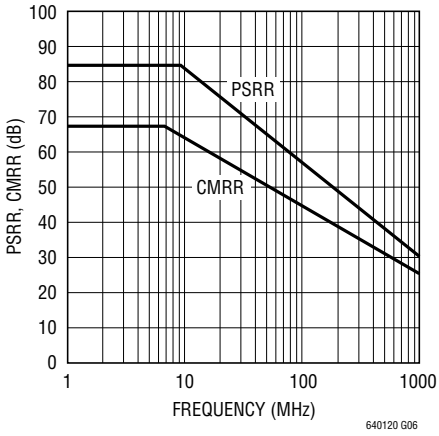
Input and Output Reflection and Reverse Isolation vs Frequency



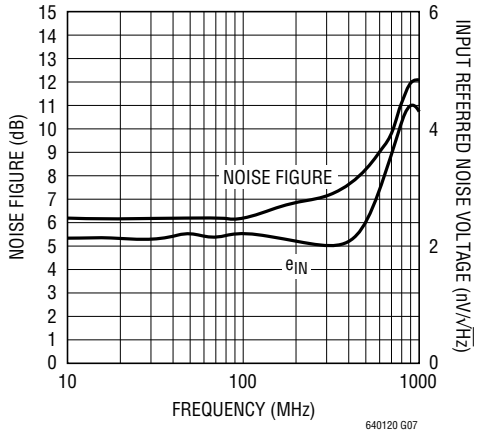
Input and Output Impedance vs Frequency



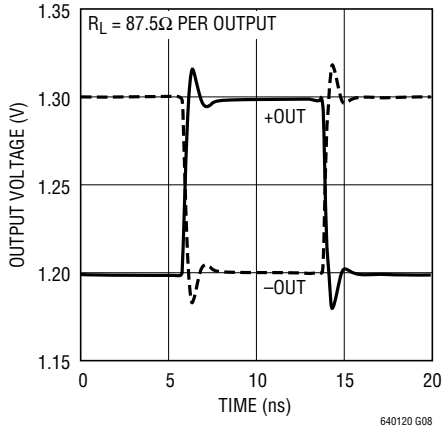
PSRR and CMRR vs Frequency



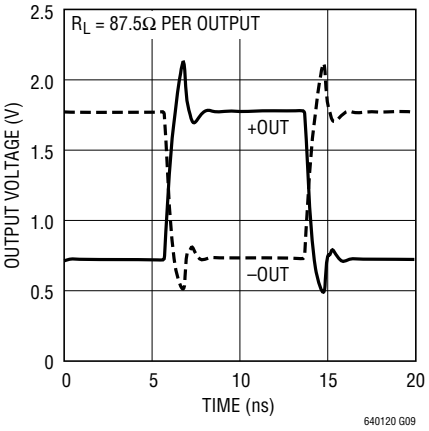
Noise Figure and Input Referred Noise Voltage vs Frequency



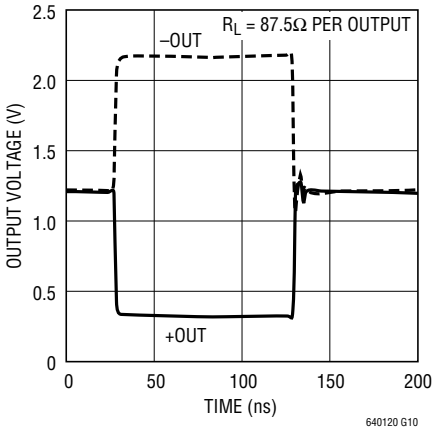
Small Signal Transient Response



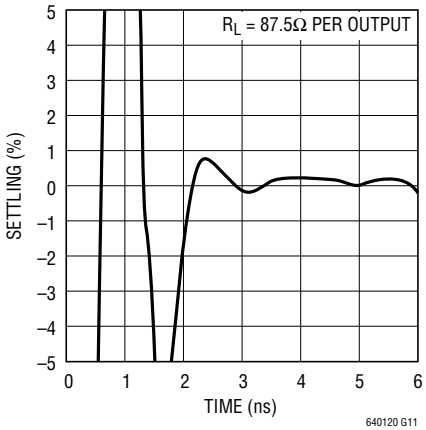
Large Signal Transient Response



Overdrive Transient Response

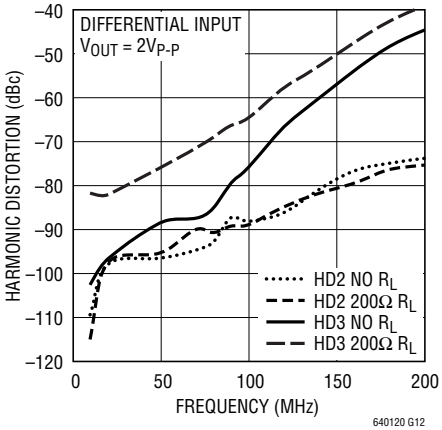


1% Settling Time for 2V Output Step

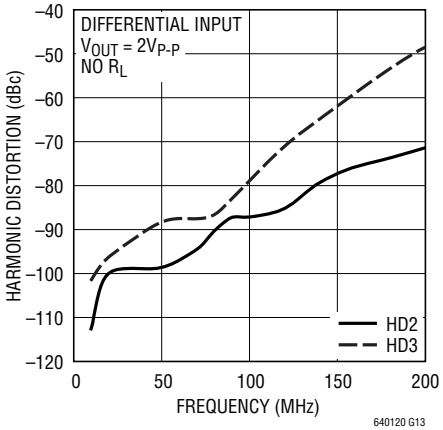


TYPICAL PERFORMANCE CHARACTERISTICS

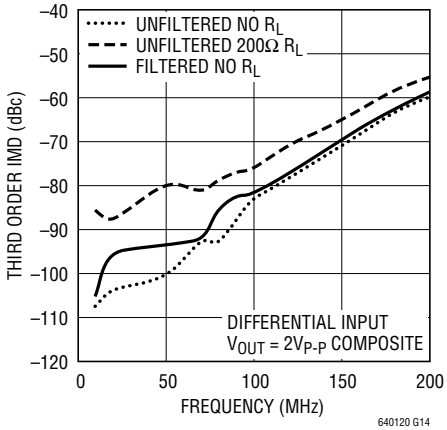
Harmonic Distortion (Unfiltered) vs Frequency



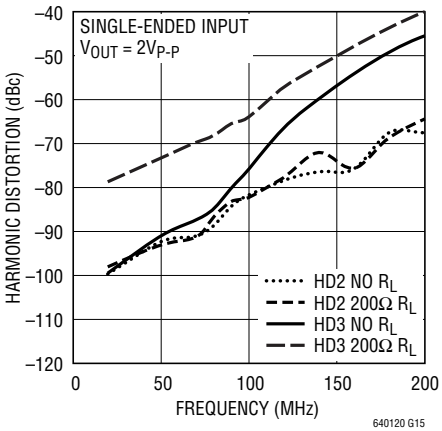
Harmonic Distortion (Filtered) vs Frequency



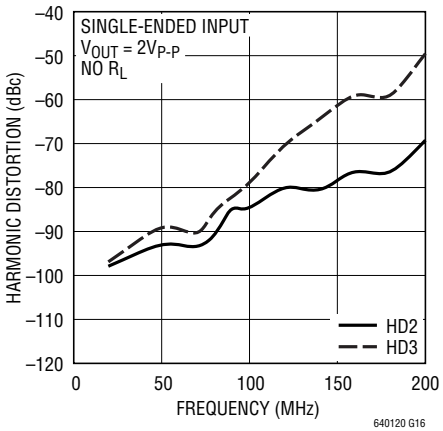
Third Order Intermodulation Distortion vs Frequency



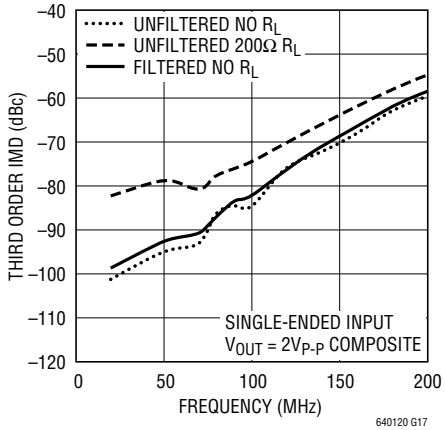
Harmonic Distortion (Unfiltered) vs Frequency



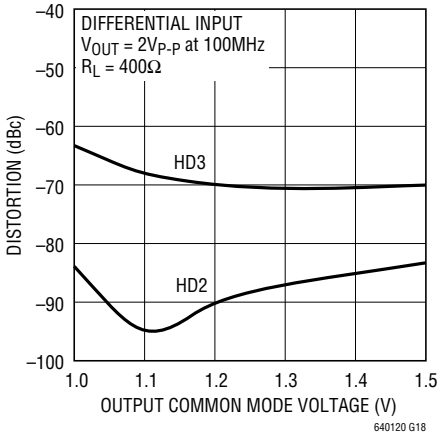
Harmonic Distortion (Filtered) vs Frequency



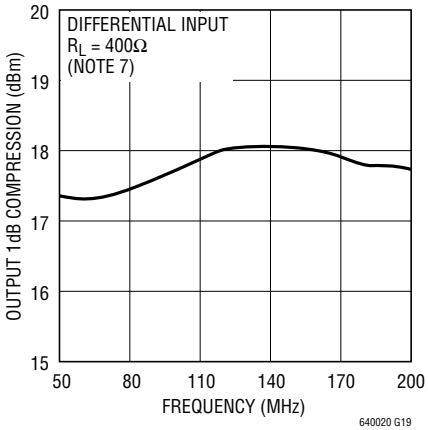
Third Order Intermodulation Distortion vs Frequency



Harmonic Distortion vs Output Common Mode Voltage (Unfiltered Outputs)

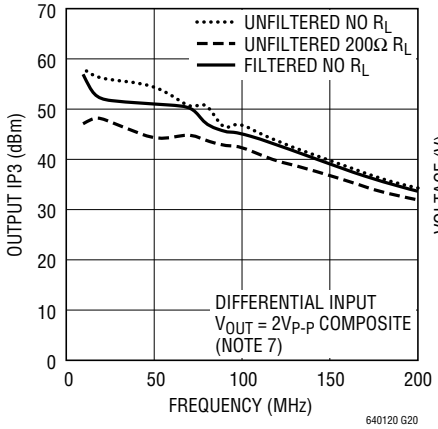


Equivalent Output 1dB Compression Point vs Frequency

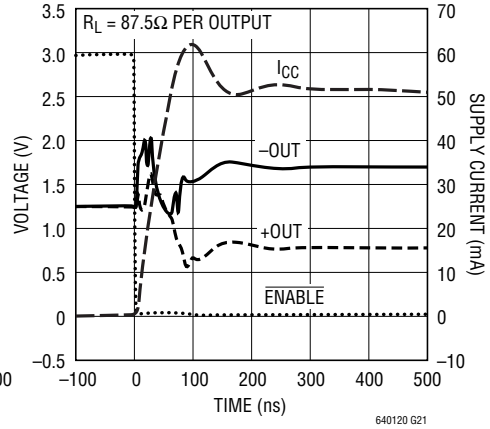


TYPICAL PERFORMANCE CHARACTERISTICS

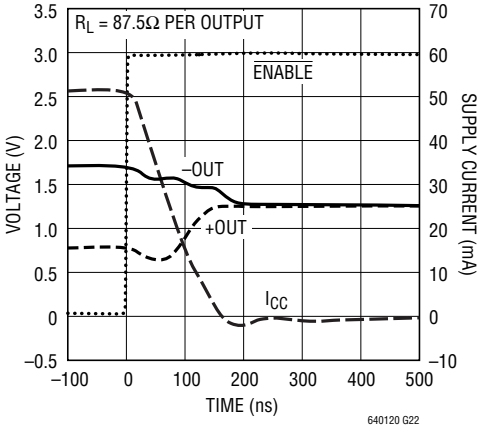
Equivalent Output Third Order Intercept vs Frequency



Turn-On Time



Turn-Off Time



PIN FUNCTIONS

V^+ (Pins 1, 3, 10): Positive Power Supply (Normally tied to 3V or 3.3V). All three pins must be tied to the same voltage. Bypass each pin with 1000pF and 0.1µF capacitors as close to the pins as possible.

V_{OCM} (Pin 2): This pin sets the output common mode voltage. A 0.1µF external bypass capacitor is recommended.

V^- (Pins 4, 9, 12, 17): Negative Power Supply. All four pins must be connected to the same voltage/ground.

–OUT, +OUT (Pins 5, 8): Unfiltered Outputs. These pins have 12.5Ω series resistors.

–OUTF, +OUTF (Pins 6, 7): Filtered Outputs. These pins have 50Ω series resistors and a 1.7pF shunt capacitance.

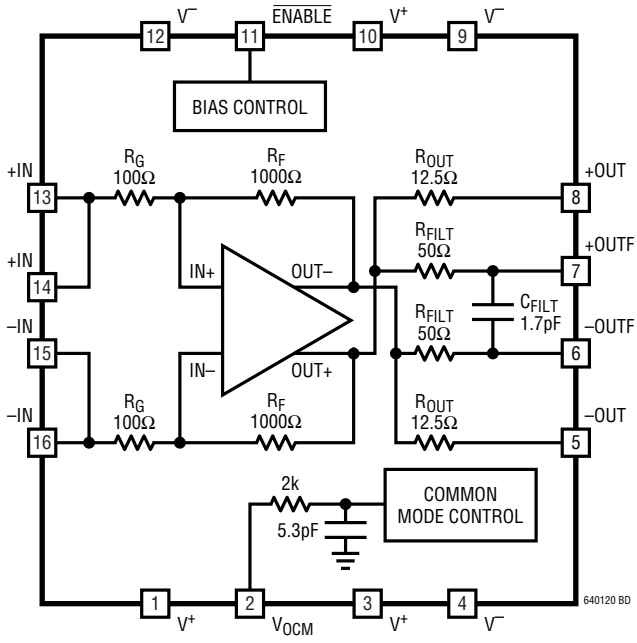
$\overline{\text{ENABLE}}$ (Pin 11): This pin is a logic input referenced to V^-. If low, the part is enabled. If high, the part is disabled and draws approximately 1mA supply current.

+IN (Pins 13, 14): Positive Input. Pins 13 and 14 are internally shorted together.

–IN (Pins 15, 16): Negative Input. Pins 15 and 16 are internally shorted together.

Exposed Pad (Pin 17): V^-. The Exposed Pad must be connected to the same voltage/ground as pins 4, 9, 12.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Circuit Operation

The LTC6401-20 is a low noise and low distortion fully differential op amp/ADC driver with:

- Operation from DC to 1.3GHz –3dB bandwidth impedance
- Fixed gain of 10V/V (20dB)
- Differential input impedance 200Ω
- Differential output impedance 25Ω
- Differential impedance of output filter 100Ω

The LTC6401-20 is composed of a fully differential amplifier with on chip feedback and output common mode voltage control circuitry. Differential gain and input impedance are set by 100Ω/1000Ω resistors in the feedback network. Small output resistors of 12.5Ω improve the circuit stability over various load conditions. They also provide a possible external filtering option, which is often desirable when the load is an ADC.

Filter resistors of 50Ω are available for additional filtering. Lowpass/bandpass filters are easily implemented with just a couple of external components. Moreover, they offer single-ended 50Ω matching in wideband applications and no external resistor is needed.

The LTC6401-20 is very flexible in terms of I/O coupling. It can be AC- or DC-coupled at the inputs, the outputs or both. Due to the internal connection between input and output, users are advised to keep input common mode voltage between 1V and 1.6V for proper operation. If the inputs are AC-coupled, the input common mode voltage is automatically biased close to V_{OCM} and thus no external circuitry is needed for bias. The LTC6401-20 provides an output common mode voltage set by V_{OCM}, which allows driving an ADC directly without external components such as a transformer or AC coupling capacitors. The input signal can be either single-ended or differential with only minor differences in distortion performance.

Input Impedance and Matching

The differential input impedance of the LTC6401-20 is 200Ω. If a 200Ω source impedance is unavailable, then the differential inputs may need to be terminated to a lower value impedance, e.g. 50Ω, in order to provide an impedance match to the source. Several choices are available. One approach is to use a differential shunt resistor (Figure 1). Another approach is to employ a wideband transformer (Figure 2). Both methods provide a wideband match. The termination resistor or the transformer must be placed close to the input pins in order to minimize the reflection due to input mismatch. Alternatively, one could apply a narrowband impedance match at the inputs of the LTC6401-20 for frequency selection and/or noise reduction.

Referring to Figure 3, LTC6401-20 can be easily configured for single-ended input and differential output without a balun. The signal is fed to one of the inputs through a matching network while the other input is connected to the same matching network and a source resistor. Because the return ratios of the two feedback paths are equal, the

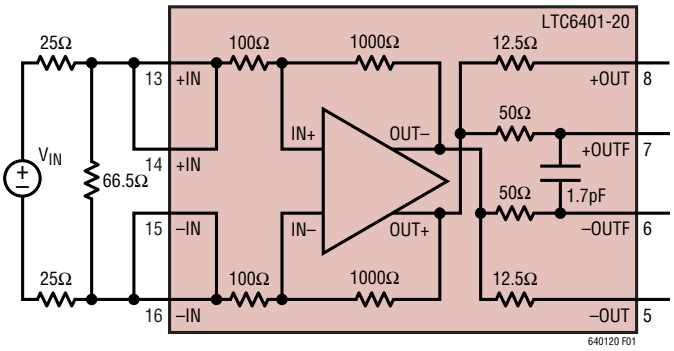


Figure 1. Input Termination for Differential 50Ω Input Impedance Using Shunt Resistor

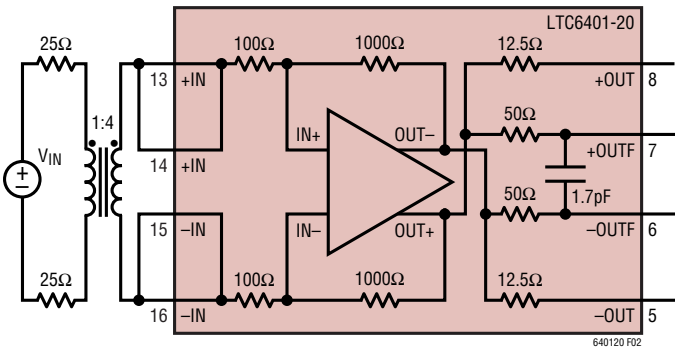


Figure 2. Input Termination for Differential 50Ω Input Impedance Using a 1:4 Balun

APPLICATIONS INFORMATION

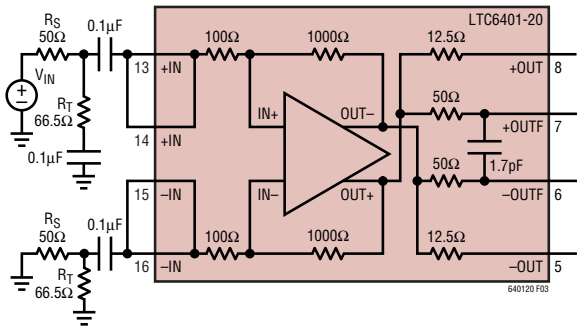


Figure 3. Input Termination for Single-Ended 50Ω Input Impedance

two outputs have the same gain and thus symmetrical swing. In general, the single-ended input impedance and termination resistor R_T are determined by the combination of R_S, R_G and R_F. For example, when R_S is 50Ω, it is found that the single-ended input impedance is 200Ω and R_T is 66.5Ω in order to match to a 50Ω source impedance.

The LTC6401-20 is unconditionally stable. However, the overall differential gain is affected by both source impedance and load impedance as shown in Figure 4:

$$A_V = \left|\frac{V_{OUT}}{V_{IN}}\right| = \frac{2000}{R_S + 200} \bullet \frac{R_L}{25 + R_L}$$

The noise performance of the LTC6401-20 also depends upon the source impedance and termination. For example, an input 1:4 balun transformer in Figure 2 improves SNR by adding 6dB of gain at the inputs. A trade-off between gain and noise is obvious when constant noise figure circle and constant gain circle are plotted within the same

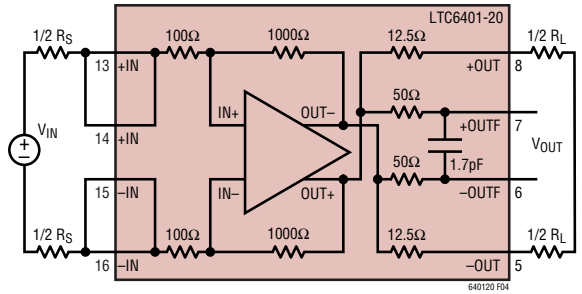


Figure 4. Calculate Differential Gain

input Smith Chart, based on which users can choose the optimal source impedance for a given gain and noise requirement.

Output Match and Filter

The LTC6401-20 can drive an ADC directly without external output impedance matching. Alternatively, the differential output impedance of 25Ω can be matched to higher value impedance, e.g. 50Ω, by series resistors or an LC network.

The internal low pass filter outputs at +OUTF/–OUTF have a –3dB bandwidth of 590MHz. External capacitor can reduce the low pass filter bandwidth as shown in Figure 5. A bandpass filter is easily implemented with only a few components as shown in Figure 6. Three 39pF capacitors and a 16nH inductor create a bandpass filter with 165MHz center frequency, –3dB frequencies at 138MHz and 200MHz.

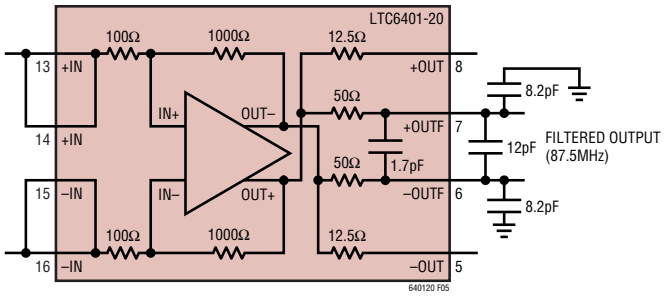


Figure 5. LTC6401-20 Internal Filter Topology Modified for Low Filter Bandwidth (Three External Capacitors)

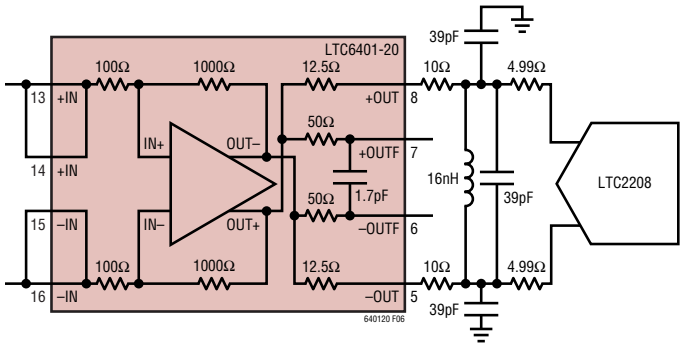


Figure 6. LTC6401-20 Application Circuit for Bandpass Filtering (Three External Capacitors, One External Inductor)

APPLICATIONS INFORMATION

Output Common Mode Adjustment

The LTC6401-20's output common mode voltage is set by the V_{OCM} pin, which is a high impedance input. The output common mode voltage is capable of tracking V_{OCM} in a range from 1V to 1.6V. Bandwidth of V_{OCM} control is typically 15MHz, which is dominated by a low pass filter connected to the V_{OCM} pin and is aimed to reduce common mode noise generation at the outputs. The internal common mode feedback loop has a –3dB bandwidth around 300MHz, allowing fast common mode rejection at the outputs of the LTC6401-20. The V_{OCM} pin should be tied to a DC bias voltage where a 0.1µF bypass capacitor is recommended. When interfacing with A/D converters such as the LT22xx families, the V_{OCM} can be normally connected to the V_{CM} pin of the ADC.

Driving A/D Converters

The LTC6401-20 has been specifically designed to interface directly with high speed A/D converters. In Figure 7, an example schematic shows the LTC6401-20 with a single-ended input driving the LTC2208, which is a 16-bit, 130Msps ADC. Two external 10Ω resistors help eliminate potential resonance associated with stray capacitance of PCB traces and bond wire inductance of either the ADC input or the driver output. V_{OCM} of the LTC6401-20 is connected to V_{CM} of the LTC2208 at 1.25V. Alternatively, a single-ended input signal can be converted to differential signal via a balun and fed to the input of the LTC6401-20. The balun also converts input impedance to match 50Ω source impedance.

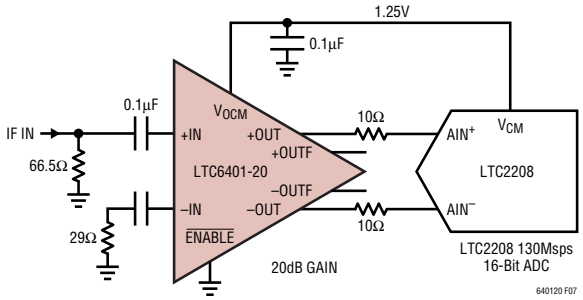


Figure 7. Single-Ended Input to LTC6401-20 and LTC2208

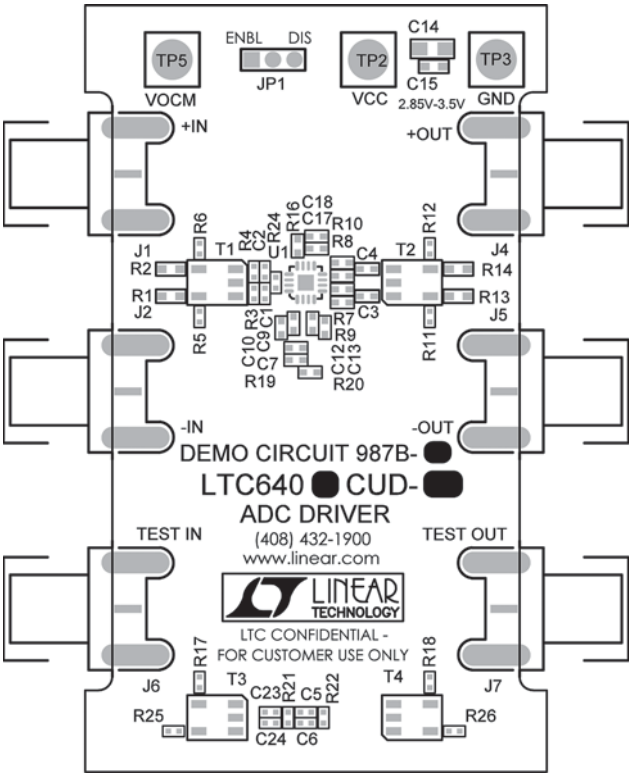
Test Circuits

Due to the fully-differential design of the LTC6401 and its usefulness in applications with differing characteristic specifications, two test circuits are used to generate the information in this datasheet. Test Circuit A is DC987B, a two-port demonstration circuit for the LTC6401 family. The schematic and silkscreen are shown below. This circuit includes input and output transformers (baluns) for single-ended-to-differential conversion and impedance transformation, allowing direct hook-up to a 2-port network analyzer. There are also series resistors at the output to present the LTC6401 with a 375Ω differential load, optimizing distortion performance. Due to the input and output transformers, the –3dB bandwidth is reduced from 1.3GHz to approximately 1.1GHz.

Test Circuit B uses a 4-port network analyzer to measure S-parameters and gain/phase response. This removes the effects of the wideband baluns and associated circuitry, for a true picture of the >1GHz S-parameters and AC characteristics.

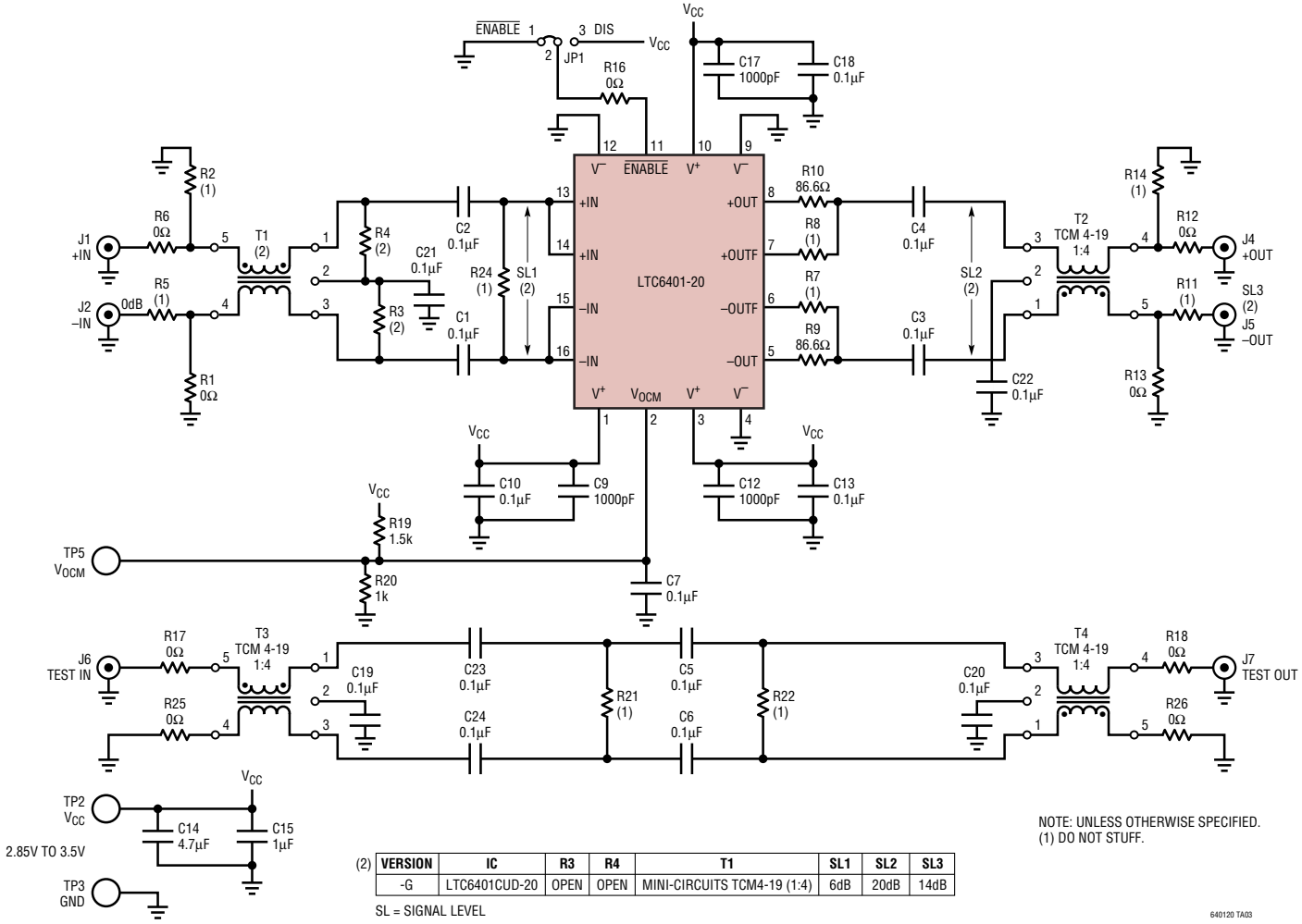
APPLICATIONS INFORMATION

Top Silkscreen



TYPICAL APPLICATION

Demo Circuit 987B Schematic (Test Circuit A)



NOTE: UNLESS OTHERWISE SPECIFIED.
(1) DO NOT STUFF.

(2)

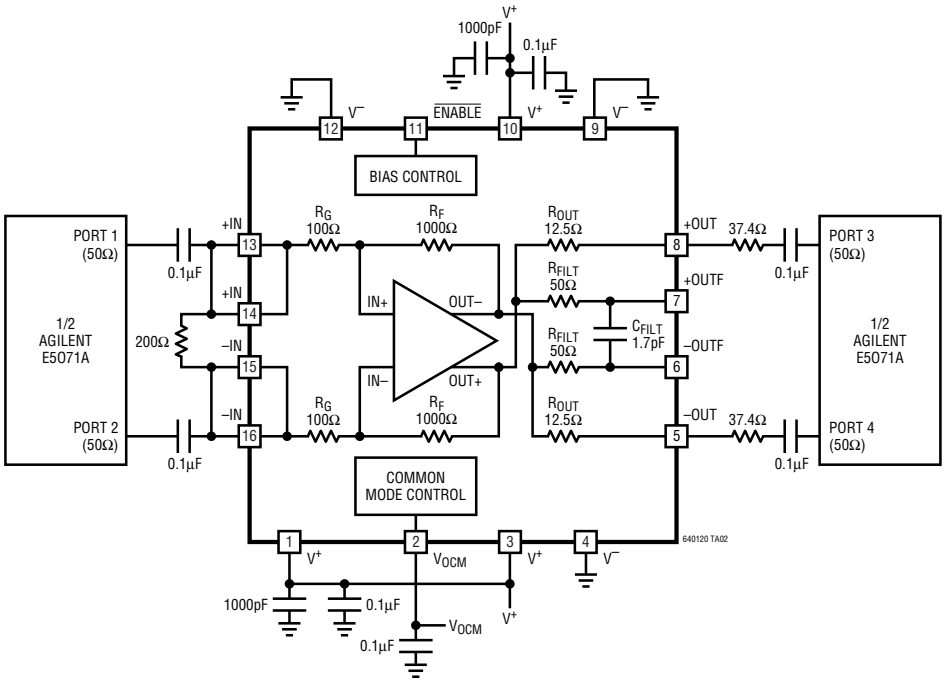
VERSION	IC	R3	R4	T1	SL1	SL2	SL3
-G	LTC6401CUD-20	OPEN	OPEN	MINI-CIRCUITS TCM4-19 (1:4)	6dB	20dB	14dB

SL = SIGNAL LEVEL

640120 TA03

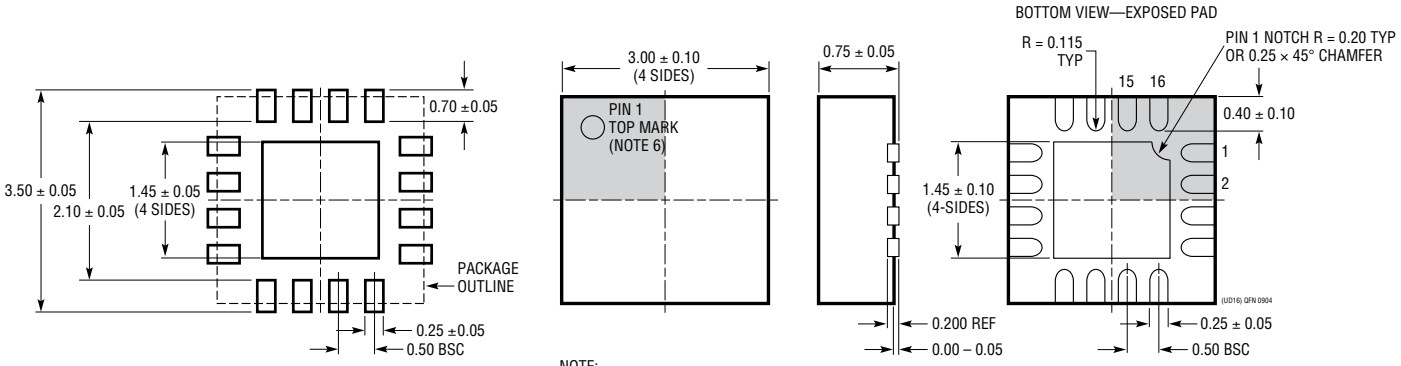
TYPICAL APPLICATION

Test Circuit B, 4-Port Analysis



PACKAGE DESCRIPTION

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691)



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
High-Speed Differential Amplifiers/Differential Op Amps		
LT1993-2	800MHz Differential Amplifier/ADC Driver	A_V = 2V/V, OIP3 = 38dBm at 70MHz
LT1993-4	900MHz Differential Amplifier/ADC Driver	A_V = 4V/V, OIP3 = 40dBm at 70MHz
LT1993-10	700MHz Differential Amplifier/ADC Driver	A_V = 10V/V, OIP3 = 40dBm at 70MHz
LT1994	Low Noise, Low Distortion Differential Op Amp	16-Bit SNR and SFDR at 1MHz, Rail-to-Rail Outputs
LT5514	Ultralow Distortion IF Amplifier/ADC Driver with Digitally Controlled Gain	OIP3 = 47dBm at 100MHz, Gain Control Range 10.5dB to 33dB
LT5524	Low Distortion IF Amplifier/ADC Driver with Digitally Controlled Gain	OIP3 = 40dBm at 100MHz, Gain Control Range 4.5dB to 37dB
LTC6400-20	1.8GHz Low Noise, Low Distortion, Differential ADC Driver	A_V = 20dB, 90mA Supply Current, IMD_3 = –65dBc at 300MHz
LT6402-6	300MHz Differential Amplifier/ADC Driver	A_V = 6dB, Distortion < –80dBc at 25MHz
LT6402-12	300MHz Differential Amplifier/ADC Driver	A_V = 12dB, Distortion < –80dBc at 25MHz
LT6402-20	300MHz Differential Amplifier/ADC Driver	A_V = 20dB, Distortion < –80dBc at 25MHz
LTC6406	3GHz Rail-to-Rail Input Differential Op Amp	1.6nV/$\sqrt{Hz}$ Noise, –72dBc Distortion at 50MHz, 18mA
LT6411	Low Power Differential ADC Driver/Dual Selectable Gain Amplifier	16mA Supply Current, IMD3 = –83dBc at 70MHz, A_V = 1, –1 or 2
High-Speed Single-Ended Output Op Amps		
LT1812/LT1813/ LT1814	High Slew Rate Low Cost Single/Dual/Quad Op Amps	8nV/$\sqrt{Hz}$ Noise, 750V/µs, 3mA Supply Current
LT1815/LT1816/ LT1817	Very High Slew Rate Low Cost Single/Dual/Quad Op Amps	6nV/$\sqrt{Hz}$ Noise, 1500V/µs, 6.5mA Supply Current
LT1818/LT1819	Ultra High Slew Rate Low Cost Single/Dual Op Amps	6nV/$\sqrt{Hz}$ Noise, 2500V/µs, 9mA Supply Current
LT6200/LT6201	Rail-to-Rail Input and Output Low Noise Single/Dual Op Amps	0.95nV/$\sqrt{Hz}$ Noise, 165MHz GBW, Distortion = –80dBc at 1MHz
LT6202/LT6203/ LT6204	Rail-to-Rail Input and Output Low Noise Single/Dual/Quad Op Amps	1.9nV/$\sqrt{Hz}$ Noise, 3mA Supply Current, 100MHz GBW
LT6230/LT6231/ LT6232	Rail-to-Rail Output Low Noise Single/Dual/Quad Op Amps	1.1nV/$\sqrt{Hz}$ Noise, 3.5mA Supply Current, 215MHz GBW
LT6233/LT6234/ LT6235	Rail-to-Rail Output Low Noise Single/Dual/Quad Op Amps	1.9nV/$\sqrt{Hz}$ Noise, 1.2mA Supply Current, 60MHz GBW
Integrated Filters		
LTC1562-2	Very Low Noise, 8th Order Filter Building Block	Lowpass and Bandpass Filters up to 300kHz
LT1568	Very Low Noise, 4th Order Filter Building Block	Lowpass and Bandpass Filters up to 10MHz
LTC1569-7	Linear Phase, Tunable 10th Order Lowpass Filter	Single-Resistor Programmable Cut-Off to 300kHz
LT6600-2.5	Very Low Noise Differential 2.5MHz Lowpass Filter	SNR = 86dB at 3V Supply, 4th Order Filter
LT6600-5	Very Low Noise Differential 5MHz Lowpass Filter	SNR = 82dB at 3V Supply, 4th Order Filter
LT6600-10	Very Low Noise Differential 10MHz Lowpass Filter	SNR = 82dB at 3V Supply, 4th Order Filter
LT6600-15	Very Low Noise Differential 15MHz Lowpass Filter	SNR = 76dB at 3V Supply, 4th Order Filter
LT6600-20	Very Low Noise Differential 20MHz Lowpass Filter	SNR = 76dB at 3V Supply, 4th Order Filter

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1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT 0907 • PRINTED IN USA

Freescale Semiconductor
Technical Data

Document Number: MHVIC915NR2
Rev. 9, 5/2006

RoHS

RF LDMOS Wideband Integrated Power Amplifier

The MHVIC915NR2 wideband integrated circuit is designed with on-chip matching that makes it usable from 750 to 1000 MHz. This multi-stage structure is rated for 26 to 28 Volt operation and covers all typical cellular base station modulation formats.

Final Application

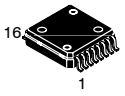
- Typical Single-Carrier N-CDMA Performance: V_{DD} = 27 Volts, I_{DQ1} = 80 mA, I_{DQ2} = 120 mA, P_{out} = 34 dBm, Full Frequency Band (746 to 960 MHz), IS-95 CDMA (Pilot, Sync, Paging, Traffic Codes 8 Through 13)
  Power Gain — 31 dB
  Power Added Efficiency — 21%
  ACPR @ 750 kHz Offset — -50 dBc in 30 kHz Bandwidth

Driver Applications

- Typical Single-Carrier N-CDMA Performance: V_{DD} = 27 Volts, I_{DQ1} = 80 mA, I_{DQ2} = 120 mA, P_{out} = 23 dBm, Full Frequency Band (869-894 MHz), IS-95 CDMA (Pilot, Sync, Paging, Traffic Codes 8 Through 13), Channel Bandwidth = 1.2288 MHz. PAR = 9.8 dB @ 0.01% Probability on CCDF.
  Power Gain — 31 dB
  Power Added Efficiency — 21%
  ACPR @ 750 kHz Offset — -60 dBc in 30 kHz Bandwidth
  ACPR @ 1.98 MHz Offset — -66 dBc in 30 kHz Bandwidth
- Typical GSM Performance: V_{DD} = 26 Volts, P_{out} = 15 W P1dB, Full Frequency Band (921-960 MHz)
  Power Gain — 30 dB @ P1dB
  Power Added Efficiency = 56% @ P1dB
- Capable of Handling 3:1 VSWR, @ 27 Vdc, 880 MHz, 15 Watts CW Output Power
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked, >9 Ohm Output)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function
- On-Chip Current Mirror g_m Reference FET for Self Biasing Application (1)
- Integrated ESD Protection
- RoHS Compliant
- In Tape and Reel. R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.

MHVIC915NR2

**746-960 MHz, 15 W, 27 V
SINGLE N-CDMA, GSM/GSM EDGE
RF LDMOS WIDEBAND
INTEGRATED POWER AMPLIFIER**



**CASE 978-03
PFP-16
PLASTIC**

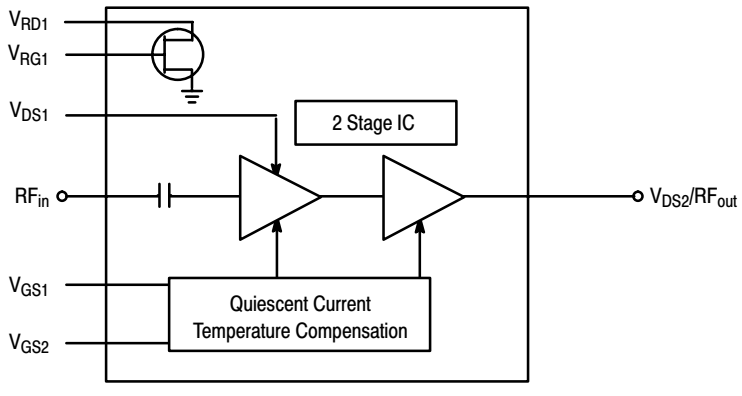
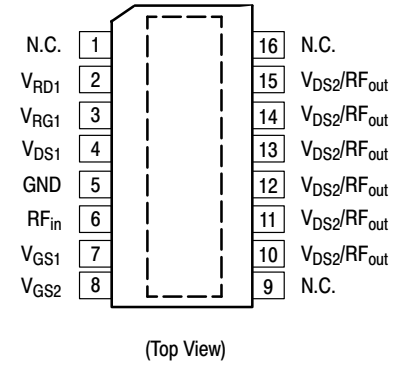


Figure 1. Block Diagram



(Top View)

Note: Exposed backside flag is source terminal for transistors.

Figure 2. Pin Connections

1. Refer to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1987.

freescale semiconductor

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	150	°C

Table 2. Thermal Characteristics

Characteristic		Symbol	Value (1)	Unit
Thermal Resistance, Junction to Case		$R_{\theta JC}$		°C/W
Driver Application (P_{out} = 0.2 W CW)	Stage 1, 27 Vdc, I_{DQ} = 80 mA		15.1	
	Stage 2, 27 Vdc, I_{DQ} = 120 mA		5.1	
Output Application (P_{out} = 2.5 W CW)	Stage 1, 27 Vdc, I_{DQ} = 80 mA		15.8	
	Stage 2, 27 Vdc, I_{DQ} = 120 mA		5.0	
GSM Application (P_{out} = 15 W CW)	Stage 1, 26 Vdc, I_{DQ} = 50 mA		13.8	
	Stage 2, 26 Vdc, I_{DQ} = 140 mA		4.5	

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	0 (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	II (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 27 Vdc, I_{DQ1} = 80 mA, I_{DQ2} = 120 mA, f = 880 MHz, Single-Carrier N-CDMA, 1.2288 MHz Channel Bandwidth Carrier. ACPR measured in 30 kHz Bandwidth @ ±750 MHz. PAR = 9.8 dB @ 0.01% Probability on CCDF					
Power Gain (P_{out} = 23 dBm)	G_{ps}	29	31	—	dB
Power Added Efficiency (P_{out} = 34 dBm)	PAE	—	21	—	%
Input Return Loss (P_{out} = 23 dBm)	IRL	—	-12	-9	dB
Adjacent Channel Power Ratio (P_{out} = 23 dBm)	ACPR	—	-60	-55	dBc
Adjacent Channel Power Ratio (P_{out} = 34 dBm)	ACPR	—	-50	—	dBc
Gain Flatness @ P_{out} = 23 dBm (865 MHz to 895 MHz)	G_F	—	0.2	0.4	dB
Bias Sense FET Drain Current V_{BSD} = 27 V $V_{BIAS\ BSG}$ = $V_{BIAS2\ Q2}$ @ I_{DQ2} = 120 mA	I_{BSD}	0.8	1.2	1.6	mA

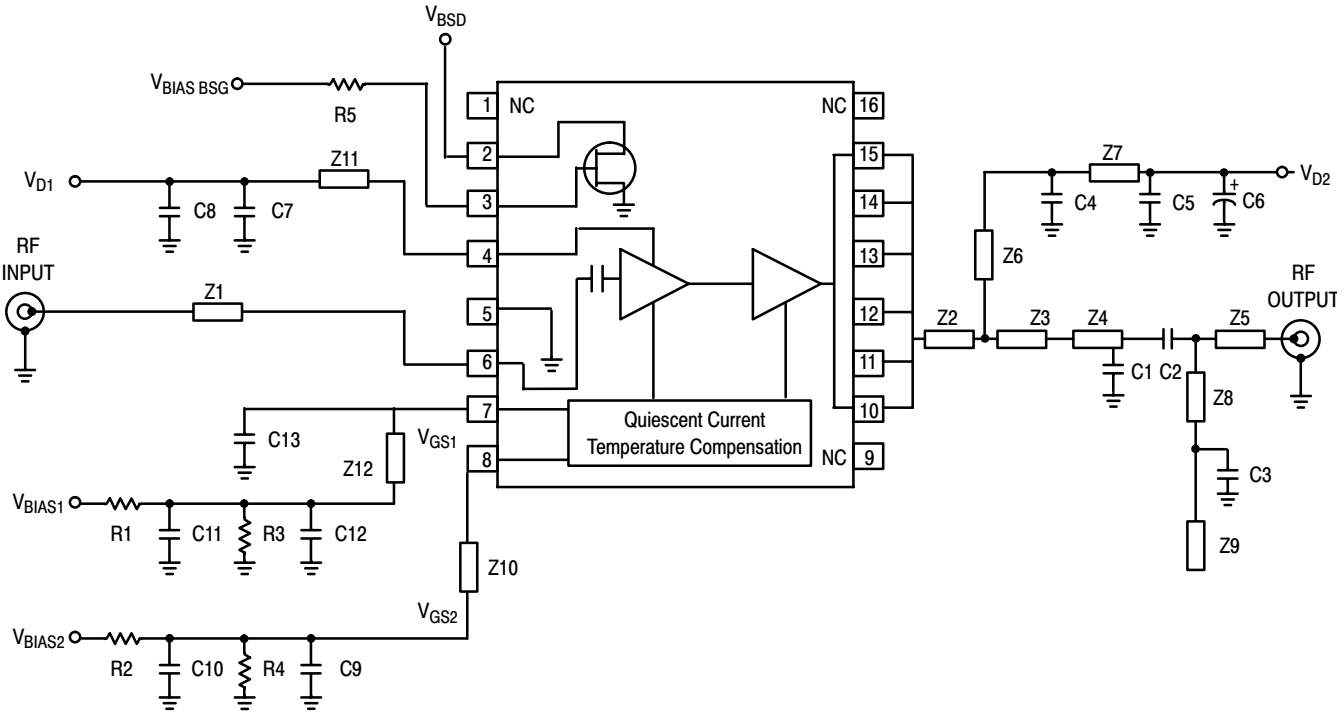
1. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

(continued)

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 27 Vdc, I_{DQ1} = 80 mA, I_{DQ2} = 120 mA, 865-895 MHz					
Quiescent Current Accuracy over Temperature (-10 to 85°C) at Nominal Value (1)	ΔI_{QT}	—	±5	—	%
Gain Flatness in 30 MHz Bandwidth @ P_{out} = 23 dBm (800 MHz to 960 MHz)	G_F	—	0.20	—	dB
Deviation from Linear Phase in 30 MHz Bandwidth @ P_{out} = 23 dBm	Φ	—	±0.2	—	°
Group Delay @ P_{out} = 23 dBm Including Output Matching	Delay	—	2.2	—	ns
Part to Part Phase Variation @ P_{out} = 23 dBm	$\Phi\Delta$	—	±10	—	°
Typical GSM Performances (In Freescale GSM Test Fixture, 50 ohm system) V_{DD} = 26 Vdc, I_{DQ1} = 50 mA, I_{DQ2} = 140 mA, 921-960 MHz, CW					
Output Power, 1 dB Compression Point	P1dB	—	15	—	W
Power Gain @ P1dB	G_{ps}	—	30	—	dB
Power Added Efficiency @ P1dB	PAE	—	56	—	%
Input Return Loss @ P1dB	IRL	—	-16	—	dB
Error Vector Magnitude @ 5 W	—	—	0.9	—	%
Intermodulation Distortion (15 W PEP, 2-Tone, 100 kHz Tone Spacing)	IMD	—	-30	—	dBc
Power Added Efficiency (15 W PEP, 2-Tone, 100 kHz Tone Spacing)	PAE	—	35	—	%

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1977.

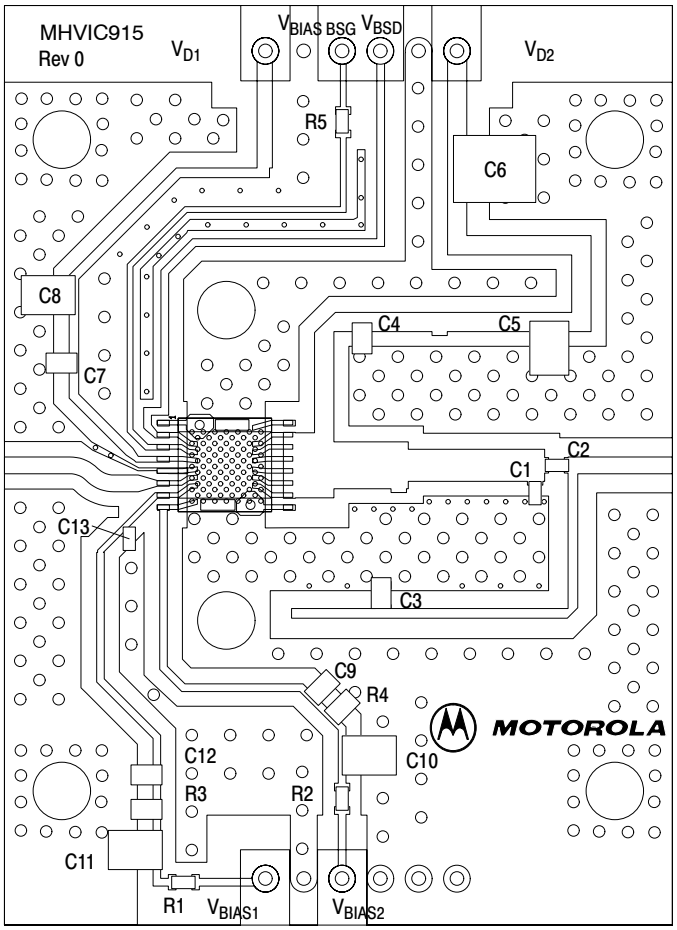


Z1	0.0438″ x 0.400″ 50 Ω Microstrip	Z7	0.0504″ x 0.480″ Microstrip
Z2	0.1709″ x 0.1004″ Microstrip (not including IC pad length)	Z8	0.0252″ x 0.843″ Microstrip
		Z9	0.0252″ x 0.167″ Microstrip
Z3	0.1222″ x 0.1944″ Microstrip	Z10	0.040″ x 0.850″ Microstrip
Z4	0.0836″ x 0.3561″ Microstrip	Z11	0.025″ x 0.400″ Microstrip
Z5	0.0438″ x 0.2725″ Microstrip	Z12	0.020″ x 0.710″ Microstrip
Z6	0.0504″ x 0.3378″ Microstrip	PCB	Rogers 4350, 0.020″, ε_r = 3.50

Figure 3. MHVIC915NR2 Test Circuit Schematic

Table 6. MHVIC915NR2 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2	4.7 pF High Q Capacitors (0603)	ATC600S4R7CW	ATC
C3, C4	47 pF NPO Capacitors (0805)	GRM40-001COG470J050BD	Murata
C5, C8, C10, C11	1 μF X7R Chip Capacitors (1214)	GRM42-2X7R105K050AL	Murata
C6	10 μF, 50 V Electrolytic Capacitor	ECEV1HA100SP	Panasonic
C7, C9, C12	0.01 μF X7R Chip Capacitors (0805)	GRM40X7R103J050BD	Murata
C13	8.2 pF NPO Chip Capacitor (0805)	GRM40-001COG8R2C050BD	Murata
R1, R2, R5	1 kΩ Chip Resistors (0603)	RM73B2AT102J	KOA Speer
R3, R4	100 kΩ Chip Resistors (0603)	RM73B2AT104J	KOA Speer



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 4. MHVIC915NR2 Test Circuit Component Layout

TYPICAL CHARACTERISTICS (FREESCALE TEST FIXTURE, 50 OHM SYSTEM)

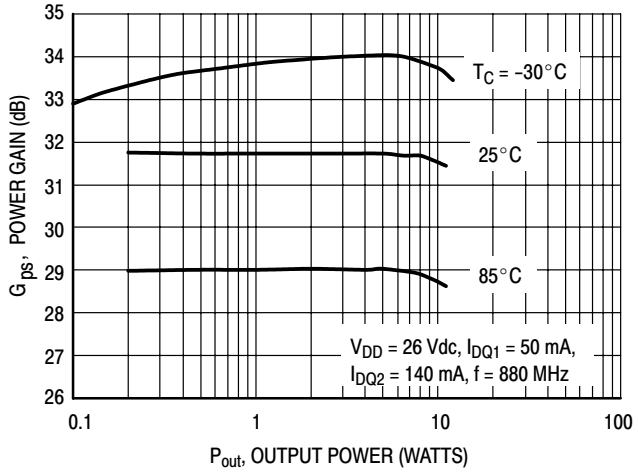


Figure 5. Power Gain versus Output Power

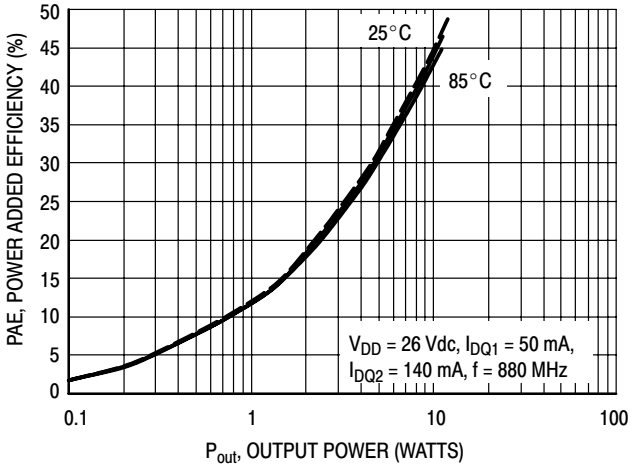


Figure 6. Power Added Efficiency versus Output Power

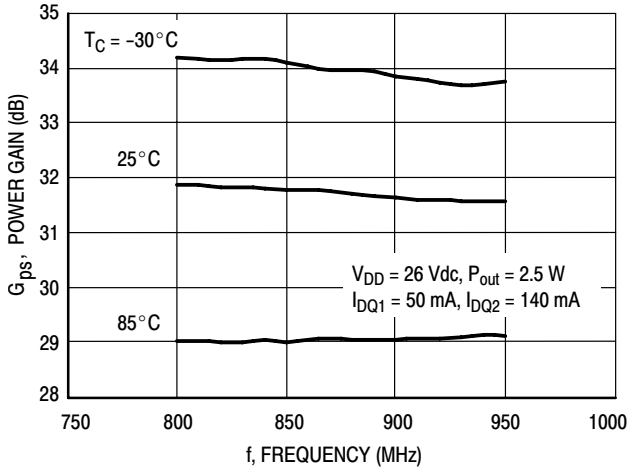


Figure 7. Power Gain versus Frequency

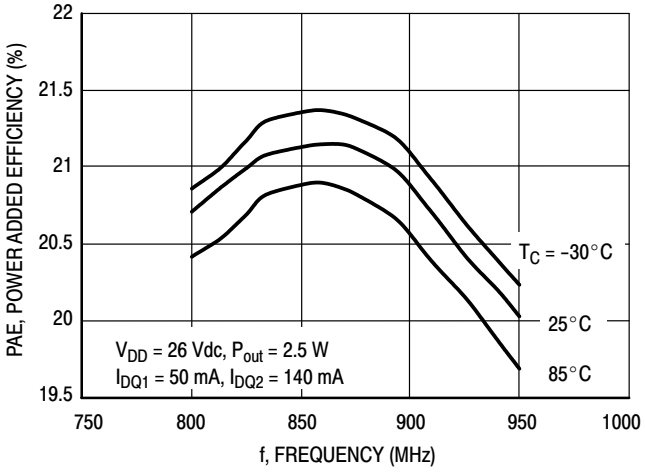


Figure 8. Power Added Efficiency versus Frequency

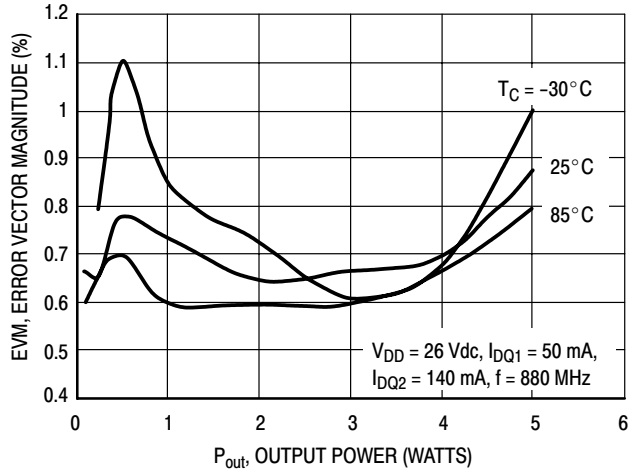


Figure 9. Error Vector Magnitude versus Output Power

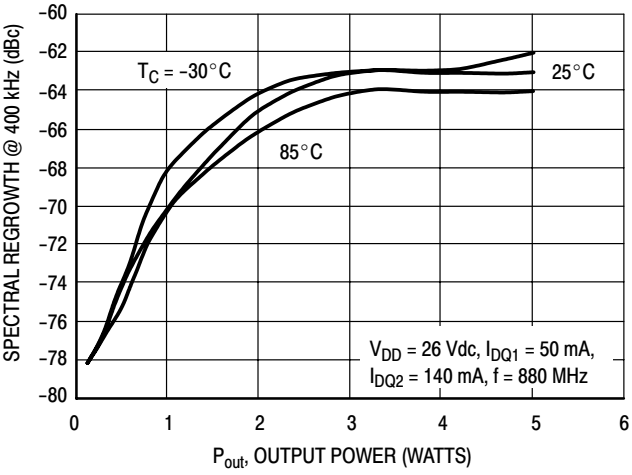


Figure 10. Spectral Regrowth @ 400 kHz versus Output Power

TYPICAL CHARACTERISTICS (FREESCALE TEST FIXTURE, 50 OHM SYSTEM)

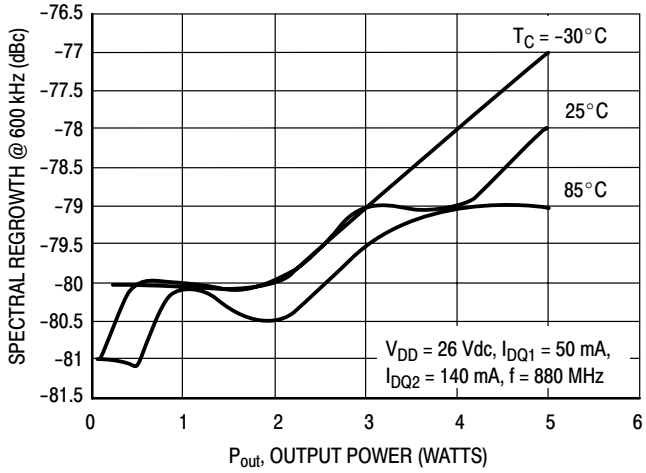


Figure 11. Spectral Regrowth @ 600 kHz versus Output Power

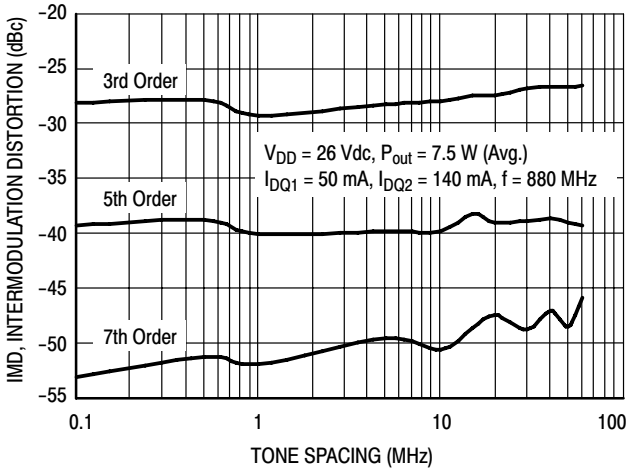


Figure 12. Two-Tone Broadband Performance

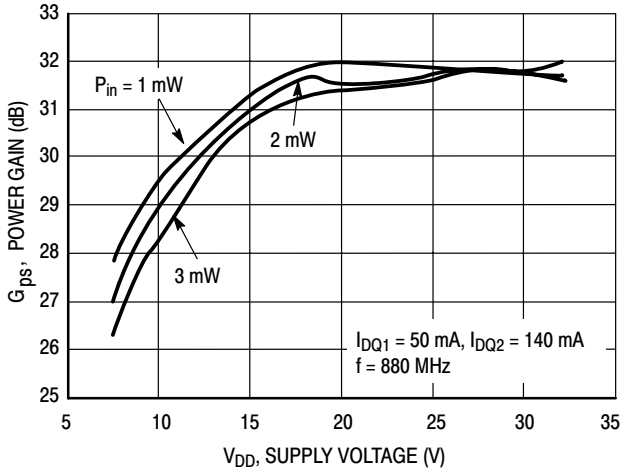


Figure 13. Power Gain versus Supply Voltage

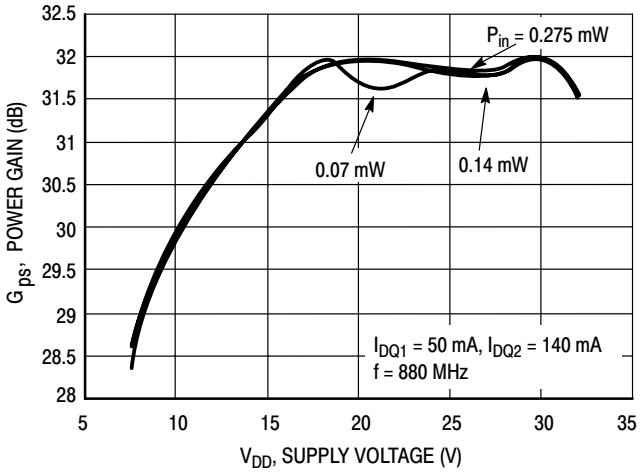


Figure 14. Power Gain versus Supply Voltage

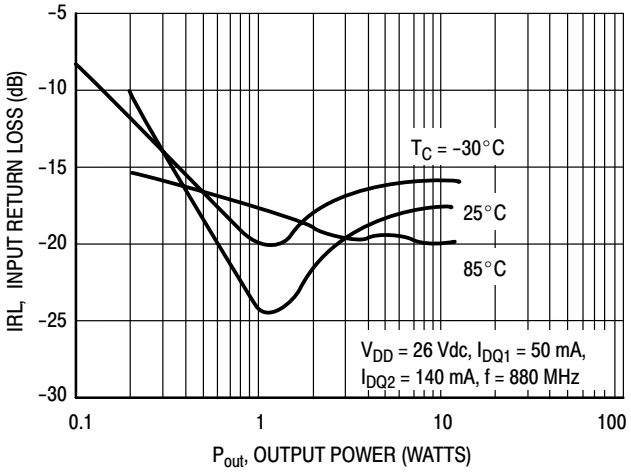


Figure 15. Input Return Loss versus Output Power

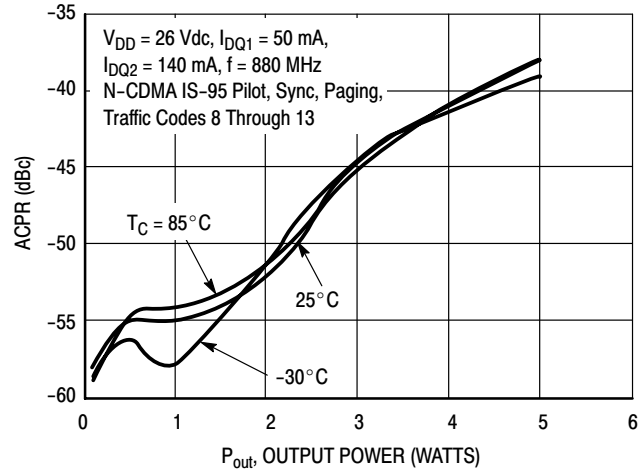
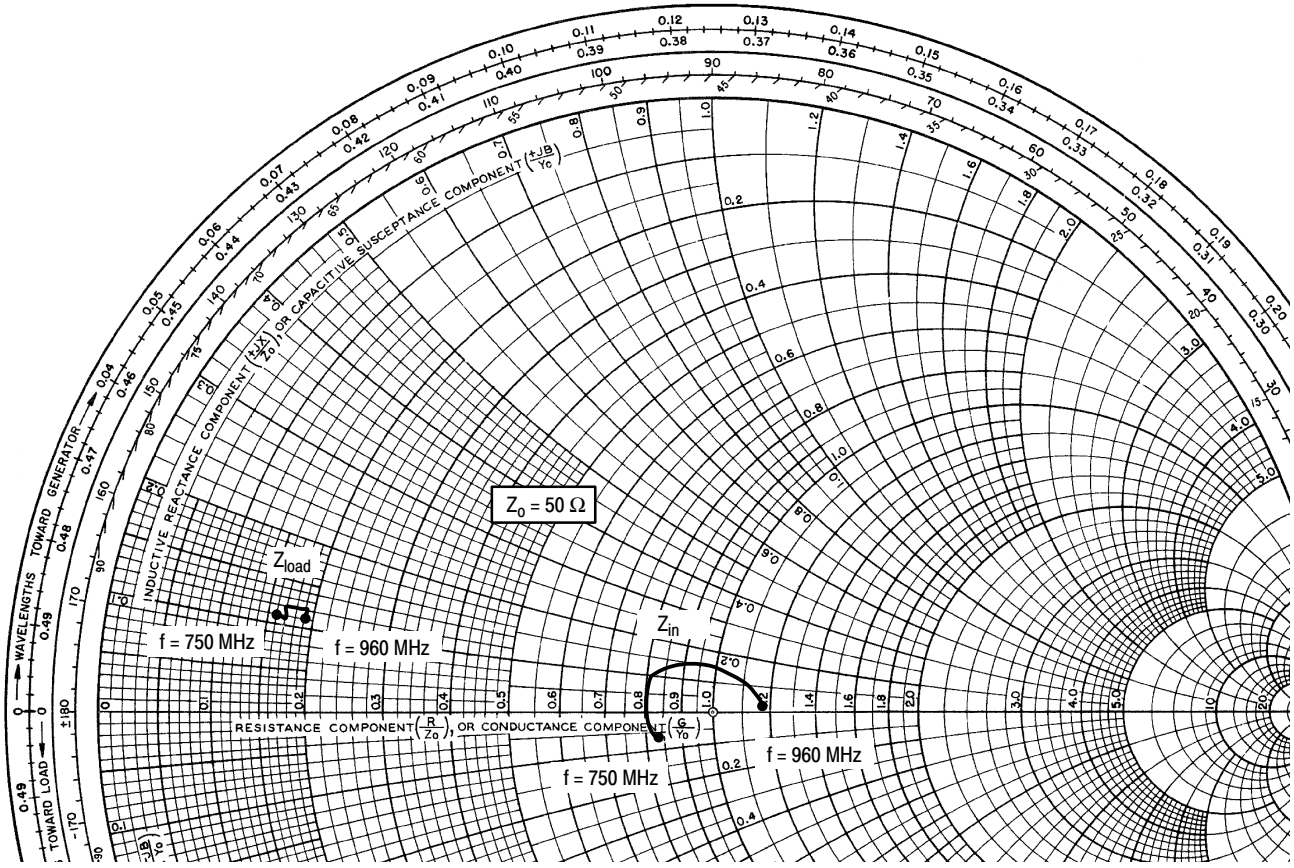


Figure 16. Adjacent Channel Power Ratio versus Output Power



V_{DD} = 26 Vdc, I_{DQ1} = 50 mA, I_{DQ2} = 140 mA, P_{out} = 1.25 W CW

f MHz	Z_{in} Ω	Z_{load} Ω
750	42.11 - j2.79	8.24 + j5.33
765	40.86 - j1.37	8.31 + j5.56
780	40.09 + j0.06	8.39 + j5.82
795	39.77 + j1.52	8.50 + j5.95
810	39.89 + j3.01	8.62 + j6.02
825	40.49 + j4.39	8.82 + j6.12
840	41.48 + j5.70	8.94 + j6.19
855	42.89 + j6.73	9.12 + j6.17
870	43.51 + j7.03	9.16 + j6.12
885	46.81 + j7.87	9.33 + j6.09
900	49.21 + j7.74	9.38 + j5.95
915	51.79 + j7.02	9.50 + j5.85
930	54.48 + j5.65	9.47 + j5.73
945	57.05 + j3.61	9.54 + j5.63
960	59.16 + j0.75	9.42 + j5.45

Z_{in} = Device input impedance as measured from RF input to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

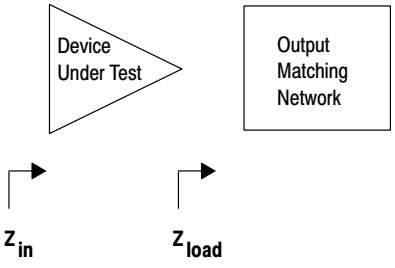
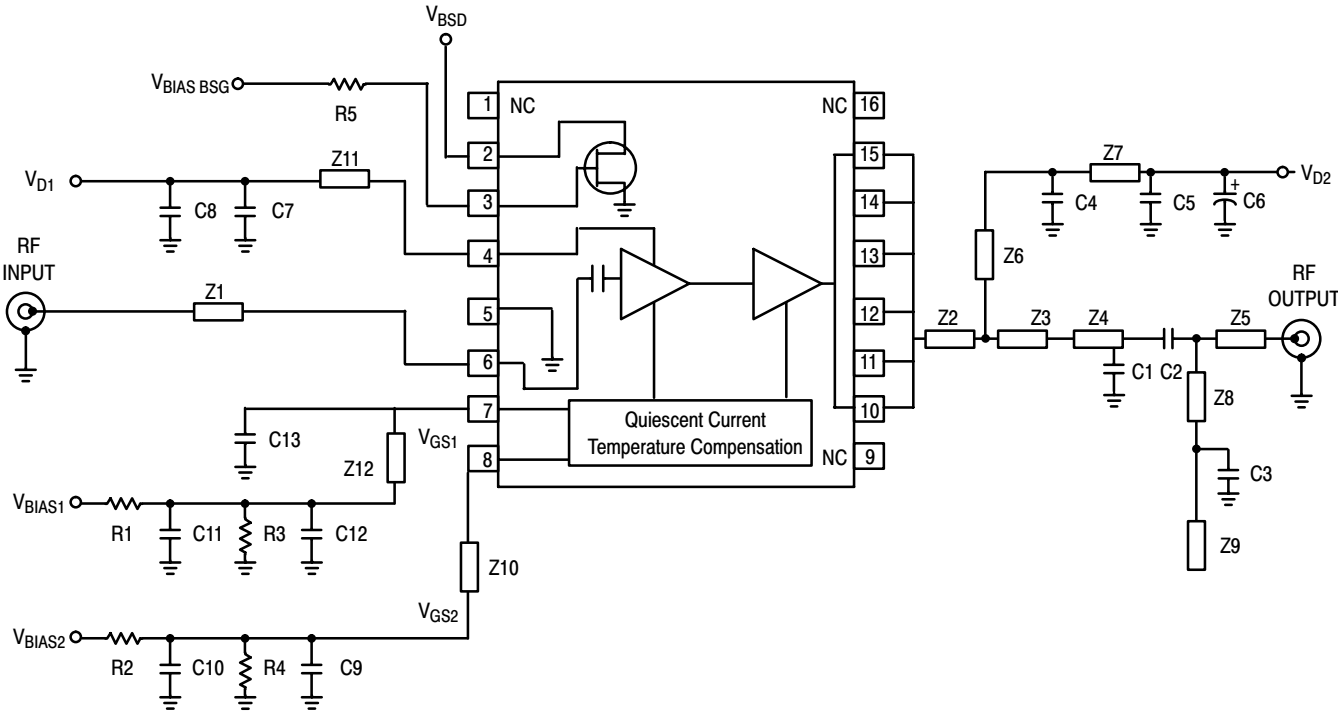


Figure 17. Series Equivalent Input and Load Impedance

DRIVER/PRE-DRIVER PERFORMANCE



Z1	0.0438″ x 0.400″ 50 Ω Microstrip	Z7	0.0504″ x 0.480″ Microstrip
Z2	0.1709″ x 0.1004″ Microstrip (not including IC pad length)	Z8	0.0252″ x 0.843″ Microstrip
		Z9	0.0252″ x 0.167″ Microstrip
Z3	0.1222″ x 0.1944″ Microstrip	Z10	0.040″ x 0.850″ Microstrip
Z4	0.0836″ x 0.3561″ Microstrip	Z11	0.025″ x 0.400″ Microstrip
Z5	0.0438″ x 0.2725″ Microstrip	Z12	0.020″ x 0.710″ Microstrip
Z6	0.0504″ x 0.3378″ Microstrip	PCB	Rogers 4350, 0.020″, ε_r = 3.50

Figure 18. MHVIC915NR2 Test Fixture Schematic—
Alternate Characterization for Driver/Pre-Driver Performance

Table 7. MHVIC915NR2 Test Fixture Component Designations and Values —
Alternate Characterization for Driver/Pre-Driver Performance

Part	Description	Part Number	Manufacturer
C1, C2	2.4 pF High Q Capacitors (0603)	ATC600S4R7CW	ATC
C3, C4	47 pF NPO Capacitors (0805)	GRM40-001COG470J050BD	Murata
C5, C8, C10, C11	1 μF X7R Chip Capacitors (1214)	GRM42-2X7R105K050AL	Murata
C6	10 μF, 50 V Electrolytic Capacitor	ECEV1HA100SP	Panasonic
C7, C9, C12	0.01 μF X7R Chip Capacitors (0805)	GRM40X7R103J050BD	Murata
C13	8.2 pF NPO Chip Capacitor (0805)	GRM40-001COG8R2C050BD	Murata
R1, R2, R5	1 kΩ Chip Resistors (0603)	RM73B2AT102J	KOA Speer
R3, R4	100 kΩ Chip Resistors (0603)	RM73B2AT104J	KOA Speer

DRIVER/PRE-DRIVER PERFORMANCE

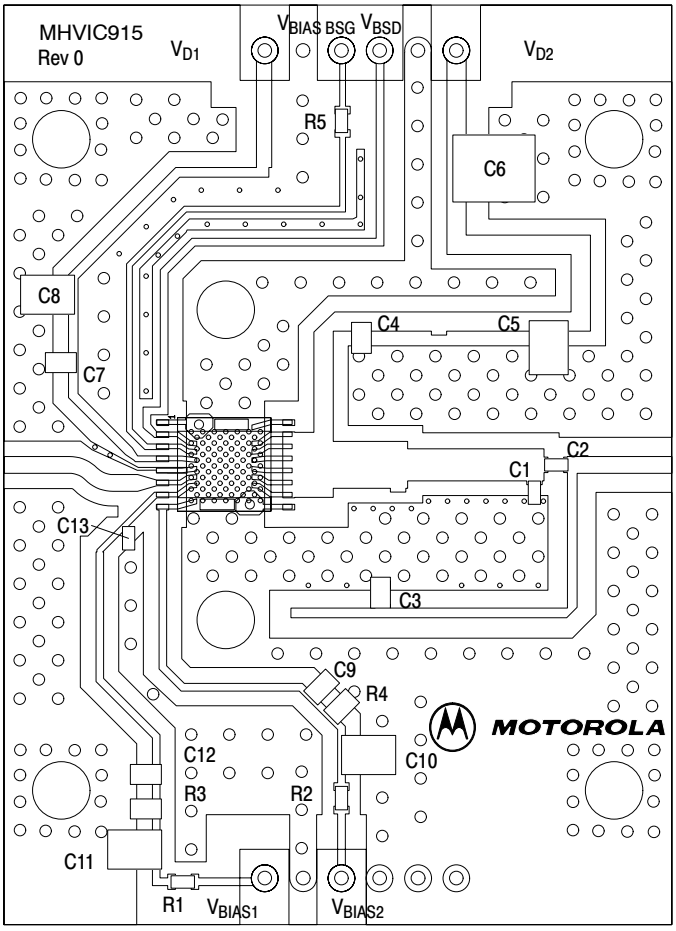


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Figure 19. MHVIC915NR2 Test Circuit Component Layout—
Alternate Characterization for Driver/Pre-Driver Performance

TYPICAL CHARACTERISTICS
DRIVER/PRE-DRIVER PERFORMANCE

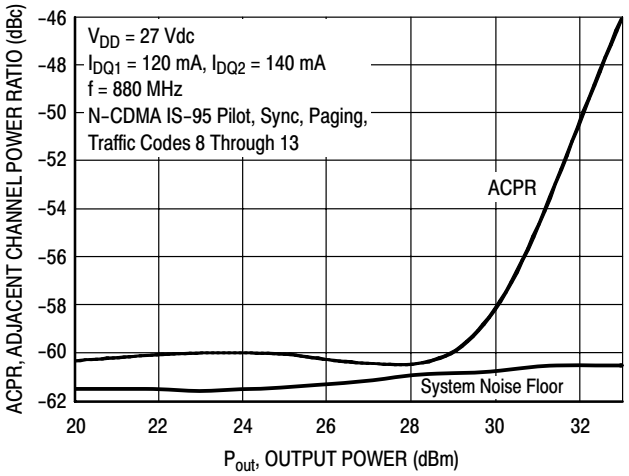
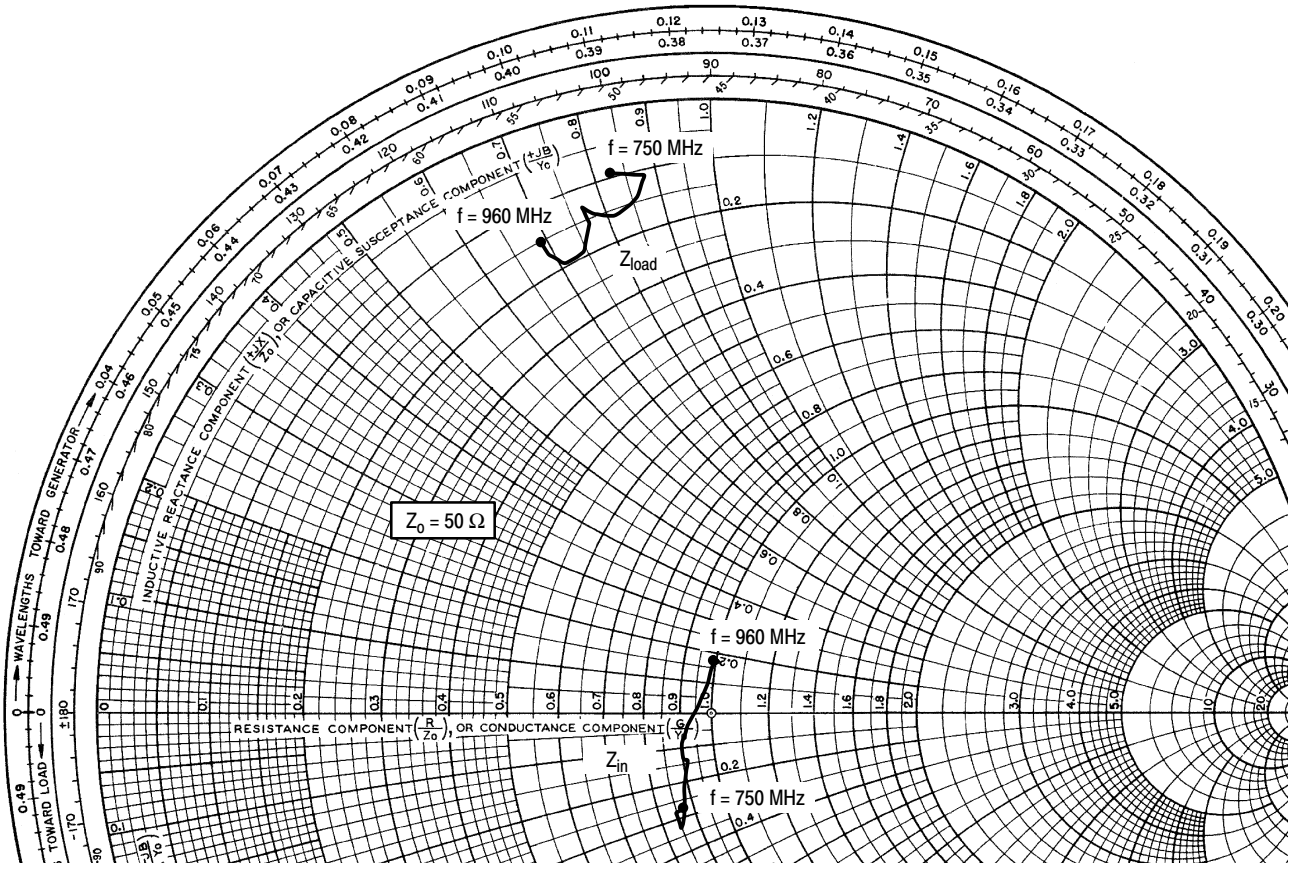


Figure 20. Single-Carrier N-CDMA ACPR versus Output Power



V_{DD} = 27 Vdc, I_{DQ1} = 120 mA, I_{DQ2} = 140 mA, P_{out} = 0.5 W CW

f MHz	Z_{in} Ω	Z_{load} Ω
750	43.5 - j13.4	4.7 + j41.5
765	42.9 - j13.9	5.5 + j43.8
780	42.7 - j14.2	6.0 + j43.7
795	42.3 - j15.9	6.8 + j42.8
810	42.7 - j16.0	7.5 + j42.2
825	44.5 - j10.5	7.8 + j40.5
840	45.5 - j7.0	7.2 + j39.2
855	45.0 - j6.5	6.3 + j38.4
870	45.0 - j4.5	6.4 + j38.7
885	46.0 - j1.5	7.9 + j38.5
900	48.3 + j2.4	9.3 + j36.8
915	49.5 + j7.3	9.4 + j35.3
930	49.6 + j7.8	8.6 + j34.5
945	49.8 + j8.4	7.8 + j34.3
960	49.5 + j8.6	7.6 + j34.3

Z_{in} = Device input impedance as measured from RF input to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

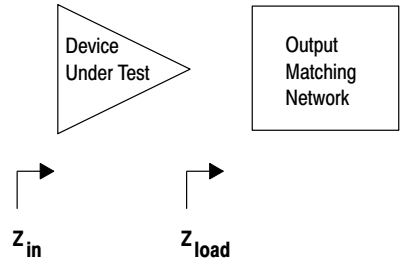
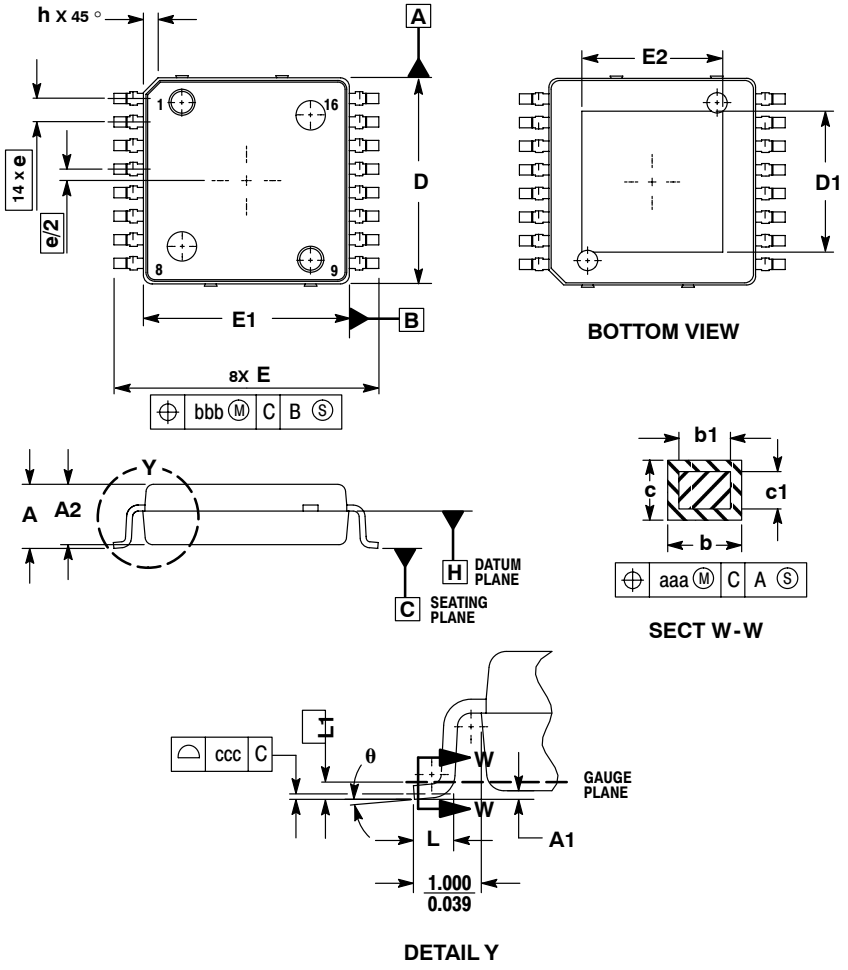


Figure 21. Series Equivalent Input and Load Impedance — Alternate Characterization for Driver/Pre-Driver Performance

NOTES

NOTES

PACKAGE DIMENSIONS



NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.

	MILLIMETERS	
DIM	MIN	MAX
A	2.000	2.300
A1	0.025	0.100
A2	1.950	2.100
D	6.950	7.100
D1	4.372	5.180
E	8.850	9.150
E1	6.950	7.100
E2	4.372	5.180
L	0.466	0.720
L1	0.250 BSC	
b	0.300	0.432
b1	0.300	0.375
c	0.180	0.279
c1	0.180	0.230
e	0.800 BSC	
h	---	0.600
θ	0°	7°
aaa	0.200	
bbb	0.200	
ccc	0.100	

CASE 978-03
ISSUE C
PFP-16
PLASTIC

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freescale™ semiconductor

Document Number: MHVIC915NR2
Rev. 9, 5/2006

Surface Mount

Low Pass Filter

SALF-865+
SALF-865

50Ω DC to 865 MHz

CASE STYLE: YY101
PRICE: $6.95 ea. QTY (1-9)

+ RoHS compliant in accordance with EU Directive (2002/95/EC)

The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications.

Maximum Ratings

Operating Temperature	-40°C to 85°C
Storage Temperature	-55°C to 100°C
Power Input	0.5W max.

Permanent damage may occur if any of these limits are exceeded.

Pin Connections

INPUT	1
OUTPUT	8
GROUND	2,3,4,5,6,7

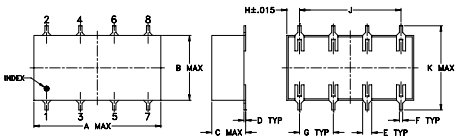
Features

- 7-section elliptic function
- excellent rejection

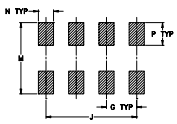
Applications

- defense communications
- receivers/transmitters
- harmonic rejection of VCOs

Outline Drawing



PCB Land Pattern



Suggested Layout,
Tolerance to be within ±.002

Outline Dimensions (inch / mm)

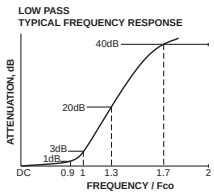
A	B	C	D	E	F	G
.75	.38	.20	.010	.050	.020	.200
19.05	9.65	5.08	0.25	1.27	0.51	5.08

H	J	K	M	N	P	wt
.075	.600	.450	.470	.100	.150	grams
1.91	15.24	11.43	11.94	2.54	3.81	1.6

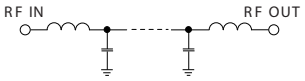
Low Pass Filter Electrical Specifications

PASSBAND (MHz) (loss <1 dB)	fco, (MHz) Nom. (loss 3 dB) Typ.	STOPBAND (MHz) (loss > 20 dB) Min.	STOPBAND (MHz) (loss > 35 dB) Min.	VSWR (:1) Pass band typ.	VSWR (:1) Stop band typ.
DC-865	980	1300-1400	1400-2550	1.4	18

typical frequency response



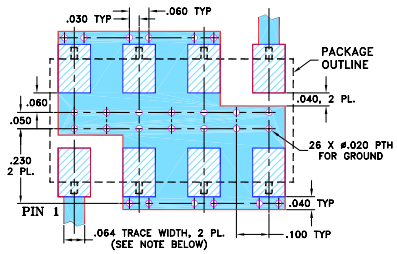
Electrical Schematic



Typical Performance Data

Frequency (MHz)	Insertion Loss (dB) x̄	Insertion Loss (dB) σ	Return Loss (dB)
1.00	0.02	0.00	52.50
200.00	0.19	0.01	18.38
425.00	0.28	0.01	18.30
650.00	0.35	0.00	25.24
800.00	0.52	0.01	18.75
865.00	0.54	0.01	29.17
900.00	0.66	0.04	21.87
910.00	0.75	0.06	18.31
980.00	2.19	0.25	6.10
1000.00	3.27	0.34	4.39
1210.00	20.21	0.60	0.48
1300.00	28.34	0.76	0.36
1400.00	40.68	1.67	0.37
1600.00	42.12	0.78	0.44
1800.00	40.14	0.36	0.43
2000.00	41.45	0.32	0.43
2400.00	53.98	1.66	0.49
2550.00	56.02	1.99	0.49
2600.00	53.42	1.94	0.47
3000.00	26.74	0.21	0.68

Demo Board MCL P/N: TB-187+
Suggested PCB Layout (PL-049)

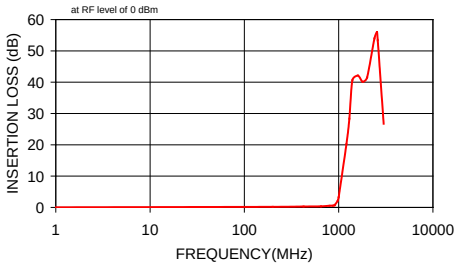


NOTES: 1. TRACE WIDTH IS SHOWN FOR ROGERS RO4350B WITH DIELECTRIC THICKNESS .030" ± .002"; COPPER: 1/2 OZ. EACH SIDE. FOR OTHER MATERIALS TRACE WIDTH MAY NEED TO BE MODIFIED.
2. BOTTOM SIDE OF THE PCB IS CONTINUOUS GROUND PLANE.

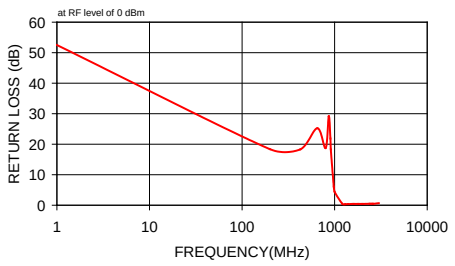
DENOTES PCB COPPER LAYOUT WITH SMOBC (SOLDER MASK OVER BARE COPPER)

DENOTES COPPER LAND PATTERN FREE OF SOLDER MASK

SALF-865
INSERTION LOSS



SALF-865
RETURN LOSS



REV. C
M111708
SALF-865
090820

- ***Low-Loss RF Filter for Mobile Systems***
- ***Low Amplitude Ripple***
- ***No Matching Network Required for Operating at 50Ω***
- ***Ultra Miniature Ceramic DCC6C SMD Package***
- ***Complies with Directive 2002/95/EC (RoHS Compliant)***

SF5912

ABSOLUTE MAXIMUM RATING (T_A=25°C)			
Parameter		Rating	Unit
Input Power Level	P_{in}	+10	dBm
DC Voltage	V_{DC}	0	V
Operating Temperature Range	T_A	-30 ~ +85	°C
Storage Temperature Range	T_{stg}	-45 ~ +85	°C

ELECTRONIC CHARACTERISTICS						
Parameter		Sym	Minimum	Typical	Maximum	Unit
Nominal Frequency (at 25°C) (Center frequency between 3dB point)		f_C	NS	806.00	NS	MHz
Insertion Loss	793.00 … 805.00 MHz	IL	-	2.0	3.5	dB
3dB Bandwidth		BW_3	-	-	-	MHz
Amplitude Ripple (p-p)	793.00 … 805.00 MHz	$\Delta\alpha$	-	0.8	1.5	dB
Input VSWR	793.00 … 805.00 MHz	-	-	1.5	2.0	-
Output VSWR	793.00 … 805.00 MHz	-	-	1.5	2.0	-
Absolute Attenuation						
	DC … 745.00 MHz	α_{rel}	50	-	-	dB
	745.00 … 757.00 MHz		50	-	-	dB
	757.00 … 775.00 MHz		30	-	-	dB
Frequency Aging	Absolute Value during the First Year	$\|fA\|$	-	-	10	ppm/yr
DC Insulation Resistance Between any Two Pins		-	1.0	-	-	MΩ
Input / Output Impedance (nominal)		-	-	50	-	Ω

NS = Not Specified

Notes:

1. The frequency f_C is defined as the midpoint between the 3dB frequencies.
2. Unless noted otherwise, all measurements are made with the filter installed in the specified test fixture that is connected to a 50Ω test system with VSWR ≤ 1.2:1. The test fixture L and C are adjusted for minimum insertion loss at the filter center frequency, f_C. Note that insertion loss, bandwidth, and passband shape are dependent on the impedance matching component values and quality.
3. Unless noted otherwise, specifications apply over the entire specified operating temperature range.
4. The specifications of this device are based on the test circuit shown above and subject to change or obsolescence without notice.
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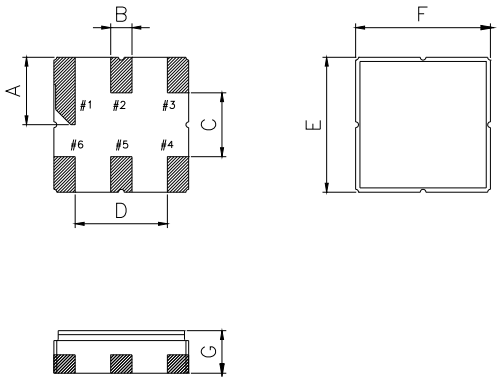
7. For questions on technology, prices and delivery please contact our sales offices or e-mail sales@vanlong.com.

PACKAGE DIMENSIONS (DCC6C)



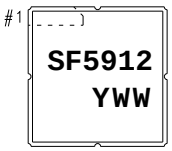
Electrical Connections

Terminals	Connection
2	Input
5	Output
1,3,4,6	Case Ground

Package Dimensions

Dimensions	Nom (mm)	Dimensions	Nom (mm)
A	1.5	E	3.0
B	0.6	F	3.0
C	1.5	G	1.1
D	1.8		

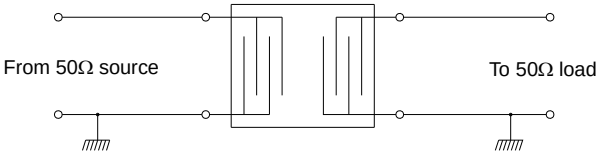
MARKING



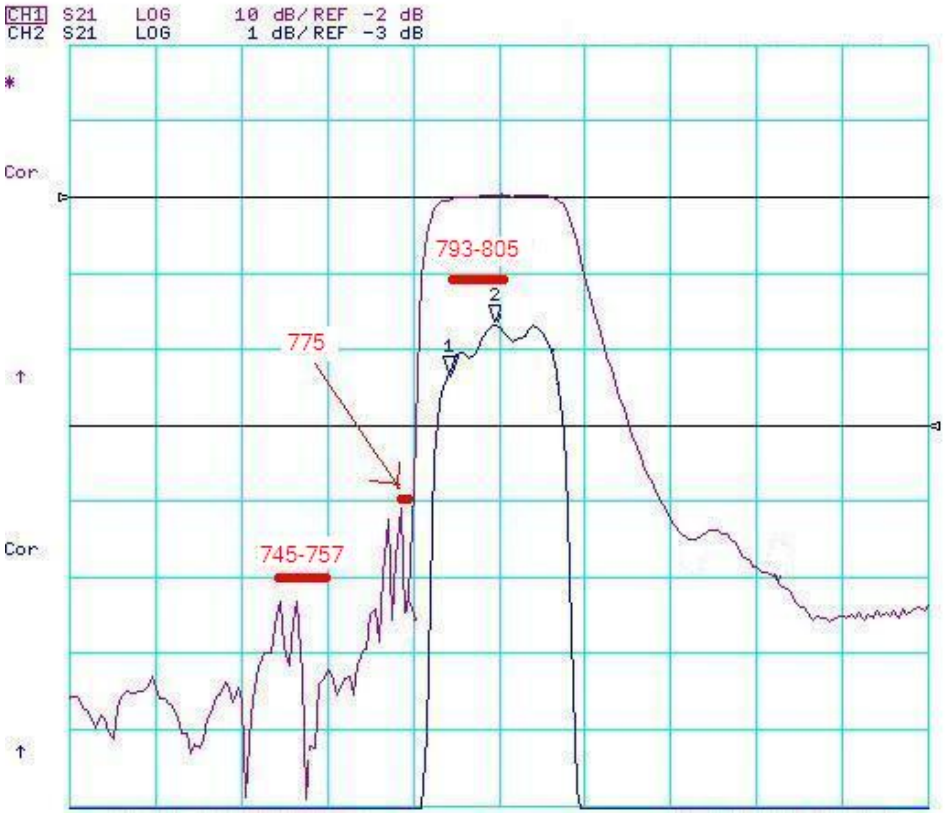
Laser or ink marking

1. SF5912 - Part Code
2. Date Code:
   Y : Last digit of year
   WW : Week No.

TEST CIRCUIT

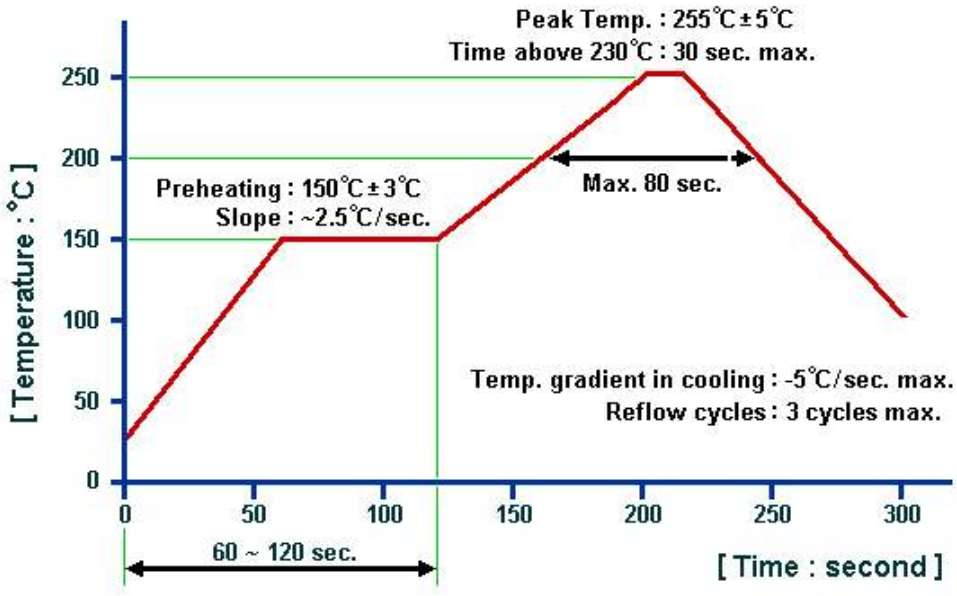


TYPICAL FREQUENCY RESPONSE



ENVIRONMENTAL CHARACTERISTICS		
Item	Condition of Test	Requirements
Random Drop	The Filter shall be measured after 3 times random drops from the height of 1.0M on concrete floor.	No visible damage and the measured values shall meet the Electronic Characteristics
Vibration	The Filter shall be measured after being applied vibration of amplitude of 1.5mm with 10 to 55Hz bands of vibration frequency to each of 3 perpendicular directions for 1 hour.	
Lead Pulling Test	Weight along with the direction of lead without any shock 1.0 Kg.	
Lead bending Test	Lead shall be subject to withstand against 90 bending at its stem. This operation shall be done toward both directions.	
Resistance to Soldering Heat	Lead terminals are immersed up to 1.5mm from the Filter's body in solder bath of 270°C ± 10°C for 10 ± 1 seconds, and then the Filter shall be measured after being placed in natural condition for 2 hour.	
Solderability	Lead terminals are immersed in resin for 5 seconds and then immersed in soldering bath of 270°C ± 10°C for 2 ± 0.5 seconds.	
High Temperature	After being placed in a chamber with +85°C ± 2°C for 96 ± 4 hours and then being placed in natural condition for 2 hour. The Filter shall be measured.	
Low Temperature	After being placed in a chamber with -40°C ± 2°C for 96 ± 4 hours and then being placed in natural condition for 2 hour. The Filter shall be measured.	
Humidity	After being placed in a chamber with 90 to 95% R.H. at +40°C ± 2°C for 96 ± 4 hours and then being placed in natural condition for 2 hour. The Filter shall be measured.	
Heat Shock	After being kept at room temperature, the Filter shall be placed at temperature of -40°C for 30 minutes, then the Filter shall be immediately placed at temperature of 85°C, after 30 minutes at temperature of 85°C, the Filter shall be returned to -40°C again. After 5 times above cycles, the Filter shall be returned to room temperature, after 2 hour in natural condition, the Filter shall be measured.	

REFLOW SOLDERING TEMPERATURE PROFILE



- ***Low-Loss RF Filter for Mobile Systems***
- ***Low Amplitude Ripple***
- ***No Matching Network Required for Operating at 50Ω***
- ***Ultra Miniature Ceramic DCC6C SMD Package***
- ***Complies with Directive 2002/95/EC (RoHS Compliant)***

SF5913

ABSOLUTE MAXIMUM RATING (T_A=25°C)			
Parameter		Rating	Unit
Input Power Level	P_{in}	+10	dBm
DC Voltage	V_{DC}	0	V
Operating Temperature Range	T_A	-30 ~ +85	°C
Storage Temperature Range	T_{stg}	-45 ~ +85	°C

ELECTRONIC CHARACTERISTICS						
Parameter		Sym	Minimum	Typical	Maximum	Unit
Nominal Frequency (at 25°C) (Center frequency between 3dB point)		f_C	NS	820.00	NS	MHz
Insertion Loss	806.00 … 824.00 MHz	IL	-	2.0	3.5	dB
3dB Bandwidth		BW_3	-	-	-	MHz
Amplitude Ripple (p-p)	806.00 … 824.00 MHz	$\Delta\alpha$	-	0.8	1.5	dB
Input VSWR	806.00 … 824.00 MHz	-	-	1.5	2.0	-
Output VSWR	806.00 … 824.00 MHz	-	-	1.5	2.0	-
Absolute Attenuation						
	DC … 764.00 MHz	α_{rel}	50	-	-	dB
	764.00 … 782.00 MHz		50	-	-	dB
	782.00 … 794.00 MHz		25	35	-	dB
Frequency Aging	Absolute Value during the First Year	$\|fA\|$	-	-	10	ppm/yr
DC Insulation Resistance Between any Two Pins		-	1.0	-	-	MΩ
Input / Output Impedance (nominal)		-	-	50	-	Ω

NS = Not Specified

Notes:

1. The frequency f_C is defined as the midpoint between the 3dB frequencies.
2. Unless noted otherwise, all measurements are made with the filter installed in the specified test fixture that is connected to a 50Ω test system with VSWR ≤ 1.2:1. The test fixture L and C are adjusted for minimum insertion loss at the filter center frequency, f_C. Note that insertion loss, bandwidth, and passband shape are dependent on the impedance matching component values and quality.
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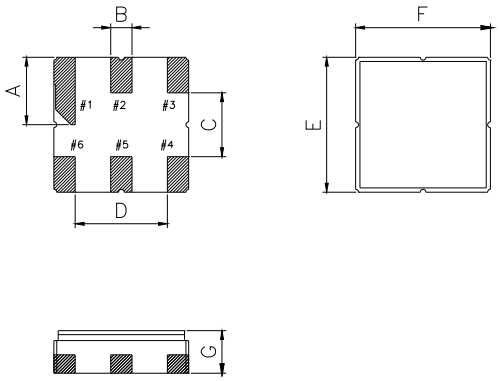
PACKAGE DIMENSIONS (DCC6C)



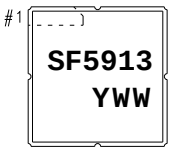
Electrical Connections

Terminals	Connection
2	Input
5	Output
1,3,4,6	Case Ground

Package Dimensions

Dimensions	Nom (mm)	Dimensions	Nom (mm)
A	1.5	E	3.0
B	0.6	F	3.0
C	1.5	G	1.1
D	1.8		

MARKING



Laser or ink marking

1. SF5913 - Part Code
2. Date Code:
   Y : Last digit of year
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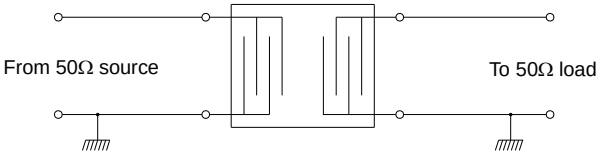
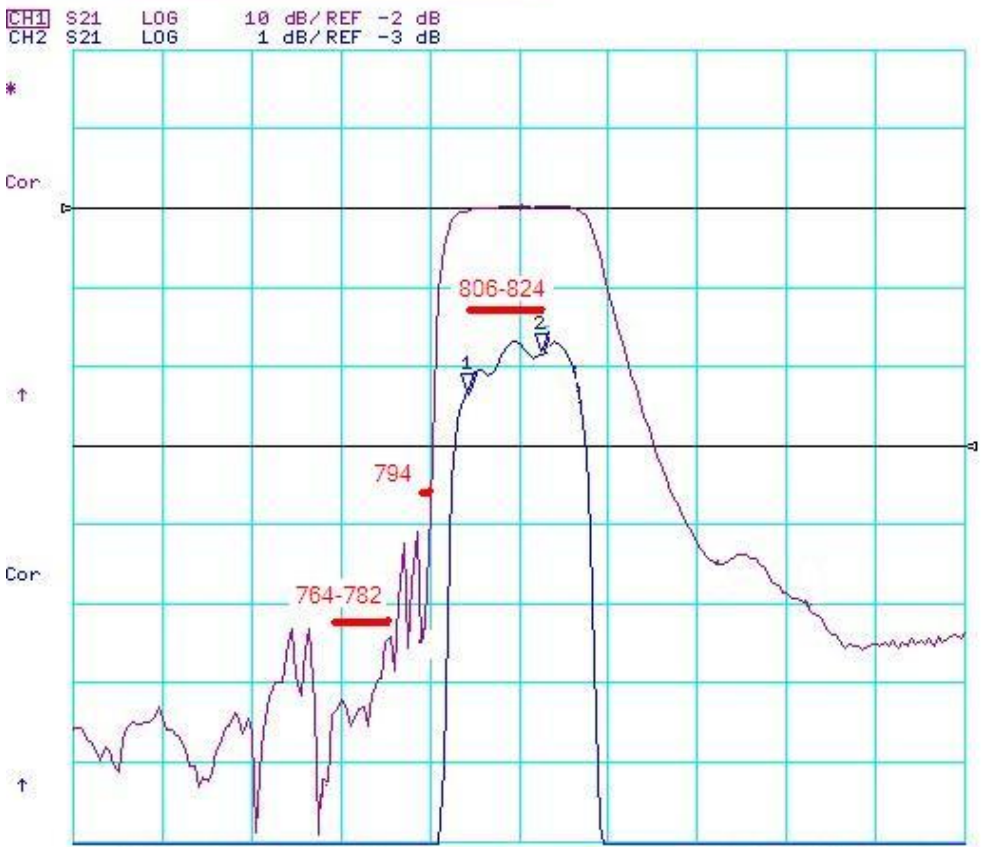
TEST CIRCUIT

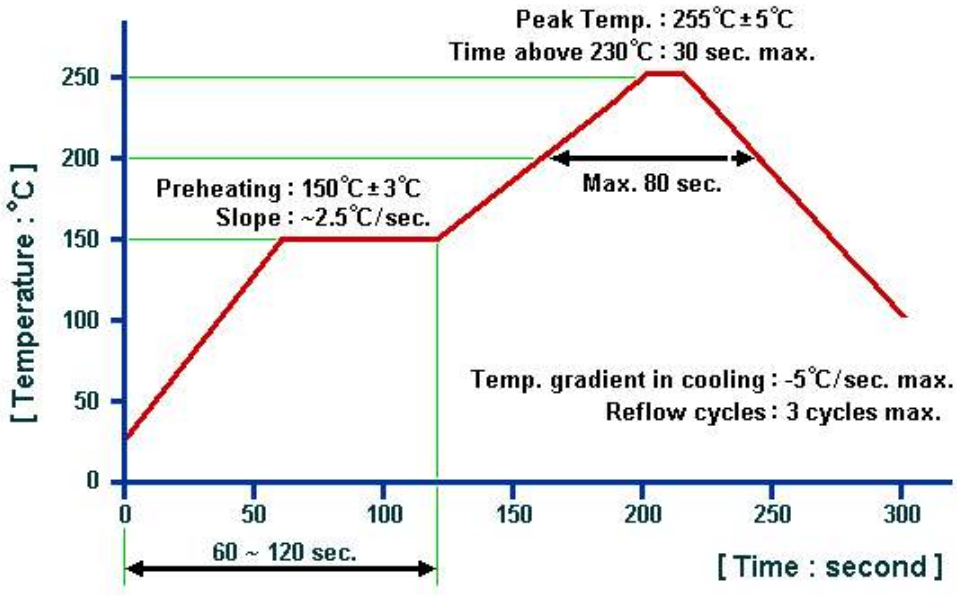


TYPICAL FREQUENCY RESPONSE



ENVIRONMENTAL CHARACTERISTICS		
Item	Condition of Test	Requirements
Random Drop	The Filter shall be measured after 3 times random drops from the height of 1.0M on concrete floor.	No visible damage and the measured values shall meet the Electronic Characteristics
Vibration	The Filter shall be measured after being applied vibration of amplitude of 1.5mm with 10 to 55Hz bands of vibration frequency to each of 3 perpendicular directions for 1 hour.	
Lead Pulling Test	Weight along with the direction of lead without any shock 1.0 Kg.	
Lead bending Test	Lead shall be subject to withstand against 90 bending at its stem. This operation shall be done toward both directions.	
Resistance to Soldering Heat	Lead terminals are immersed up to 1.5mm from the Filter's body in solder bath of 270°C ± 10°C for 10 ± 1 seconds, and then the Filter shall be measured after being placed in natural condition for 2 hour.	
Solderability	Lead terminals are immersed in resin for 5 seconds and then immersed in soldering bath of 270°C ± 10°C for 2 ± 0.5 seconds.	
High Temperature	After being placed in a chamber with +85°C ± 2°C for 96 ± 4 hours and then being placed in natural condition for 2 hour. The Filter shall be measured.	
Low Temperature	After being placed in a chamber with -40°C ± 2°C for 96 ± 4 hours and then being placed in natural condition for 2 hour. The Filter shall be measured.	
Humidity	After being placed in a chamber with 90 to 95% R.H. at +40°C ± 2°C for 96 ± 4 hours and then being placed in natural condition for 2 hour. The Filter shall be measured.	
Heat Shock	After being kept at room temperature, the Filter shall be placed at temperature of -40°C for 30 minutes, then the Filter shall be immediately placed at temperature of 85°C, after 30 minutes at temperature of 85°C, the Filter shall be returned to -40°C again. After 5 times above cycles, the Filter shall be returned to room temperature, after 2 hour in natural condition, the Filter shall be measured.	

REFLOW SOLDERING TEMPERATURE PROFILE



- ***Low-Loss RF Filter for Mobile Systems***
- ***Low Amplitude Ripple***
- ***No Matching Network Required for Operating at 50Ω***
- ***Ultra Miniature Ceramic DCC6C SMD Package***
- ***Complies with Directive 2002/95/EC (RoHS Compliant)***

SF5914

ABSOLUTE MAXIMUM RATING (T_A=25°C)			
Parameter		Rating	Unit
Input Power Level	P_{in}	+10	dBm
DC Voltage	V_{DC}	0	V
Operating Temperature Range	T_A	-30 ~ +85	°C
Storage Temperature Range	T_{stg}	-45 ~ +85	°C

ELECTRONIC CHARACTERISTICS						
Parameter		Sym	Minimum	Typical	Maximum	Unit
Nominal Frequency (at 25°C) (Center frequency between 3dB point)		f_C	NS	866.00	NS	MHz
Insertion Loss	851.00 … 869.00 MHz	IL	-	2.0	3.5	dB
3dB Bandwidth		BW_3	-	-	-	MHz
Amplitude Ripple (p-p)	851.00 … 869.00 MHz	$\Delta\alpha$	-	0.8	1.5	dB
Input VSWR	851.00 … 869.00 MHz	-	-	1.5	2.0	-
Output VSWR	851.00 … 869.00 MHz	-	-	1.5	2.0	-
Absolute Attenuation						
	DC … 809.00 MHz	α_{rel}	50	-	-	dB
	809.00 … 827.00 MHz		45	-	-	dB
	827.00 … 839.00 MHz		20	35	-	dB
Frequency Aging	Absolute Value during the First Year	$\|fA\|$	-	-	10	ppm/yr
DC Insulation Resistance Between any Two Pins		-	1.0	-	-	MΩ
Input / Output Impedance (nominal)		-	-	50	-	Ω

NS = Not Specified

Notes:

1. The frequency f_C is defined as the midpoint between the 3dB frequencies.
2. Unless noted otherwise, all measurements are made with the filter installed in the specified test fixture that is connected to a 50Ω test system with VSWR ≤ 1.2:1. The test fixture L and C are adjusted for minimum insertion loss at the filter center frequency, f_C. Note that insertion loss, bandwidth, and passband shape are dependent on the impedance matching component values and quality.
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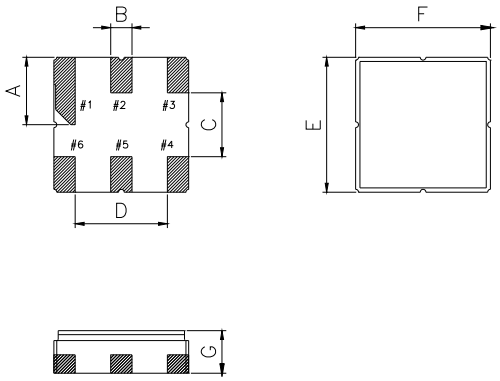
PACKAGE DIMENSIONS (DCC6C)



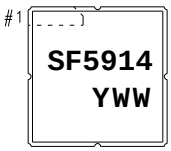
Electrical Connections

Terminals	Connection
2	Input
5	Output
1,3,4,6	Case Ground

Package Dimensions

Dimensions	Nom (mm)	Dimensions	Nom (mm)
A	1.5	E	3.0
B	0.6	F	3.0
C	1.5	G	1.1
D	1.8		

MARKING



Laser or ink marking

1. SF5914 - Part Code
2. Date Code:
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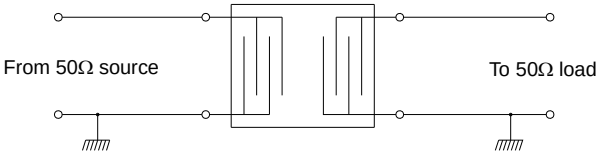
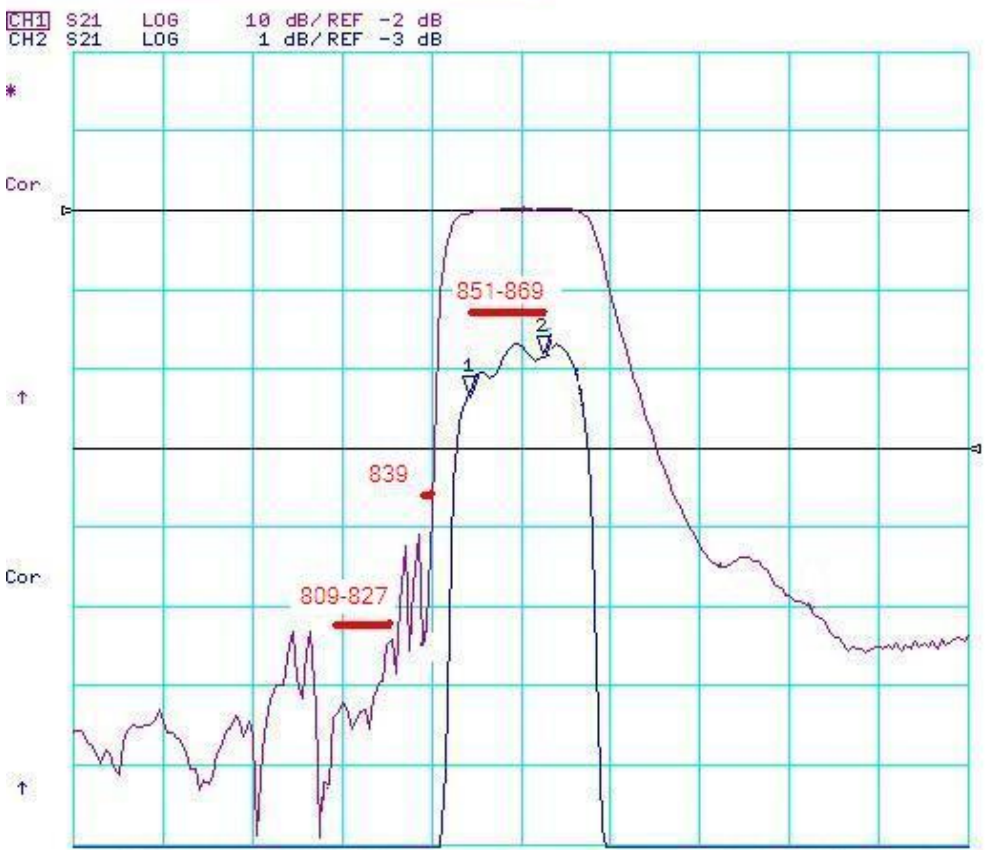
   WW : Week No.

TEST CIRCUIT



TYPICAL FREQUENCY RESPONSE



ENVIRONMENTAL CHARACTERISTICS		
Item	Condition of Test	Requirements
Random Drop	The Filter shall be measured after 3 times random drops from the height of 1.0M on concrete floor.	No visible damage and the measured values shall meet the Electronic Characteristics
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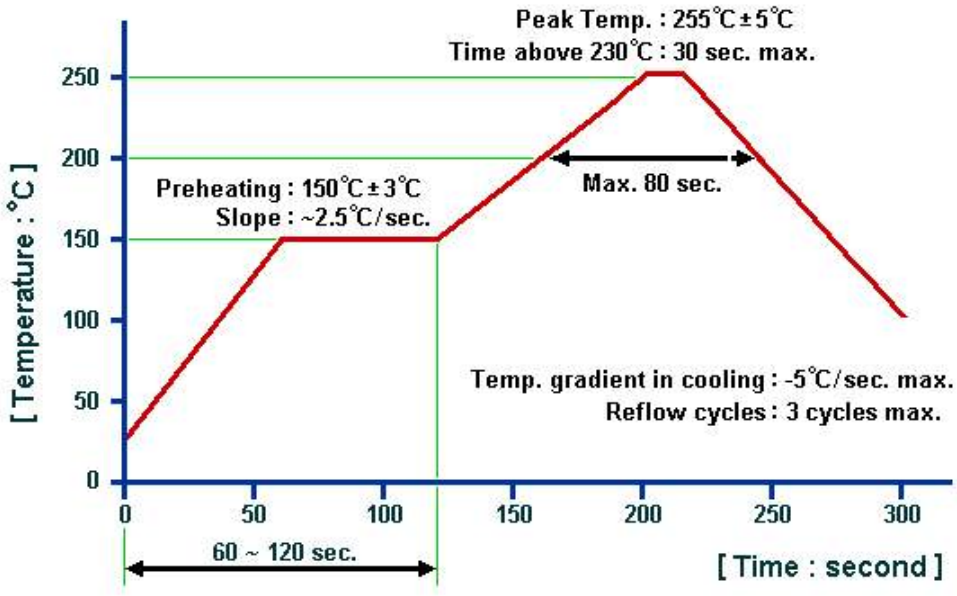
Lead Pulling Test	Weight along with the direction of lead without any shock 1.0 Kg.	
Lead bending Test	Lead shall be subject to withstand against 90 bending at its stem. This operation shall be done toward both directions.	
Resistance to Soldering Heat	Lead terminals are immersed up to 1.5mm from the Filter's body in solder bath of 270°C ± 10°C for 10 ± 1 seconds, and then the Filter shall be measured after being placed in natural condition for 2 hour.	
Solderability	Lead terminals are immersed in resin for 5 seconds and then immersed in soldering bath of 270°C ± 10°C for 2 ± 0.5 seconds.	
High Temperature	After being placed in a chamber with +85°C ± 2°C for 96 ± 4 hours and then being placed in natural condition for 2 hour. The Filter shall be measured.	
Low Temperature	After being placed in a chamber with -40°C ± 2°C for 96 ± 4 hours and then being placed in natural condition for 2 hour. The Filter shall be measured.	
Humidity	After being placed in a chamber with 90 to 95% R.H. at +40°C ± 2°C for 96 ± 4 hours and then being placed in natural condition for 2 hour. The Filter shall be measured.	
Heat Shock	After being kept at room temperature, the Filter shall be placed at temperature of -40°C for 30 minutes, then the Filter shall be immediately placed at temperature of 85°C, after 30 minutes at temperature of 85°C, the Filter shall be returned to -40°C again. After 5 times above cycles, the Filter shall be returned to room temperature, after 2 hour in natural condition, the Filter shall be measured.	

REFLOW SOLDERING TEMPERATURE PROFILE



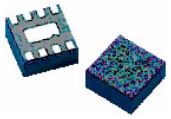
RFMD
rfmd.com

Preliminary

SPF-5122Z

50MHz to 4000MHz, GaAs pHEMT LOW NOISE MMIC AMPLIFIER

RoHS Compliant and Pb-Free Product

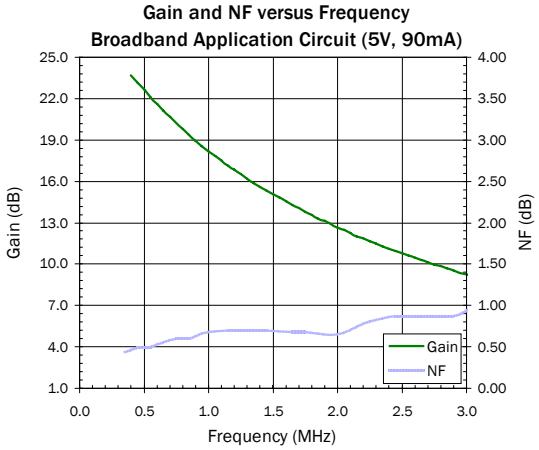


Product Description

The SPF-5122Z is a high performance pHEMT MMIC LNA designed for operation from 50MHz to 4000MHz. The on-chip active bias network provides stable current over temperature and process threshold voltage variations. The SPF-5122Z offers ultra-low noise figure and high linearity performance in a gain block configuration. Its single-supply operation and integrated matching networks make implementation remarkably simple. A high maximum input power specification make it ideal for high dynamic range receivers.

Optimum Technology Matching® Applied

- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ InGaP HBT
- ☐ SiGe BiCMOS
- ☐ Si BiCMOS
- ☐ SiGe HBT
- ☑ GaAs pHEMT
- ☐ Si CMOS
- ☐ Si BJT
- ☐ GaN HEMT
- ☐ RF MEMS



Features

- Ultra-Low Noise Figure=0.60dB @ 900MHz
- Gain=18.9dB @ 900MHz
- High Linearity: OIP3=40.5dBm @ 1900MHz
- Channel Power=13.4dBm (-65dBc IS95 ACPR, 880MHz)
- P_{1dB}=23.4dBm @ 1900MHz
- Single-Supply Operation: 5V @ Idq=90mA
- Flexible Biasing Options: 3-5V, Adjustable Current
- Broadband Internal Matching

Applications

- Cellular, PCS, W-CDMA, ISM, WiMAX Receivers
- PA Driver Amplifier
- Low Noise, High Linearity Gain Block Applications

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Small Signal Power Gain		18.9		dB	0.9GHz
		12.9		dB	1.96GHz
Output Power at 1dB Compression		23.0		dBm	0.9GHz
		23.4		dBm	1.9GHz
Output Third Order Intercept Point		37.9		dBm	0.9GHz
		40.5		dBm	1.9GHz
Noise Figure		0.59		dB	0.9GHz
		0.64		dB	1.9GHz
Input Return Loss		-14.6		dB	0.9 GHz
		-21.0		dB	1.9GHz
Output Return Loss		-16.8		dB	0.9GHz
		-13.0		dB	1.9GHz
Reverse Isolation		-24.1		dB	0.9GHz
		-18.4		dB	1.9GHz
Device Operating Voltage		5.00	5.25	V	
Device Operating Current		90		mA	Quiescent
Thermal Resistance		65		°C/W	Junction to lead

Test Conditions: V_D=5V, I_{DQ}=90mA, OIP_3 Tone Spacing=1MHz, P_{OUT} per tone=0dBm
Z_S=Z_L=50Ω, 25°C, Broadband Application Circuit

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or sales-support@rfmd.com.

Absolute Maximum Ratings

Parameter	Rating	Unit
Max Device Current (I_D)	120	mA
Max Device Voltage (V_D)	5.5	V
Max RF Input Power	27	dBm
Max Dissipated Power	660	mW
Max Junction Temperature (T_J)	150	°C
Operating Temperature Range (T_L)	-40 to + 85	°C
Max Storage Temperature	-65 to +150	°C
ESD Rating - Human Body Model (HBM)	Class 1B	
Moisture Sensitivity Level (MSL)	MSL 1	

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page one.

Bias Conditions should also satisfy the following expression:
$I_D V_D < (T_J - T_L)/R_{TH}$, j-l and $T_L = T_{LEAD}$

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Typical RF Performance - Broadband Application Circuit with V_D=5V, I_D=90mA

Parameter	Unit	0.1 GHz*	0.4 GHz	0.9 GHz	1.5 GHz	1.9 GHz	2.2 GHz	2.5 GHz	3.5 GHz	3.8 GHz
Small Signal Gain	dB	27.0	24.0	19.0	15.0	13.0	12.0	11.0	6.0	7.0
Noise Figure	dB	0.42	0.47	0.59	0.70	0.64	0.73	0.86	1.35	1.27
Output IP3	dBm	33.0	36.0	38.0	39.5	40.5	41.0	41.5	40.5	41.5
Output P1dB	dBm	22.3	22.7	23.0	23.2	23.4	23.7	23.9	22.2	22.9
Input Return Loss	dB	-9.5	-10.0	-14.5	-20.0	-21.0	-22.0	-22.5	-15.0	-11.5
Output Return Loss	dB	-29.0	-19.5	-17.0	-14.0	-13.0	-12.5	-12.5	-7.5	-15.5
Reverse Isolation	dB	-32.0	-29.0	-24.0	-20.0	-18.5	-17.5	-16.5	-15.5	-13.5

Test Conditions: V_D=5V, I_{DQ}=90mA, OIP_3 Tone Spacing=1MHz, P_{OUT} per tone=0dBm, T_L=25°C, Z_S=Z_L=50Ω, *Bias Tee Data @ 100MHz

1. Input RL can be improved in the 800MHz to 1000MHz band by adding a series inductor between the DC block and device input.

Typical RF Performance - Broadband Application Circuit with V_D=3V, I_D=58mA

Parameter	Unit	0.1 GHz*	0.4 GHz	0.9 GHz	1.5 GHz	1.9 GHz	2.2 GHz	2.5 GHz	3.5 GHz	3.8 GHz
Small Signal Gain	dB	26.0	23.0	18.5	14.5	12.5	11.5	10.5	6.0	6.5
Noise Figure	dB	0.35	0.44	0.58	0.65	0.61	0.69	0.79	1.25	1.19
Output IP3	dBm	31.5	33.0	34.5	36.0	36.5	37.0	37.5	37.0	37.5
Output P1dB	dBm	18.8	18.9	19.1	19.4	19.9	20.2	20.1	18.9	19.2
Input Return Loss	dB	-8.0	-9.0	-13.0	-16.5	-18.5	-19.0	-19.0	-13.5	-10.0
Output Return Loss	dB	-26.0	-28.5	-23.5	-18.0	-16.5	-16.0	-15.5	-9.0	-14.0
Reverse Isolation	dB	-31.0	-28.0	-23.0	-19.0	-17.5	-16.0	-15.0	-14.5	-12.5

Test Conditions: V_D=3V, I_{DQ}=58mA, OIP_3 Tone Spacing=1MHz, P_{OUT} per tone=0dBm, T_L=25°C, Z_S=Z_L=50Ω, *Bias Tee Data @ 100MHz

1. Input RL can be improved in the 800MHz to 1000MHz band by adding a series inductor between the DC block and device input.

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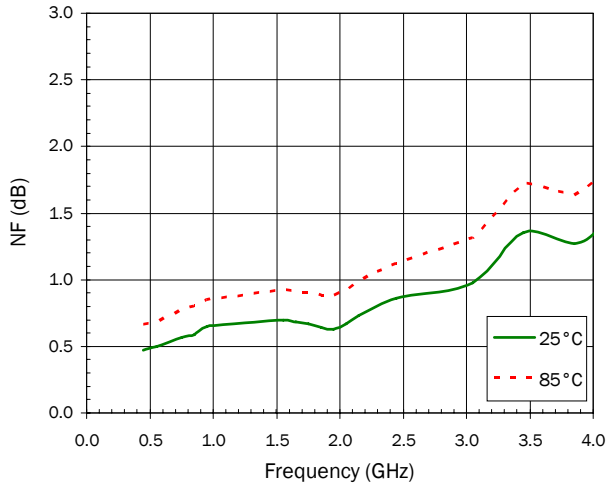
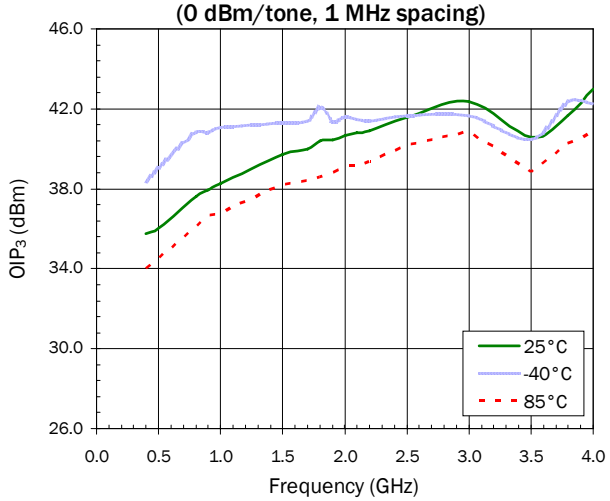
Typical RF Performance - Broadband Application Circuit with V_D=5V, I_D=90mA

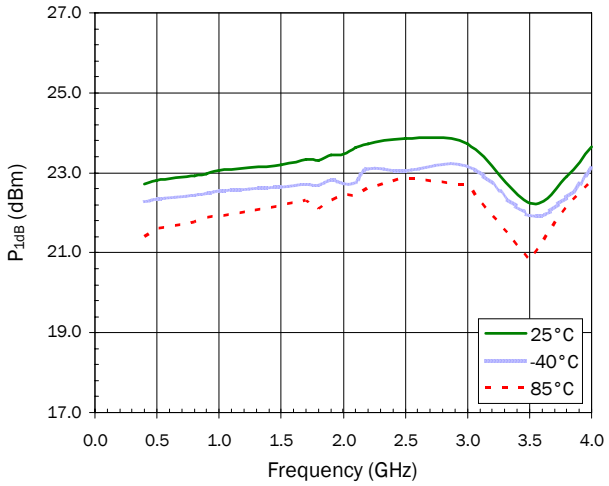
NF versus Frequency



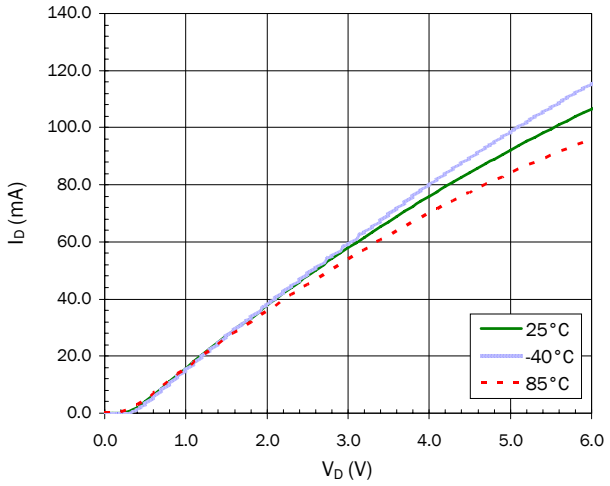
OIP_3 versus Frequency
(0 dBm/tone, 1 MHz spacing)



P_{1dB} versus Frequency

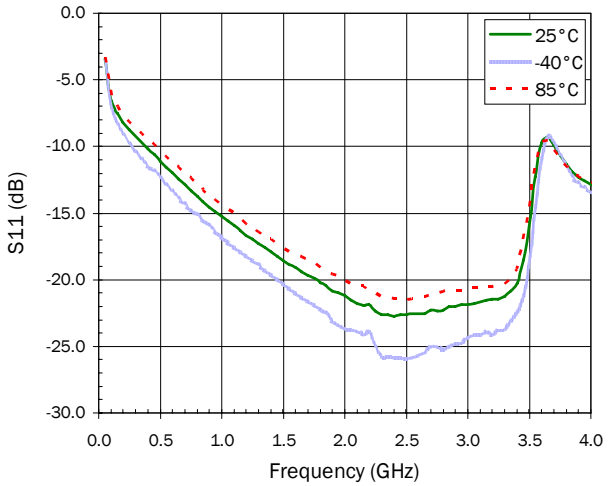


Device Current versus Voltage

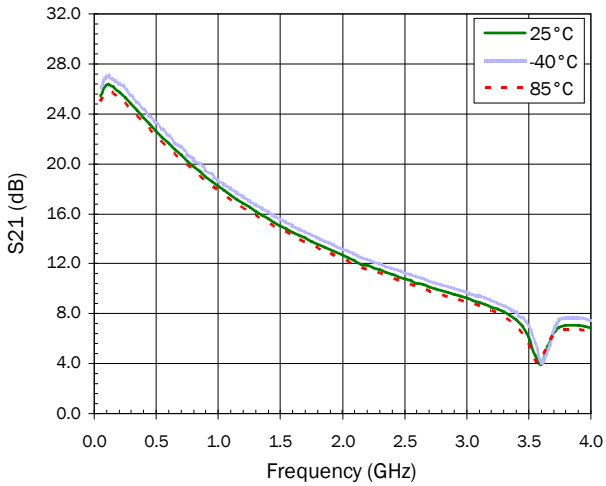


Typical RF Performance - Broadband Application Circuit with V_D=5V, I_D=90mA

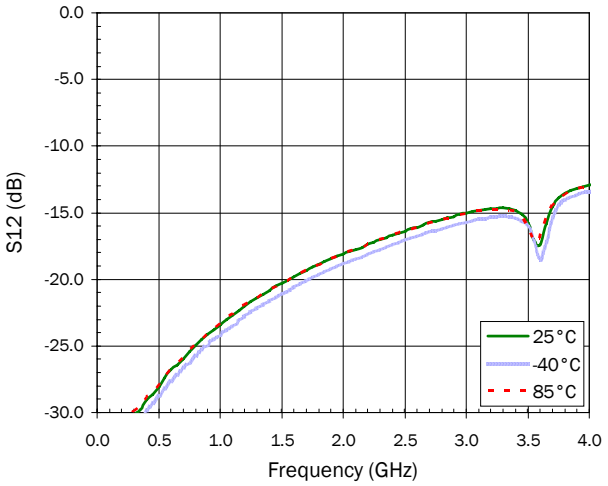
S11 versus Frequency



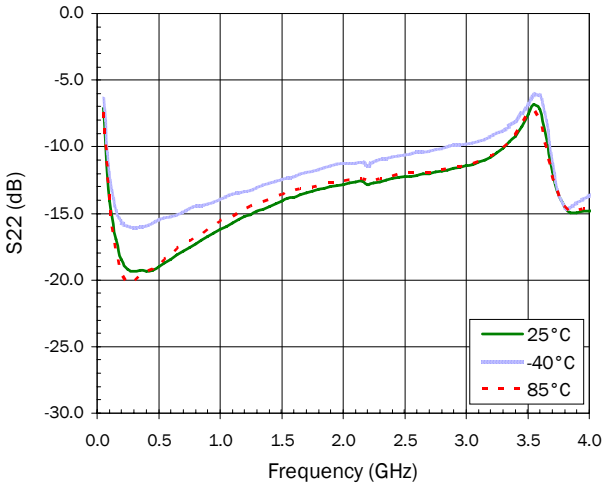
S21 versus Frequency



S12 versus Frequency



S22 versus Frequency



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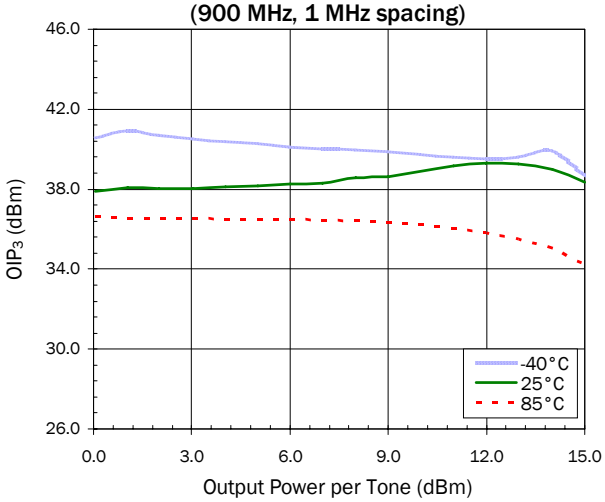
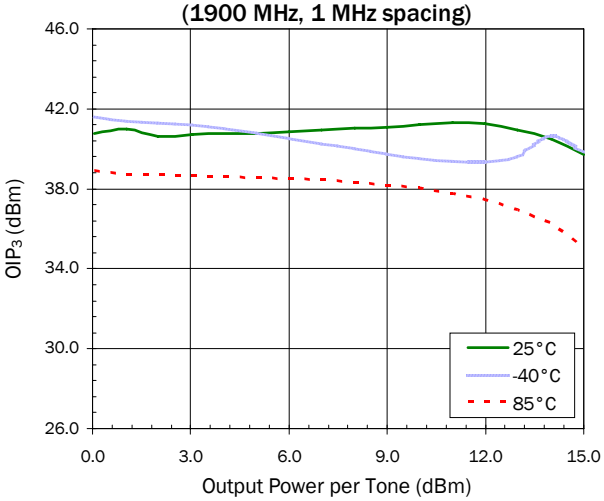
Typical RF Performance - Broadband Application Circuit with V_D=5V, I_D=90mA

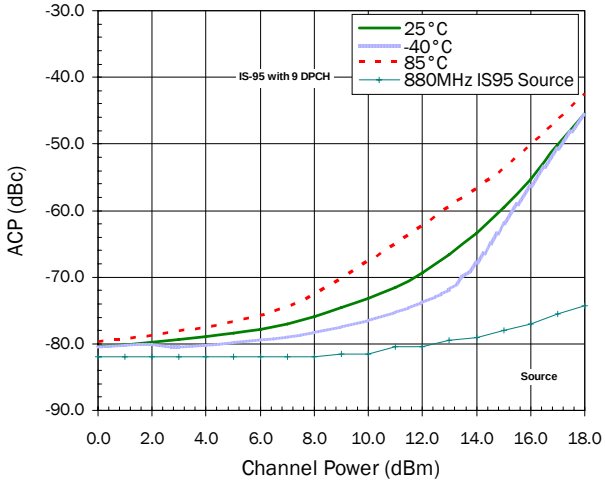
OIP_3 versus Power
(900 MHz, 1 MHz spacing)



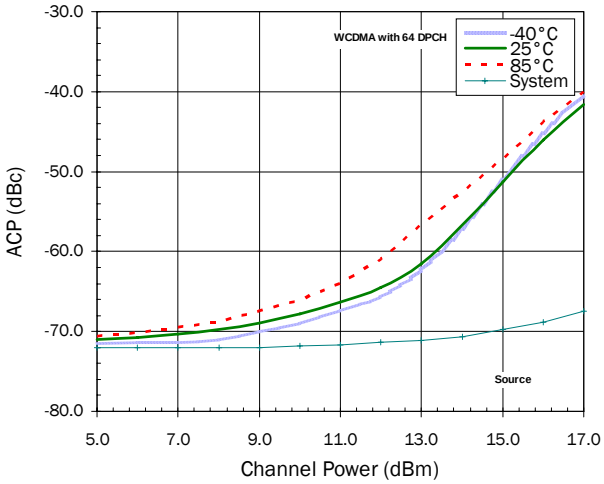
OIP_3 versus Power
(1900 MHz, 1 MHz spacing)



ACP versus Channel Power @ 880MHz

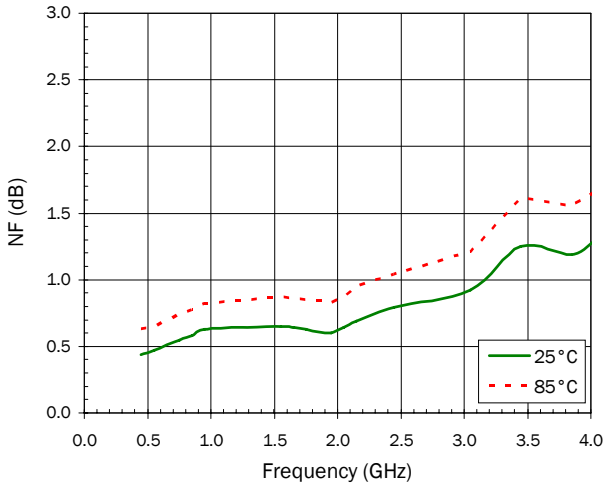


ACP versus Channel Power @ 2140MHz

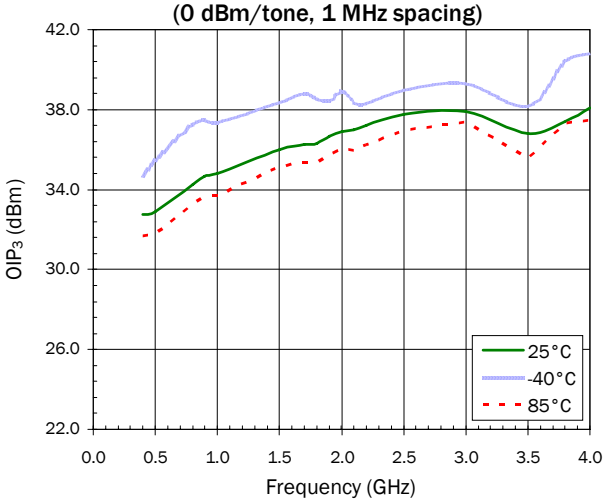


Typical RF Performance - Broadband Application Circuit with V_D=3V, I_D=58mA

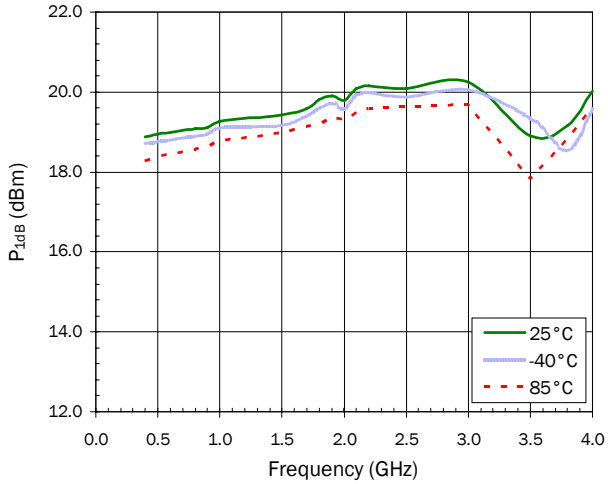
NF versus Frequency



OIP_3 versus Frequency
(0 dBm/tone, 1 MHz spacing)



P_{1dB} versus Frequency



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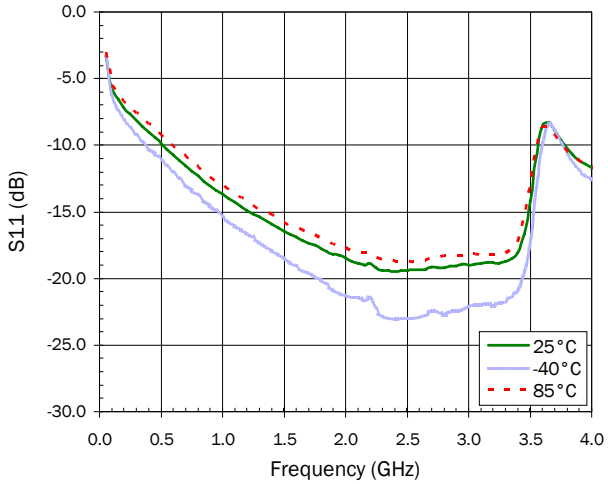
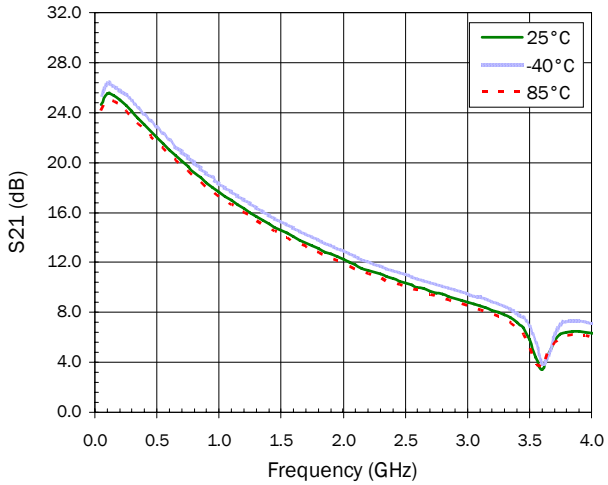
Typical RF Performance - Broadband Application Circuit with V_D=3V, I_D=58mA

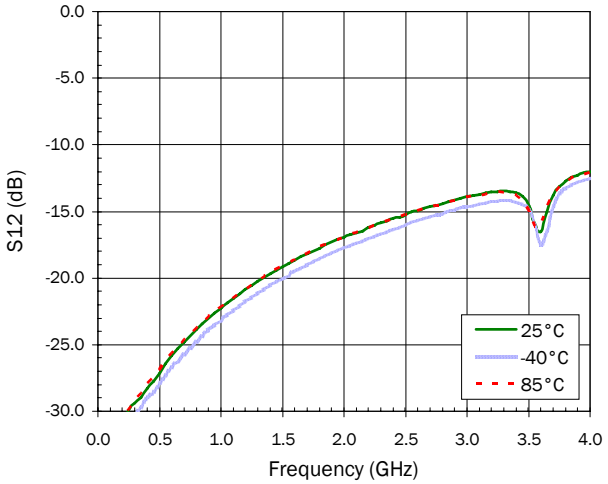
S11 versus Frequency



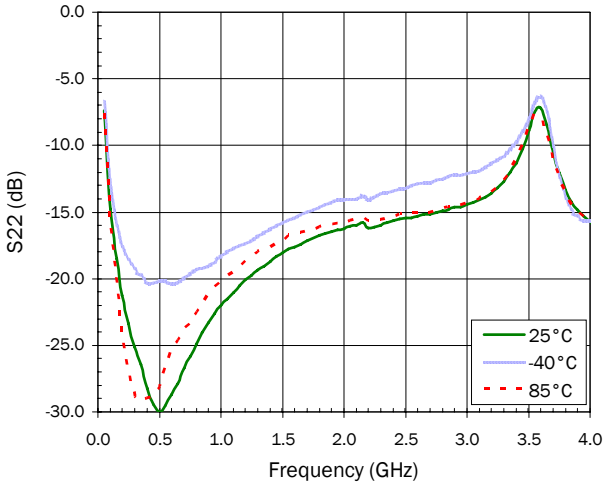
S21 versus Frequency



S12 versus Frequency



S22 versus Frequency



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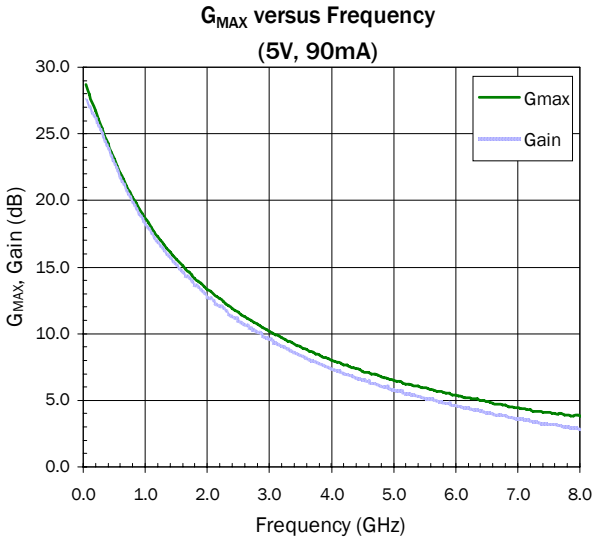
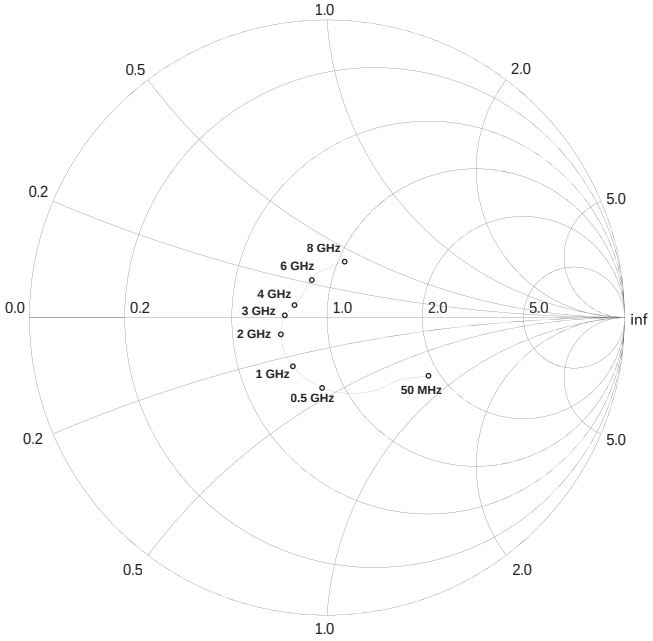
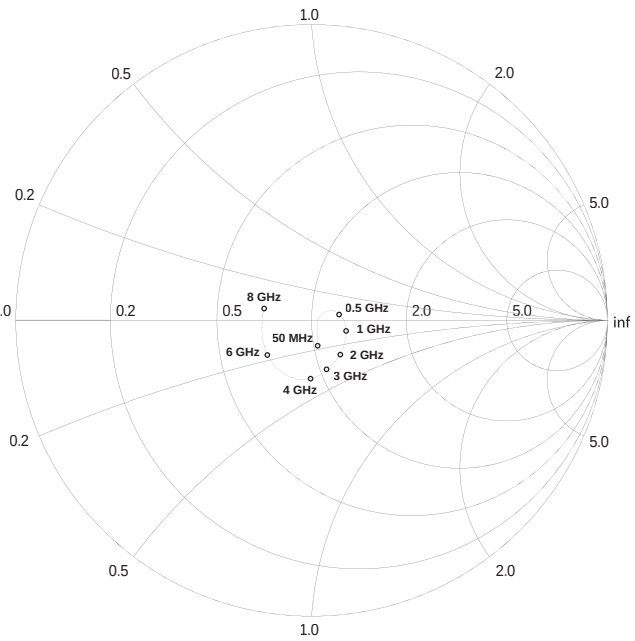
De-embedded Device S-parameters (Bias Tee Data)



S11 versus Frequency (5V 46mA)



S22 versus Frequency (5V 46mA)



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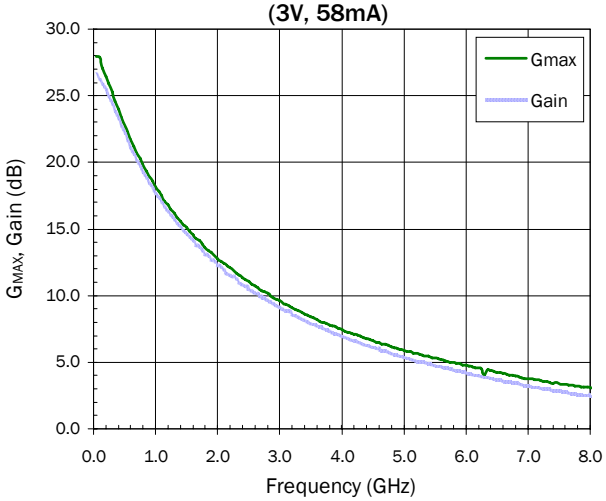
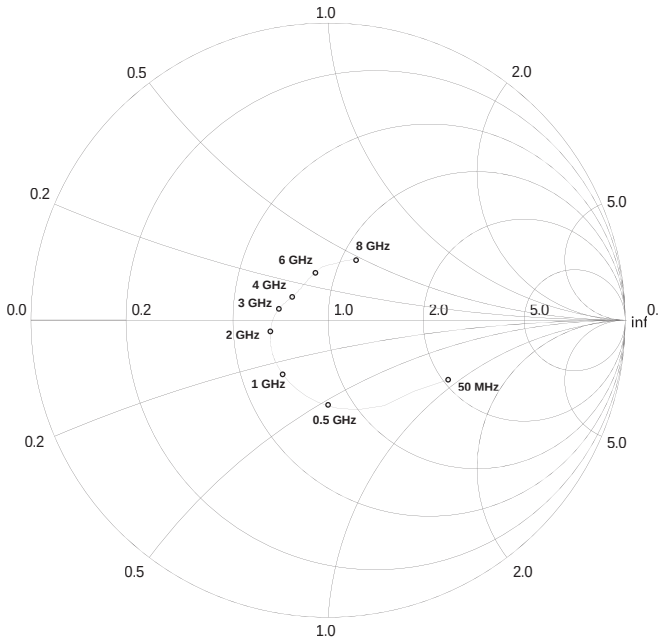
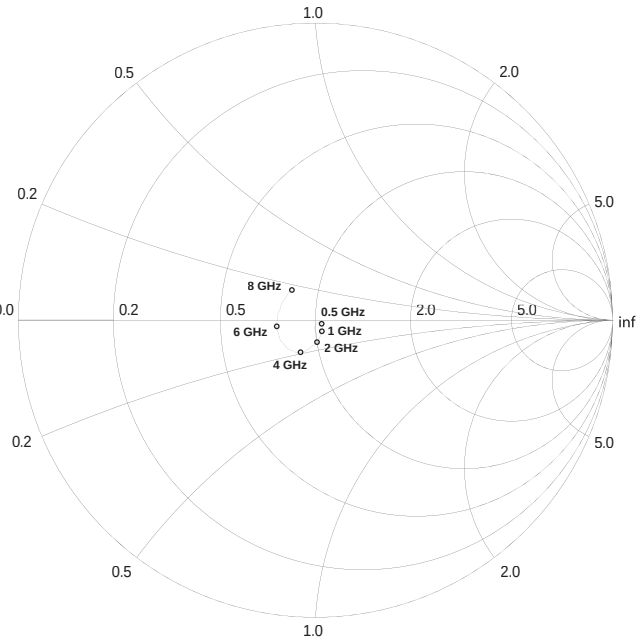
G_{MAX} versus Frequency (3V, 58mA)



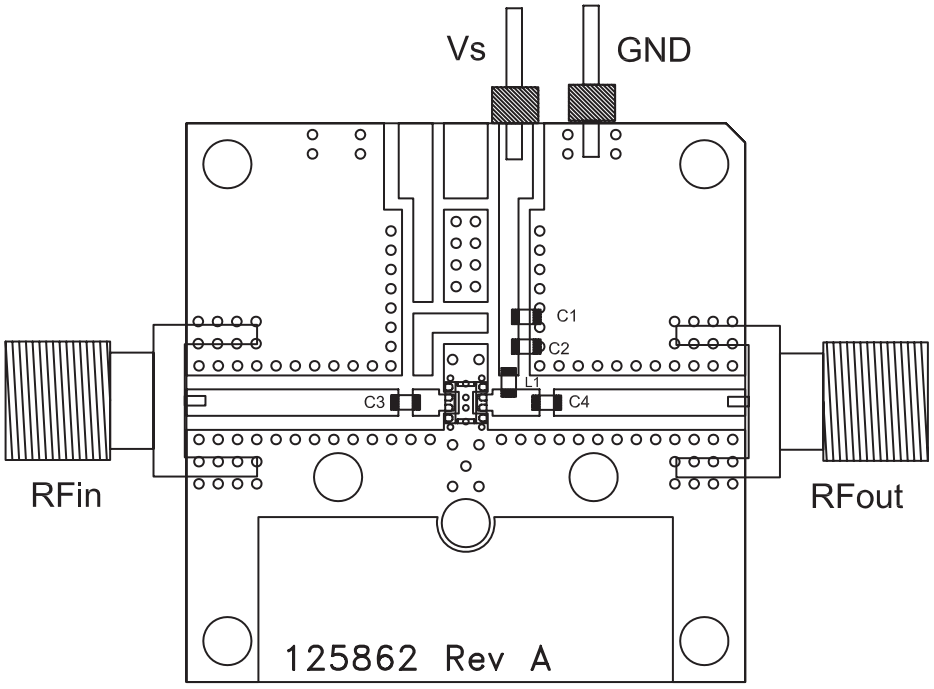
S11 versus Frequency (3V 25mA)



S22 versus Frequency (3V 25mA)



Evaluation Board Layout and Bill of Materials

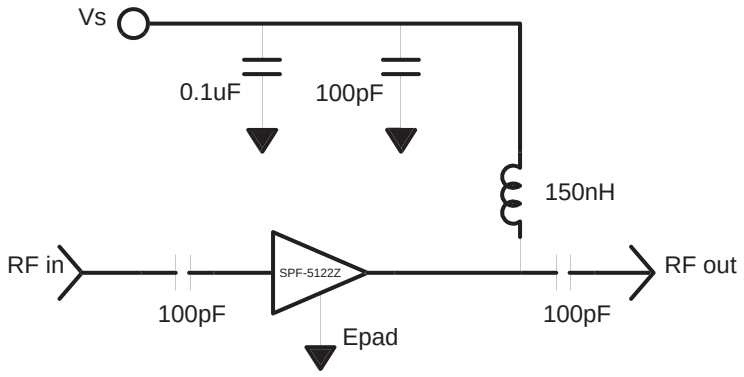


Bill of Materials (SPF-5122Z, 400MHz to 3000MHz

C1 TAJB104KLRH, Rohm, 0.1uF
C2 MCH185A101JK, Rohm, 100pF
C3 MCH185A101JK, Rohm, 100pF
C4 MCH185A101JK, Rohm, 100pF
L1 LL1608-FSR15J, Toko, 150nH
PCB 125862-A

Application Schematic

(400MHz to 3000MHz)



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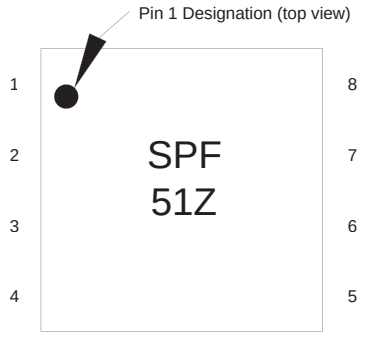
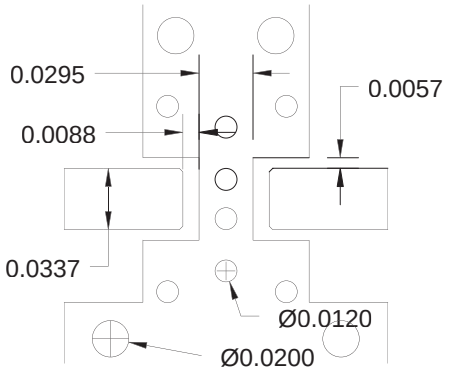
Pin	Function	Description
1,3,5, 6,8	N/A	Ground or No-Connect. No connection internal
2	RF IN	RF Input, DC coupled and matched to 50Ω. An external DC block is required.
4	N/A	Ground or No-Connect. Internally Grounded.
7	RF OUT/BIAS	RF Output, Bias applied through this pin. Matched to 50Ω.
EPAD	GND	EPAD must be conductively attached to RF and DC ground.

Part Identification

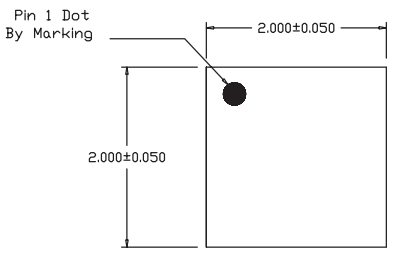


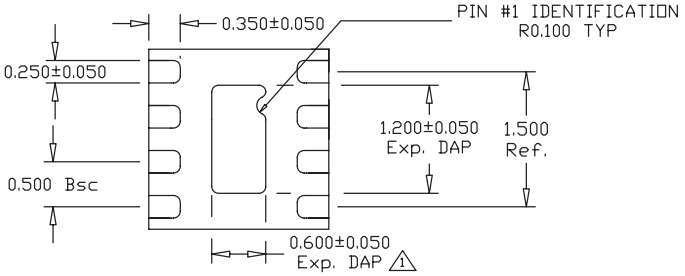
Suggested Pad Layout



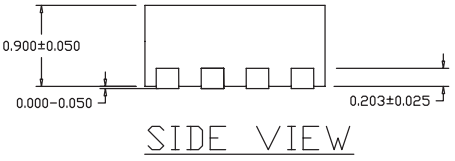
Package Drawing

Dimensions in inches (millimeters)
Refer to drawing posted at www.rfmd.com for tolerances.





Notes:
1. LF Base Metal – Olin 194
2. Exterior Platng
   Basic PN – Sn/Pb 85/15
   Z Option – 100% Matte Sn
3. Flammability Rating
   94V0
4. Marking
   Laser or White Phenolic
   Ink.



Ordering Information

Part Number	Description	Reel Size	Devices/Reel
SPF-5122Z	Lead Free, RoHS Compliant	7”	3000
SPF-5122Z-EVB1	400MHz to 3000MHz Evaluation Board	N/A	N/A

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TQP3M9009

High Linearity LNA Gain Block

Applications

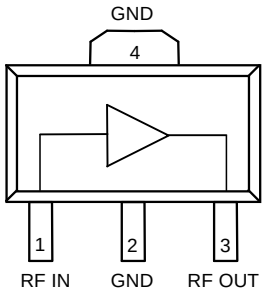
- Repeaters
- Mobile Infrastructure
- LTE / WCDMA / EDGE / CDMA
- General Purpose Wireless

3-pin SOT-89 Package

Product Features

- 50-4000 MHz
- 21.8 dB Gain @ 1.9 GHz
- +39.5 dBm Output IP3
- 1.3 dB Noise Figure @ 1.9 GHz
- 50 Ohm Cascadable Gain Block
- Unconditionally stable
- High input power capability
- +5V Single Supply, 125 mA Current
- SOT-89 Package

Functional Block Diagram



General Description

The TQP3M9009 is a cascadable, high linearity gain block amplifier in a low-cost surface-mount package. At 1.9 GHz, the amplifier is targeted to provide 21.8 dB gain, +39.5 dBm OIP3, and 1.3 dB Noise Figure while only drawing 125 mA current. The device is housed in a leadfree/green/RoHS-compliant industry-standard SOT-89 package using a NiPdAu plating to eliminate the possibility of tin whiskering.

The TQP3M9009 has the benefit of having high gain across a broad range of frequencies while also providing very low noise. This allows the device to be used in both receiver and transmitter chains for high performance systems. The amplifier is internally matched using a high performance E-pHEMT process and only requires an external RF choke and blocking/bypass capacitors for operation from a single +5V supply. The internal active bias circuit also enables stable operation over bias and temperature variations.

The TQP3M9009 covers the 0.05-4 GHz frequency band and is targeted for wireless infrastructure or other applications requiring high linearity and/or low noise figure.

Pin Configuration

Pin #	Symbol
1	RF Input
3	RF Output / Vcc
2, 4	Ground

Ordering Information

Part No.	Description
TQP3M9009	High Linearity LNA Gain Block
TQP3M9009-PCB_IF	TQP3M9009 EVB 0.05-0.5 GHz
TQP3M9009-PCB_RF	TQP3M9009 EVB 0.5-4 GHz

Standard T/R size = 1000 pieces on a 7” reel.

Specifications

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to +150 °C
RF Input Power,CW,50 Ω, T=25ºC	+23 dBm
Device Voltage,V_{dd}	+7 V
Reverse Device Voltage	-0.3 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{dd}	+4.75	+5	+5.25	V
T(case)	-40		85	°C
Tj (for>10^6 hours MTTF)			190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: +25ºC, +5V Vsupply, 50 Ω system.

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		50		4000	MHz
Test Frequency			1900		MHz
Gain		20	21.8	23	dB
Input Return Loss			13		dB
Output Return Loss			14		dB
Output P1dB			+22		dBm
Output IP3	See Note 1.	+36.5	+39.5		dBm
Noise Figure			1.3		dB
Vdd			+5		V
Current, Idd			125	150	mA
Thermal Resistance (jnc to case) θ_{jc}				34	°C/W

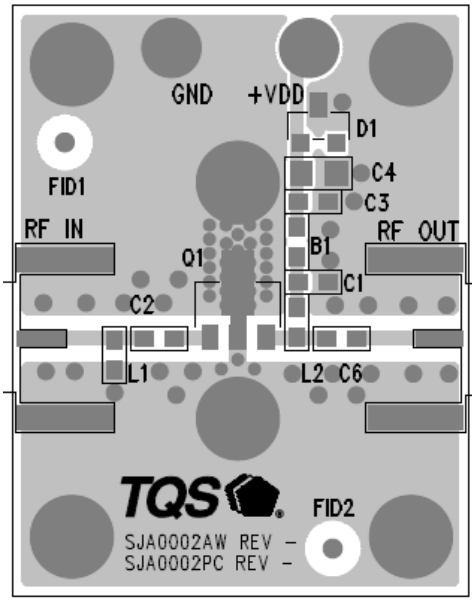
Notes
1. OIP3 measured with two tones at an output power of +3 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule.

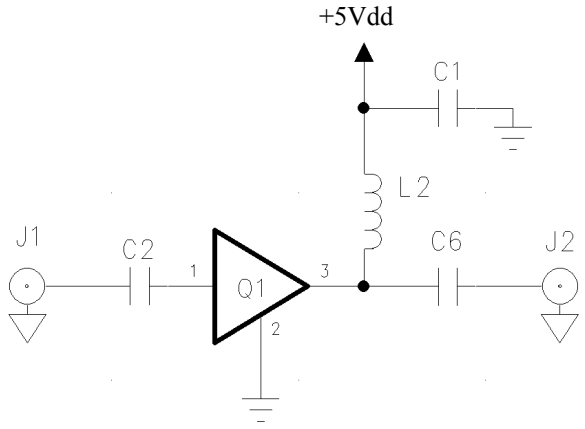
Device Characterization

V_{dd} = +5 V, I_{dd} = 125 mA, T = +25 °C, calibrated to device leads

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-16.66	-149.04	27.36	171.55	-29.65	1.22	-13.56	179.33
100	-14.86	-157.51	27.12	166.00	-29.37	-1.50	-13.09	174.97
200	-13.56	-165.34	26.70	156.36	-29.26	-5.67	-12.78	159.12
400	-12.51	-173.30	26.14	137.87	-29.42	-14.20	-13.06	133.47
600	-11.37	178.88	25.53	119.50	-29.63	-21.58	-13.69	110.30
800	-10.40	169.81	24.85	102.41	-30.03	-28.26	-14.46	86.04
1000	-9.76	160.89	24.16	86.01	-30.28	-35.35	-15.64	62.04
1200	-9.31	150.48	23.40	70.36	-30.96	-40.26	-16.58	37.31
1400	-8.84	139.39	22.82	55.48	-31.05	-46.78	-17.14	11.49
1600	-8.51	128.52	22.31	41.20	-31.76	-51.29	-17.34	-12.33
1800	-8.33	116.42	21.66	27.52	-32.00	-58.53	-17.04	-33.75
2000	-8.16	104.69	21.23	13.67	-32.50	-63.59	-16.80	-57.05
2200	-8.01	92.36	20.82	0.68	-33.07	-66.83	-16.28	-76.12
2400	-8.06	79.88	20.33	-13.12	-33.72	-72.40	-15.48	-95.17
2600	-8.13	66.42	20.02	-26.88	-34.02	-77.18	-14.43	-113.34
2800	-8.14	51.54	19.74	-41.54	-34.42	-81.16	-13.66	-128.34
3000	-8.00	35.02	19.52	-55.82	-35.18	-86.54	-12.61	-142.44
3200	-8.13	17.50	19.28	-71.00	-36.25	-88.92	-11.99	-157.55
3400	-7.86	-3.63	19.10	-87.06	-36.83	-94.66	-11.31	-167.91
3600	-7.65	-26.69	18.91	-103.86	-37.20	-96.43	-10.62	-179.13
3800	-7.20	-52.39	18.59	-121.75	-38.27	-102.65	-10.05	170.24
4000	-6.39	-79.22	18.17	-140.35	-39.25	-102.05	-9.83	159.78

Application Circuit Configuration





Notes:
1. See PC Board Layout, page 8 for more information.
2. Components shown on the silkscreen but not on the schematic are not used.
3. B1 (0 Ω jumper) may be replaced with copper trace in the target application layout.
4. The recommended component values are dependent upon the frequency of operation.
5. All components are of 0603 size unless stated on the schematic.

Bill of Material

Reference Designation	Frequency (MHz)	
	TQP3M9009-PCB_IF	TQP3M9009-PCB_RF
	50 - 500	500 - 4000
Q1	TQP3M9009	
C2, C6	1000 pF	100 pF
C1	0.01 uF	0.01 uF
L2	330 nH	68 nH
L1, D1, C3, C4	Do Not Place	
B1	0 Ω	

Notes:
1. Performances can be optimized at frequency of interest by using recommended component values shown in the table below.

Reference Designation	Frequency (MHz)			
	500	2000	2500	3500
C2, C6	100 pF	22 pF	22 pF	22 pF
L2	82 nH	22 nH	18 nH	15 nH

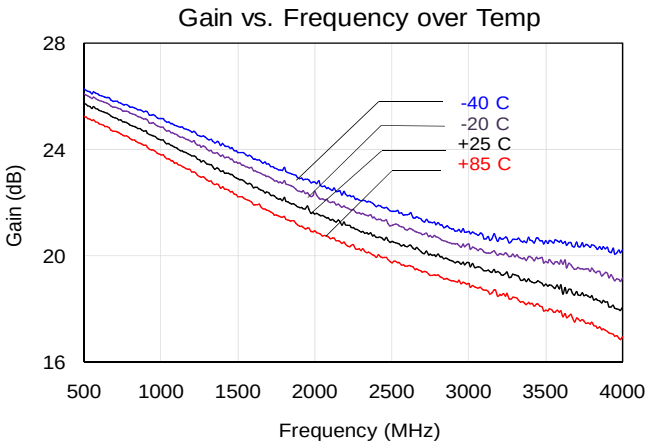
Typical Performance 500-4000 MHz

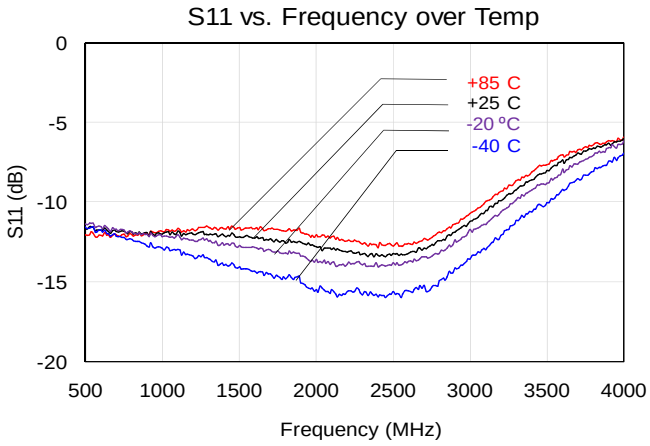
Test conditions unless otherwise noted: +25ºC, +5V, 125 mA, 50 Ω system. The data shown below is measured on TQP3M9009-PCB_RF.

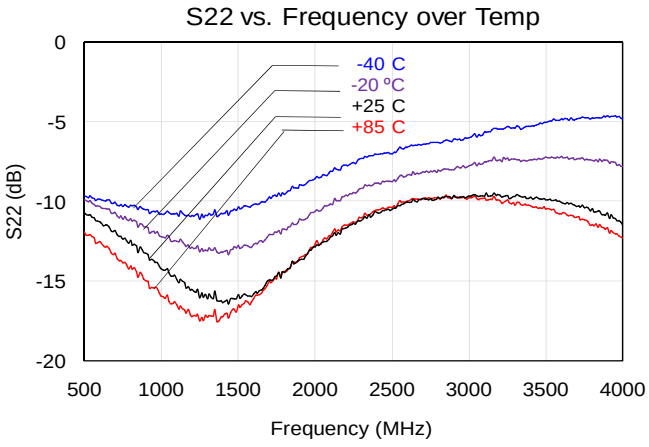
Frequency	MHz	500	900	1900	2700	3500	4000
Gain	dB	25.7	24.7	21.8	20	18.9	18
Input Return Loss	dB	12	12	13	13	8	6
Output Return Loss	dB	11	13	14	10	10	11.5
Output P1dB	dBm	+22.5	+21.8	+22	+21.6	+21.8	+20.7
OIP3 [1]	dBm	+41.4	+40.5	+39.5	+39	+37.9	+35.8
Noise Figure [2]	dB	0.9	0.9	1.3	1.7	2.1	2.4

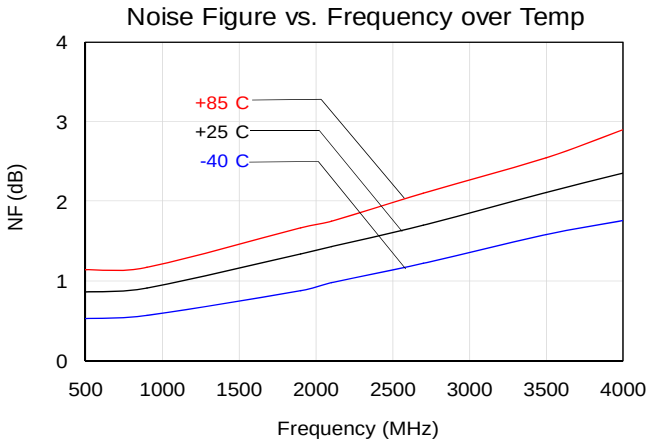
Notes:
1. OIP3 measured with two tones at an output power of +3 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule.
2. Noise figure data shown in the table above is measured on evaluation board which includes board losses of around 0.1 dB @ 2 GHz.

RF Performance Plots



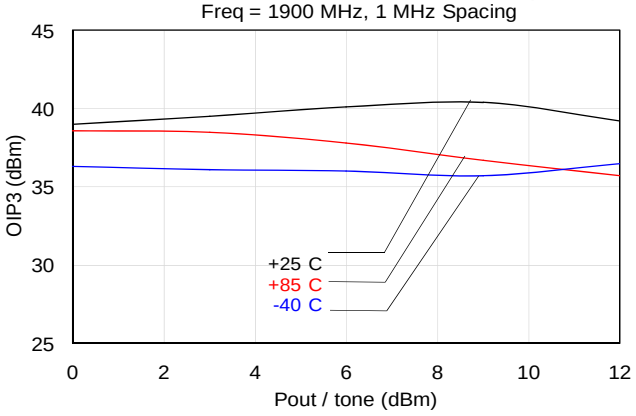




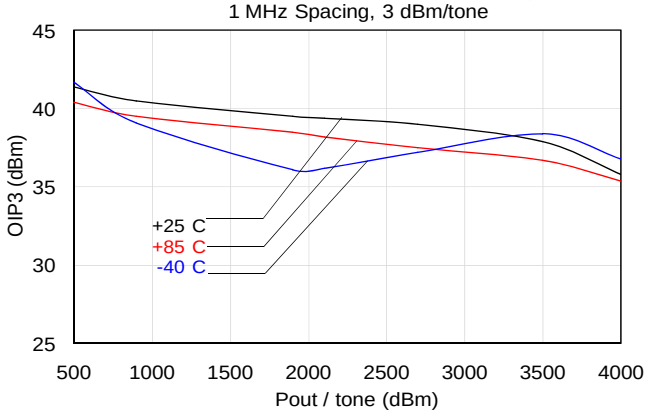


RF Performance Plots

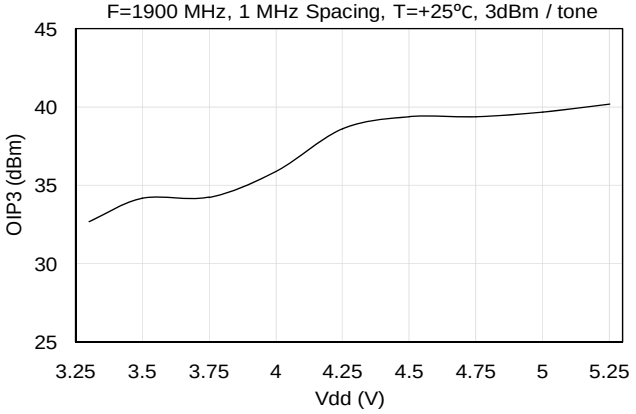
OIP3 vs. Pout / tone over Temp
Freq = 1900 MHz, 1 MHz Spacing



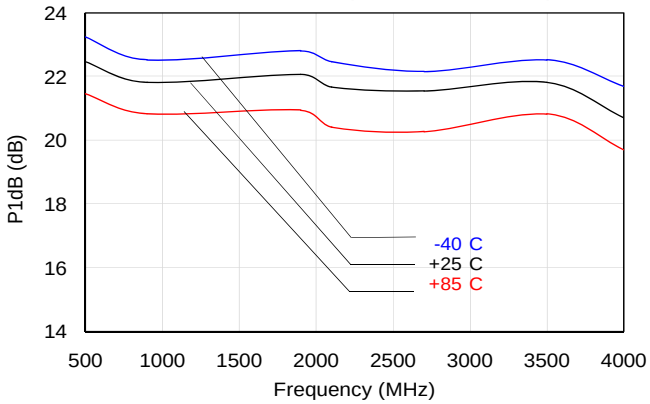
OIP3 vs. Frequency over Temp
1 MHz Spacing, 3 dBm/tone



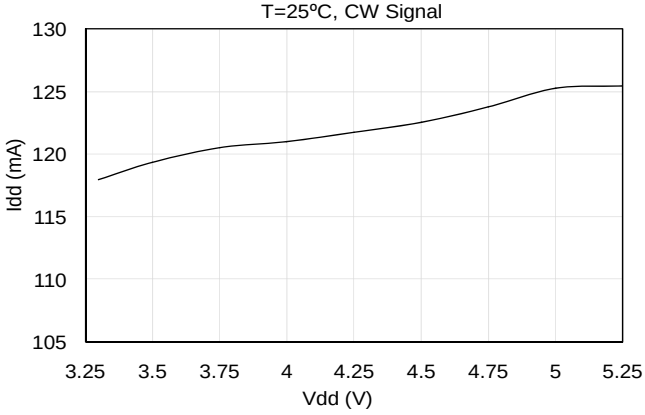
OIP3 vs. Vdd
F=1900 MHz, 1 MHz Spacing, T=+25ºC, 3dBm / tone



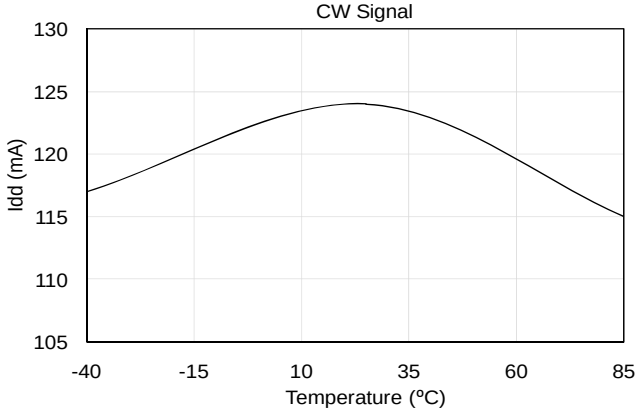
P1dB vs. Frequency over Temp



Idd vs. Vdd
T=25ºC, CW Signal



Idd vs. Temperature
CW Signal



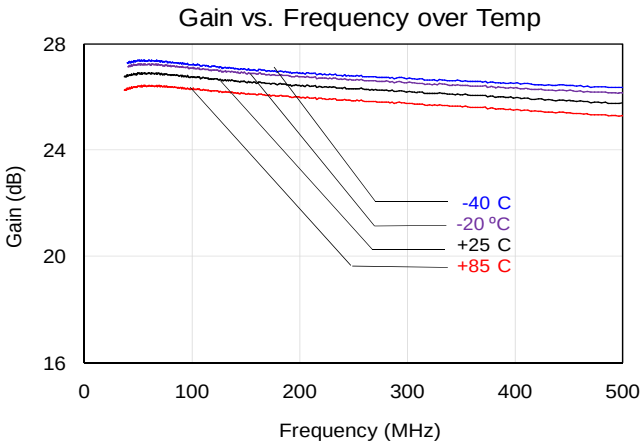
Typical Performance 50-500 MHz

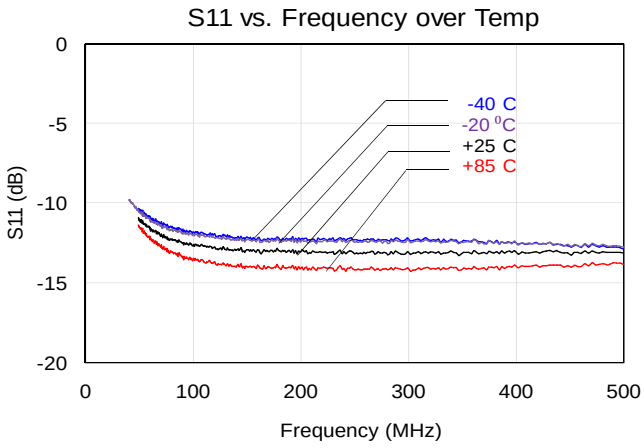
Test conditions unless otherwise noted: +25ºC, +5V, 125 mA, 50 Ω system. The data shown below is measured on TQP3M9009-PCB_IF.

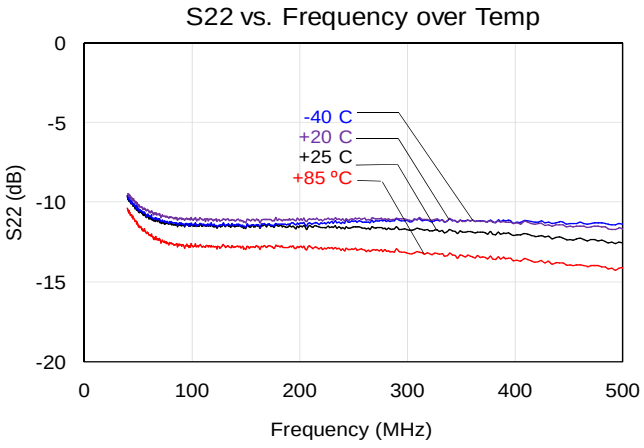
Frequency	MHz	70	100	200	500
Gain	dB	27	26.8	26.4	25.8
Input Return Loss	dB	12	13	13	13
Output Return Loss	dB	11	11	12	13
Output P1dB	dBm	+21.6	+21.9	+21.9	+22.2
OIP3 [1]	dBm	+37.6	+38.8	+39	+41.4
Noise Figure [2]	dB	1.4	1.3	0.9	0.9

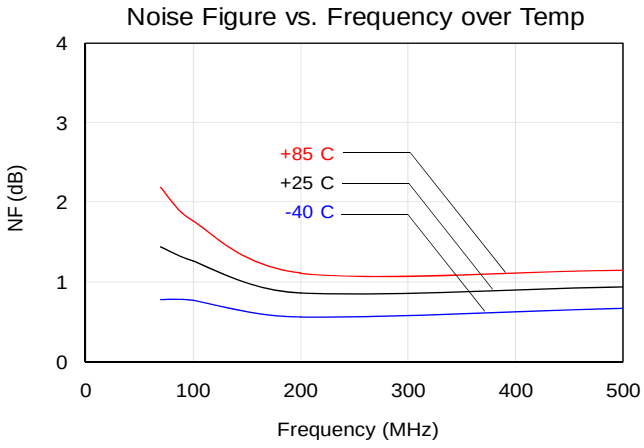
Notes:
1. OIP3 measured with two tones at an output power of +3 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule.
2. Noise figure data shown in the table above is measured on evaluation board which includes board losses of around 0.1 dB @ 2 GHz.

IF Performance Plots

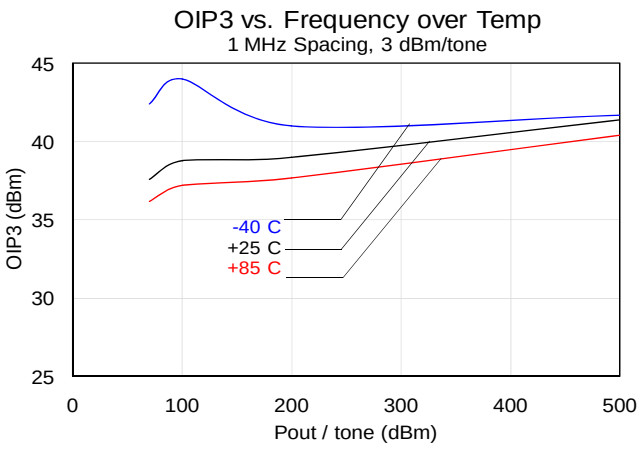


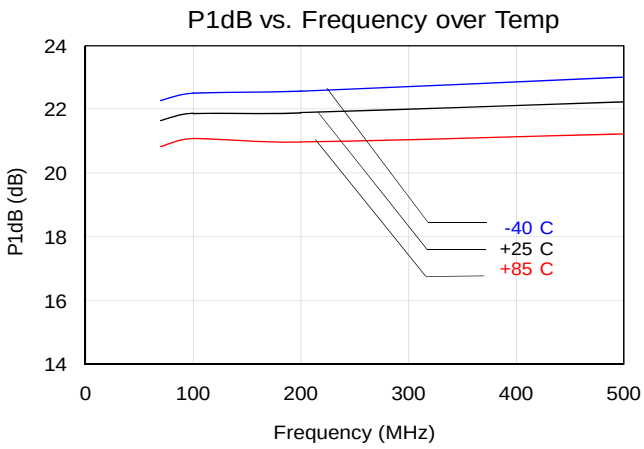




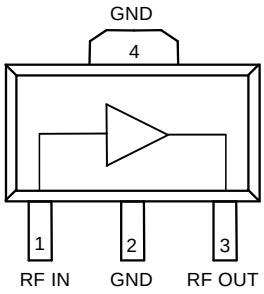


IF Performance Plots





Pin Configuration and Description



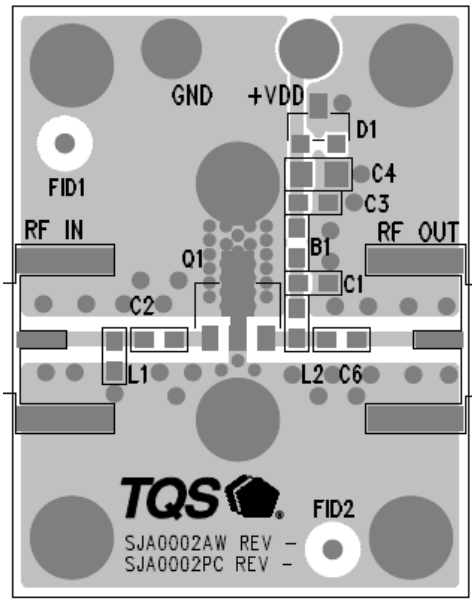
Pin	Symbol	Description
1	RF IN	Input, matched to 50 ohms, External DC block is required.
2, 4	GND	RF/DC Ground Connection.
3	RFout / Vdd	Output, matched to 50 ohms, External DC Block is required and supply voltage

Applications Information

PC Board Layout

Top RF layer is .014" NELCO N4000-13, ϵ_r = 3.9, 4 total layers (0.062" thick) for mechanical rigidity. Metal layers are 1-oz copper. 50 ohm Microstrip line details: width = .029", spacing = .035".

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from supplier to supplier, careful process development is recommended.

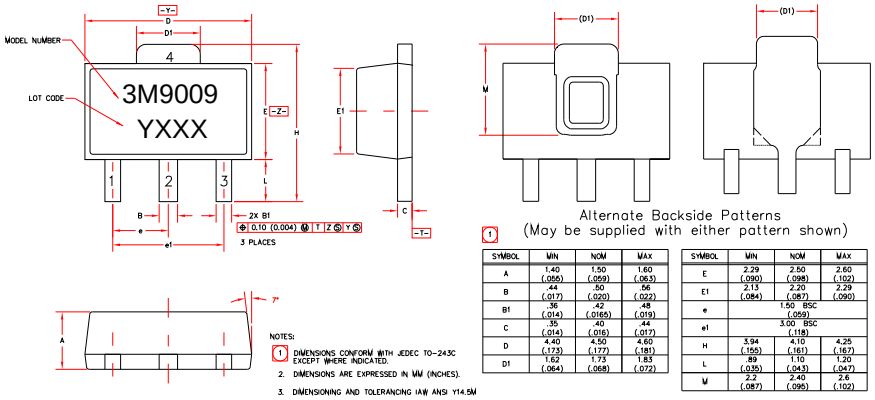


Mechanical Information

Package Information and Dimensions

This package is lead-free/RoHS-compliant. The plating material on the leads is NiPdAu. It is compatible with both lead-free (maximum 260 °C reflow temperature) and lead (maximum 245 °C reflow temperature) soldering processes.

The component will be marked with a "3M9009" designator with an alphanumeric lot code on the top surface of package. The "Y" represents the last digit of the year the part was manufactured; the "XXX" is an auto generated number.

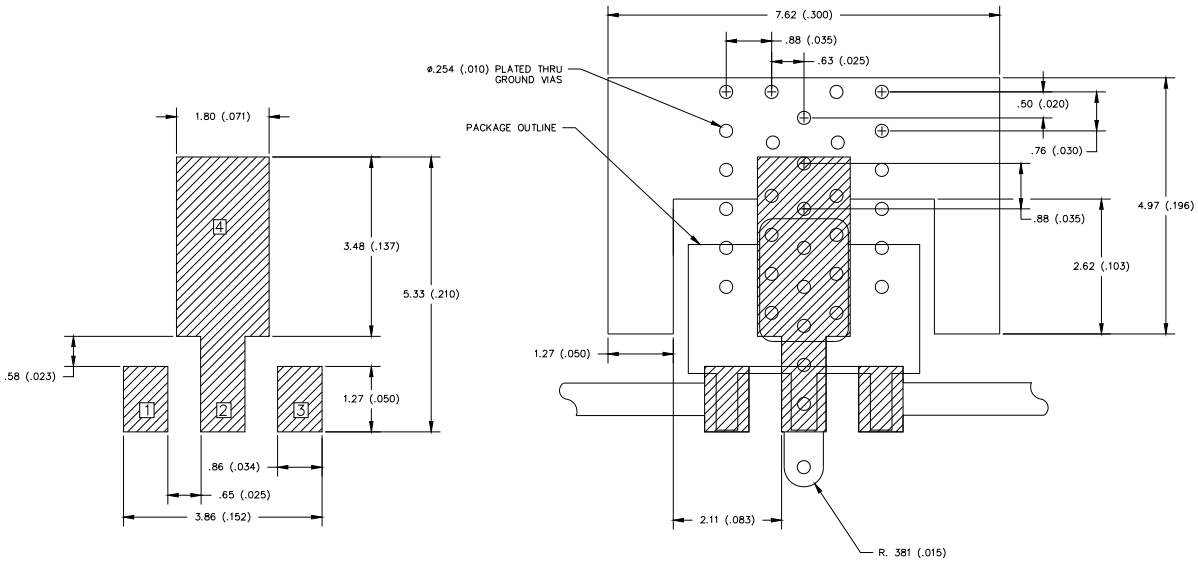


SYMBOL	MIN	NOM	MAX
A	1.40 (.055)	1.50 (.059)	1.60 (.063)
B	.44 (.017)	.50 (.020)	.56 (.022)
B1	.36 (.014)	.42 (.0165)	.48 (.019)
C	.35 (.014)	.40 (.016)	.44 (.017)
D	4.40 (.173)	4.50 (.177)	4.60 (.181)
D1	1.62 (.064)	1.73 (.068)	1.83 (.072)

SYMBOL	MIN	NOM	MAX
E	2.29 (.090)	2.50 (.098)	2.60 (.102)
E1	2.13 (.084)	2.20 (.087)	2.29 (.090)
e	1.50 BSC (.059)		
e1	3.00 BSC (.118)		
H	3.94 (.155)	4.10 (.161)	4.25 (.167)
L	.89 (.035)	1.10 (.043)	1.20 (.047)
M	2.2 (.087)	2.40 (.095)	2.6 (.102)

Mounting Configuration

All dimensions are in millimeters (inches). Angles are in degrees.



Notes:

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. RF trace width depends upon the PC board material and construction.
4. Use 1 oz. Copper minimum.

Product Compliance Information

ESD Information

Caution! ESD-Sensitive Device

ESD Rating:	Class 1A
Value:	Passes ≥ 250 V to < 500 V.
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

ESD Rating:	Class IV
Value:	Passes ≥ 1000 V
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101

MSL Rating

Level 3 at +260 °C convection reflow
The part is rated Moisture Sensitivity Level 3 at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260°

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

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For technical questions and application information:

Email: sjcapplications.engineering@tqs.com

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Virtex-6 CXT Family Data Sheet

DS153 (v1.1) February 5, 2010 **Advance Product Specification**

General Description

Virtex®-6 CXT FPGAs provide designers needing power-optimized 3.75 Gb/s transceiver performance with an optimized ratio of built-in system-level blocks. These include 36 Kb block RAM/FIFOs, up to 15 Mb of block RAM, up to 768 DSP48E1 slices, enhanced mixed-mode clock management blocks, PCI Express® (GEN 1) compatible integrated blocks, a tri-mode Ethernet media access controller (MAC), up to 241K logic cells, and strong IP support. Using the third generation ASMBL™ (Advanced Silicon Modular Block) column-based architecture, the Virtex-6 CXT family also contains SelectIO™ technology with built-in digitally controlled impedance, ChipSync™ source-synchronous interface blocks, enhanced mixed-mode clock management blocks, and advanced configuration options. Customers needing higher transceiver speeds, greater I/O performance, additional Ethernet MACs, or greater capacity should instead use the Virtex-6 LXT or SXT families. Built on a 40 nm state-of-the-art copper process technology, Virtex-6 CXT FPGAs are a programmable alternative to custom ASIC technology. Virtex-6 CXT FPGAs are the programmable silicon foundation for Targeted Design Platforms that deliver integrated software and hardware components to enable designers to focus on innovation as soon as their development cycle begins.

Summary of Virtex-6 CXT FPGA Features

- Advanced, high-performance, FPGA Logic
  - Real 6-input look-up table (LUT) technology
  - Dual LUT5 (5-input LUT) option
  - LUT/dual flip-flop pair for applications requiring rich register mix
  - Improved routing efficiency
  - 64-bit (or 32 x 2-bit) distributed LUT RAM option
  - SRL32/dual SRL16 with registered outputs option
- Powerful mixed-mode clock managers (MMCM)
  - MMCM blocks provide zero-delay buffering, frequency synthesis, clock-phase shifting, input-jitter filtering, and phase-matched clock division
- 36-Kb block RAM/FIFOs
  - Dual-port RAM blocks
  - Programmable
    - Dual-port widths up to 36 bits
    - Simple dual-port widths up to 72 bits
  - Enhanced programmable FIFO logic
  - Built-in optional error-correction circuitry
  - Optionally use each block as two independent 18 Kb blocks
- High-performance parallel SelectIO technology
  - 1.2 to 2.5V I/O operation
  - Source-synchronous interfacing using ChipSync™ technology
  - Digitally controlled impedance (DCI) active termination
  - Flexible fine-grained I/O banking
  - High-speed memory interface support with integrated write-leveling capability
- Advanced DSP48E1 slices
  - 25 x 18, two's complement multiplier/accumulator
  - Optional pipelining
  - New optional pre-adder to assist filtering applications
  - Optional bitwise logic functionality
  - Dedicated cascade connections
- Flexible configuration options
  - SPI and Parallel Flash interface
  - Multi-bitstream support with dedicated fallback reconfiguration logic
  - Automatic bus width detection
- Integrated interface blocks for PCI Express designs
  - Designed to the PCI Express Base Specification 1.1
  - Gen1 Endpoint (2.5 Gb/s) support with GTX transceivers
  - x1, x2, x4, or x8 lane support per block
  - One virtual channel, eight traffic classes
- GTX transceivers: 150 Mb/s to 3.75 Gb/s
- Integrated 10/100/1000 Mb/s Ethernet MAC block
  - Supports 1000BASE-X PCS/PMA and SGMII using GTX transceivers
  - Supports MII, GMII, and RGMII using SelectIO technology resources
- 40 nm copper CMOS process technology
- 1.0V core voltage
- Two speed grades (-1 and -2)
- Two temperature grades (commercial and industrial)
- High signal-integrity flip-chip packaging available in standard or Pb-free package options
- Compatibility across sub-families: CXT, LXT, and SXT devices are footprint compatible in the same package

Virtex-6 CXT FPGA Feature Summary

Table 1: **Virtex-6 CXT FPGA Feature Summary by Device**

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP48E1 Slices(2)	Block RAM Blocks			MMCMs(4)	Interface Blocks for PCI Express	Ethernet MACs(5)	Maximum GTX Transceivers	Total I/O Banks(6)	Max User I/O(7)
		Slices(1)	Max Distributed RAM (Kb)		18 Kb(3)	36 Kb	Max (Kb)						
XC6VCX75T	74,496	11,640	1,045	288	312	156	5,616	6	1	1	12	9	360
XC6VCX130T	128,000	20,000	1,740	480	528	264	9,504	10	2	1	16	15	600
XC6VCX195T	199,680	31,200	3,040	640	688	344	12,384	10	2	1	16	15	600
XC6VCX240T	241,152	37,680	3,650	768	832	416	14,976	12	2	1	16	18	600

Notes:
1. Each Virtex-6 FPGA slice contains four LUTs and eight flip-flops, only some slices can use their LUTs as distributed RAM or SRLs.
2. Each DSP48E1 slice contains a 25 x 18 multiplier, an adder, and an accumulator.
3. Block RAMs are fundamentally 36 Kbits in size. Each block can also be used as two independent 18 Kb blocks.
4. Each CMT contains two mixed-mode clock managers (MMCM).
5. This table lists individual Ethernet MACs per device.
6. Does not include configuration Bank 0.
7. This number does not include GTX transceivers.

Virtex-6 CXT FPGA Device-Package Combinations and Maximum I/Os

Virtex-6 CXT FPGA package combinations with the maximum available I/Os per package are shown in Table 2.

Table 2: **Virtex-6 CXT FPGA Device-Package Combinations and Maximum Available I/Os**

Package	FF484 FFG484		FF784 FFG784		FF1156 FFG1156	
Size (mm)	23 x 23		29 x 29		35 x 35	
Device	GTs	I/O	GTs	I/O	GTs	I/O
XC6VCX75T	8 GTXs	240	12 GTXs	360		
XC6VCX130T	8 GTXs	240	12 GTXs	400	16 GTXs	600
XC6VCX195T			12 GTXs	400	16 GTXs	600
XC6VCX240T			12 GTXs	400	16 GTXs	600

Notes:
1. Flip-chip packages are also available in Pb-Free versions (FFG).

Virtex-6 CXT FPGA Ordering Information

The Virtex-6 CXT FPGA ordering information shown in Figure 1 applies to all packages including Pb-Free.

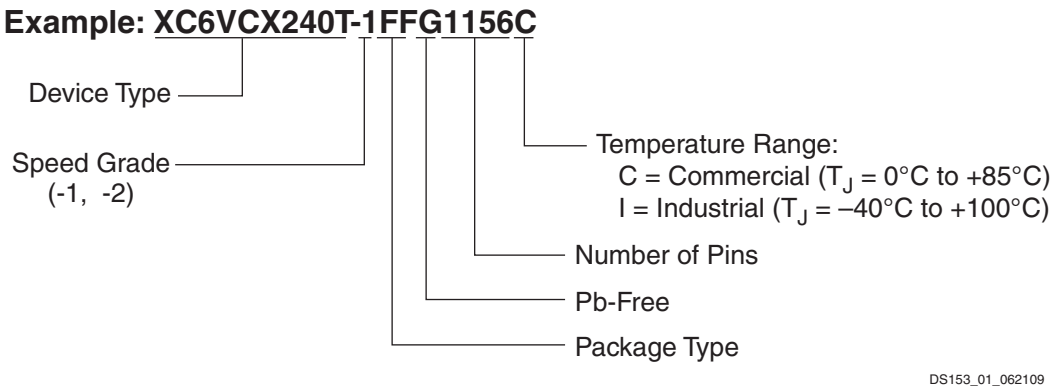

Figure 1: **Virtex-6 CXT FPGA Ordering Information**

Virtex-6 CXT FPGA Documentation

In addition to the data sheet information found herein, complete and up-to-date documentation of the Virtex-6 family of FPGAs is available on the Xilinx website and available for download:

Virtex-6 FPGA Configuration Guide (UG360)

This all-encompassing configuration guide includes chapters on configuration interfaces (serial and parallel), multi-bitstream management, bitstream encryption, boundary-scan and JTAG configuration, and reconfiguration techniques.

Virtex-6 FPGA SelectIO Resources User Guide (UG361)

This guide describes the SelectIO™ resources available in all the Virtex-6 devices.

Virtex-6 FPGA Clocking Resources User Guide (UG362)

This guide describes the clocking resources available in all the Virtex-6 devices, including the MMCM and clock buffers.

Virtex-6 FPGA Memory Resources User Guide (UG363)

This guide describes the Virtex-6 device block RAM and FIFO capabilities.

Virtex-6 FPGA CLB User Guide (UG364)

This guide describes the capabilities of the configurable logic blocks (CLB) available in all Virtex-6 devices.

Virtex-6 FPGA DSP48E1 Slice User Guide (UG369)

This guide describes the architecture of the DSP48E1 slice in Virtex-6 FPGAs and provides configuration examples.

Virtex-6 FPGA GTX Transceivers User Guide (UG366)

This guide describes the GTX transceivers available in all the Virtex-6 CXT FPGAs.

Virtex-6 FPGA Tri-Mode Ethernet MAC User Guide (UG368)

This guide describes the dedicated tri-mode Ethernet media access controller (TEMAC) available in all the Virtex-6 CXT FPGAs.

Virtex-6 FPGA Data Sheet: DC and Switching Characteristics (DS152)

Reference this data sheet when considering device migration to the Virtex-6 LXT and SXT families. It contains the DC and Switching Characteristic specifications specifically for the Virtex-6 LXT and SXT families.

Virtex-6 FPGA Packaging and Pinout Specifications (UG365)

These specifications includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications of the Virtex-6 LXT and SXT families. Reference these specifications when considering device migration to the Virtex-6 LXT and SXT families.

Configuration Bitstream Overview for CXT Devices

This section contains two tables similar to those in the *Virtex-6 FPGA Configuration Guide* only updated for the CXT family. The Virtex-6 FPGA bitstream contains commands to the FPGA configuration logic as well as configuration data. Table 3 gives a typical bitstream length and Table 4 gives the specific device ID codes for the Virtex-6 CXT devices.

Table 3: **Virtex-6 CXT FPGA Bitstream Length**

Device	Total Number of Configuration Bits
XC6VCX75T	26,239,328
XC6VCX130T	43,719,776
XC6VCX195T	61,552,736
XC6VCX240T	73,859,552

Table 4: **Virtex-6 FPGA Device ID Codes**

Device	ID Code (Hex)
XC6VCX75T	0x042C4093
XC6VCX130T	0x042CA093
XC6VCX195T	0x042CC093
XC6VCX240T	0x042D0093

CLB Overview for CXT Devices

Table 5, updated specifically for the CXT family from a similar table in the *Virtex-6 FPGA CLB User Guide*, shows the available resources in all Virtex-6 FPGA CLBs.

Table 5: **Virtex-6 CXT FPGA Logic Resources Available in All CLBs**

Device	Total Slices	SLICELs	SLICEMs	Number of 6-Input LUTs	Maximum Distributed RAM (Kb)	Shift Register (Kb)	Number of Flip-Flops
XC6VCX75T	11,640	7,460	4,180	46,560	1045	522.5	93,120
XC6VCX130T	20,000	13,040	6,960	80,000	1740	870	160,000
XC6VCX195T	31,200	19,040	12,160	124,800	3140	1570	249,600
XC6VCX240T	37,680	23,080	14,600	150,720	3770	1885	301,440

Regional Clock Management for CXT Devices

Table 6, updated from the *Virtex-6 FPGA Clocking Resources User Guide* specifically for the CXT family, shows the number of clock regions in all Virtex-6 CXT FPGA CLBs.

Table 6: **Virtex-6 CXT FPGA Clock Regions**

Device	Number of Clock Regions
XC6VCX75T	6
XC6VCX130T	10
XC6VCX195T	10
XC6VCX240T	12

CXT Packaging Specifications

Table 7, updated from the *Virtex-6 FPGA Packaging and Pinout Specifications* specifically for the CXT family, shows the number of GTX transceiver I/O channels. Table 8 shows the number of available I/Os and the number of differential I/O pairs for each Virtex-6 device/package combination.

Table 7: **Number of Serial Transceivers (GTs) I/O Channels/Device**

I/O Channels	Device			
	CX75T(1)	CX130T(2)	CX195T(3)	CX240T(4)
MGTRXP	8 or 12	8, 12, or 16	12 or 16	12 or 16
MGTRXN	8 or 12	8, 12, or 16	12 or 16	12 or 16
MGTTXP	8 or 12	8, 12, or 16	12 or 16	12 or 16
MGTTXN	8 or 12	8, 12, or 16	12 or 16	12 or 16

Notes:

1. The XC6VCX75T has 8 GTX I/O channels in the FF484/FFG484 package and 12 GTX I/O channels in the FF784/FFG784 package.
2. The XC6VCX130T has 8 GTX I/O channels in the FF484/FFG484 package, 12 GTX I/O channels in the FF784/FFG784 package, and 16 GTX I/O channels in the FF1156/FFG1156 package.
3. The XC6VCX195T has 12 GTX I/O channels in the FF784/FFG784 package and 16 GTX I/O channels in the FF1156/FFG1156 package.
4. The XC6VCX240T has 12 GTX I/O channels in the FF784/FFG784 package and 16 GTX I/O channels in the FF1156/FFG1156 package.

Table 8: **Available I/O Pin/Device/Package Combinations**

Virtex-6 CXT Device	User I/O Pins	Virtex-6 CXT FPGA Package		
		FF484	FF784	FF1156
XC6VCX75T	Available User I/Os	240	360	–
	Differential I/O Pairs	120	180	–
XC6VCX130T	Available User I/Os	240	400	600
	Differential I/O Pairs	120	200	300
XC6VCX195T	Available User I/Os	–	400	600
	Differential I/O Pairs	–	200	300
XC6VCX240T	Available User I/Os	–	400	600
	Differential I/O Pairs	–	200	300

GTX Transceivers in CXT Devices

CXT devices have between 8 to 16 gigabit transceiver circuits. Each GTX transceiver is a combined transmitter and receiver capable of operating at a data rate between 155 Mb/s and 3.75 Gb/s. The transmitter and receiver are independent circuits that use separate PLLs to multiply the reference frequency input by certain programmable numbers between 2 and 25, to become the bit-serial data clock. Each GTX transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation

FF484 Package Placement Diagrams

Figure 2 and Figure 3 show the placement diagrams for the GTX transceivers in the FF484 package.

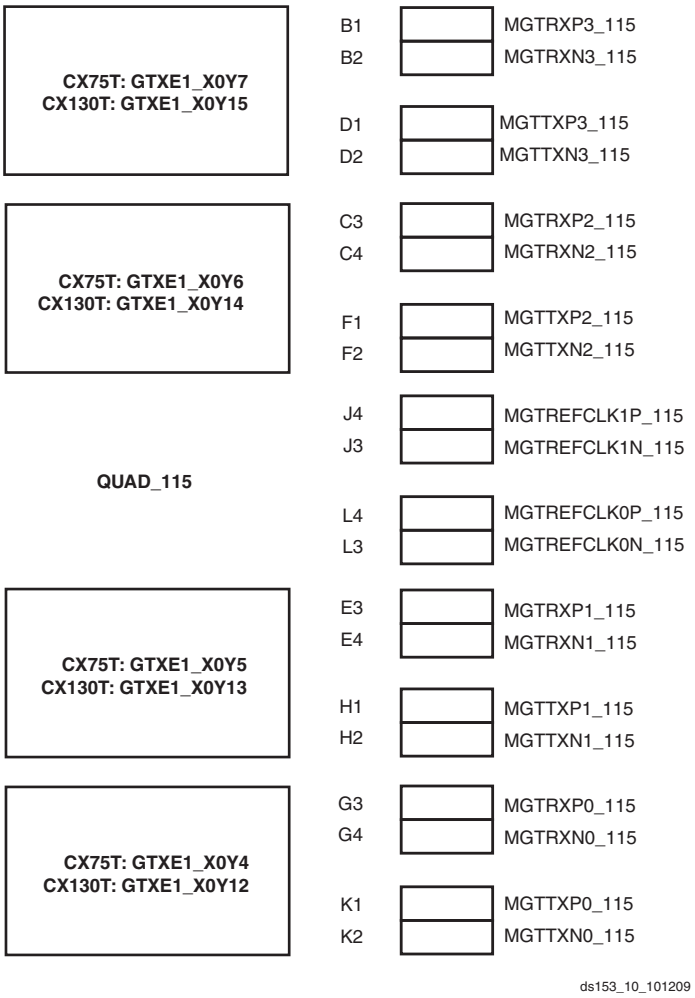

Figure 2: **Placement Diagram for the FF484 Package (1 of 2)**

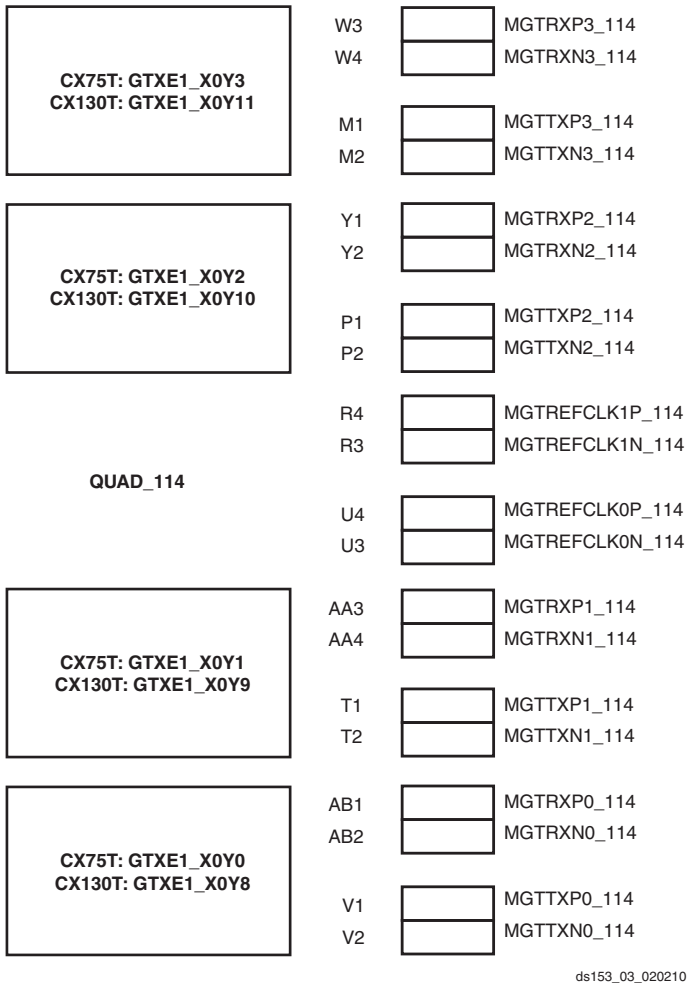

Figure 3: **Placement Diagram for the FF484 Package (2 of 2)**

FF784 Package Placement Diagrams

Figure 4 through Figure 6 show the placement diagrams for the GTX transceivers in the FF784 package.

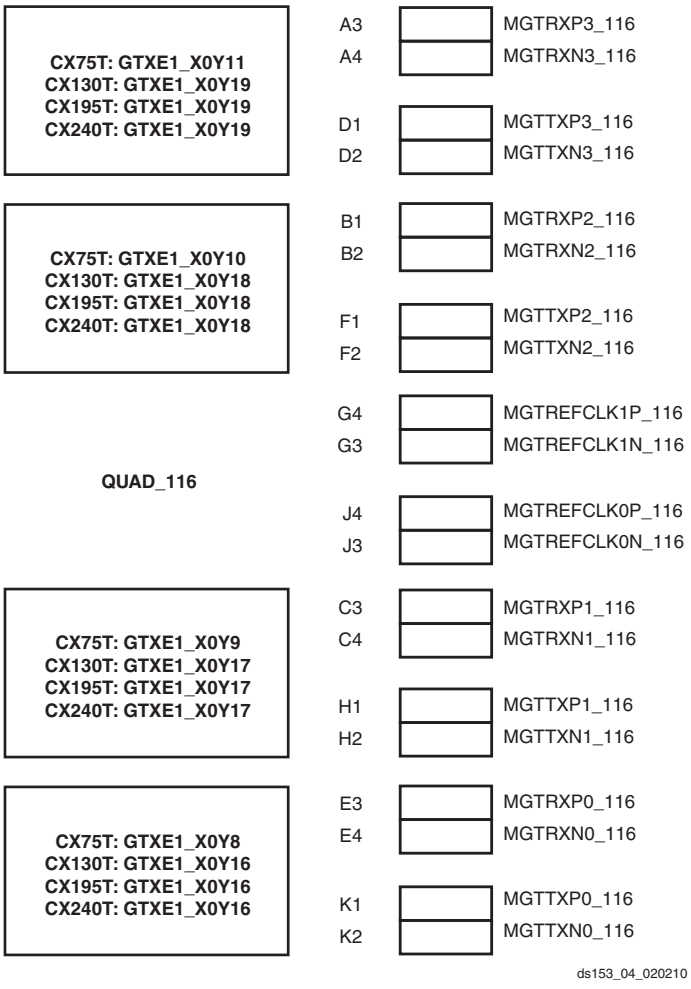

Figure 4: **Placement Diagram for the FF784 Package (1 of 3)**

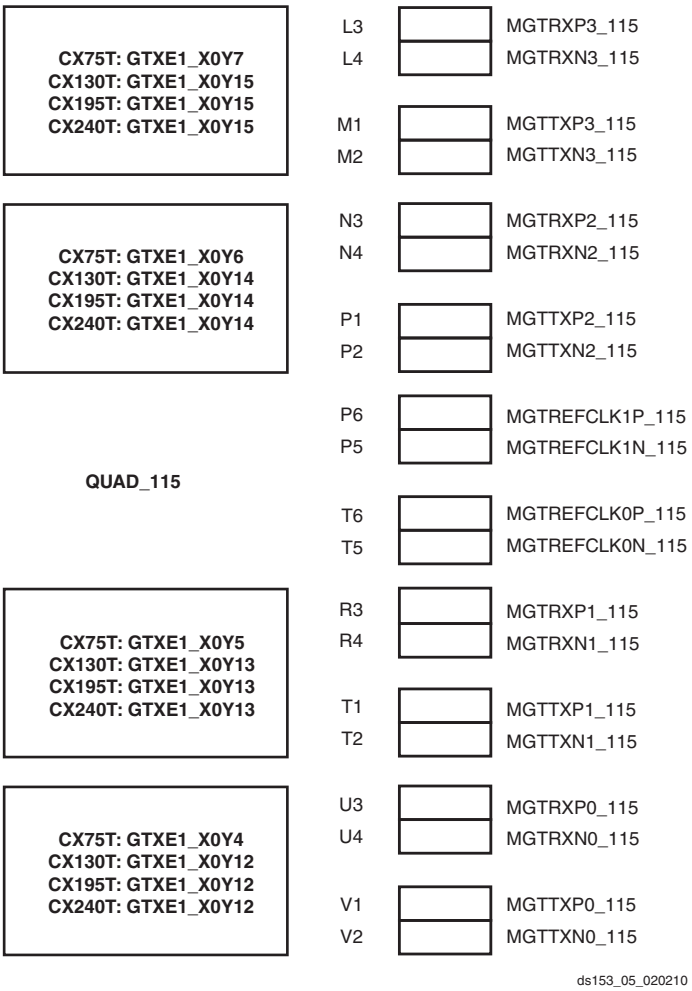

Figure 5: **Placement Diagram for the FF784 Package (2 of 3)**

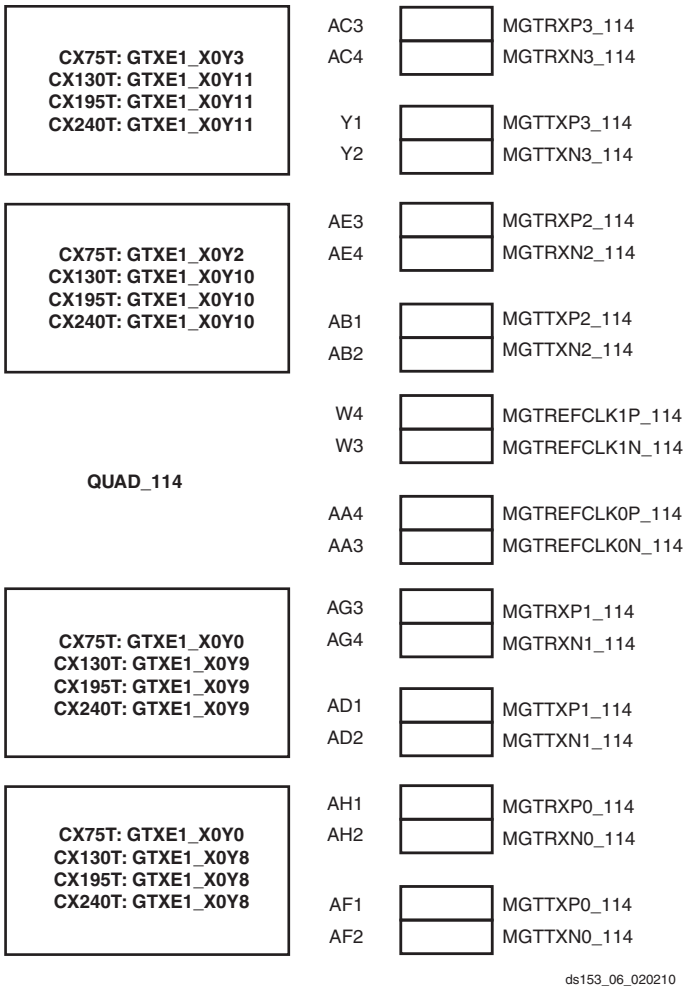

Figure 6: **Placement Diagram for the FF784 Package (3 of 3)**

FF1156 Package Placement Diagrams

Figure 7 through Figure 10 show the placement diagrams for the GTX transceivers in the FF1156 package.

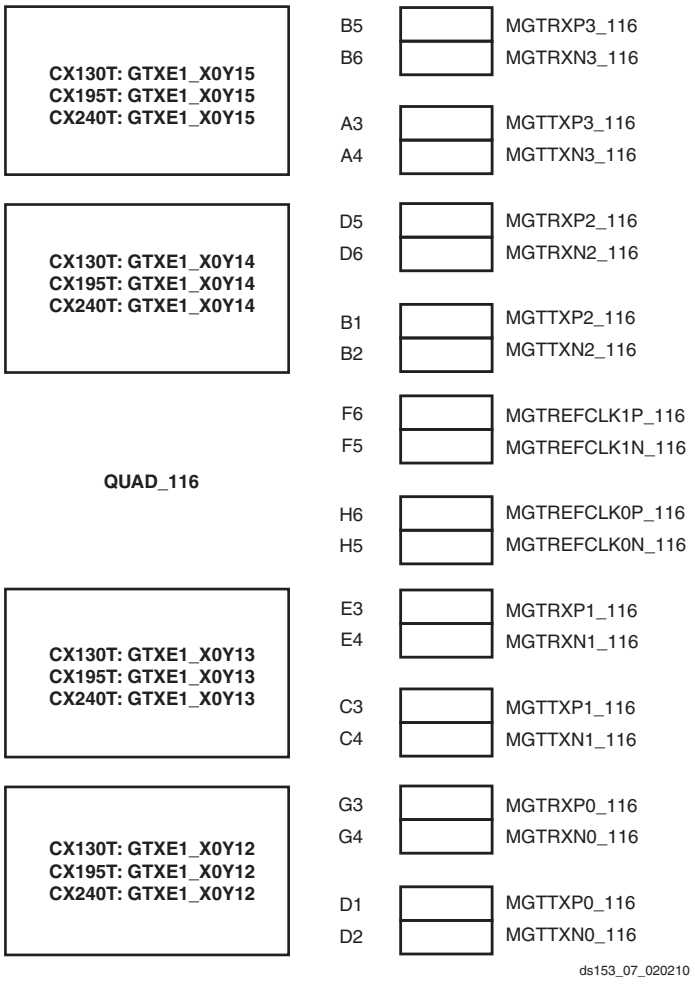

Figure 7: **Placement Diagram for the FF1156 Package (1 of 4)**

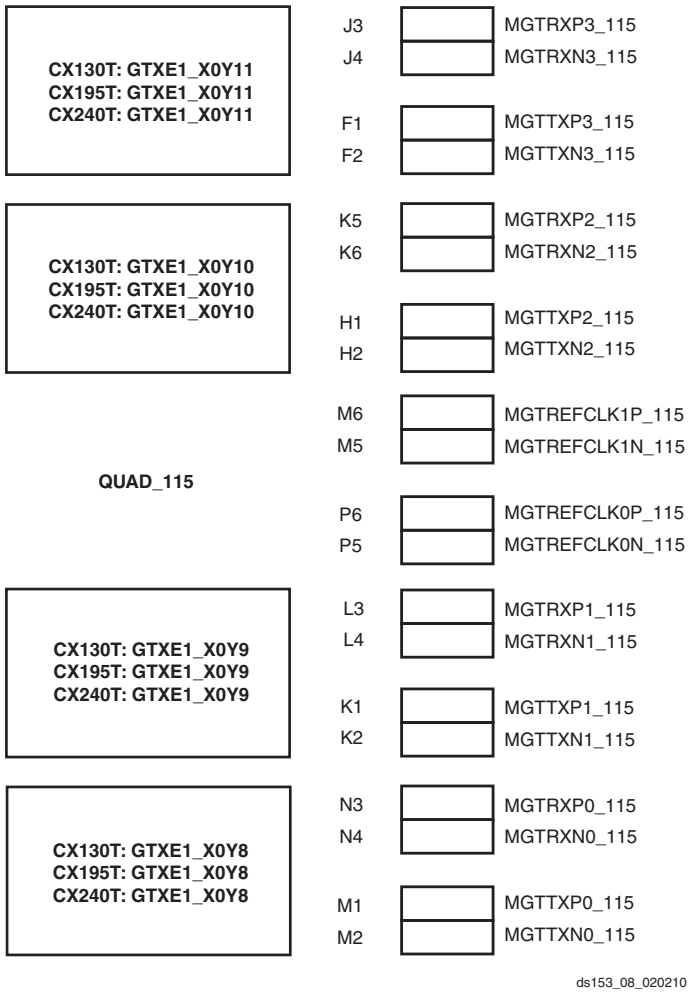

Figure 8: **Placement Diagram for the FF1156 Package (2 of 4)**

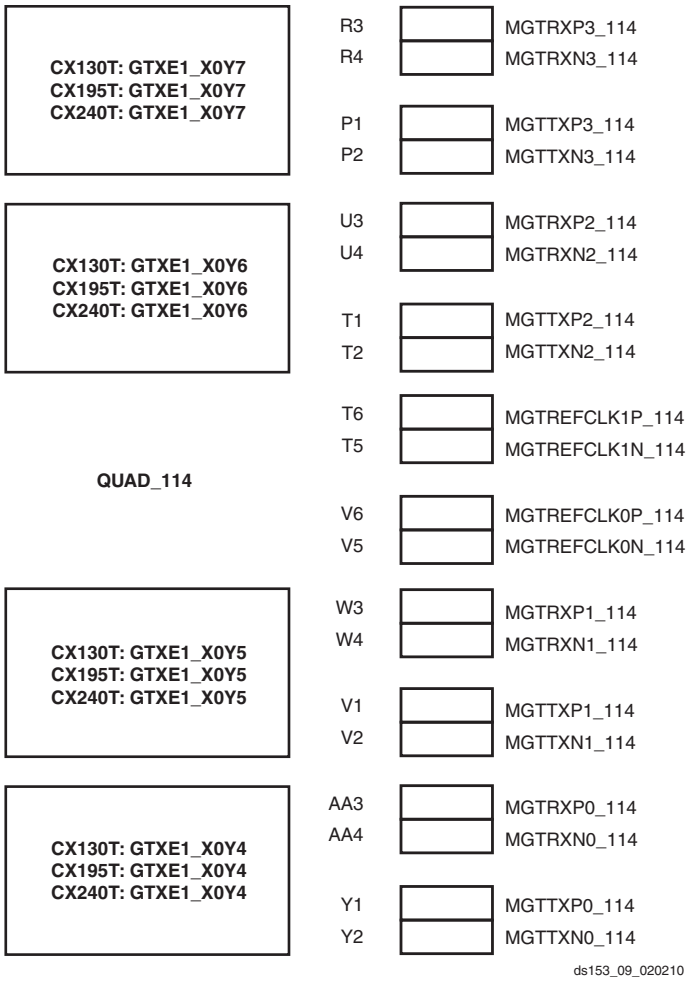

Figure 9: **Placement Diagram for the FF1156 Package (3 of 4)**

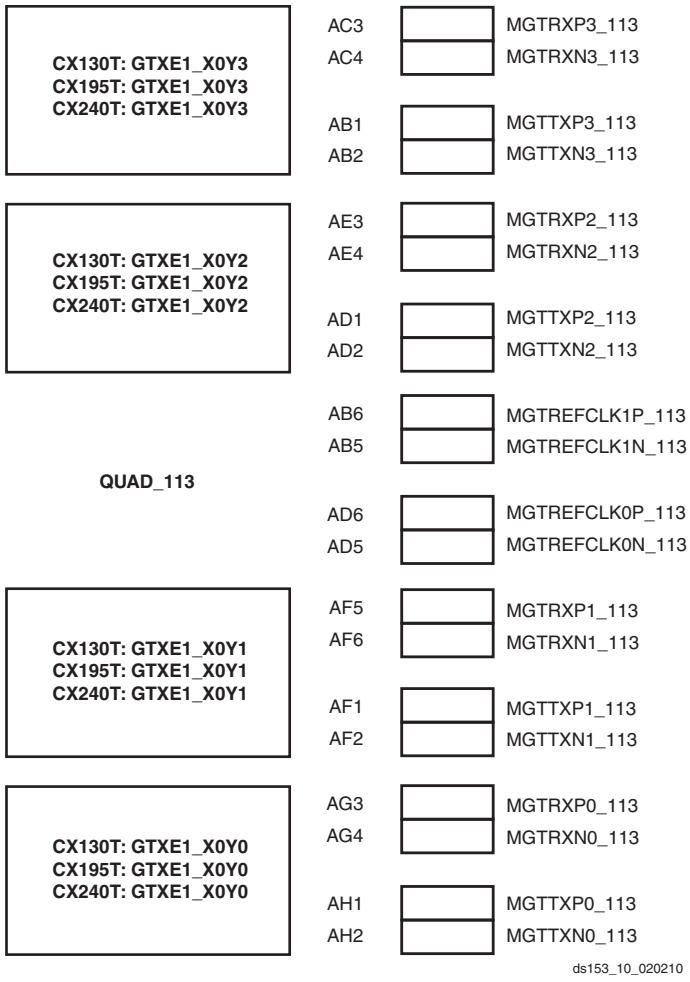

Figure 10: **Placement Diagram for the FF1156 Package (4 of 4)**

Virtex-6 CXT FPGA Electrical Characteristics Introduction

Virtex-6 CXT FPGAs are available in -2 and -1 speed grades, with -2 having the highest performance. Virtex-6 CXT FPGA DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade industrial device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

All specifications are subject to change without notice.

Virtex-6 CXT FPGA DC Characteristics

Table 9: **Absolute Maximum Ratings**

Symbol	Description		Units
V_{CCINT}	Internal supply voltage relative to GND	–0.5 to 1.1	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	–0.5 to 3.0	V
V_{CCO}	Output drivers supply voltage relative to GND	–0.5 to 3.0	V
V_{BATT}	Key memory battery backup supply	–0.5 to 3.0	V
V_{REF}	Input reference voltage	–0.5 to 3.0	V
V_{IN}(3)	2.5V or below I/O input voltage relative to GND(4) (user and dedicated I/Os)	–0.75 to V_{CCO} + 0.5	V
V_{TS}	Voltage applied to 3-state 2.5V or below output(4) (user and dedicated I/Os)	–0.75 to V_{CCO} + 0.5	V
T_{STG}	Storage temperature (ambient)	–65 to 150	°C
T_{SOL}	Maximum soldering temperature(2)	+220	°C
T_J	Maximum junction temperature(2)	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. For soldering guidelines and thermal considerations, see *Virtex-6 FPGA Packaging and Pinout Specification*.
3. 2.5V I/O absolute maximum limit applied to DC and AC signals.
4. For 2.5V I/O operation, refer to the *Virtex-6 FPGA SelectIO Resources User Guide*.

Table 10: **Recommended Operating Conditions**

Symbol	Description	Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND, T_J = 0°C to +85°C	0.95	1.05	V
V_{CCAUX}	Auxiliary supply voltage relative to GND, T_J = 0°C to +85°C	2.375	2.625	V
V_{CCO}(1,3,4)	Supply voltage relative to GND, T_J = 0°C to +85°C	1.14	2.625	V
V_{IN}	2.5V supply voltage relative to GND, T_J = 0°C to +85°C	GND – 0.20	2.625	V
	2.5V and below supply voltage relative to GND, T_J = 0°C to +85°C	GND – 0.20	V_{CCO} + 0.2	V
I_{IN}	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.		10	mA
V_{BATT}(2)	Battery voltage relative to GND, T_J = 0°C to +85°C	1.0	2.5	V

Notes:
1. Configuration data is retained even if V_{CCO} drops to 0V.
2. V_{BATT} is required only when using bitstream encryption. If battery is not used, connect V_{BATT} to either ground or V_{CCAUX}.
3. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, and 2.5V.
4. The configuration supply voltage V_{CC_CONFIG} is also known as V_{CCO_0}
5. All voltages are relative to ground.

Table 11: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Data Rate	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)					V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)					V
I_{REF}	V_{REF} leakage current per pin					µA
I_L	Input or output leakage current per pin (sample-tested)					µA
C_{IN}	Input capacitance (sample-tested)					pF
I_{RPU}(1)	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V					µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V					µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V					µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V					µA
I_{RPD}(1)	Pad pull-down (when selected) @ V_{IN} = 2.5V					µA
I_{BATT}(2)	Battery supply current					nA
n	Temperature diode ideality factor					n
r	Series resistance					Ω

Notes:
1. Typical values are specified at nominal voltage, 25°C.
2. Maximum value specified for worst case process at 25°C.

Quiescent Supply Current: Important Note

Typical values for quiescent supply current are specified at nominal voltage, 85°C junction temperatures (T_j). Xilinx recommends analyzing static power consumption at T_j = 85°C because the majority of designs operate near the high end of the commercial temperature range. Quiescent supply current is specified by speed grade for Virtex-6 CXT devices. Use the XPOWER™ Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified in Table 12.

Table 12: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed and Temperature Grade		Units
			-2 (C & I)	-1 (C & I)	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC6VCX75T	927	927	mA
		XC6VCX130T	1563	1563	mA
		XC6VCX195T	2059	2059	mA
		XC6VCX240T	2478	2478	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC6VCX75T	1	1	mA
		XC6VCX130T	1	1	mA
		XC6VCX195T	1	1	mA
		XC6VCX240T	2	2	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC6VCX75T	45	45	mA
		XC6VCX130T	75	75	mA
		XC6VCX195T	113	113	mA
		XC6VCX240T	135	135	mA

Notes:
1. Typical values are specified at nominal voltage, 85°C junction temperatures (Tj). Industrial (I) grade devices have the same typical values as commercial (C) grade devices at 85°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply.

Virtex-6 CXT devices require a power-on sequence of V_{CCINT}, V_{CCAUX}, and V_{CCO}. If the requirement can not be met, then V_{CCAUX} must always be powered prior to V_{CCO}. V_{CCAUX} and V_{CCO} can be powered by the same supply, therefore, both V_{CCAUX} and V_{CCO} are permitted to ramp simultaneously. Similarly, for the power-down sequence, V_{CCO} must be powered down prior to V_{CCAUX}.

Table 13 shows the minimum current required by Virtex-6 devices for proper power-on and configuration. If the current minimums shown in Table 13 are met, the device powers on after all three supplies have passed through their power-on reset threshold voltages. The FPGA must be configured after V_{CCINT} is applied.

Once initialized and configured, use the XPOWER tools to estimate current drain on these supplies.

Table 13: **Power-On Current for Virtex-6 CXT Devices**

Device	$I_{CCINTMIN}$		$I_{CCAUXMIN}$		I_{CCOMIN}		Units
	Typ(1)	Max	Typ(1)	Max	Typ(1)	Max	
XC6VCX75T							mA
XC6VCX130T							mA
XC6VCX195T							mA
XC6VCX240T							mA

Notes:
1. Typical values are specified at nominal voltage, 25°C.

Table 14: **Power Supply Ramp Time**

Symbol	Description	Ramp Time	Units
V_{CCINT}	Internal supply voltage relative to GND	0.20 to 50.0	ms
V_{CCO}	Output drivers supply voltage relative to GND	0.20 to 50.0	ms
V_{CCAUX}	Auxiliary supply voltage relative to GND	0.20 to 50.0	ms

SelectIO™ DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 15: **SelectIO DC Input and Output Levels**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVCMOS25, LVDCI25	–0.3	0.7	1.7	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	Note(3)	Note(3)
LVCMOS18, LVDCI18	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	0.45	V_{CCO} – 0.45	Note(4)	Note(4)
LVCMOS15, LVDCI15	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note(4)	Note(4)
LVCMOS12	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note(5)	Note(5)
HSTL I_12	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	6.3	6.3
HSTL I(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	8	–8
HSTL II(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	16	–16
HSTL III(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	24	–8
DIFF HSTL I(2)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
DIFF HSTL II(2)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
SSTL2 I	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	8.1	–8.1
SSTL2 II	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
DIFF SSTL2 I	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	–	–	–	–
DIFF SSTL2 II	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	–	–	–	–
SSTL18 I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.47	V_{TT} + 0.47	6.7	–6.7
SSTL18 II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.60	V_{TT} + 0.60	13.4	–13.4
DIFF SSTL18 I	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	–	–	–	–
DIFF SSTL18 II	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	–	–	–	–
SSTL15								
DIFF SSTL15					–	–	–	–

Notes:
1. Tested according to relevant specifications.
2. Applies to both 1.5V and 1.8V HSTL.
3. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
4. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
5. Supported drive strengths of 2, 4, 6, or 8 mA.
6. For detailed interface specific DC voltage levels, see the *Virtex-6 FPGA SelectIO Resources User Guide*.

HT DC Specifications (HT_25)

Table 16: **HT DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OD}	Differential Output Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	495	600	715	mV
ΔV_{OD}	Change in V_{OD} Magnitude		–15		15	mV
V_{OCM}	Output Common Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	495	600	715	mV
ΔV_{OCM}	Change in V_{OCM} Magnitude		–15		15	mV
V_{ID}	Input Differential Voltage		200	600	1000	mV
ΔV_{ID}	Change in V_{ID} Magnitude		–15		15	mV
V_{ICM}	Input Common Mode Voltage		440	600	780	mV
ΔV_{ICM}	Change in V_{ICM} Magnitude		–15		15	mV

LVDS DC Specifications (LVDS_25)

Table 17: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.825			V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High (($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.250	1.375	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High (($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.3	1.2	2.2	V

Extended LVDS DC Specifications (LVDSEXT_25)

Table 18: **Extended LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals		–	1.785	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.715	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High (($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	350	–	820	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.250	1.375	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High (($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	–	1000	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ±350 mV	0.3	1.2	2.2	V

LVPECL DC Specifications (LVPECL_25)

These values are valid when driving a 100Ω differential load only, i.e., a 100Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 19 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see the *Virtex-6 FPGA SelectIO Resources User Guide*.

Table 19: **LVPECL DC Specifications**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{OH}	Output High Voltage	V_{CC} – 1.025	1.545	V_{CC} – 0.88	V
V_{OL}	Output Low Voltage	V_{CC} – 1.81	0.795	V_{CC} – 1.62	V
V_{ICM}	Input Common-Mode Voltage	0.6		2.2	V
V_{IDIFF}	Differential Input Voltage(1,2)	0.100		1.5	V

Notes:
1. Recommended input maximum voltage not to exceed V_{CCAUX} + 0.2V.
2. Recommended input minimum voltage not to go below –0.5V.

GTX Transceiver Specifications

GTX Transceiver DC Characteristics

Table 20: **Absolute Maximum Ratings for GTX Transceivers**

Symbol	Description	Min	Max	Units
MGTAVCC_N MGTAVCC_S	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	–0.5	1.1	V
MGTAVTT_N MGTAVTT_S	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	–0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage			V
$V_{MGTREFCLK}$	Reference clock absolute input voltage			V

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 21: **Recommended Operating Conditions for GTX Transceivers(1)(2)**

Symbol	Description	Min	Max	Units
MGTAVCC_N MGTAVCC_S	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	0.95	1.05	V
MGTAVTT_N MGTAVTT_S	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	1.14	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	1.14	1.26	V

Notes:
1. Each voltage listed requires the filter circuit described in *Virtex-6 FPGA RocketIO GTX Transceiver User Guide*.
2. Voltages are specified for the temperature range of T_J = –40°C to +100°C.

Table 22: **DC Characteristics Over Recommended Operating Conditions for GTX Transmitters(1)**

Symbol	Description	Min	Typ	Max	Units
$I_{MGTAVTT}$	GTX transmitter termination supply current(2)				mA
$I_{MGTAVTTRCAL}$	GTX transceiver resistor termination calibration supply current				mA
$I_{MGTAVCC}$	GTX transceiver internal analog supply current				mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	100.0 ± 1% tolerance			Ω

Notes:
1. Typical values are specified at nominal voltage, 25°C, with a 3.125 Gb/s line rate.
2. I_{CC} numbers are given per GTX transceiver operating with default settings.
3. Values for currents other than the values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 23: **GTX Transceiver Quiescent Supply Current**

Symbol	Description	Typ(1)	Max	Units
I_{AVTTQ}	Quiescent MGTAVTT (transmitter termination) supply current			mA
I_{AVCCQ}	Quiescent MGTAVCC (analog) supply current			mA

Notes:
1. Typical values are specified at nominal voltage, 25°C.
2. Device powered and unconfigured.
3. Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
4. GTX transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTX transceivers.

GTX Transceiver DC Input and Output Levels

Table 24 summarizes the DC output specifications of the GTX transceivers in Virtex-6 FPGAs. Figure 11 shows the single-ended output voltage swing. Figure 12 shows the peak-to-peak differential output voltage.

Consult the *Virtex-6 FPGA RocketIO GTX Transceiver User Guide* for further details.

Table 24: **GTX Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled	125		2000	mV
V_{IN}	Input voltage	DC coupled MGTAVTT_N/S = 1.2V	–400		MGTAVTT	mV
V_{CMIN}	Common mode input voltage	DC coupled MGTAVTT_N/S = 1.2V		2/3 MGTAVTT_N/S		mV
DV_{PPOUT}	Differential peak-to-peak output voltage(1)				1000	mV
V_{SEOUT}	Single-ended output voltage swing(1)				500	mV
$V_{CMOUTDC}$	DC common mode output voltage.	Equation based	MGTAVTT_N/S – DV_{PPOUT}/2			mV
R_{IN}	Differential input resistance			100		Ω
R_{OUT}	Differential output resistance			100		Ω
T_{OSKEW}	Transmitter output skew					ps
C_{EXT}	Recommended external AC coupling capacitor(2)			100		nF

Notes:
1. The output swing and preemphasis levels are programmable using the attributes discussed in *Virtex-6 FPGA RocketIO GTX Transceiver User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

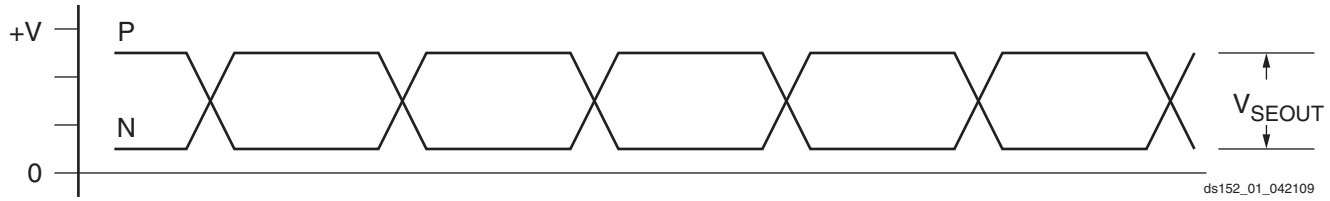

Figure 11: **Single-Ended Output Voltage Swing**

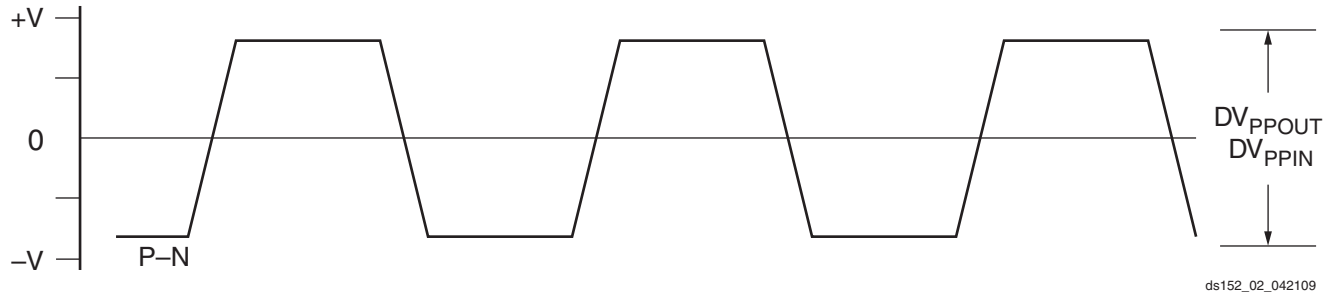

Figure 12: **Peak-to-Peak Differential Output Voltage**

Table 25 summarizes the DC specifications of the clock input of the GTX transceiver. Figure 13 shows the single-ended input voltage swing. Figure 14 shows the peak-to-peak differential clock input voltage swing. Consult the *Virtex-6 FPGA RocketIO GTX Transceiver User Guide* for further details.

Table 25: **GTX Transceiver Clock DC Input Level Specification(1)**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage			800		mV
V_{ISE}	Single-ended input voltage			400		mV
R_{IN}	Differential input resistance			100		Ω
C_{EXT}	Required external AC coupling capacitor			100		nF

Notes:
1. V_{MIN} = 0V and V_{MAX} = MGTAVCC

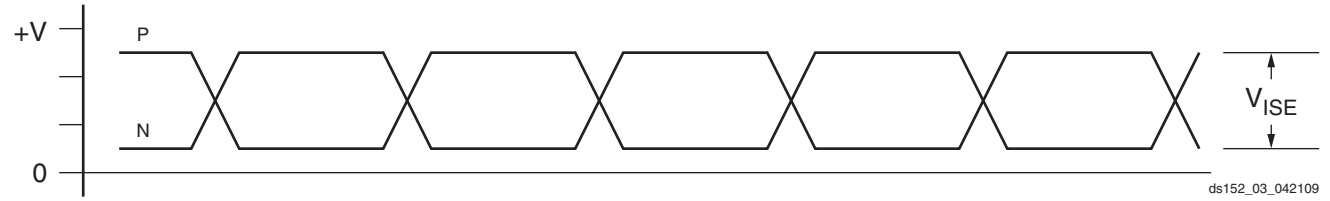

Figure 13: **Single-Ended Clock Input Voltage Swing Peak-to-Peak**

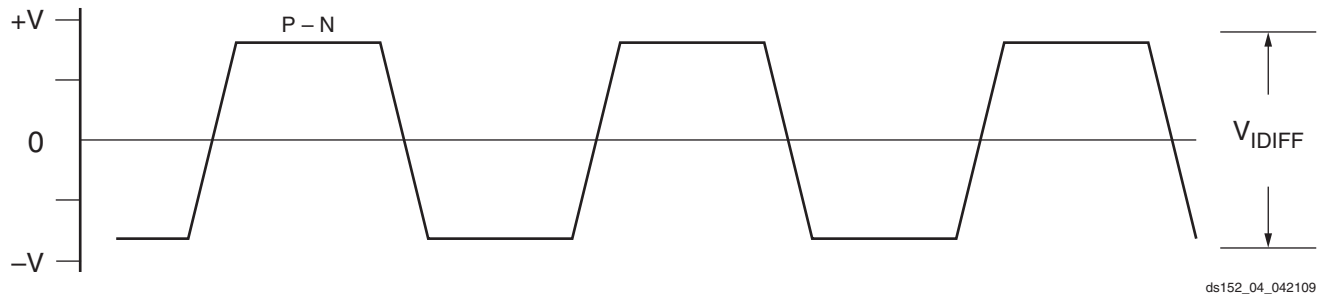

Figure 14: **Differential Clock Input Voltage Swing Peak-to-Peak**

GTX Transceiver Switching Characteristics

Consult *Virtex-6 FPGA RocketIO GTX Transceiver User Guide* for further information.

Table 26: **GTX Transceiver Performance**

Symbol	Description	Speed Grade		Units
		-2	-1	
F_{GTXMAX}	Maximum GTX transceiver data rate	3.75	3.125	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	2.7	2.7	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	1.35	1.35	GHz

Table 27: **Dynamic Reconfiguration Port (DRP) in the GTX Transceiver Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
$F_{GTXDRPCLK}$	GTXDRPCLK maximum frequency	100	100	MHz

Table 28: **GTX Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		67.5		375	MHz
T_{RCLK}	Reference clock rise time	20% – 80%		200		ps
T_{FCLK}	Reference clock fall time	80% – 20%		200		ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only. See Table 29 for USRCLK2 and USRCLK duty cycle requirements		50		%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock			1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock				µs

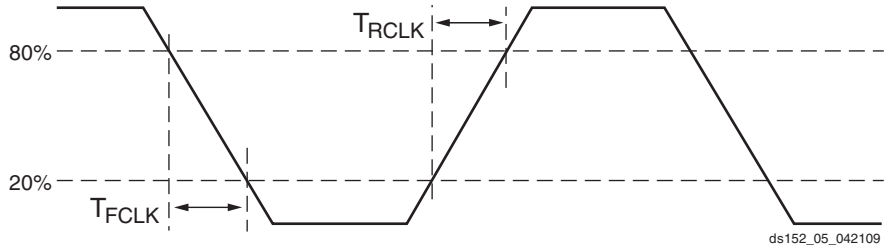

Figure 15: **Reference Clock Timing Parameters**

Table 29: **GTX Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Conditions	Speed Grade		Units
			-2	-1	
F_{TXOUT}	TXOUTCLK maximum frequency	Internal 20-bit data path			MHz
		Internal 16-bit data path			MHz
F_{RXREC}	RXRECCLK maximum frequency				MHz
T_{RX}	RXUSRCLK maximum frequency				MHz
T_{RX2}	RXUSRCLK2 maximum frequency	1 byte interface			MHz
		2 byte interface			MHz
		4 byte interface			MHz
T_{TX}	TXUSRCLK maximum frequency				MHz
T_{TX2}	TXUSRCLK2 maximum frequency	1 byte interface			MHz
		2 byte interface			MHz
		4 byte interface			MHz

Notes:
1. Clocking must be implemented as described in *Virtex-6 FPGA RocketIO GTX Transceiver User Guide*.

Table 30: **GTX Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTXTX}	Serial data rate range		0.15		F_{GTXMAX}	Gb/s
T_{RTX}	TX Rise time	20%–80%				ps
T_{FTX}	TX Fall time	80%–20%				ps
T_{LLSKEW}	TX lane-to-lane skew(1)					ps
$V_{TXOOBVDPP}$	Electrical idle amplitude				20	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time					ns
$T_{J3.75}$	Total Jitter(2)	3.75 Gb/s				UI
$D_{J3.75}$	Deterministic Jitter(2)					UI
$T_{J3.125}$	Total Jitter(2)	3.125 Gb/s				UI
$D_{J3.125}$	Deterministic Jitter(2)					UI
$T_{J3.125L}$	Total Jitter(2)	3.125 Gb/s(3)				UI
$D_{J3.125L}$	Deterministic Jitter(2)					UI
$T_{J2.5}$	Total Jitter(2)	2.5 Gb/s				UI
$D_{J2.5}$	Deterministic Jitter(2)					UI
$T_{J1.25}$	Total Jitter(2)	1.25 Gb/s				UI
$D_{J1.25}$	Deterministic Jitter(2)					UI
T_{J675}	Total Jitter(2)	675 Mb/s				UI
D_{J675}	Deterministic Jitter(2)					UI

Table 30: **GTX Transceiver Transmitter Switching Characteristics *(Cont'd)***

Symbol	Description	Condition	Min	Typ	Max	Units
T_{J150}	Total Jitter(2)	150 Mb/s				UI
D_{J150}	Deterministic Jitter(2)					UI

Notes:
1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to four consecutive GTX transceiver sites.
2. Using PLL_DIVSEL_FB = 2, INTDATAWIDTH = 1. These values are NOT intended for protocol specific compliance determinations.
3. PLL frequency at 1.5625 GHz and OUTDIV = 1.

Table 31: **GTX Transceiver Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GTXRX}	Serial data rate	RX oversampler not enabled	0.675		F_{GTXMAX}	Gb/s
		RX oversampler enabled	0.15		0.675	Gb/s
$T_{RXELECIDLE}$	TIme for RXELECIDLE to respond to loss or restoration of data					ns
$R_{XOOBVDPP}$	OOB detect threshold peak-to-peak		60		150	mV
R_{XSST}	Receiver spread-spectrum tracking(1)	Modulated @ 33 KHz				ppm
R_{XRL}	Run length (CID)	Internal AC capacitor bypassed				UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	CDR 2nd-order loop disabled				ppm
		CDR 2nd-order loop enabled				ppm
SJ Jitter Tolerance(2)						
$JT\_SJ_{3.75}$	Sinusoidal Jitter(3)	3.75 Gb/s				UI
$JT\_SJ_{3.125}$	Sinusoidal Jitter(3)	3.125 Gb/s				UI
$JT\_SJ_{3.125L}$	Sinusoidal Jitter(3)	3.125 Gb/s(4)				UI
$JT\_SJ_{2.5}$	Sinusoidal Jitter(3)	2.5 Gb/s				UI
$JT\_SJ_{1.25}$	Sinusoidal Jitter(3)	1.25 Gb/s				UI
JT_SJ_{675}	Sinusoidal Jitter(3)	675 Mb/s				UI
JT_SJ_{150}	Sinusoidal Jitter(3)	150 Mb/s				UI
SJ Jitter Tolerance with Stressed Eye(2)						
$JT\_TJSE_{3.125}$	Total Jitter with Stressed Eye	3.125 Gb/s				UI
$JT\_SJSE_{3.125}$	Sinusoidal Jitter with Stressed Eye	3.125 Gb/s				UI

Notes:
1. Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
2. All jitter values are based on a Bit Error Ratio of $1e^{-12}$.
3. Using 80 MHz sinusoidal jitter only in the absence of deterministic and random jitter.
4. PLL frequency at 1.5625 GHz and OUTDIV = 1.

Ethernet MAC Switching Characteristics

Consult *Virtex-6 FPGA Embedded Tri-mode Ethernet MAC User Guide* for further information.

Table 32: **Maximum Ethernet MAC Performance**

Symbol	Description	Conditions	Speed Grade		Units
			-2	-1	
$F_{TEMACCLIENT}$	Client interface maximum frequency	10 Mb/s – 8-bit width	2.5(1)	2.5(1)	MHz
		100 Mb/s – 8-bit width	25(2)	25(2)	MHz
		1000 Mb/s – 8-bit width	125	125	MHz
		1000 Mb/s – 16-bit width	62.5	62.5	MHz
$F_{TEMACPHY}$	Physical interface maximum frequency	10 Mb/s – 4-bit width	2.5	2.5	MHz
		100 Mb/s – 4-bit width	25	25	MHz
		1000 Mb/s – 8-bit width	125	125	MHz

Notes:

1. When not using clock enable, the F_{MAX} is lowered to 1.25 MHz.
2. When not using clock enable, the F_{MAX} is lowered to 12.5 MHz.

Integrated Interface Block for PCI Express Designs Switching Characteristics

Table 33: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade		Units
		-2	-1	
$F_{PCIECORE}$	Core clock maximum frequency	250	250	MHz
$F_{PCIEUSER}$	User clock maximum frequency	250	250	MHz

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-6 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the "Switching Characteristics," page 24.

Table 34: **Interface Performances**

Description	Speed Grade	
	-2	-1
Networking Applications		
SFI-4.1 (SDR LVDS Interface)		
SPI-4.2 (DDR LVDS Interface)		
Memory Interfaces		
DDR2		
DDR3		
QDR II + SRAM		
RLDRAM II		

Switching Characteristics

All values represented in this data sheet are based on the advanced speed specification (version 1.0). Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

Table 35 correlates the current status of each Virtex-6 device on a per speed grade basis.

Table 35: **Virtex-6 Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC6VCX75T	-2, -1		
XC6VCX130T	-2, -1		
XC6VCX195T	-2, -1		
XC6VCX240T	-2, -1		

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-6 devices.

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases. Table 36 lists the production released Virtex-6 family member, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE™ software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 36: **Virtex-6 Device Production Software and Speed Specification Release**

Device	Speed Grade Designations	
	-2	-1
XC6VCX75T		
XC6VCX130T		
XC6VCX195T		
XC6VCX240T		

Notes:
1. Blank entries indicate a device and/or speed grade in advance or preliminary status.

IOB Pad Input/Output/3-State Switching Characteristics

Table 37 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 38 summarizes the value of T_{IOTPHZ}. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 37: **IOB Switching Characteristics**

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-2	-1	-2	-1	-2	-1	
LVDS_25	1.15	1.15	1.68	1.68	1.68	1.68	ns
LVDSEXT_25	1.15	1.15	1.84	1.84	1.84	1.84	ns
HT_25	1.15	1.15	1.78	1.78	1.78	1.78	ns
BLVDS_25	1.15	1.15	1.67	1.67	1.67	1.67	ns
RSDS_25 (point to point)	1.15	1.15	1.68	1.68	1.68	1.68	ns
HSTL_I	1.12	1.12	1.73	1.73	1.73	1.73	ns
HSTL_II	1.12	1.12	1.74	1.74	1.74	1.74	ns
HSTL_III	1.12	1.12	1.71	1.71	1.71	1.71	ns
HSTL_I_18	1.12	1.12	1.75	1.75	1.75	1.75	ns
HSTL_II_18	1.12	1.12	1.81	1.81	1.81	1.81	ns
HSTL_III_18	1.12	1.12	1.71	1.71	1.71	1.71	ns
SSTL2_I	1.12	1.12	1.77	1.77	1.77	1.77	ns
SSTL2_II	1.12	1.12	1.72	1.72	1.72	1.72	ns
SSTL15	1.12	1.12	1.71	1.71	1.71	1.71	ns
LVCMOS25, Slow, 2 mA	0.70	0.70	6.01	6.01	6.01	6.01	ns
LVCMOS25, Slow, 4 mA	0.70	0.70	3.79	3.79	3.79	3.79	ns
LVCMOS25, Slow, 6 mA	0.70	0.70	3.08	3.08	3.08	3.08	ns
LVCMOS25, Slow, 8 mA	0.70	0.70	2.72	2.72	2.72	2.72	ns
LVCMOS25, Slow, 12 mA	0.70	0.70	2.17	2.17	2.17	2.17	ns
LVCMOS25, Slow, 16 mA	0.70	0.70	2.29	2.29	2.29	2.29	ns
LVCMOS25, Slow, 24 mA	0.70	0.70	2.02	2.02	2.02	2.02	ns
LVCMOS25, Fast, 2 mA	0.70	0.70	6.04	6.04	6.04	6.04	ns
LVCMOS25, Fast, 4 mA	0.70	0.70	3.82	3.82	3.82	3.82	ns
LVCMOS25, Fast, 6 mA	0.70	0.70	2.99	2.99	2.99	2.99	ns
LVCMOS25, Fast, 8 mA	0.70	0.70	2.65	2.65	2.65	2.65	ns
LVCMOS25, Fast, 12 mA	0.70	0.70	2.08	2.08	2.08	2.08	ns
LVCMOS25, Fast, 16 mA	0.70	0.70	2.13	2.13	2.13	2.13	ns
LVCMOS25, Fast, 24 mA	0.70	0.70	1.99	1.99	1.99	1.99	ns

Table 37: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-2	-1	-2	-1	-2	-1	
LVCMOS18, Slow, 2 mA	0.76	0.76	5.12	5.12	5.12	5.12	ns
LVCMOS18, Slow, 4 mA	0.76	0.76	3.39	3.39	3.39	3.39	ns
LVCMOS18, Slow, 6 mA	0.76	0.76	2.75	2.75	2.75	2.75	ns
LVCMOS18, Slow, 8 mA	0.76	0.76	2.51	2.51	2.51	2.51	ns
LVCMOS18, Slow, 12 mA	0.76	0.76	2.17	2.17	2.17	2.17	ns
LVCMOS18, Slow, 16 mA	0.76	0.76	2.14	2.14	2.14	2.14	ns
LVCMOS18, Fast, 2 mA	0.76	0.76	4.84	4.84	4.84	4.84	ns
LVCMOS18, Fast, 4 mA	0.76	0.76	3.11	3.11	3.11	3.11	ns
LVCMOS18, Fast, 6 mA	0.76	0.76	2.61	2.61	2.61	2.61	ns
LVCMOS18, Fast, 8 mA	0.76	0.76	2.28	2.28	2.28	2.28	ns
LVCMOS18, Fast, 12 mA	0.76	0.76	1.97	1.97	1.97	1.97	ns
LVCMOS18, Fast, 16 mA	0.76	0.76	1.98	1.98	1.98	1.98	ns
LVCMOS15, Slow, 2 mA	0.90	0.90	4.29	4.29	4.29	4.29	ns
LVCMOS15, Slow, 4 mA	0.90	0.90	3.10	3.10	3.10	3.10	ns
LVCMOS15, Slow, 6 mA	0.90	0.90	2.68	2.68	2.68	2.68	ns
LVCMOS15, Slow, 8 mA	0.90	0.90	2.23	2.23	2.23	2.23	ns
LVCMOS15, Slow, 12 mA	0.90	0.90	2.13	2.13	2.13	2.13	ns
LVCMOS15, Slow, 16 mA	0.90	0.90	2.04	2.04	2.04	2.04	ns
LVCMOS15, Fast, 2 mA	0.90	0.90	4.28	4.28	4.28	4.28	ns
LVCMOS15, Fast, 4 mA	0.90	0.90	2.78	2.78	2.78	2.78	ns
LVCMOS15, Fast, 6 mA	0.90	0.90	2.42	2.42	2.42	2.42	ns
LVCMOS15, Fast, 8 mA	0.90	0.90	2.11	2.11	2.11	2.11	ns
LVCMOS15, Fast, 12 mA	0.90	0.90	1.97	1.97	1.97	1.97	ns
LVCMOS15, Fast, 16 mA	0.90	0.90	1.96	1.96	1.96	1.96	ns
LVCMOS12, Slow, 2 mA	0.99	0.99	3.75	3.75	3.75	3.75	ns
LVCMOS12, Slow, 4 mA	0.99	0.99	2.93	2.93	2.93	2.93	ns
LVCMOS12, Slow, 6 mA	0.99	0.99	2.41	2.41	2.41	2.41	ns
LVCMOS12, Slow, 8 mA	0.99	0.99	2.25	2.25	2.25	2.25	ns
LVCMOS12, Fast, 2 mA	0.99	0.99	3.39	3.39	3.39	3.39	ns
LVCMOS12, Fast, 4 mA	0.99	0.99	2.51	2.51	2.51	2.51	ns
LVCMOS12, Fast, 6 mA	0.99	0.99	2.11	2.11	2.11	2.11	ns
LVCMOS12, Fast, 8 mA	0.99	0.99	2.02	2.02	2.02	2.02	ns
LVDCI_25	0.70	0.70	2.26	2.26	2.26	2.26	ns
LVDCI_18	0.76	0.76	2.47	2.47	2.47	2.47	ns
LVDCI_15	0.90	0.90	2.24	2.24	2.24	2.24	ns
LVDCI_DV2_25	0.70	0.70	2.01	2.01	2.01	2.01	ns
LVDCI_DV2_18	0.76	0.76	2.00	2.00	2.00	2.00	ns
LVDCI_DV2_15	0.90	0.90	1.91	1.91	1.91	1.91	ns

Table 37: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-2	-1	-2	-1	-2	-1	
LVPECL_25	1.15	1.15	1.65	1.65	1.65	1.65	ns
HSTL_I_12	1.12	1.12	1.78	1.78	1.78	1.78	ns
HSTL_I_DCI	1.12	1.12	1.66	1.66	1.66	1.66	ns
HSTL_II_DCI	1.12	1.12	1.68	1.68	1.68	1.68	ns
HSTL_II_T_DCI	1.12	1.12	1.66	1.66	1.66	1.66	ns
HSTL_III_DCI	1.12	1.12	1.62	1.62	1.62	1.62	ns
HSTL_I_DCI_18	1.12	1.12	1.68	1.68	1.68	1.68	ns
HSTL_II_DCI_18	1.12	1.12	1.62	1.62	1.62	1.62	ns
HSTL_II _T_DCI_18	1.12	1.12	1.68	1.68	1.68	1.68	ns
HSTL_III_DCI_18	1.12	1.12	1.69	1.69	1.69	1.69	ns
DIFF_HSTL_I_18	1.15	1.15	1.75	1.75	1.75	1.75	ns
DIFF_HSTL_I_DCI_18	1.15	1.15	1.68	1.68	1.68	1.68	ns
DIFF_HSTL_I	1.15	1.15	1.73	1.73	1.73	1.73	ns
DIFF_HSTL_I_DCI	1.15	1.15	1.66	1.66	1.66	1.66	ns
DIFF_HSTL_II_18	1.15	1.15	1.81	1.81	1.81	1.81	ns
DIFF_HSTL_II_DCI_18	1.15	1.15	1.62	1.62	1.62	1.62	ns
DIFF_HSTL_II _T_DCI_18	1.15	1.15	1.68	1.68	1.68	1.68	ns
DIFF_HSTL_II	1.15	1.15	1.74	1.74	1.74	1.74	ns
DIFF_HSTL_II_DCI	1.15	1.15	1.68	1.68	1.68	1.68	ns
SSTL2_I_DCI	1.12	1.12	1.70	1.70	1.70	1.70	ns
SSTL2_II_DCI	1.12	1.12	1.67	1.67	1.67	1.67	ns
SSTL2_II_T_DCI	1.12	1.12	1.70	1.70	1.70	1.70	ns
SSTL18_I	1.12	1.12	1.75	1.75	1.75	1.75	ns
SSTL18_II	1.12	1.12	1.67	1.67	1.67	1.67	ns
SSTL18_I_DCI	1.12	1.12	1.67	1.67	1.67	1.67	ns
SSTL18_II_DCI	1.12	1.12	1.63	1.63	1.63	1.63	ns
SSTL18_II_T_DCI	1.12	1.12	1.67	1.67	1.67	1.67	ns
SSTL15_T_DCI	1.12	1.12	1.68	1.68	1.68	1.68	ns
SSTL15_DCI	1.12	1.12	1.68	1.68	1.68	1.68	ns
DIFF_SSTL2_I	1.15	1.15	1.77	1.77	1.77	1.77	ns
DIFF_SSTL2_I_DCI	1.15	1.15	1.70	1.70	1.70	1.70	ns
DIFF_SSTL2_II	1.15	1.15	1.72	1.72	1.72	1.72	ns
DIFF_SSTL2_II_DCI	1.15	1.15	1.67	1.67	1.67	1.67	ns
DIFF_SSTL2_II_T_DCI	1.15	1.15	1.70	1.70	1.70	1.70	ns
DIFF_SSTL18_I	1.15	1.15	1.75	1.75	1.75	1.75	ns
DIFF_SSTL18_I_DCI	1.15	1.15	1.67	1.67	1.67	1.67	ns
DIFF_SSTL18_II	1.15	1.15	1.67	1.67	1.67	1.67	ns
DIFF_SSTL18_II_DCI	1.15	1.15	1.63	1.63	1.63	1.63	ns

Table 37: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-2	-1	-2	-1	-2	-1	
DIFF_SSTL18_II_T_DCI	1.15	1.15	1.67	1.67	1.67	1.67	ns
DIFF_SSTL15	1.12	1.12	1.71	1.71	1.71	1.71	ns
DIFF_SSTL15_DCI	1.12	1.12	1.68	1.68	1.68	1.68	ns
DIFF_SSTL15_T_DCI	1.12	1.12	1.68	1.68	1.68	1.68	ns

Table 38: **IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})**

Symbol	Description	Speed Grade		Units
		-2	-1	
T_{IOTPHZ}	T input to Pad high-impedance	2	2	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 39 shows the test setup parameters used for measuring input delay.

Table 39: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L (1,2)	V_H (1,2)	V_{MEAS} (1,4,5)	V_{REF} (1,3,5)
LVCMOS, 2.5V	LVCMOS25	0	2.5	1.25	–
LVCMOS, 1.8V	LVCMOS18	0	1.8	0.9	–
LVCMOS, 1.5V	LVCMOS15	0	1.5	0.75	–
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL, Class III	HSTL_III	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.08
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	V_{REF} – 1.00	V_{REF} + 1.00	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	0(6)	
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	0(6)	
HT (HyperTransport), 2.5V	LDT_25	0.6 – 0.125	0.6 + 0.125	0(6)	

Notes:
1. The input delay measurement methodology parameters for LVDCI are the same for LVCMOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 16.
6. The value given is the differential input voltage.

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 16 and Figure 17.

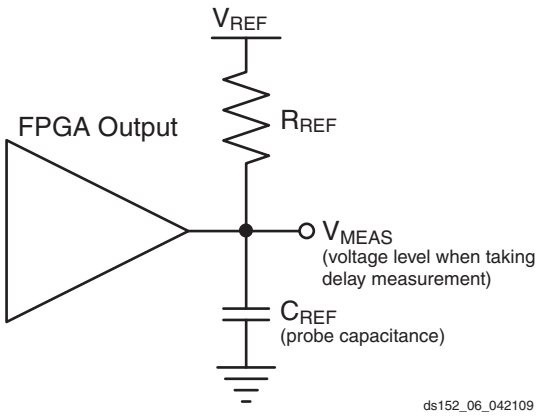

Figure 16: **Single Ended Test Setup**

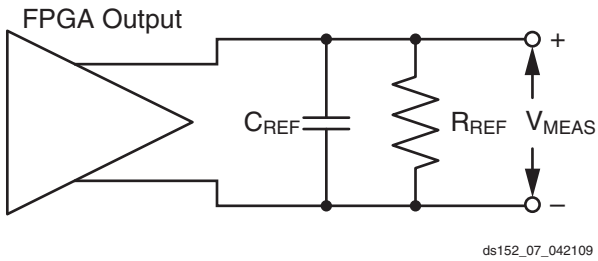

Figure 17: **Differential Test Setup**

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 40.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 40: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.2V	LVCMOS12	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	100	0	0[4]	1.2
LVDSEXT (LVDS Extended Mode), 2.5V	LVDS_25	100	0	0[4]	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0[4]	0

Table 40: **Output Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
HT (HyperTransport), 2.5V	LDT_25	100	0	0[4]	0.6
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	100	0	0[4]	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25, HSLVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V_{REF}	0.75
HSTL, Class III, with DCI	HSTL_III_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V_{REF}	0.9
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termi.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V_{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V_{REF}	1.25

Notes:
1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. Per PCI specifications.
3. Per PCI-X specifications.
4. The value given is the differential input voltage.

Input/Output Logic Switching Characteristics

Table 41: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup/Hold				
T_{ICE1CK}/T_{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.27/0.05	0.27/0.05	ns
T_{ISRCK}/T_{ICKSR}	SR pin Setup/Hold with respect to CLK	0.96/–0.09	0.96/–0.09	ns
T_{IDOCK}/T_{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	0.10/0.54	0.10/0.54	ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)	0.14/0.41	0.14/0.39	ns
Combinatorial				
T_{IDI}	D pin to O pin propagation delay, no Delay	0.20	0.20	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IODELAY)	0.25	0.25	ns
Sequential Delays				
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.64	0.64	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY)	0.68	0.68	ns
T_{ICKQ}	CLK to Q outputs	0.71	0.71	ns
T_{RQ_ILOGIC}	SR pin to OQ/TQ out	1.15	1.15	ns
T_{GSRQ_ILOGIC}	Global Set/Reset to Q outputs	10.51	10.51	ns
Set/Reset				
T_{RPW_ILOGIC}	Minimum Pulse Width, SR inputs	1.30	1.30	ns, Min

Table 42: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup/Hold				
T_{ODCK}/T_{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.51/–0.11	0.51/–0.11	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.09/–0.05	0.09/–0.05	ns
T_{OSRCK}/T_{OCKSR}	SR pin Setup/Hold with respect to CLK	0.70/–0.29	0.70/–0.29	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.51/–0.10	0.51/–0.10	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.10/–0.05	0.10/–0.05	ns
Combinatorial				
T_{DOQ}	D1 to OQ out or T1 to TQ out	1.01	1.01	ns
Sequential Delays				
T_{OCKQ}	CLK to OQ/TQ out	0.71	0.71	ns
T_{RQ}	SR pin to OQ/TQ out	1.05	1.05	ns
T_{GSRQ}	Global Set/Reset to Q outputs	10.51	10.51	ns
Set/Reset				
T_{RPW}	Minimum Pulse Width, SR inputs	1.30	1.30	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 43: **ISERDES Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup/Hold for Control Lines				
$T_{ISCCK\_BITSLIP}/T_{ISCKC\_BITSLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV	0.09/0.17	0.09/0.17	ns
$T_{ISCCK\_CE}/T_{ISCKC\_CE}$(2)	CE pin Setup/Hold with respect to CLK (for CE1)	0.21/0.58	0.21/0.58	ns
$T_{ISCCK\_CE2}/T_{ISCKC\_CE2}$(2)	CE pin Setup/Hold with respect to CLKDIV (for CE2)	–0.06/0.31	–0.06/0.31	ns
Setup/Hold for Data Lines				
T_{ISDCK_D}/T_{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.04/0.14	0.04/0.14	ns
$T_{ISDCK\_DDLY}/T_{ISCKD\_DDLY}$	DDLY pin Setup/Hold with respect to CLK (using IODELAY)	0.08/0.09	0.08/0.09	ns
$T_{ISDCK\_D\_DDR}/T_{ISCKD\_D\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode	0.04/0.14	0.04/0.14	ns
$T_{ISDCK\_DDLY\_DDR}$ $T_{ISCKD\_DDLY\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY)	0.08/0.09	0.08/0.09	ns
Sequential Delays				
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.56	0.56	ns
Propagation Delays				
T_{ISDO_DO}	D input to DO output pin	0.25	0.25	ns

Notes:
1. Recorded at 0 tap value.
2. T_{ISCCK_CE2} and T_{ISCKC_CE2} are reported as $T_{ISCCK\_CE}/T_{ISCKC\_CE}$ in TRACE report.

Output Serializer/Deserializer Switching Characteristics

Table 44: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup/Hold				
T_{OSDCK_D}/T_{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	0.30/–0.12	0.30/–0.12	ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input Setup/Hold with respect to CLK	0.51/–0.08	0.51/–0.08	ns
$T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1)	T input Setup/Hold with respect to CLKDIV	0.31/–0.08	0.31/–0.08	ns
$T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$	OCE input Setup/Hold with respect to CLK	0.09/–0.05	0.09/–0.05	ns
T_{OSCCK_S}	SR (Reset) input Setup with respect to CLKDIV	0.07	0.07	ns
$T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$	TCE input Setup/Hold with respect to CLK	0.10/–0.05	0.10/–0.05	ns
Sequential Delays				
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.82	0.82	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.82	0.82	ns
Combinatorial				
T_{OSDO_TTQ}	T input to TQ Out	0.97	0.97	ns

Notes:
1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

Input/Output Delay Switching Characteristics

Table 45: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
IDELAYCTRL				
T_{DLYCCO_RDY}	Reset to Ready for IDELAYCTRL	3	3	µs
$F_{IDELAYCTRL\_REF}$	REFCLK frequency	200	200	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum Reset pulse width	50	50	ns
IODELAY				
$T_{IDELAYRESOLUTION}$	IODELAY Chain Delay Resolution	1/(32 x 2 x F_{REF})		ps
$T_{IDELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern. (1)	0	0	ps
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23).(2)	±5	±5	ps
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23).(3)	±9	±9	ps
$T_{IODELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IODELAY	320	320	MHz
T_{IODCCK_CE} / T_{IODCKC_CE}	CE pin Setup/Hold with respect to CK	0.65/–0.09	0.65/–0.09	ns
T_{IODCK_INC}/ T_{IODCKC_INC}	INC pin Setup/Hold with respect to CK	0.31/–0.00	0.31/–0.00	ns
T_{IODCCK_RST}/ T_{IODCKC_RST}	RST pin Setup/Hold with respect to CK	0.69/–0.08	0.69/–0.08	ns
T_{IODDO_T}	TSCONTROL delay to MUXE/MUXF switching and through IODELAY	Note 4	Note 4	ps
$T_{IODDO\_IDATAIN}$	Propagation delay through IODELAY	Note 4	Note 4	ps
$T_{IODDO\_ODATAIN}$	Propagation delay through IODELAY	Note 4	Note 4	ps

Notes:
1. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
2. When HIGH_PERFORMANCE mode is set to TRUE
3. When HIGH_PERFORMANCE mode is set to FALSE.
4. Delay depends on IODELAY tap setting. See TRACE report for actual values.

CLB Switching Characteristics

Table 46: **CLB Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Combinatorial Delays				
T_{ILO}	An – Dn LUT address to A	0.08	0.09	ns, Max
	An – Dn LUT address to AMUX/CMUX	0.23	0.26	ns, Max
	An – Dn LUT address to BMUX_A	0.37	0.42	ns, Max
T_{ITO}	An – Dn inputs to A – D Q outputs	0.79	0.91	ns, Max
T_{AXA}	AX inputs to AMUX output	0.42	0.48	ns, Max
T_{AXB}	AX inputs to BMUX output	0.47	0.53	ns, Max
T_{AXC}	AX inputs to CMUX output	0.52	0.60	ns, Max
T_{AXD}	AX inputs to DMUX output	0.55	0.63	ns, Max
T_{BXB}	BX inputs to BMUX output	0.39	0.45	ns, Max

Table 46: **CLB Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade		Units
		-2	-1	
T_{BXD}	BX inputs to DMUX output	0.50	0.58	ns, Max
T_{CXB}	CX inputs to CMUX output	0.34	0.38	ns, Max
T_{CXD}	CX inputs to DMUX output	0.40	0.45	ns, Max
T_{DXD}	DX inputs to DMUX output	0.38	0.44	ns, Max
T_{OPCYA}	An input to COUT output	0.42	0.49	ns, Max
T_{OPCYB}	Bn input to COUT output	0.42	0.48	ns, Max
T_{OPCYC}	Cn input to COUT output	0.35	0.40	ns, Max
T_{OPCYD}	Dn input to COUT output	0.33	0.38	ns, Max
T_{AXCY}	AX input to COUT output	0.33	0.38	ns, Max
T_{BXCY}	BX input to COUT output	0.28	0.32	ns, Max
T_{CXCY}	CX input to COUT output	0.20	0.23	ns, Max
T_{DXCY}	DX input to COUT output	0.19	0.22	ns, Max
T_{BYP}	CIN input to COUT output	0.08	0.09	ns, Max
T_{CINA}	CIN input to AMUX output	0.28	0.32	ns, Max
T_{CINB}	CIN input to BMUX output	0.29	0.34	ns, Max
T_{CINC}	CIN input to CMUX output	0.30	0.34	ns, Max
T_{CIND}	CIN input to DMUX output	0.33	0.38	ns, Max
Sequential Delays				
T_{CKO}	Clock to AQ – DQ outputs	0.39	0.44	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK				
T_{DICK}/T_{CKDI}	A – D input to CLK on A – D Flip Flops	0.43/0.19	0.49/0.22	ns, Min
$T_{CECK\_CLB}/T_{CKCE\_CLB}$	CE input to CLK on A – D Flip Flops	0.32/–0.02	0.37/–0.02	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D Flip Flops	0.51/–0.09	0.59/–0.09	ns, Min
T_{CINCK}/T_{CKCIN}	CIN input to CLK on A – D Flip Flops	0.23/0.15	0.27/0.17	ns, Min
Set/Reset				
T_{SRMIN}	SR input minimum pulse width	0.97	0.97	ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops	0.68	0.78	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	0.59	0.67	ns, Max
F_{TOG}	Toggle frequency (for export control)	1098.00	1098.00	MHz

Notes:
1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. These items are of interest for Carry Chain applications.

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 47: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Sequential Delays				
T_{SHCKO}	Clock to A – B outputs	1.36	1.56	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	1.71	1.96	ns, Max
Setup and Hold Times Before/After Clock CLK				
T_{DS}/T_{DH}	A – D inputs to CLK	0.87/0.22	1.00/0.26	ns, Min
T_{AS}/T_{AH}	Address An inputs to clock	0.27/0.70	0.31/0.80	ns, Min
T_{WS}/T_{WH}	WE input to clock	0.40/–0.01	0.45/0.00	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.41/–0.02	0.47/–0.01	ns, Min
Clock CLK				
T_{MPW}	Minimum pulse width	1.04	1.20	ns, Min
T_{MCP}	Minimum clock period	2.08	2.40	ns, Min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 48: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Sequential Delays				
T_{REG}	Clock to A – D outputs	1.58	1.82	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output	1.93	2.22	ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output	1.55	1.78	ns, Max
Setup and Hold Times Before/After Clock CLK				
T_{WS}/T_{WH}	WE input	0.08/–0.01	0.09/0.00	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.09/–0.02	0.11/–0.01	ns, Min
T_{DS}/T_{DH}	A – D inputs to CLK	0.93/0.24	1.07/0.28	ns, Min
Clock CLK				
T_{MPW}	Minimum pulse width	0.89	1.02	ns, Min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Block RAM and FIFO Switching Characteristics

Table 49: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Block RAM and FIFO Clock-to-Out Delays				
T_{RCKO_DO} and $T_{RCKO\_DO\_REG}$(1)	Clock CLK to DOUT output (without output register)(2)(3)	2.08	2.39	ns, Max
	Clock CLK to DOUT output (with output register)(4)(5)	0.75	0.86	ns, Max
$T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$	Clock CLK to DOUT output with ECC (without output register)(2)(3)	3.30	3.79	ns, Max
	Clock CLK to DOUT output with ECC (with output register)(4)(5)	0.86	0.98	ns, Max
T_{RCKO_CASC} and $T_{RCKO\_CASC\_REG}$	Clock CLK to DOUT output with Cascade (without output register)(2)	3.18	3.65	ns, Max
	Clock CLK to DOUT output with Cascade (with output register)(4)	1.58	1.81	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs(6)	0.91	1.05	ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointers outputs(7)	0.91	1.05	ns, Max
$T_{RCKO\_RDCOUNT}$	Clock CLK to FIFO Read Counter	1.09	1.25	ns, Max
$T_{RCKO\_WRCOUNT}$	Clock CLK to FIFO Write Counter	1.09	1.25	ns, Max
$T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$	Clock CLK to BITERR (with output register)	0.76	0.87	ns, Max
	Clock CLK to BITERR (without output register)	2.84	3.26	ns, Max
$T_{RCKO\_PARITY\_ECC}$	Clock CLK to ECCPARITY in standard ECC mode	1.48	1.70	ns, Max
	Clock CLK to ECCPARITY in ECC encode only mode	1.06	1.21	ns, Max
$T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$	Clock CLK to RDADDR output with ECC (without output register)	0.90	1.03	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.92	1.06	ns, Max
Setup and Hold Times Before/After Clock CLK				
$T_{RCCK\_ADDR}/T_{RCKC\_ADDR}$	ADDR inputs(8)	0.62/0.32	0.72/0.37	ns, Min
T_{RDCK_DI}/T_{RCKD_DI}	DIN inputs(9)	1.11/0.34	1.28/0.39	ns, Min
$T_{RDCK\_DI\_ECC}/T_{RCKD\_DI\_ECC}$	DIN inputs with block RAM ECC in standard mode(9)	0.59/0.34	0.68/0.39	ns, Min
	DIN inputs with block RAM ECC encode only(9)	0.85/0.34	0.97/0.39	ns, Min
	DIN inputs with FIFO ECC in standard mode(9)	1.02/0.34	1.17/0.39	ns, Min
	DIN inputs with FIFO ECC encode only(9)			ns, Min
$T_{RCCK\_CLK}/T_{RCKC\_CLK}$	Inject single/double bit error in ECC mode	1.20/0.29	1.38/0.33	ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	Block RAM Enable (EN) input	0.41/0.30	0.47/0.34	ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.22/0.31	0.25/0.35	ns, Min
$T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$	Synchronous RSTREG input	0.28/0.26	0.32/0.29	ns, Min
$T_{RCCK\_RSTRAM}/T_{RCKC\_RSTRAM}$	Synchronous RSTRAM input	0.41/0.27	0.47/0.31	ns, Min
T_{RCCK_WE}/T_{RCKC_WE}	Write Enable (WE) input (Block RAM only)	0.52/0.22	0.60/0.25	ns, Min
$T_{RCCK\_WREN}/T_{RCKC\_WREN}$	WREN FIFO inputs	0.55/0.30	0.64/0.34	ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	RDEN FIFO inputs	0.55/0.30	0.63/0.34	ns, Min
Reset Delays				
T_{RCO_FLAGS}	Reset RST to FIFO Flags/Pointers(10)	1.10	1.27	ns, Max
$T_{RCCK\_RST}/T_{RCKC\_RST}$	FIFO reset timing(11)			ns, Min

Table 49: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade		Units
		-2	-1	
Maximum Frequency				
F_{MAX}	Block RAM(12)	400	350	MHz
$F_{MAX\_CASCADE}$	Block RAM in cascade configuration(12)	400	347	MHz
F_{MAX_FIFO}	FIFO in all modes	400	350	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	325	282	MHz

Notes:

1. TRACE will report all of these parameters as T_{RCKO_DO}.
2. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, T_{RCKO_WRERR}.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. T_{RCKO_DI} includes both A and B inputs as well as the parity inputs of A and B.
10. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. The FIFO reset must be asserted for at least three positive clock edges.
12. In Read First mode, the maximum frequencies are 50 MHz lower than specified in this table.

DSP48E1 Switching Characteristics

Table 50: **DSP48E1 Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup and Hold Times of Data/Control Pins to the Input Register Clock				
$T_{DSPDCK\_\{A, ACIN; B, BCIN\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{A, ACIN; B, BCIN\}\_\{AREG; BREG\}}$	{A, ACIN, B, BCIN} input to {A, B} register CLK	0.28/0.34	0.32/0.39	ns
$T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$	C input to C register CLK	0.16/0.24	0.18/0.27	ns
$T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$	D input to D register CLK			ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock				
$T_{DSPDCK\_\{A, ACIN, B, BCIN\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, ACIN, B, BCIN\}\_PREG\_MULT}$	{A, ACIN, B, BCIN} input to M register CLK	3.22/–0.04	3.70/–0.04	ns
$T_{DSPDCK\_\{A, D\}\_ADREG}$/ $T_{DSPCKD–\{A, D\}\_ADREG}$	{A, D} input to AD register CLK			ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock				
$T_{DSPDCK\_\{A, ACIN, B, BCIN\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, ACIN, B, BCIN\}\_PREG\_MULT}$	{A, ACIN, B, BCIN} input to P register CLK using multiplier	4.94/–0.04	5.68/–0.04	ns
$T_{DSPDCK\_D\_DREG\_MULT}$/ $T_{DSPCKD\_D\_DREG\_MULT}$	D input to P register CLK			ns
$T_{DSPDCK\_\{A, ACIN, B, BCIN\}\_PREG}$/ $T_{DSPCKD\_\{A, ACIN, B, BCIN\}\_PREG}$	{A, ACIN, B, BCIN} input to P register CLK not using multiplier	1.89/–0.04	2.18/–0.04	ns
$T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK	1.64/0.04	1.89/0.05	ns
$T_{DSPDCK\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_PREG}$/ $T_{DSPCKD\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_PREG}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to P register CLK	1.56/–0.04	1.79/–0.05	ns
Setup and Hold Times of the CE Pins				
$T_{DSPDCK\_\{CEA; CEB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{CEA; CEB\}\_\{AREG; BREG\}}$	{CEA; CEB} input to {A; B} register CLK	0.12/0.25	0.14/0.29	ns
$T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$	CEC input to C register CLK	0.13/0.23	0.16/0.27	ns
$T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$	CED input to D register CLK			ns
$T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$	CEM input to M register CLK	0.15/0.25	0.18/0.28	ns
$T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$	CEP input to P register CLK	0.38/0.03	0.44/0.03	ns
Setup and Hold Times of the RST Pins				
$T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK	0.38/0.22	0.43/0.25	ns
$T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK	0.23/0.09	0.27/0.11	ns
$T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK			ns
$T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.26/0.30	0.30/0.35	ns
$T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$	RSTP input to P register CLK	0.33/0.05	0.38/0.06	ns

Table 50: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade		Units
		-2	-1	
Combinatorial Delays from Input Pins to Output Pins				
$T_{DSPDO\_\{A, B\}\_\{P, CARRYOUT\}\_MULT}$	{A, B} input to {P, CARRYOUT} output using multiplier	5.08	5.84	ns
$T_{DSPDO\_D\_\{P, CARRYOUT\}\_MULT}$	D input to {P, CARRYOUT} output using multiplier			ns
$T_{DSPDO\_\{A, B\}\_\{P, CARRYOUT\}}$	{A, B} input to {P, CARRYOUT} output not using multiplier	2.07	2.38	ns
$T_{DSPDO\_\{C, CARRYIN\}\_\{P, CARRYOUT\}}$	{C, CARRYIN} input to {P, CARRYOUT} output	1.83	2.10	ns
Combinatorial Delays from Input Pins to Cascading Output Pins				
$T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.65	0.75	ns
$T_{DSPDO\_\{A, B\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MULT}$	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	5.24	6.03	ns
$T_{DSPDO\_D\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MULT}$	D input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier			ns
$T_{DSPDO\_\{A, B\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}$	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	2.19	2.52	ns
$T_{DSPDO\_\_\{C, CARRYIN\}\_\{PCOUT, CARRYCASCOUT,MULTSIGNOUT\}}$	{C, CARRYIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.95	2.25	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins				
$T_{DSPDO\_\{ACIN, BCIN\}\_\{P, CARRYOUT\}\_MULT}$	{ACIN, BCIN} input to {P, CARRYOUT} output using multiplier	4.97	5.72	ns
$T_{DSPDO\_\{ACIN, BCIN\}\_\{P, CARRYOUT}$	{ACIN, BCIN} input to {P, CARRYOUT} output not using multiplier	1.92	2.21	ns
$T_{DSPDO\_\{ACIN; BCIN\}\_\{ACOUT; BCOUT\}}$	{ACIN, BCIN} input to {ACOUT, BCOUT} output	0.49	0.57	ns
$T_{DSPDO\_\{ACIN, BCIN\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MULT}$	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	5.10	5.86	ns
$T_{DSPDO\_\{ACIN, BCIN\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}$	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	2.05	2.35	ns
$T_{DSPDO\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_\{P, CARRYOUT\}}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {P, CARRYOUT} output	1.60	1.83	ns
$T_{DSPDO\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.72	1.98	ns
Clock to Outs from Output Register Clock to Output Pins				
$T_{DSPCKO\_\{P, CARRYOUT\}\_PREG}$	CLK (PREG) to {P, CARRYOUT} output	0.50	0.57	ns
$T_{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_PREG}$	CLK (PREG) to {CARRYCASCOUT, PCOUT, MULTSIGNOUT} output	0.66	0.76	ns

Table 50: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade		Units
		-2	-1	
Clock to Outs from Pipeline Register Clock to Output Pins				
$T_{DSPCKO\_\{P, CARRYOUT\}\_MREG}$	CLK (MREG) to {P, CARRYOUT} output	2.30	2.65	ns
$T_{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MREG}$	CLK (MREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	2.43	2.79	ns
$T_{DSPCKO\_\{P, CARRYOUT\}\_ADREG\_MULT}$	CLK (ADREG) to {P, CARRYOUT} output			ns
$T_{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_ADREG\_MULT}$	CLK (ADREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output			ns
Clock to Outs from Input Register Clock to Output Pins				
$T_{DSPCKO\_\{P, CARRYOUT\}\_\{AREG, BREG\}\_MULT}$	CLK (AREG, BREG) to {P, CARRYOUT} output using multiplier	5.36	6.16	ns
$T_{DSPCKO\_\{P, CARRYOUT\}\_\{AREG, BREG\}}$	CLK (AREG, BREG) to {P, CARRYOUT} output not using multiplier	2.27	2.61	ns
$T_{DSPCKO\_\{P, CARRYOUT\}\_CREG}$	CLK (CREG) to {P, CARRYOUT} output	2.27	2.61	ns
$T_{DSPCKO\_\{P, CARRYOUT\}\_DREG\_MULT}$	CLK (DREG) to {P, CARRYOUT} output			ns
Clock to Outs from Input Register Clock to Cascading Output Pins				
$T_{DSPCKO\_\{ACOUT; BCOUT\}\_\{AREG; BREG\}}$	CLK (AREG, BREG) to {P, CARRYOUT} output	0.89	1.02	ns
$T_{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_\{AREG, BREG\}\_MULT}$	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	5.49	6.31	ns
$T_{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_\{AREG, BREG\}}$	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	2.40	2.76	ns
$T_{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_DREG\_MULT}$	CLK (DREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier			ns
$T_{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_CREG}$	CLK (CREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	2.40	2.76	ns
Maximum Frequency				
F_{MAX}	With all registers used	350	275	MHz
F_{MAX_PATDET}	With pattern detector	350	275	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	262	227	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	248	215	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG}$	Without ADREG			MHz
$F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$	Without ADREG with pattern detect			MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)			MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect			MHz

Configuration Switching Characteristics

Table 51: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Power-up Timing Characteristics				
T_{PL}	Program Latency		3	ms, Max
T_{POR}	Power-on-Reset			ms, Min/Max
T_{ICCK}	CCLK (output) delay			ns, Min
$T_{PROGRAM}$	Program Pulse Width		250	ns, Min
Master/Slave Serial Mode Programming Switching(1)				
T_{DCCK}/T_{CCKD}	DIN Setup/Hold, slave mode		4.0/0.0	ns, Min
T_{DSCCK}/T_{SCCKD}	DIN Setup/Hold, master mode		4.0/0.0	ns, Min
T_{CCO}	DOUT		6	ns, Max
F_{MCCK}	Maximum Frequency, master mode with respect to nominal CCLK.		100	MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance, master mode with respect to nominal CCLK.			%
F_{MSCCK}	Slave mode external CCLK	100	100	MHz
SelectMAP Mode Programming Switching(1)				
T_{SMDCCK}/T_{SMCCKD}	SelectMAP Data Setup/Hold		4.0/0.0	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CS_B Setup/Hold		4.0/0.0	ns, Min
T_{SMCCKW}/T_{SMWCCK}	RDWR_B Setup/Hold		9.0/0.0	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330 Ω pull-up resistor required)		7	ns, Min
T_{SMCO}	CCLK to DATA out in readback		8	ns, Max
T_{SMCKBY}	CCLK to BUSY out in readback		6	ns, Max
F_{SMCCK}	Maximum Frequency with respect to nominal CCLK.	100	100	MHz, Max
F_{RBCCK}	Maximum Readback Frequency with respect to nominal CCLK			MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance with respect to nominal CCLK.			%
Boundary-Scan Port Timing Specifications				
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI Setup time before TCK/ Hold time after TCK		2.5/2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output valid		6	ns, Max
F_{TCK}	Maximum configuration TCK clock frequency	66	66	MHz, Max
F_{TCKB}	Maximum boundary-scan TCK clock frequency	66	66	MHz, Max
BPI Master Flash Mode Programming Switching				
T_{BPICCO}(4)	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge		4	ns
T_{BPIDCC}/T_{BPICCD}	Setup/Hold on D[15:0] data input pins		4.0/0.0	ns
$T_{INITADDR}$	Minimum period of initial ADDR[25:0] address cycles		3	CCLK cycles
SPI Master Flash Mode Programming Switching				
$T_{SPIDCC}/T_{SPIDCCD}$	DIN Setup/Hold before/after the rising CCLK edge		2.5/0.0	ns
T_{SPICCM}	MOSI clock to out		4	ns

Table 51: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade		Units
		-2	-1	
$T_{SPICCFC}$	FCS_B clock to out			ns
$T_{FSINIT}/T_{FSINITH}$	FS[2:0] to INIT_B rising edge Setup and Hold			µs
CCLK Output (Master Modes)				
T_{MCCKL}	Master CCLK clock minimum duty cycle Low		45	%, Min
T_{MCCKH}	Master CCLK clock minimum duty cycle High		55	%, Max
CCLK Input (Slave Modes)				
T_{SCCKL}	Slave CCLK clock minimum Low time		2.5	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time		2.5	ns, Min
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK				
F_{DCK}	Maximum frequency for DCLK	200	200	MHz
$T_{MMCMDCK\_DADDR}/T_{MMCMCKD\_DADDR}$	DADDR Setup/Hold	1.63/0.00	1.63/0.00	ns
$T_{MMCMDCK\_DI}/T_{MMCMCKD\_DI}$	DI Setup/Hold	1.63/0.00	1.63/0.00	ns
$T_{MMCMDCK\_DEN}/T_{MMCMCKD\_DEN}$	DEN Setup/Hold time	1.63/0.00	1.63/0.00	ns
$T_{MMCMDCK\_DWE}/T_{MMCMCKD\_DWE}$	DWE Setup/Hold time	1.63/0.00	1.63/0.00	ns
$T_{MMCMCKO\_DO}$	CLK to out of DO(3)	3.64	3.64	ns
$T_{MMCMCKO\_DRDY}$	CLK to out of DRDY	0.38	0.38	ns

Notes:
1. Maximum frequency and setup/hold timing parameters are for 2.5V configuration voltage.
2. To support longer delays in configuration, use the design solutions described in *Virtex-6 FPGA SelectIO Resources User Guide*.
3. DO will hold until next DRP operation.
4. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

Clock Buffers and Networks

Table 52: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Devices	Speed Grade		Units
			-2	-1	
$T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1)	CE pins Setup/Hold	All	0.15/0.00	0.15/0.00	ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins Setup/Hold	All	0.15/0.00	0.15/0.00	ns
T_{BCCKO_O}(2)	BUFGCTRL delay from I0/I1 to O	XC6VCX75T	0.09	0.09	ns
		XC6VCX130T	0.09	0.09	ns
		XC6VCX195T	0.09	0.09	ns
		XC6VCX240T	0.09	0.09	ns
Maximum Frequency					
F_{MAX}	Global clock tree (BUFG)	XC6VCX75T	700	700	MHz
		XC6VCX130T	700	700	MHz
		XC6VCX195T	700	700	MHz
		XC6VCX240T	700	700	MHz

Notes:
1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX_VIRTEX4 primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 53: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade		Units
		-2	-1	
T_{BIOCKO_O}	Clock to out delay from I to O	0.19	0.19	ns
Maximum Frequency				
F_{MAX}	I/O clock tree (BUFIO)	710	710	MHz

Table 54: **Regional Clock Switching Characteristics (BUFR)**

Symbol	Description	Devices	Speed Grade		Units
			-2	-1	
T_{BRCKO_O}	Clock to out delay from I to O	XC6VCX75T	0.75	0.75	ns
		XC6VCX130T	0.75	0.75	ns
		XC6VCX195T	0.75	0.75	ns
		XC6VCX240T	0.75	0.75	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	XC6VCX75T	0.37	0.37	ns
		XC6VCX130T	0.37	0.37	ns
		XC6VCX195T	0.37	0.37	ns
		XC6VCX240T	0.37	0.37	ns
T_{BRDO_O}	Propagation delay from CLR to O	All	0.83	0.83	ns
Maximum Frequency					
F_{MAX}	Regional clock tree (BUFR)	All	300	300	MHz

Table 55: **Horizontal Clock Buffer Switching Characteristics (BUFH)**

Symbol	Description	Devices	Speed Grade		Units
			-2	-1	
T_{BHCKO_O}	BUFH delay from I to O	All	0.13	0.13	ns
$T_{BHCCK\_CE}/T_{BHCKC\_CE}$	CE pin Setup and Hold	All	0.05/0.05	0.05/0.05	ns
Maximum Frequency					
F_{MAX}	Horizontal clock buffer (BUFH)	All	700	700	MHz

MMCM Switching Characteristics

Table 56: **MMCM Specification**

Symbol	Description	Speed Grade		Units
		-2	-1	
F_{INMAX}	Maximum Input Clock Frequency	700	700	MHz
F_{INMIN}	Minimum Input Clock Frequency	10	10	MHz
$F_{INJITTER}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max		
F_{INDUTY}	Allowable Input Duty Cycle: 10—49 MHz	25/75		%
	Allowable Input Duty Cycle: 50—199 MHz	30/70		%
	Allowable Input Duty Cycle: 200—399 MHz	35/65		%
	Allowable Input Duty Cycle: 400—499 MHz	40/60		%
	Allowable Input Duty Cycle: >500 MHz	45/55		%
F_{MIN_PSCLK}	Minimum Dynamic Phase Shift Clock Frequency	0.01	0.01	MHz
F_{MAX_PSCLK}	Maximum Dynamic Phase Shift Clock Frequency	450	450	MHz
F_{VCOMIN}	Minimum MMCM VCO Frequency	400	400	MHz
F_{VCOMAX}	Maximum MMCM VCO Frequency	1200	1200	MHz
$F_{BANDWIDTH}$	Low MMCM Bandwidth at Typical(1)	1.00	1.00	MHz
	High MMCM Bandwidth at Typical(1)	4.00	4.00	MHz
$T_{STATPHAOFFSET}$	Static Phase Offset of the MMCM Outputs	0.12	0.12	ps
$T_{OUTJITTER}$	MMCM Output Jitter(2)	Note 1		
$T_{OUTDUTY}$	MMCM Output Clock Duty Cycle Precision(3)	0.20	0.20	ps
$T_{LOCKMAX}$	MMCM Maximum Lock Time	100	100	µs
F_{OUTMAX}	MMCM Maximum Output Frequency	700	700	MHz
F_{OUTMIN}	MMCM Minimum Output Frequency(4)	3.13	3.13	MHz
$T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max		
$RST_{MINPULSE}$	Minimum Reset Pulse Width	5.00	5.00	ns
F_{PFDMAX}	Maximum Frequency at the Phase Frequency Detector	550	550	MHz
F_{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	10.00	10.00	MHz
$T_{FBDELAY}$	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle		
$T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$	Setup and Hold of Phase Shift Enable	1.04/0.00	1.04/0.00	ns
$T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$	Setup and Hold of Phase Shift Increment/Decrement	1.04/0.00	1.04/0.00	ns
$T_{MMCMCKO\_PSDONE}$	Phase Shift Clock-to-Out of PSDONE	0.38	0.38	ns

Notes:
1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. Values for this parameter are available in the Architecture Wizard.
3. Includes global clock buffer.
4. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

Virtex-6 CXT Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 57. Values are expressed in nanoseconds unless otherwise noted.

Table 57: **Global Clock Input to Output Delay Without MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *without* MMCM.					
T_{ICKOF}	Global Clock input and OUTFF *without* MMCM	XC6VCX75T	5.84	5.84	ns
		XC6VCX130T	5.95	5.95	ns
		XC6VCX195T	6.08	6.08	ns
		XC6VCX240T	6.08	6.08	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 58: **Global Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* MMCM.					
$T_{ICKOFMMCMGC}$	Global Clock Input and OUTFF *with* MMCM	XC6VCX75T	4.45	4.45	ns
		XC6VCX130T	4.56	4.56	ns
		XC6VCX195T	4.56	4.56	ns
		XC6VCX240T	4.56	4.56	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 59: **Clock-Capable Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
LVCMOS25 Clock-capable Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* MMCM.					
$T_{ICKOFMMCMCC}$	Clock-capable Clock Input and OUTFF *with* MMCM	XC6VCX75T	4.32	4.32	ns
		XC6VCX130T	4.43	4.43	ns
		XC6VCX195T	4.43	4.43	ns
		XC6VCX240T	4.43	4.43	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Virtex-6 CXT Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 60. Values are expressed in nanoseconds unless otherwise noted.

Table 60: **Global Clock Input Setup and Hold Without MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)					
T_{PSFD}/ T_{PHFD}	Full Delay (Legacy Delay or Default Delay) Global Clock Input and IFF(2) without MMCM	XC6VCX75T	2.03/–0.08	2.03/–0.08	ns
		XC6VCX130T	2.26/–0.07	2.26/–0.07	ns
		XC6VCX195T	2.26/–0.10	2.26/–0.10	ns
		XC6VCX240T	2.26/–0.10	2.26/–0.10	ns

Notes:
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Table 61: **Global Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)					
$T_{PSMMCMGC}$/ $T_{PHMMCMGC}$	No Delay Global Clock Input and IFF(2) with MMCM	XC6VCX75T	0.12/1.31	0.12/1.31	ns
		XC6VCX130T	0.12/1.42	0.12/1.42	ns
		XC6VCX195T	0.13/1.43	0.13/1.43	ns
		XC6VCX240T	0.13/1.43	0.13/1.43	ns

Notes:
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 62: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
Input Setup and Hold Time Relative to Clock-capable Clock Input Signal for LVCMOS25 Standard.(1)					
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No Delay Clock-capable Clock Input and IFF(2) with MMCM	XC6VCX75T	0.19/1.18	0.19/1.18	ns
		XC6VCX130T	0.19/1.29	0.19/1.29	ns
		XC6VCX195T	0.20/1.30	0.20/1.30	ns
		XC6VCX240T	0.20/1.30	0.20/1.30	ns

Notes:
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Clock Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-6 FPGA clock transmitter and receiver data-valid windows.

Table 63: **Duty Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion (1)	All			ns
T_{CKSKEW}	Global Clock Tree Skew (2)	XC6VCX75T	0.17	0.17	ns
		XC6VCX130T	0.28	0.28	ns
		XC6VCX195T	0.29	0.29	ns
		XC6VCX240T	0.29	0.29	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All			ns
T_{DCD_BUFH}	Horizontal clock buffer duty cycle distortion	All			ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	All			ns
$T_{BUFIOSKEW2}$	I/O clock tree skew across three clock regions	All			ns
$T_{BUFHSKEW}$	Horizontal clock buffer skew across one clock region	All			ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All			ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 64: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package Skew(1)	XC6VCX75T	FF484		ps
			FF784		ps
		XC6VCX130T	FF484		ps
			FF784		ps
			FF1156		ps
		XC6VCX195T	FF784		ps
			FF1156		ps
		XC6VCX240T	FF784	146	ps
			FF1156	182	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Table 65: **Sample Window**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
T_{SAMP}	Sampling Error at Receiver Pins(1)	All			ps
T_{SAMP_BUFIO}	Sampling Error at Receiver Pins using BUFIO(2)	All			ps

Notes:
1. This parameter indicates the total sampling error of Virtex-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of Virtex-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IODELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 66: **Pin-to-Pin Setup/Hold and Clock-to-Out**

Symbol	Description	Speed Grade		Units
		-2	-1	
Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO				
T_{PSCS}/T_{PHCS}	Setup/Hold of I/O clock			ns
Pin-to-Pin Clock-to-Out Using BUFIO				
$T_{ICKOFCS}$	Clock-to-Out of I/O clock			ns

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
07/08/09	1.0	Initial Xilinx release.
02/05/10	1.1	Removed Figure 11: Placement Diagram for the FF1156 Package (5 of 5) from page 11 as there are only 16 GTX transcievers in the FF1156 package. Corrected the placement diagrams in Figure 2 through Figure 10.

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