Dual 8-/10-/12-/14-/16-Bit 250 MSPS Digital-to-Analog Converters

AD9741/AD9743/AD9745/AD9746/AD9747

FEATURES

High dynamic range, dual DACs
Low noise and intermodulation distortion
Single carrier WCDMA ACLR = 80 dBc @ 61.44 MHz IF
Innovative switching output stage permits useable outputs beyond Nyquist frequency
LVCMOS inputs with dual-port or optional interleaved single-port operation
Differential analog current outputs are programmable from 8.6 mA to 31.7 mA full scale
Auxiliary 10-bit current DACs with source/sink capability for external offset nulling
Internal 1.2 V precision reference voltage source
Operates from 1.8 V and 3.3 V supplies
315 mW power dissipation
Small footprint, Pb-free, 72-Lead LFCSP

APPLICATIONS

Wireless infrastructure:
WCDMA, CDMA2000, TD-SCDMA, WiMAX
Wideband communications:
LMDS/MMDS, point-to-point
Instrumentation:
RF signal generators, arbitrary waveform generators

GENERAL DESCRIPTION

The AD9741/AD9743/AD9745/AD9746/AD9747 are pin-compatible, high dynamic range, dual digital-to-analog converters (DACs) with 8-/10-/12-/ 14-/16-bit resolutions and sample rates of up to 250 MSPS. The devices include specific features for direct conversion transmit applications, including gain and offset compensation, and they interface seamlessly with analog quadrature modulators, such as the ADL5370.

A proprietary, dynamic output architecture permits synthesis of analog outputs even above Nyquist by shifting energy away from the fundamental and into the image frequency.

Full programmability is provided through a serial peripheral interface (SPI) port. In addition, some pin-programmable features are offered for those applications without a controller.

PRODUCT HIGHLIGHTS

1. Low noise and intermodulation distortion (IMD) enables high quality synthesis of wideband signals.
2. Proprietary switching output for enhanced dynamic performance.
3. Programmable current outputs and dual auxiliary DACs provide flexibility and system enhancements.

FUNCTIONAL BLOCK DIAGRAM

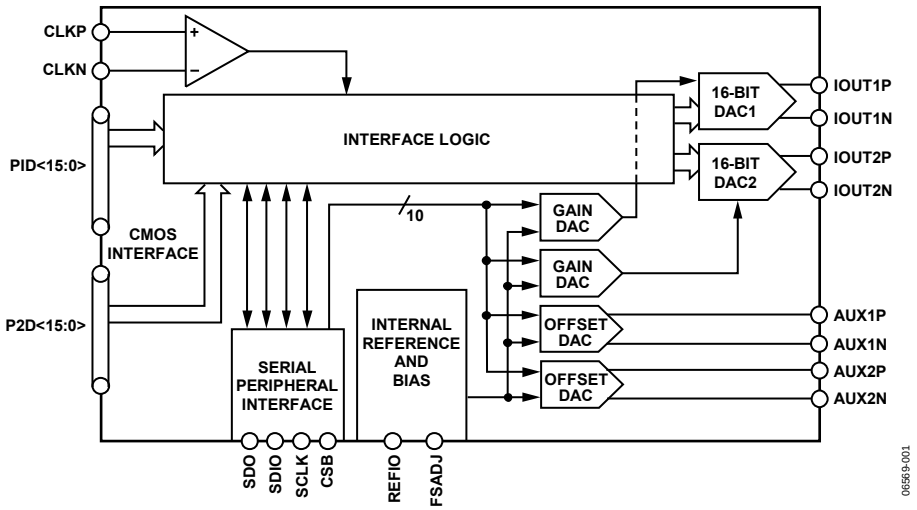

Figure 1.

Rev. 0

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REVISION HISTORY

5/07—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{FS} = 20 mA, full-scale digital input, maximum sample rate, unless otherwise noted.

Table 1. AD9741, AD9743, and AD9745

	AD9741			AD9743			AD9745			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		8			10			12		Bits
ACCURACY										
Differential Nonlinearity (DNL)		±0.03			±0.05			±0.13		LSB
Integral Nonlinearity (INL)		±0.05			±0.10			±0.25		LSB
MAIN DAC OUTPUTS										
Offset Error		±0.001			±0.001			±0.001		%FSR
Offset Error Temperature Coefficient		1.0			1.0			1.0		ppm/°C
Gain Error		±2.0			±2.0			±2.0		%FSR
Gain Error Temperature Coefficient		100			100			100		ppm/°C
Gain Matching (DAC1 to DAC2)		±1.0			±1.0			±1.0		%FSR
Full-Scale Output Current	8.6		31.7	8.6		31.7	8.6		31.7	mA
Output Compliance Voltage	−1.0		+1.0	−1.0		+1.0	−1.0		+1.0	V
Output Resistance		10			10			10		MΩ
AUXILIARY DAC OUTPUTS										
Resolution		10			10			10		Bits
Full-Scale Output Current	−2.0		+2.0	−2.0		+2.0	−2.0		+2.0	mA
Output Compliance Voltage Range—Sink Current	0.8		1.6	0.8		1.6	0.8		1.6	V
Output Compliance Voltage Range—Source Current	0		1.6	0		1.6	0		1.6	V
Output Resistance		1			1			1		MΩ
Monotonicity	10			10			10			Bits
REFERENCE INPUT/OUTPUT										
Output Voltage		1.2			1.2			1.2		V
Output Voltage Temperature Coefficient		10			10			10		ppm/°C
External Input Voltage Range	1.15		1.3	1.15		1.3	1.15		1.3	V
Input or Output Resistance		5			5			5		kΩ
POWER SUPPLY VOLTAGES										
AVDD33, DVDD33	3.13		3.47	3.13		3.47	3.13		3.47	V
CVDD18, DVDD18	1.70		1.90	1.70		1.90	1.70		1.90	V
POWER SUPPLY CURRENTS										
I_{AVDD33}		56	60		56	60		56	60	mA
I_{DVDD33}		10	14		10	14		11	15	mA
I_{CVDD18}		18	22		18	22		18	22	mA
I_{DVDD18}		28	32		29	33		30	34	mA
POWER DISSIPATION										
f_{DAC} = 250 MSPS, f_{OUT} = 20 MHz		300	345		300	345		305	350	mW
DAC Outputs Disabled		115			115			120		mW
Full Device Power-Down		3			3			3		mW
OPERATING TEMPERATURE	−40		+85	−40		+85	−40		+85	°C

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{FS} = 20 mA, full-scale digital input, maximum sample rate, unless otherwise noted. The AD9745 is repeated in Table 2 so the user can compare it with all other parts.

Table 2. AD9745, AD9746, and AD9747

	AD9745			AD9746			AD9747			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		12			14			16		Bits
ACCURACY										
Differential Nonlinearity (DNL)		±0.13			±0.5			±2.0		LSB
Integral Nonlinearity (INL)		±0.25			±1.0			±4.0		LSB
MAIN DAC OUTPUTS										
Offset Error		±0.001			±0.001			±0.001		%FSR
Offset Error Temperature Coefficient		0.1			0.1			0.1		ppm/°C
Gain Error		±2.0			±2.0			±2.0		%FSR
Gain Error Temperature Coefficient		100			100			100		ppm/°C
Gain Matching (DAC1 to DAC2)		±1.0			±1.0			±1.0		%FSR
Full-Scale Output Current	8.6		31.7	8.6		31.7	8.6		31.7	mA
Output Compliance Voltage	−1.0		+1.0	−1.0		+1.0	−1.0		+1.0	V
Output Resistance		10			10			10		MΩ
AUXILIARY DAC OUTPUTS										
Resolution		10			10			10		Bits
Full-Scale Output Current	−2.0		+2.0	−2.0		+2.0	−2.0		+2.0	mA
Output Compliance Voltage Range—Sink Current	0.8		1.6	0.8		1.6	0.8		1.6	V
Output Compliance Voltage Range—Source Current	0		1.6	0		1.6	0		1.6	V
Output Resistance		1			1			1		MΩ
Monotonicity	10			10			10			Bits
REFERENCE INPUT/OUTPUT										
Output Voltage		1.2			1.2			1.2		V
Output Voltage Temperature Coefficient		10			10			10		ppm/°C
External Input Voltage Range	1.15		1.3	1.15		1.3	1.15		1.3	V
Input or Output Resistance		5			5			5		kΩ
POWER SUPPLY VOLTAGES										
AVDD33, DVDD33	3.13		3.47	3.13		3.47	3.13		3.47	V
CVDD18, DVDD18	1.70		1.90	1.70		1.90	1.70		1.90	V
POWER SUPPLY CURRENTS										
I_{AVDD33}		56	60		56	60		56	60	mA
I_{DVDD33}		11	15		12	16		12	16	mA
I_{CVDD18}		18	22		18	22		18	22	mA
I_{DVDD18}		30	34		31	35		32	36	mA
POWER DISSIPATION										
f_{DAC} = 250 MSPS, f_{OUT} = 20 MHz		305	350		310	355		310	355	mW
DAC Outputs Disabled		120			125			125		mW
Full Device Power-Down		3			3			3		mW
OPERATING TEMPERATURE	−40		+85	−40		+85	−40		+85	°C

AC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{FS} = 20 mA, full-scale digital input, maximum sample rate, unless otherwise noted.

Table 3. AD9741, AD9743, and AD9745

	AD9741			AD9743			AD9745			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SPURIOUS FREE DYNAMIC RANGE (SFDR)										
f_{DAC} = 250 MSPS, f_{OUT} = 20 MHz		70			80			82		dBc
f_{DAC} = 250 MSPS, f_{OUT} = 70 MHz		70			70			70		dBc
f_{DAC} = 250 MSPS, f_{OUT} = 180 MHz[1]		64			64			66		dBc
INTERMODULATION DISTORTION (IMD)										
f_{DAC} = 250 MSPS, f_{OUT} = 20 MHz		80			80			86		dBc
f_{DAC} = 250 MSPS, f_{OUT} = 70 MHz		80			80			80		dBc
f_{DAC} = 250 MSPS, f_{OUT} = 180 MHz[1]		72			72			74		dBc
CROSSTALK										
f_{DAC} = 250 MSPS, f_{OUT} = 20 MHz		80			80			80		dBc
f_{DAC} = 250 MSPS, f_{OUT} = 70 MHz		80			80			80		dBc
f_{DAC} = 250 MSPS, f_{OUT} = 180 MHz[1]		80			80			80		dBc
ADJACENT CHANNEL LEAKAGE RATIO (ACLR) SINGLE CARRIER WCDMA										
f_{DAC} = 245.76 MSPS, f_{OUT} = 15.36 MHz		54			66			76		dBc
f_{DAC} = 245.76 MSPS, f_{OUT} = 61.44 MHz		54			66			76		dBc
f_{DAC} = 245.76 MSPS, f_{OUT} = 184.32 MHz[1]		54			64			72		dBc
NOISE SPECTRAL DENSITY (NSD)										
f_{DAC} = 245.76 MSPS, f_{OUT} = 15.36 MHz		−132			−144			−155		dBm/Hz
f_{DAC} = 245.76 MSPS, f_{OUT} = 61.44 MHz		−132			−144			−155		dBm/Hz
f_{DAC} = 245.76 MSPS, f_{OUT} = 184.32 MHz[1]		−135			−147			−155		dBm/Hz

[1] Mix Mode.

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{FS} = 20 mA, full-scale digital input, maximum sample rate, unless otherwise noted. The AD9745 is repeated in Table 4 so the user can compare it with all other parts.

Table 4. AD9745, AD9746, and AD9747

	AD9745			AD9746			AD9747			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SPURIOUS FREE DYNAMIC RANGE (SFDR)										
f_{DAC} = 250 MSPS, f_{OUT} = 20 MHz		82			82			82		dBc
f_{DAC} = 250 MSPS, f_{OUT} = 70 MHz		70			70			70		dBc
f_{DAC} = 250 MSPS, f_{OUT} = 180 MHz[1]		66			66			66		dBc
INTERMODULATION DISTORTION (IMD)										
f_{DAC} = 250 MSPS, f_{OUT} = 20 MHz		86			86			86		dBc
f_{DAC} = 250 MSPS, f_{OUT} = 70 MHz		80			80			80		dBc
f_{DAC} = 250 MSPS, f_{OUT} = 180 MHz[1]		74			74			74		dBc
CROSSTALK										
f_{DAC} = 250 MSPS, f_{OUT} = 20 MHz		80			80			80		dBc
f_{DAC} = 250 MSPS, f_{OUT} = 70 MHz		80			80			80		dBc
f_{DAC} = 250 MSPS, f_{OUT} = 180 MHz[1]		80			80			80		dBc
ADJACENT CHANNEL LEAKAGE RATIO (ACLR) SINGLE CARRIER WCDMA										
f_{DAC} = 245.76 MSPS, f_{OUT} = 15.36 MHz		76			78			82		dBc
f_{DAC} = 245.76 MSPS, f_{OUT} = 61.44 MHz		76			78			80		dBc
f_{DAC} = 245.76 MSPS, f_{OUT} = 184.32 MHz[1]		72			74			74		dBc
NOISE SPECTRAL DENSITY (NSD)										
f_{DAC} = 245.76 MSPS, f_{OUT} = 15.36 MHz		−155			−163			−165		dBm/Hz
f_{DAC} = 245.76 MSPS, f_{OUT} = 61.44 MHz		−155			−160			−162		dBm/Hz
f_{DAC} = 245.76 MSPS, f_{OUT} = 184.32 MHz[1]		−155			−158			−160		dBm/Hz

[1] Mix Mode.

DIGITAL AND TIMING SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{FS} = 20 mA, full-scale digital input, maximum sample rate, unless otherwise noted.

Table 5. AD9741/AD9743/AD9745/AD9746/AD9747

Parameter	Min	Typ	Max	Unit
DAC CLOCK INPUTS (CLKP, CLKN)				
Differential Peak-to-Peak Voltage	400	800	1600	mV
Single-Ended Peak-to-Peak Voltage			800	mV
Common-Mode Voltage	300	400	500	mV
Input Current			1	µA
Input Frequency			250	MHz
DATA CLOCK OUTPUT (DCO)				
Output Voltage High	2.4			V
Output Voltage Low			0.4	V
Output Current			10	mA
DAC Clock to Data Clock Output Delay (t_{DCO})	2.0	2.2	2.8	ns
DATA PORT INPUTS				
Input Voltage High	2.0			V
Input Voltage Low			0.8	V
Input Current			1	µA
Data to DAC Clock Setup Time (t_{DBS} Dual-Port Mode)	400			ps
Data to DAC Clock Hold Time (t_{DBH} Dual-Port Mode)	1200			ps
DAC Clock to Analog Output Data Latency (Dual-Port Mode)			7	Cycles
Data or IQSEL Input to DAC Clock Setup Time (t_{DBS} Single-Port Mode)	400			ps
Data or IQSEL Input to DAC Clock Hold Time (t_{DBH} Single-Port Mode)	1200			ps
DAC Clock to Analog Output Data Latency (Single-Port Mode)			8	Cycles
SERIAL PERIPHERAL INTERFACE				
SCLK Frequency (f_{SCLK})			40	MHz
SCLK Pulse Width High (t_{PWH})	10			ns
SCLK Pulse Width Low (t_{PWL})	10			ns
CSB to SCLK Setup Time (t_S)	1			ns
CSB to SCLK Hold Time (t_H)	0			ns
SDIO to SCLK Setup Time (t_{DS})	1			ns
SDIO to SCLK Hold Time (t_{DH})	0			ns
SCLK to SDIO/SDO Data Valid Time (t_{DV})			1	ns
RESET Pulse Width High	10			ns
WAKE-UP TIME AND OUTPUT LATENCY				
From DAC Outputs Disabled		200		µs
From Full Device Power-Down		1200		µs
DAC Clock to Analog Output Latency (Dual-Port Mode)		7		Cycles
DAC Clock to Analog Output Latency (Single-Port Mode)		8		Cycles

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	With Respect to	Rating
AVDD33, DVDD33	AVSS DVSS CVSS	−0.3 V to +3.6 V
DVDD18, CVDD18	AVSS DVSS CVSS	−0.3 V to +1.98 V
AVSS	DVSS CVSS	−0.3 V to +0.3 V
DVSS	AVSS CVSS	−0.3 V to +0.3 V
CVSS	AVSS DVSS	−0.3 V to +0.3 V
REFIO	AVSS	−0.3 V to AVDD33 + 0.3 V
IOUT1P, IOUT1N, IOUT2P, IOUT2P, AUX1P, AUX1N, AUX2P, AUX2N	AVSS	−1.0 V to AVDD33 + 0.3 V
P1D15 to P1D0, P2D15 to P2D0	DVSS	−0.3 V to DVDD33 + 0.3 V
CLKP, CLKN	CVSS	−0.3 V to CVDD18 + 0.3 V
RESET, CSB, SCLK, SDIO, SDO	DVSS	−0.3 V to DVDD33 + 0.3 V
Junction Temperature		125°C
Storage Temperature		−65°C to +150°C

THERMAL RESISTANCE

Thermal resistance tested using JEDEC standard 4-layer thermal test board with no airflow.

Table 7.

Package Type	θ_{JA}	Unit
CP-72-1 (Exposed Pad Soldered to PCB)	25	°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

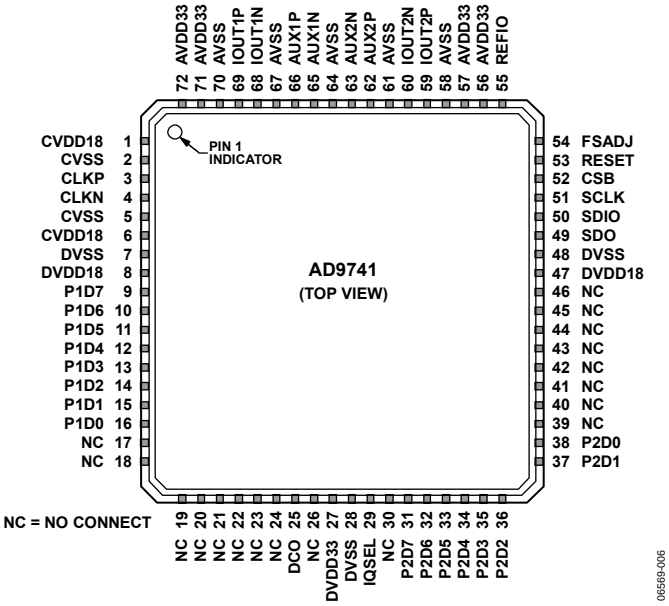


Figure 2. AD9741 Pin Configuration

Table 8. AD 9741 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 6	CVDD18	Clock Supply Voltage (1.8 V).
2, 5	CVSS	Clock Supply Common (0 V).
3	CLKP	Differential DAC Clock Input.
4	CLKN	Complementary Differential DAC Clock Input.
7, 28, 48	DVSS	Digital Supply Common (0 V).
8, 47	DVDD18	Digital Core Supply Voltage (1.8 V).
9 to 16	P1D<7:0>	Port 1 Data Bit Inputs.
17 to 24, 26, 30, 39 to 46	NC	No Connect.
25	DCO	Data Clock Output. Use to clock data source.
27	DVDD33	Digital I/O Supply Voltage (3.3 V).
29	IQSEL	I/Q Framing Signal for Single-Port Mode Operation.
31 to 38	P2D<7:0>	Port 2 Data Bit Inputs.
49	SDO	Serial Peripheral Interface Data Output.
50	SDIO	Serial Peripheral Interface Data Input and Optional Data Output.
51	SCLK	Serial Peripheral Interface Clock Input.
52	CSB	Serial Peripheral Interface Chip Select Input. Active low.
53	RESET	Hardware Reset. Active high.
54	FSADJ	Full-Scale Current Output Adjust. Connect a 10 kΩ resistor to AVSS.
55	REFIO	Reference Input/Output. Connect a 0.1 µF capacitor to AVSS.
56, 57, 71, 72	AVDD33	Analog Supply Voltage (3.3 V).
58, 61, 64, 67, 70	AVSS	Analog Supply Common (0 V).
59	IOUT2P	DAC2 Current Output True. Sources full-scale current when input data bits are all 1.
60	IOUT2N	DAC2 Current Output Complement. Sources full-scale current when data bits are all 0.
62	AUX2P	Auxiliary DAC2 Default Current Output Pin.
63	AUX2N	Auxiliary DAC2 Optional Output Pin. Enable through SPI.
65	AUX1N	Auxiliary DAC1 Optional Output Pin. Enable through SPI.
66	AUX1P	Auxiliary DAC1 Default Current Output Pin.
68	IOUT1N	Complementary DAC1 Current Output. Sources full-scale current when data bits are all 0.
69	IOUT1P	DAC1 Current Output. Sources full-scale current when data bits are all 1.
EPAD	AVSS	Exposed Thermal Pad. Must be soldered to copper pour on top surface of PCB for mechanical stability and must be electrically tied to low impedance GND plane for low noise performance.

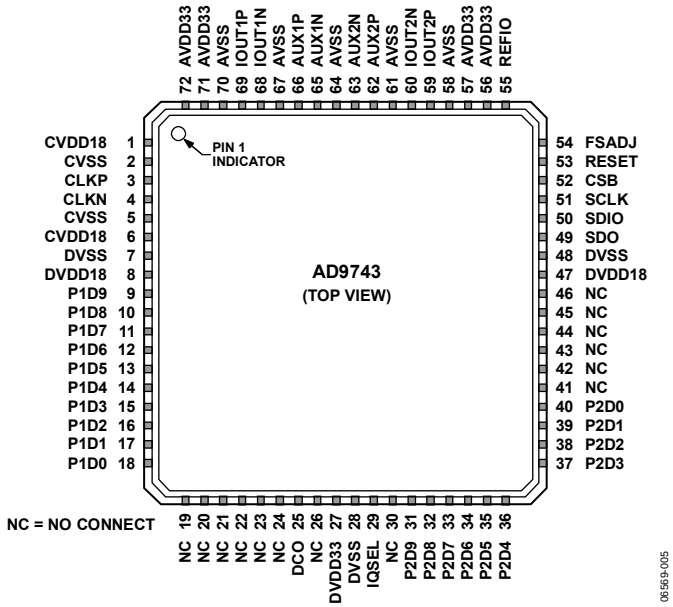


Figure 3. AD9743 Pin Configuration

Table 9. AD 9743 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 6	CVDD18	Clock Supply Voltage (1.8 V).
2, 5	CVSS	Clock Supply Common (0 V).
3	CLKP	Differential DAC Clock Input.
4	CLKN	Complementary Differential DAC Clock Input.
7, 28, 48	DVSS	Digital Supply Common (0 V).
8, 47	DVDD18	Digital Core Supply Voltage (1.8 V).
9 to 18	P1D<9:0>	Port 1 Data Bit Inputs.
19 to 24, 26, 30, 41 to 46	NC	No Connect.
25	DCO	Data Clock Output. Use to clock data source.
27	DVDD33	Digital I/O Supply Voltage (3.3 V).
29	IQSEL	I/Q Framing Signal for Single-Port Mode Operation.
31 to 40	P2D<9:0>	Port 2 Data Bit Inputs.
49	SDO	Serial Peripheral Interface Data Output.
50	SDIO	Serial Peripheral Interface Data Input and Optional Data Output.
51	SCLK	Serial Peripheral Interface Clock Input.
52	CSB	Serial Peripheral Interface Chip Select Input. Active low.
53	RESET	Hardware Reset. Active high.
54	FSADJ	Full-Scale Current Output Adjust. Connect a 10 kΩ resistor to AVSS.
55	REFIO	Reference Input/Output. Connect a 0.1 µF capacitor to AVSS.
56, 57, 71, 72	AVDD33	Analog Supply Voltage (3.3 V).
58, 61, 64, 67, 70	AVSS	Analog Supply Common (0 V).
59	IOUT2P	DAC2 Current Output True. Sources full-scale current when input data bits are all 1.
60	IOUT2N	DAC2 Current Output Complement. Sources full-scale current when data bits are all 0.
62	AUX2P	Auxiliary DAC2 Default Current Output Pin.
63	AUX2N	Auxiliary DAC2 Optional Output Pin. Enable through SPI.
65	AUX1N	Auxiliary DAC1 Optional Output Pin. Enable through SPI.
66	AUX1P	Auxiliary DAC1 Default Current Output Pin.
68	IOUT1N	Complementary DAC1 Current Output. Sources full-scale current when data bits are all 0.
69	IOUT1P	DAC1 Current Output. Sources full-scale current when data bits are all 1.
EPAD	AVSS	Exposed Thermal Pad. Must be soldered to copper pour on top surface of PCB for mechanical stability and must be electrically tied to low impedance GND plane for low noise performance.

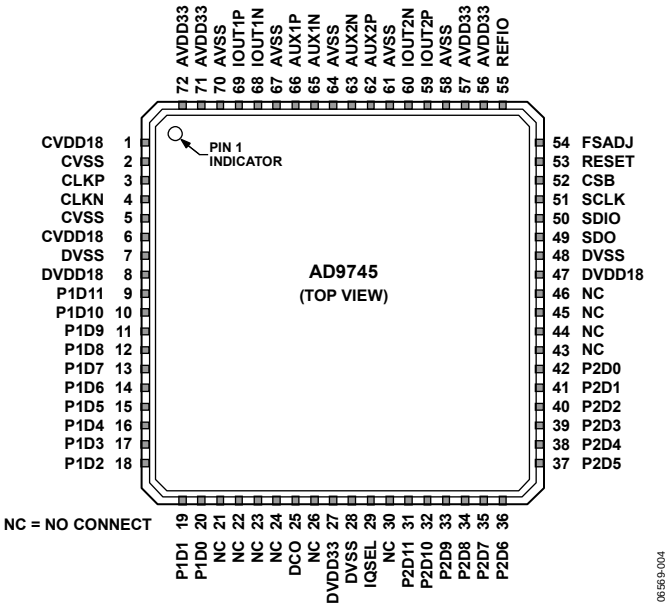


Figure 4. AD9745 Pin Configuration

Table 10. AD9745 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 6	CVDD18	Clock Supply Voltage (1.8 V).
2, 5	CVSS	Clock Supply Common (0 V).
3	CLKP	Differential DAC Clock Input.
4	CLKN	Complementary Differential DAC Clock Input.
7, 28, 48	DVSS	Digital Supply Common (0 V).
8, 47	DVDD18	Digital Core Supply Voltage (1.8 V).
9 to 20	P1D<11:0>	Port 1 Data Bit Inputs.
21 to 24, 26, 30, 43 to 46	NC	No Connect.
25	DCO	Data Clock Output. Use to clock data source.
27	DVDD33	Digital I/O Supply Voltage (3.3 V).
29	IQSEL	I/Q Framing Signal for Single-Port Mode Operation.
31 to 42	P2D<11:0>	Port 2 Data Bit Inputs.
49	SDO	Serial Peripheral Interface Data Output.
50	SDIO	Serial Peripheral Interface Data Input and Optional Data Output.
51	SCLK	Serial Peripheral Interface Clock Input.
52	CSB	Serial Peripheral Interface Chip Select Input. Active low.
53	RESET	Hardware Reset. Active high.
54	FSADJ	Full-Scale Current Output Adjust. Connect 10 kΩ resistor to AVSS.
55	REFIO	Reference Input/Output. Connect a 0.1 µF capacitor to AVSS.
56, 57, 71, 72	AVDD33	Analog Supply Voltage (3.3 V).
58, 61, 64, 67, 70	AVSS	Analog Supply Common (0 V).
59	IOUT2P	DAC2 Current Output True. Sources full-scale current when input data bits are all 1.
60	IOUT2N	DAC2 Current Output Complement. Sources full-scale current when data bits are all 0.
62	AUX2P	Auxiliary DAC2 Default Current Output Pin.
63	AUX2N	Auxiliary DAC2 Optional Output Pin. Enable through SPI.
65	AUX1N	Auxiliary DAC1 Optional Output Pin. Enable through SPI.
66	AUX1P	Auxiliary DAC1 Default Current Output Pin.
68	IOUT1N	Complementary DAC1 Current Output. Sources full-scale current when data bits are all 0.
69	IOUT1P	DAC1 Current Output. Sources full-scale current when data bits are all 1.
EPAD	AVSS	Exposed Thermal Pad. Must be soldered to copper pour on top surface of PCB for mechanical stability and must be electrically tied to low impedance GND plane for low noise performance.

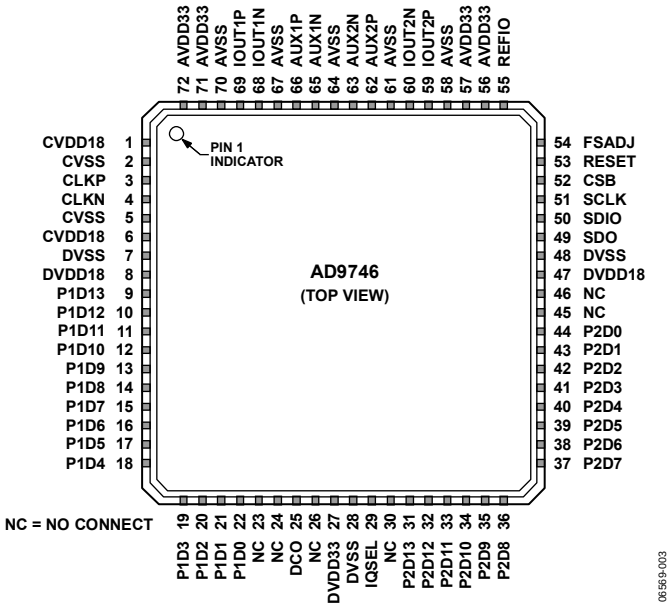


Figure 5. AD9746 Pin Configuration

Table 11. AD9746 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 6	CVDD18	Clock Supply Voltage (1.8 V).
2, 5	CVSS	Clock Supply Common (0 V).
3	CLKP	Differential DAC Clock Input.
4	CLKN	Complementary Differential DAC Clock Input.
7, 28, 48	DVSS	Digital Supply Common (0 V).
8, 47	DVDD18	Digital Core Supply Voltage (1.8 V).
9 to 22	P1D<13:0>	Port 1 Data Bit Inputs.
23, 24, 26, 30, 45, 46	NC	No Connect.
25	DCO	Data Clock Output. Use to clock data source.
27	DVDD33	Digital I/O Supply Voltage (3.3 V).
29	IQSEL	I/Q Framing Signal for Single-Port Mode Operation.
31 to 44	P2D<13:0>	Port 2 Data Bit Inputs.
49	SDO	Serial Peripheral Interface Data Output.
50	SDIO	Serial Peripheral Interface Data Input and Optional Data Output.
51	SCLK	Serial Peripheral Interface Clock Input.
52	CSB	Serial Peripheral Interface Chip Select Input. Active low.
53	RESET	Hardware Reset. Active high.
54	FSADJ	Full-Scale Current Output Adjust. Connect a 10 kΩ resistor to AVSS.
55	REFIO	Reference Input/Output. Connect a 0.1 µF capacitor to AVSS.
56, 57, 71, 72	AVDD33	Analog Supply Voltage (3.3 V).
58, 61, 64, 67, 70	AVSS	Analog Supply Common (0 V).
59	IOUT2P	DAC2 Current Output True. Sources full-scale current when input data bits are all 1.
60	IOUT2N	DAC2 Current Output Complement. Sources full-scale current when data bits are all 0.
62	AUX2P	Auxiliary DAC2 Default Current Output Pin.
63	AUX2N	Auxiliary DAC2 Optional Output Pin. Enable through SPI.
65	AUX1N	Auxiliary DAC1 Optional Output Pin. Enable through SPI.
66	AUX1P	Auxiliary DAC1 Default Current Output Pin.
68	IOUT1N	Complementary DAC1 Current Output. Sources full-scale current when data bits are all 0.
69	IOUT1P	DAC1 Current Output. Sources full-scale current when data bits are all 1.
EPAD	AVSS	Exposed Thermal Pad. Must be soldered to copper pour on top surface of PCB for mechanical stability and must be electrically tied to low impedance GND plane for low noise performance.

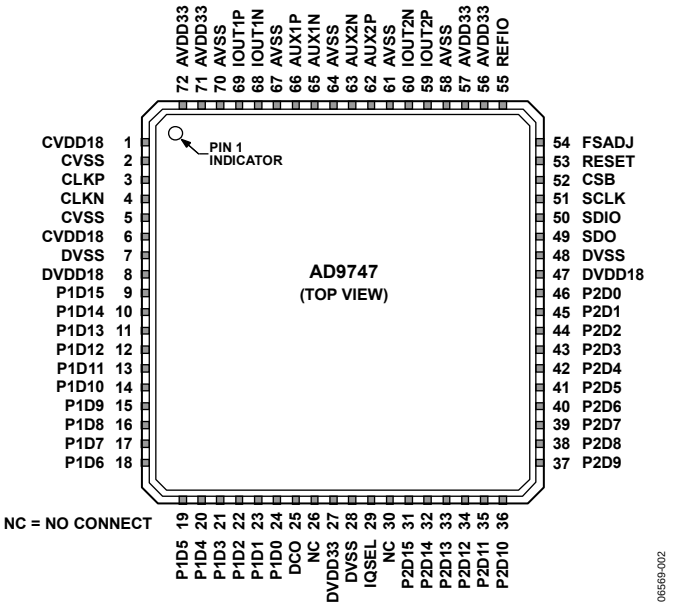


Figure 6. AD9747 Pin Configuration

Table 12. AD9747 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 6	CVDD18	Clock Supply Voltage (1.8 V).
2, 5	CVSS	Clock Supply Common (0 V).
3	CLKP	Differential DAC Clock Input.
4	CLKN	Complementary Differential DAC Clock Input.
7, 28, 48	DVSS	Digital Supply Common (0 V).
8, 47	DVDD18	Digital Core Supply Voltage (1.8 V).
9 to 24	P1D<15:0>	Port 1 Data Bit Inputs.
25	DCO	Data Clock Output. Use to clock data source.
26, 30	NC	No Connect.
27	DVDD33	Digital I/O Supply Voltage (3.3 V).
29	IQSEL	I/Q Framing Signal for Single-Port Mode Operation.
31 to 46	P2D<15:0>	Port 2 Data Bit Inputs.
49	SDO	Serial Peripheral Interface Data Output.
50	SDIO	Serial Peripheral Interface Data Input and Optional Data Output.
51	SCLK	Serial Peripheral Interface Clock Input.
52	CSB	Serial Peripheral Interface Chip Select Input. Active low.
53	RESET	Hardware Reset. Active high.
54	FSADJ	Full-Scale Current Output Adjust. Connect a 10 kΩ resistor to AVSS.
55	REFIO	Reference Input/Output. Connect a 0.1 µF capacitor to AVSS.
56, 57, 71, 72	AVDD33	Analog Supply Voltage (3.3 V).
58, 61, 64, 67, 70	AVSS	Analog Supply Common (0 V).
59	IOUT2P	DAC2 Current Output. Sources full-scale current when input data bits are all 1.
60	IOUT2N	Complementary DAC2 Current Output. Sources full-scale current when data bits are all 0.
62	AUX2P	Auxiliary DAC2 Default Current Output Pin.
63	AUX2N	Auxiliary DAC2 Optional Output Pin. Enable through SPI.
65	AUX1N	Auxiliary DAC1 Optional Output Pin. Enable through SPI.
66	AUX1P	Auxiliary DAC1 Default Current Output Pin.
68	IOUT1N	Complementary DAC1 Current Output. Sources full-scale current when data bits are all 0.
69	IOUT1P	DAC1 Current Output. Sources full-scale current when data bits are all 1.
EPAD	AVSS	Exposed Thermal Pad. Must be soldered to copper pour on top surface of PCB for mechanical stability and must be electrically tied to low impedance GND plane for low noise performance.

TYPICAL PERFORMANCE CHARACTERISTICS

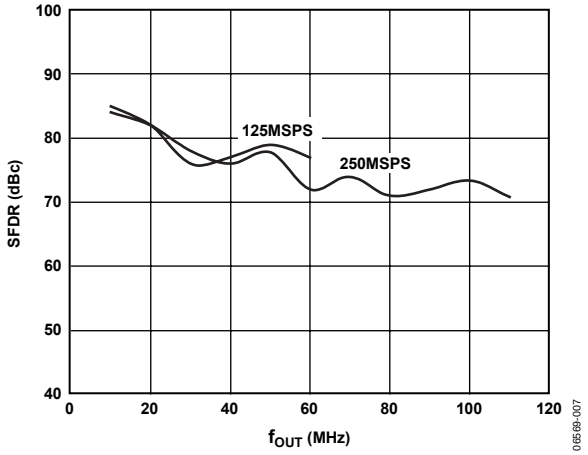


Figure 7. AD9747 SFDR vs. f_{OUT}, Normal Mode

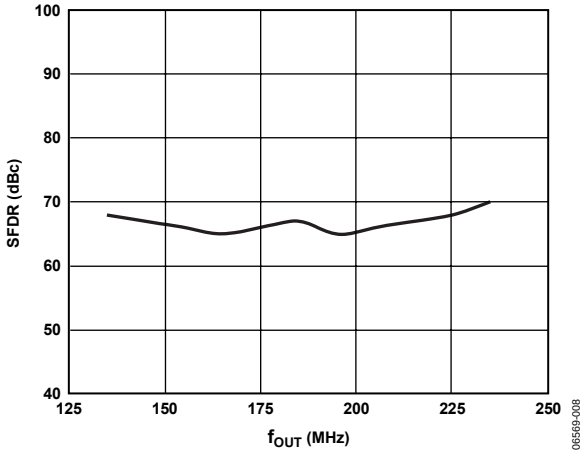


Figure 8. AD9747 SFDR vs. f_{OUT}, Mix Mode, 250 MSPS

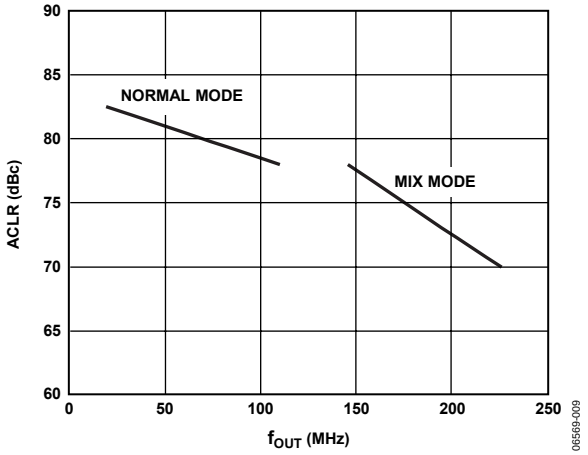


Figure 9. AD9747 ACLR vs. f_{OUT}, Single Carrier WCDMA, 245.76 MSPS

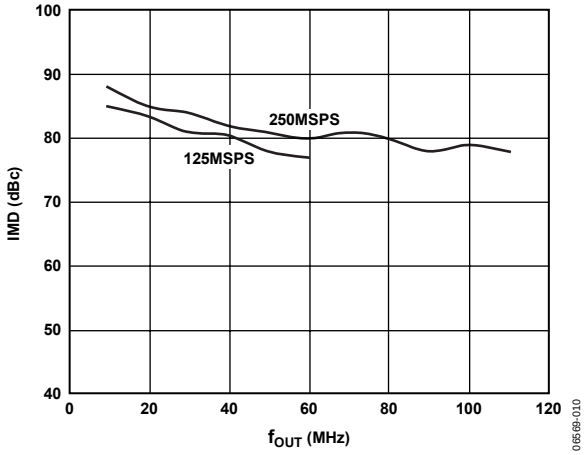


Figure 10. AD9747 IMD vs. f_{OUT}, Normal Mode

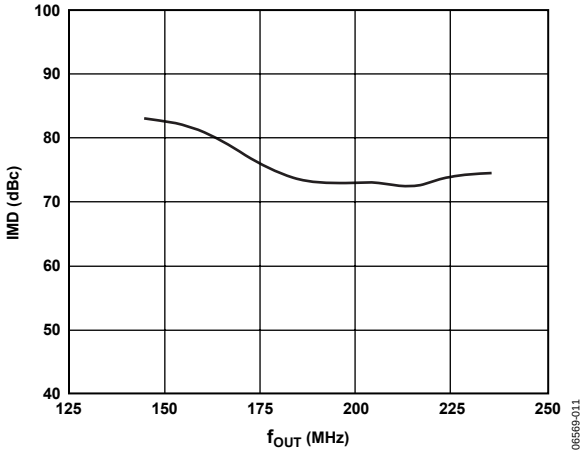


Figure 11. AD9747 IMD vs. f_{OUT}, Mix Mode, 250 MSPS

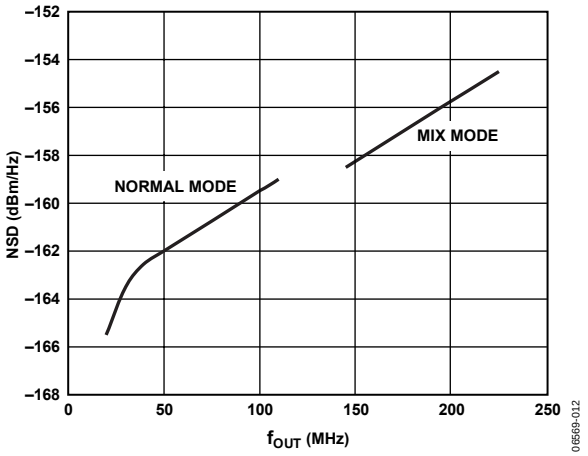


Figure 12. AD9747 NSD vs. f_{OUT}, Single Carrier WCDMA, 245.76 MSPS

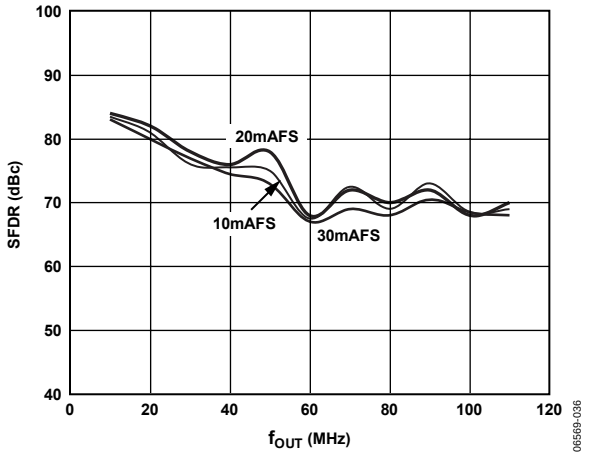


Figure 13. AD9747 SFDR vs. Analog Output, 250 MSPS

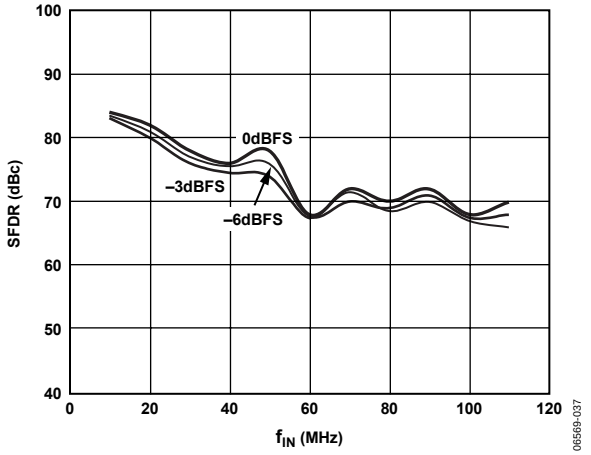


Figure 14. AD9747 SFDR vs. Digital Input, 250 MSPS

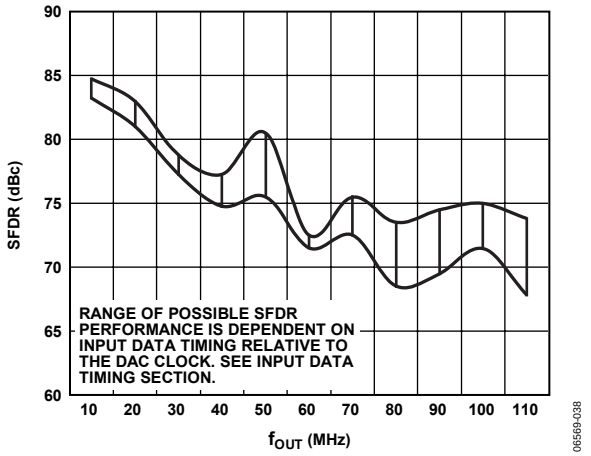


Figure 15. AD9747 SFDR vs. f_{OUT} Over Input Data Timing

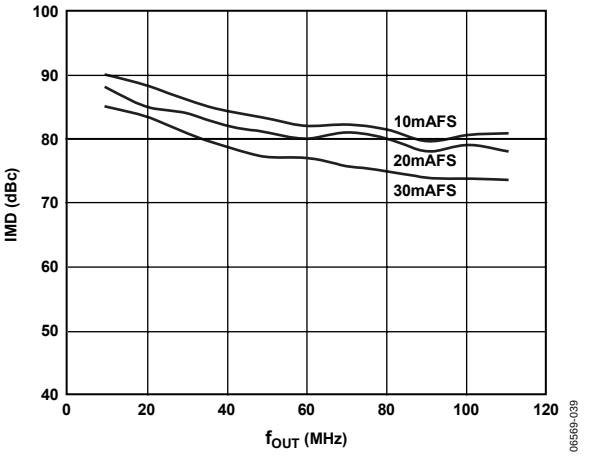


Figure 16. AD9747 IMD vs. Analog Output, 250 MSPS

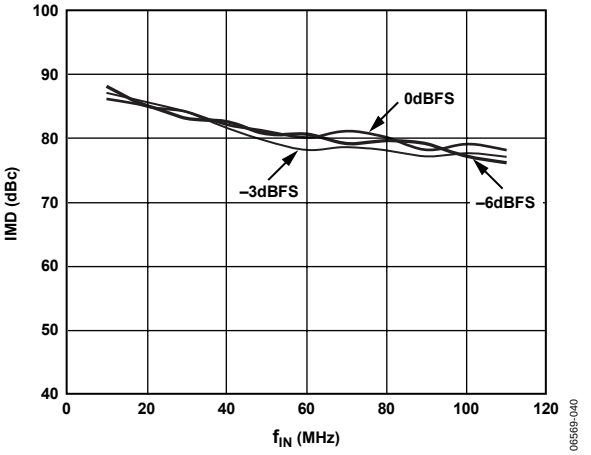


Figure 17. AD9747 IMD vs. Digital Input, 250 MSPS

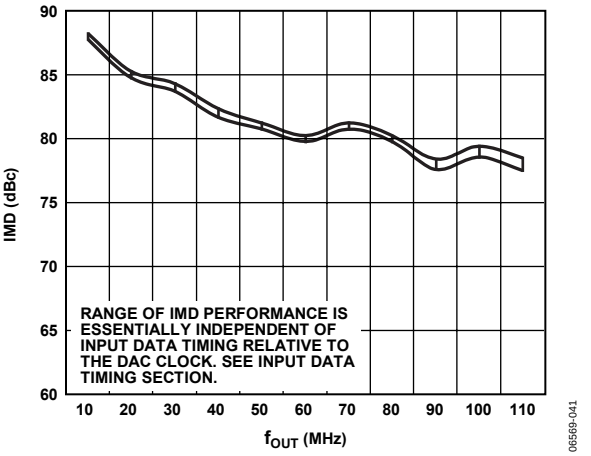


Figure 18. AD9747 IMD vs. f_{OUT} Over Input Data Timing

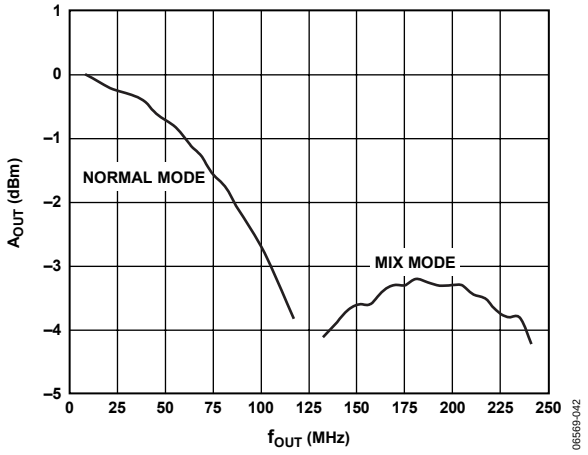


Figure 19. Nominal Power in the Fundamental, I_{FS} = 20 mA

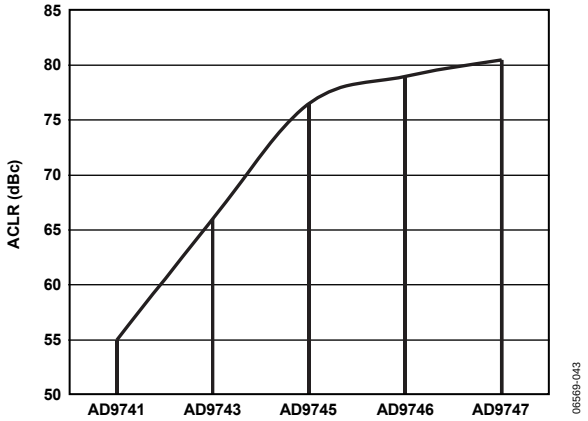


Figure 20. ACLR vs. Bit Resolution, Single Carrier WCDMA, 245.76 MSPS, $f_{CARRIER}$ = 61.44 MHz

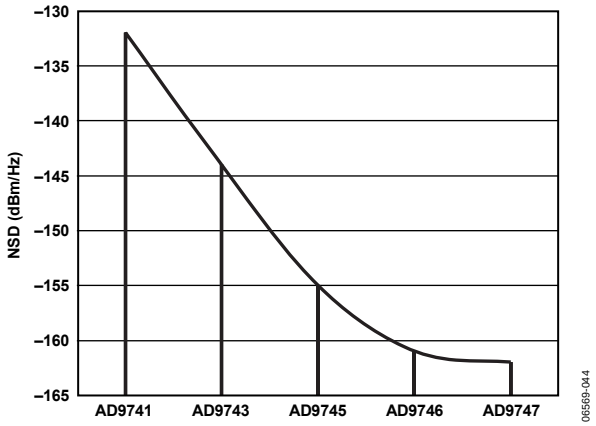


Figure 21. NSD vs. Bit Resolution, Single Carrier WCDMA, 245.76 MSPS, $f_{CARRIER}$ $f_{CARRIER}$ = 61.44 MHz

TERMINOLOGY

Integral Nonlinearity (INL)
The maximum deviation of the actual analog output from the ideal output, as determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)
A measure of the maximum deviation in analog output associated with any single value change in the digital input code relative to an ideal LSB.

Monotonicity
A DAC is monotonic if the analog output increases or remains constant in response to an increase in the digital input.

Offset Error
The deviation of the output current from the ideal zero-scale current. For differential outputs, 0 mA is expected at I_{OUTP} when all inputs are low, and 0 mA is expected at I_{OUTN} when all inputs are high.

Gain Error
The deviation of the output current from the ideal full-scale current. Actual full-scale output current is determined by subtracting the output (when all inputs are low) from the output (when all inputs are high).

Output Compliance Range
The range of allowable voltage seen by the analog output of a current output DAC. Operation beyond the compliance limits may cause output stage saturation and/or a breakdown resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change in a parameter from ambient temperature (25°C) to either T_{MIN} or T_{MAX} and is typically reported as ppm/°C.

Spurious-Free Dynamic Range (SFDR)
The difference in decibels between the peak amplitude of a test tone and the peak amplitude of the largest spurious signal over the specified bandwidth.

Intermodulation Distortion (IMD)
The difference in decibels between the maximum peak amplitude of two test tones and the maximum peak amplitude of the distortion products created from the sum or difference of integer multiples of the test tones.

Adjacent Channel Leakage Ratio (ACLR)
The ratio between the measured power of a wideband signal within a channel relative to the measured power in an empty adjacent channel.

Noise Spectral Density (NSD)
The measured noise power over a 1 Hz bandwidth seen at the analog output.

THEORY OF OPERATION

The AD9741/AD9743/AD9745/AD9746/AD9747 combine many features to make them very attractive for wired and wireless communications systems. The dual DAC architecture facilitates easy interfacing to common quadrature modulators when designing single sideband transmitters. In addition, the speed and performance of the devices allow wider bandwidths and more carriers to be synthesized than in previously available products.

All features and options are software programmable through the SPI port.

SERIAL PERIPHERAL INTERFACE

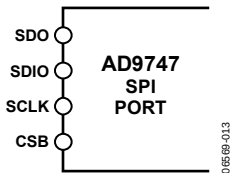


Figure 22. SPI Port

The SPI port is a flexible, synchronous serial communications port allowing easy interfacing to many industry-standard microcontrollers and microprocessors. The port is compatible with most synchronous transfer formats including both the Motorola SPI and Intel® SSR protocols.

The interface allows read and write access to all registers that configure the AD9741/AD9743/AD9745/AD9746/AD9747. Single or multiple byte transfers are supported as well as MSB-first or LSB-first transfer formats. Serial data input/output can be accomplished through a single bidirectional pin (SDIO) or through two unidirectional pins (SDIO/SDO).

The serial port configuration is controlled by Register 0x00, Bits<7:6>. It is important to note that any change made to the serial port configuration occurs immediately upon writing to the last bit of this byte. Therefore, it is possible with a multibyte transfer to write to this register and change the configuration in the middle of a communication cycle. Care must be taken to compensate for the new configuration within the remaining bytes of the current communication cycle.

Use of a single-byte transfer when changing the serial port configuration is recommended to prevent unexpected device behavior.

GENERAL OPERATION OF THE SERIAL INTERFACE

There are two phases to any communication cycle with the AD9741/AD9743/AD9745/AD9746/AD9747: Phase 1 and Phase 2. Phase 1 is the instruction cycle, which writes an instruction byte into the device. This byte provides the serial port controller with information regarding Phase 2 of the communication cycle: the data transfer cycle.

The Phase 1 instruction byte defines whether the upcoming data transfer is read or write, the number of bytes in the data transfer, and a reference register address for the first byte of the data transfer. A logic high on the CSB pin followed by a logic low resets the SPI port to its initial state and defines the start of the instruction cycle. From this point, the next eight rising SCLK edges define the eight bits of the instruction byte for the current communication cycle.

The remaining SCLK edges are for Phase 2 of the communication cycle, which is the data transfer between the serial port controller and the system controller. Phase 2 can be a transfer of 1, 2, 3, or 4 data bytes as determined by the instruction byte. Using multibyte transfers is usually preferred although single-byte data transfers are useful to reduce CPU overhead or when only a single register access is required.

All serial port data is transferred to and from the device in synchronization with the SCLK pin. Input data is always latched on the rising edge of SCLK whereas output data is always valid after the falling edge of SCLK. Register contents change immediately upon writing to the last bit of each transfer byte.

When synchronization is lost, the device has the ability to asynchronously terminate an I/O operation whenever the CSB pin is taken to logic high. Any unwritten register content data is lost if the I/O operation is aborted. Taking CSB low then resets the serial port controller and restarts the communication cycle.

INSTRUCTION BYTE

The instruction byte contains the information shown in the following bit map.

MSB							LSB
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
R/W	N1	N0	A4	A3	A2	A1	A0

Bit 7, R/W, determines whether a read or a write data transfer occurs after the instruction byte write. Logic high indicates a read operation. Logic 0 indicates a write operation.

Bits<6:5>, N1 and N0, determine the number of bytes to be transferred during the data transfer cycle. The bits decode as shown in Table 13.

Table 13. Byte Transfer Count

N1	N0	Description
0	0	Transfer one byte
0	1	Transfer two bytes
1	0	Transfer three bytes
1	1	Transfer four bytes

Bits<4:0>, A4, A3, A2, A1, and A0, determine which register is accessed during the data transfer of the communications cycle. For multibyte transfers, this address is a starting or ending address depending on the current data transfer mode. For MSB-first format, the specified address is an ending address or the most significant address in the current cycle. Remaining register addresses for multiple byte data transfers are generated

internally by the serial port controller by decrementing from the specified address. For LSB-first format, the specified address is a beginning address or the least significant address in the current cycle. Remaining register addresses for multiple byte data transfers are generated internally by the serial port controller by incrementing from the specified address.

MSB/LSB TRANSFERS

The serial port can support both MSB-first and LSB-first data formats. This functionality is controlled by Register 0x00, Bit 6. The default is Logic 0, which is MSB-first format.

When using MSB-first format (LSBFIRST = 0), the instruction and data bit must be written from MSB to LSB. Multibyte data transfers in MSB-first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes are loaded into sequentially lower address locations. In MSB-first mode, the serial port internal address generator decrements for each byte of the multibyte data transfer.

When using LSB-first format (LSBFIRST = 1), the instruction and data bit must be written from LSB to MSB. Multibyte data transfers in LSB-first format start with an instruction byte that includes the register address of the least significant data byte. Subsequent data bytes are loaded into sequentially higher address locations. In LSB-first mode, the serial port internal address generator increments for each byte of the multibyte data transfer.

Use of a single-byte transfer when changing the serial port data format is recommended to prevent unexpected device behavior.

SERIAL INTERFACE PORT PIN DESCRIPTIONS

Chip Select Bar (CSB)

Active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communication lines. CSB must stay low during the entire communication cycle. Incomplete data transfers are aborted anytime the CSB pin goes high. SDO and SDIO pins go to a high impedance state when this input is high.

Serial Clock (SCLK)

The serial clock pin is used to synchronize data to and from the device and to run the internal state machines. The maximum frequency of SCLK is 40 MHz. All data input is registered on the rising edge of SCLK. All data is driven out on the falling edge of SCLK.

Serial Data I/O (SDIO)

Data is always written into the device on this pin. However, SDIO can also function as a bidirectional data output line. The configuration of this pin is controlled by Register 0x00, Bit 7. The default is Logic 0, which configures the SDIO pin as unidirectional.

Serial Data Out (SDO)

Data is read from this pin for protocols that use separate lines for transmitting and receiving data. The configuration of this pin is controlled by Register 0x00, Bit 7. If this bit is set to a Logic 1, the SDO pin does not output data and is set to a high impedance state.

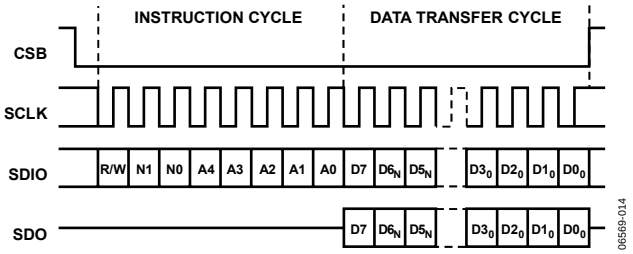


Figure 23. Serial Register Interface—MSB First

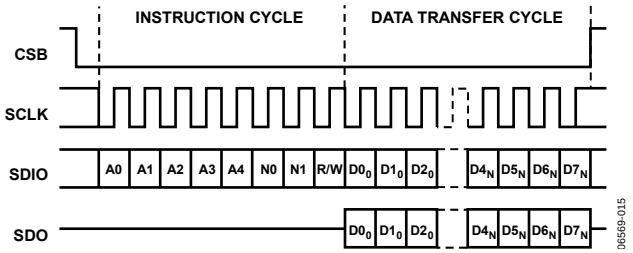


Figure 24. Serial Register Interface Timing—LSB First

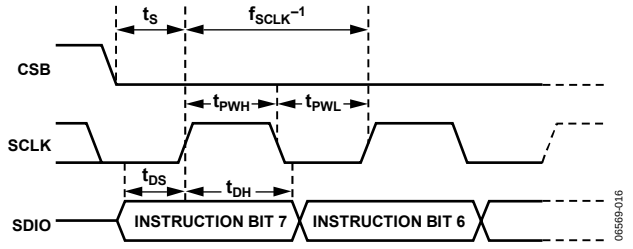


Figure 25. Timing Diagram for SPI Register Write

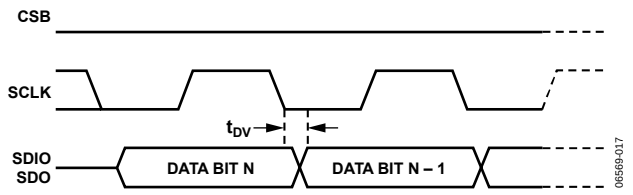


Figure 26. Timing Diagram for SPI Register Read

SPI REGISTER MAP

Reading any register returns previously written values for all defined register bits, unless otherwise noted. Change serial port configuration or execute software reset in single byte instruction only to avoid unexpected device behavior.

Table 14.

Register Name	Address	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPI Control	0x00	0x00	SDIODIR	LSBFIRST	SWRESET					
Data Control	0x02	0x00	DATTYPE	ONEPORT		INVDCO				
Power Down	0x03	0x00	PD_DCO		PD_AUX2	PD_AUX1	PD_BIAS	PC_CLK	PD_DAC2	PD_DAC1
DAC Mode Select	0x0A	0x00					DAC1MOD<1:0>		DAC2MOD<1:0>	
DAC1 Gain LSB	0x0B	0xF9	DAC1FSC<7:0>							
DAC1 Gain MSB	0x0C	0x01							DAC1FSC<9:8>	
AUX DAC1 LSB	0x0D	0x00	AUXDAC1<7:0>							
AUX DAC1 MSB	0x0E	0x00	AUX1PIN	AUX1DIR					AUXDAC1<9:8>	
DAC2 Gain LSB	0x0F	0xF9	DAC2FSC<7:0>							
DAC2 Gain MSB	0x10	0x01							DAC2FSC<9:8>	
AUX DAC2 LSB	0x11	0x00	AUXDAC2<7:0>							
AUX DAC2 MSB	0x12	0x00	AUX2PIN	AUX2DIR					AUXDAC2<9:8>	

SPI REGISTER DESCRIPTIONS

Table 15.

Register	Address	Bit	Name	Description
SPI Control	0x00	7	SDIODIR	0, operate SPI in 4-wire mode, SDIO pin operates as an input only
				1, operate SPI in 3-wire mode, SDIO pin operates as a bidirectional I/O line
		6	LSBFIRST	0, LSBFIRST off, SPI serial data mode is MSB to LSB
				1, LSBFIRST on, SPI serial data mode is LSB to MSB
		5	SWRESET	0, resume normal operation following software RESET
				1, software RESET; loads default values to all registers (except Register 0x00)
Data Control	0x02	7	DATTYPE	0, DAC input data is twos complement binary format
				1, DAC input data is unsigned binary format
		6	ONEPORT	0, normal two port input mode
				1, optional single port input mode, interleaved data received on Port 1 only
		4	INVDCO	1, inverts data clock output signal
Power Down	0x03	7	PD_DCO	1, power down data clock output
		5	PD_AUX2	1, power down AUX2 DAC
		4	PD_AUX1	1, power down AUX1 DAC
		3	PD_BIAS	1, power down reference voltage bias circuit
		2	PD_CLK	1, power down DAC clock input circuit
		1	PD_DAC2	1, power down DAC2 analog output
		0	PD_DAC1	1, power down DAC1 analog output
DAC Mode Select	0x0A	3:2	DAC1MOD<1:0>	00, selects normal mode, DAC1
				01, selects mix mode, DAC1
				10, selects return-to-zero mode, DAC1
		1:0	DAC2MOD<1:0>	00, selects normal mode, DAC2
				01, selects mix mode, DAC2
				10, selects return-to-zero mode, DAC2
DAC1 Gain	0x0B	7:0	DAC1FSC<7:0>	DAC1 full-scale 10-bit adjustment word
	0x0C	1:0	DAC1FSC<9:8>	0x03FF, sets full-scale current to the maximum value of 31.66 mA
				0x01F9, sets full-scale current to the nominal value of 20.0 mA
				0x0000, sets full-scale current to the minimum value of 8.64 mA
AUX DAC1	0x0D	7:0	AUXDAC1<7:0>	Auxiliary DAC1 10-bit output current adjustment word
	0x0E	1:0	AUXDAC1<9:8>	0x03FF, sets output current magnitude to 2.0 mA
				0x0200, sets output current magnitude to 1.0 mA
				0x0000, sets output current magnitude to 0.0 mA
		7	AUX1PIN	0, AUX1P output pin is active
				1, AUX1N output pin is active
		6	AUX1DIR	0, configures AUX1 DAC output to source current
				1, configures AUX1 DAC output to sink current
DAC2 Gain	0x0F	7:0	DAC2FSC<7:0>	DAC2 full-scale 10-bit adjustment word
	0x10	1:0	DAC2FSC<9:8>	0x03FF, sets full-scale current to the maximum value of 31.66 mA
				0x01F9, sets full-scale current to the nominal value of 20.0 mA
				0x0000, sets full-scale current to the minimum value of 8.64 mA
AUX DAC2	0x11	7:0	AUXDAC2<7:0>	Auxiliary DAC2 10-bit output current adjustment word
	0x12	1:0	AUXDAC2<9:8>	0x03FF, sets output current magnitude to 2.0 mA
				0x0200, sets output current to 1.0 mA
				0x0000, sets output current to 0.0 mA
		7	AUX2PIN	0, AUX2P output pin is active
				1, AUX2N output pin is active
		6	AUX2DIR	0, configures AUX2 DAC output to source current
				1, configures AUX2 DAC output to sink current

DIGITAL INPUTS AND OUTPUTS

The AD9741/AD9743/AD9745/AD9746/AD9747 can operate in two data input modes: dual-port mode and single-port mode. For the default dual-port mode (ONEPORT = 0), each DAC receives data from a dedicated input port. In single-port mode (ONEPORT = 1), however, both DACs receive data from Port 1. In single-port mode, DAC1 and DAC2 data is interleaved and the IQSEL input is used to steer data to the correct DAC.

In single-port mode, when the IQSEL input is high, Port 1 data is delivered to DAC1 and when IQSEL is low, Port 1 data is delivered to DAC2. The IQSEL input should always coincide and be time-aligned with the other data bus signals. In single-port mode, minimum setup and hold times apply to the IQSEL input as well as to the input data signals. In dual-port mode, the IQSEL input is ignored.

In dual-port mode, the data must be delivered at the sample rate (up to 250 MSPS). In single-port mode, data must be delivered at twice the sample rate. Because the data inputs function only up to 250 MSPS, it is only practical to operate the DAC clock at up to 125 MHz in single-port mode.

In both dual-port and single-port modes, a data clock output (DCO) signal is available as a fixed time base with which to stimulate data from an FPGA. This output signal always operates at the sample rate. It may be inverted by asserting the INVDCO bit.

INPUT DATA TIMING

With most DACs, signal-to-noise ratio (SNR) is a function of the relationship between the position of the clock edges and the point in time at which the input data changes. The AD9741/AD9743/AD9745/AD9746/AD9747 are rising edge triggered and thus exhibit greater SNR sensitivity when the data transition is close to this edge.

The specified minimum setup and hold times define a window of time, within each data period, where the data is sampled correctly. Generally, users should position data to arrive relative to the DAC clock and well beyond the minimum setup and minimum hold times. This becomes increasingly more important at increasingly higher sample rates.

DUAL-PORT MODE TIMING

The timing diagram for the dual-port mode is shown in Figure 27.

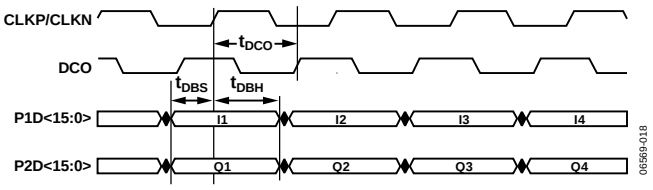


Figure 27. Data Interface Timing, Dual-Port Mode

In Figure 27, data samples for DAC1 are labeled Ix and data samples for DAC2 are labeled Qx. Note that the differential DAC clock input is shown in a logical sense (CLKP/CLKN). The data clock output is labeled DCO.

Setup and hold times are referenced to the positive transition of the DAC clock. Data should arrive at the input pins such that the minimum setup and hold times are met. Note that the data clock output has a fixed time delay from the DAC clock and may be a more convenient signal to use to confirm timing.

SINGLE-PORT MODE TIMING

The single-port mode timing diagram is shown in Figure 28.

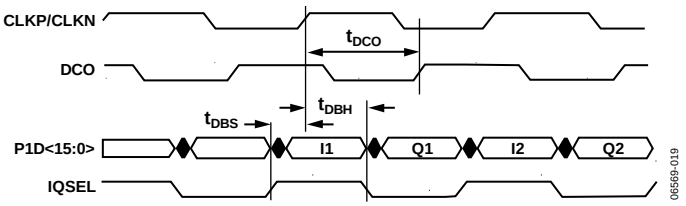


Figure 28. Data Interface Timing, Single-Port Mode

In single-port mode, data for both DACs is received on the Port 1 input bus. Ix and Qx data samples are interleaved and arrive twice as fast as in dual-port mode. Accompanying the data is the IQSEL input signal, which steers incoming data to its respective DAC. When IQSEL is high, data is steered to DAC1 and when IQSEL is low, data is steered to DAC2. IQSEL should coincide as well as be time-aligned with incoming data.

SPI PORT, RESET, AND PIN MODE

In general, when the AD9741/AD9743/AD9745/AD9746/AD9747 are powered up, an active high pulse applied to the RESET pin should follow. This insures the default state of all control register bits. In addition, once the RESET pin goes low, the SPI port can be activated, so CSB should be held high.

For applications without a controller, the AD9741/AD9743/AD9745/AD9746/AD9747 also support pin mode operation, which allows some functional options to be pin, selected without the use of the SPI port. Pin mode is enabled anytime the RESET pin is held high. In pin mode, the four SPI port pins take on secondary functions, as shown in Table 16.

Table 16. SPI Pin Functions (Pin Mode)

Pin Name	Pin Mode Description
SCLK	ONEPORT (Register 0x02, Bit 6), bit value (1/0) equals pin state (high/low)
SDIO	DATTYPE (Register 0x02, Bit 7), bit value (1/0) equals pin state (high/low)
CSB	Enable Mix Mode, if CSB is high, Register 0x0A is set to 0x05 putting both DAC1 and DAC2 into mix mode
SDO	Enable full power-down, if SDO is high, Register 0x03 is set to 0xFF

In pin mode, all register bits are reset to their default values with the exception of those that are controlled by the SPI pins.

Note also that the RESET pin should be allowed to float and must be pulled low. Connect an external 10 kΩ resistor to DVSS. This avoids unexpected behavior in noisy environments.

DRIVING THE DAC CLOCK INPUT

The DAC clock input requires a low jitter drive signal. It is a PMOS differential pair powered from the CVDD18 supply. Each pin can safely swing up to 800 mV p-p at a common-mode voltage of about 400 mV. Though these levels are not directly LVDS-compatible, CLKP and CLKN can be driven by an ac-coupled, dc-offset LVDS signal, as shown in Figure 29.

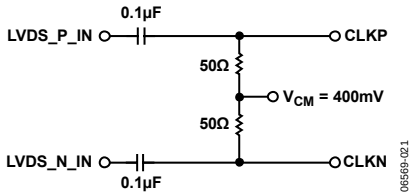


Figure 29. LVDS DAC Clock Drive Circuit

Using a CMOS or TTL clock is also acceptable for lower sample rates. It can be routed through an LVDS translator and then ac-coupled as described previously, or alternatively, it can be transformer-coupled and clamped, as shown in Figure 30.

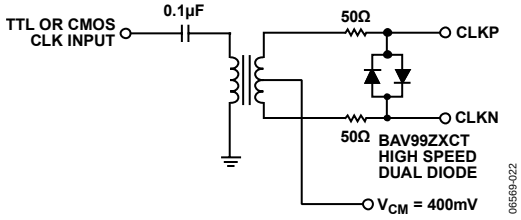


Figure 30. TTL or CMOS DAC Clock Drive Circuit

If a sine wave signal is available, it can be transformer-coupled directly to the DAC clock inputs, as shown in Figure 31.

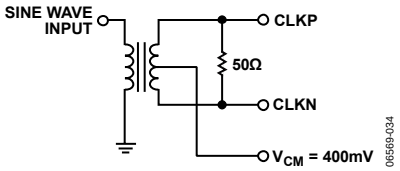


Figure 31. Sine Wave DAC Clock Drive Circuit

The 400 mV common-mode bias voltage can be derived from the CVDD18 supply through a simple divider network, as shown in Figure 32.

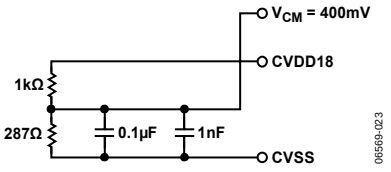


Figure 32. DAC Clock VCM Circuit

It is important to use CVDD18 and CVSS for any clock bias circuit as noise that is coupled onto the clock from another power supply is multiplied by the DAC input signal and degrades performance.

FULL-SCALE CURRENT GENERATION

The full-scale currents on DAC1 and DAC2 are functions of the current drawn through an external resistor connected to the FSADJ pin (Pin 54). The required value for this resistor is 10 kΩ. An internal amplifier sets the current through the resistor to force a voltage equal to the band gap voltage of 1.2 V. This develops a reference current in the resistor of 120 µA.

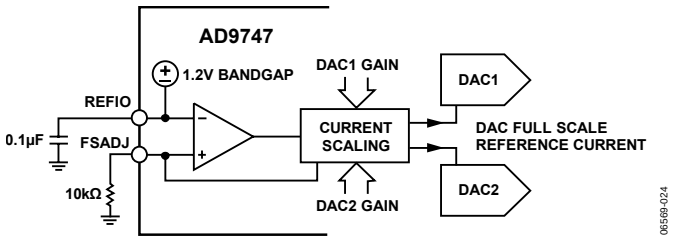


Figure 33. Reference Circuitry

REFIO (Pin 55) should be bypassed to ground with a 0.1 µF capacitor. The band gap voltage is present on this pin and can be buffered for use in external circuitry. The typical output impedance is near 5 kΩ. If desired, an external reference can be connected to REFIO to overdrive the internal reference.

Internal current mirrors provide a means for adjusting the DAC full-scale currents. The gain for DAC1 and DAC2 can be adjusted independently by writing to the DAC1FSC<9:0> and DAC2FSC<9:0> register bits. The default value of 0x01F9 for the DAC gain registers gives an I_{FS} of 20 mA, where I_{FS} equals

$$I_{FS} = \frac{1.2\text{ V}}{10{,}000} \times \left(72 + \left(\frac{3}{16} \times DAC\,\text{n}\,FSC\right)\right)$$

The full-scale output current range is 8.6 mA to 31.7 mA for register values 0x000 to 0x3FF.

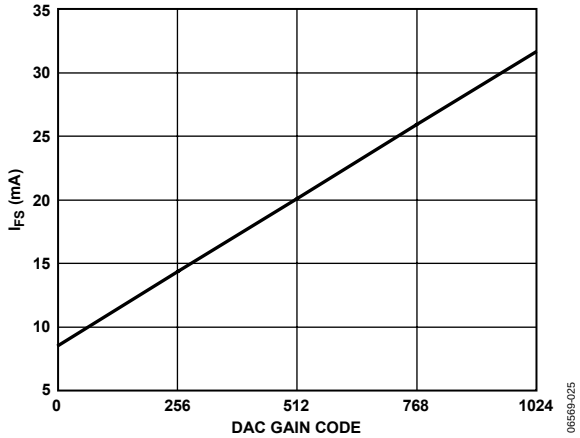


Figure 34. I_{FS} vs. DAC Gain Code

DAC TRANSFER FUNCTION

Each DAC output of the AD9741/AD9743/AD9745/AD9746/AD9747 drives complementary current outputs I_{OUTP} and I_{OUTN}. I_{OUTP} provides a near full-scale current output (I_{FS}) when all bits are high. For example,

$$DAC\ CODE = 2^N - 1$$

where:
N = 8-/10-/12-/14-/16-bits (for AD9741/AD9743/AD9745/AD9746/AD9747 respectively), and I_{OUTN} provides no current.

The current output appearing at I_{OUTP} and I_{OUTN} is a function of both the input code and I_{FS} and can be expressed as

$$I_{OUTP} = (DAC\ DATA/2^N) \times I_{FS} \quad (1)$$

$$I_{OUTN} = ((2^N - 1) - DAC\ DATA)/2^N \times I_{FS} \quad (2)$$

where $DAC\ DATA$ = 0 to $2^N - 1$ (decimal representation).

The two current outputs typically drive a resistive load directly or via a transformer. If dc coupling is required, I_{OUTP} and I_{OUTN} should be connected to matching resistive loads (R_{LOAD}) that are tied to analog common (AVSS). The single-ended voltage output appearing at the I_{OUTP} and I_{OUTN} pins is

$$V_{OUTP} = I_{OUTP} \times R_{LOAD} \quad (3)$$

$$V_{OUTN} = I_{OUTN} \times R_{LOAD} \quad (4)$$

Note that to achieve the maximum output compliance of 1 V at the nominal 20 mA output current, R_{LOAD} must be set to 50 Ω. Also note that the full-scale value of V_{OUTP} and V_{OUTN} should not exceed the specified output compliance range to maintain specified distortion and linearity performance.

There are two distinct advantages to operating the AD9741/AD9743/AD9745/AD9746/AD9747 differentially. First, differential operation helps cancel common-mode error sources associated with I_{OUTP} and I_{OUTN}, such as noise, distortion, and dc offsets. Second, the differential code dependent current and subsequent output voltage (V_{DIFF}) is twice the value of the single-ended voltage output (V_{OUTP} or V_{OUTN}), providing 2× signal power to the load.

$$V_{DIFF} = (I_{OUTP} - I_{OUTN}) \times R_{LOAD} \quad (5)$$

ANALOG MODES OF OPERATION

The AD9741/AD9743/AD9745/AD9746/AD9747 utilize a proprietary quad-switch architecture that lowers the distortion of the DAC output by eliminating a code dependent glitch that occurs with conventional dual-switch architectures. But whereas this architecture eliminates the code dependent glitches, it creates a constant glitch at a rate of 2 × f_{DAC}. For communications systems and other applications requiring good frequency domain performance, this is seldom problematic.

The quad-switch architecture also supports two additional modes of operation; mix mode and return-to-zero (RZ) mode. The waveforms of these two modes are shown in Figure 35. In mix mode, the output is inverted every other half clock cycle. This effectively chops the DAC output at the sample rate. This chopping has the effect of frequency shifting the sinc roll-off from dc to f_{DAC}. Additionally, there is a second subtle effect on the output spectrum. The shifted spectrum is shaped by a second sinc function with a first null at 2 × f_{DAC}. The reason for this shaping is that the data is not continuously varying at twice the clock rate, but is simply repeated.

In RZ mode, the output is set to midscale on every other half clock cycle. The output is similar to the DAC output in normal mode except that the output pulses are half the width and half the area. Because the output pulses have half the width, the sinc function is scaled in frequency by 2 and has a first null at 2 × f_{DAC}. Because the area of the pulses is half that of the pulses in normal mode, the output power is half the normal mode output power.

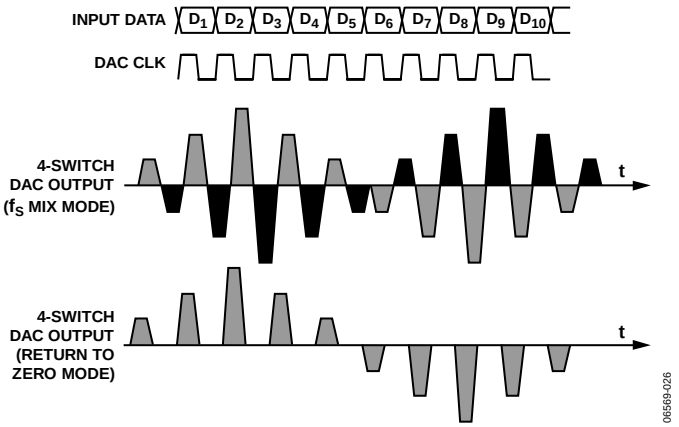


Figure 35. Mix Mode and RZ Mode DAC Waveforms

The functions that shape the output spectrums for normal mode, mix mode, and RZ mode, are shown in Figure 36. Switching between the modes reshapes the sinc roll off inherent at the DAC output. This ability to change modes in the AD9741/AD9743/AD9745/D9746/AD9747 makes the parts suitable for direct IF applications. The user can place a carrier anywhere in the first three Nyquist zones depending on the operating mode selected. The performance and maximum amplitude in all three zones are impacted by this sinc roll off depending on where the carrier is placed, as shown in Figure 36.

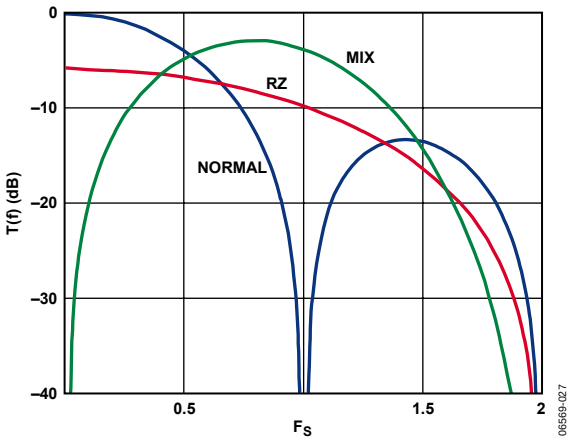


Figure 36. Transfer Function for Each Analog Operating Mode

AUXILIARY DACS

Two auxiliary DACs are provided on the AD9741/AD9743/AD9745/AD9746/AD9747. A functional diagram is shown in Figure 37. The auxiliary DACs are current output devices with two output pins, AUXP and AUXN. The active pin can be programmed to either source or sink current. When either sinking or sourcing, the full-scale current magnitude is 2 mA. The available compliance range at the auxiliary DAC outputs depends on whether the output is configured to a sink or source current. When sourcing current, the compliance voltage is 0 V to 1.6 V, but when sinking current, the output compliance voltage reduces to 0.8 V to 1.6 V. Either output can be used, but only one output of the auxiliary DAC (P or N) is active at any time. The inactive pin is always in a high impedance state (>100 kΩ).

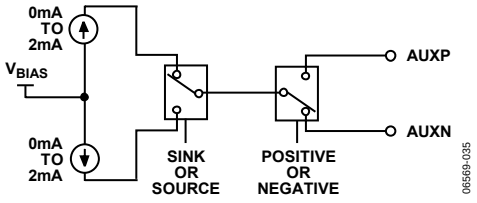


Figure 37. Auxiliary DAC Functional Diagram

In a single side band transmitter application, the combination of the input referred dc offset voltage of the quadrature modulator and the DAC output offset voltage can result in local oscillator (LO) feedthrough at the modulator output, which degrades system performance. The auxiliary DACs can be used to remove the dc offset and the resulting LO feedthrough. The circuit configuration for using the auxiliary DACs for performing dc offset correction depends on the details of the DAC and modulator interface. An example of a dc-coupled configuration with low-pass filtering is outlined in the Power Dissipation section.

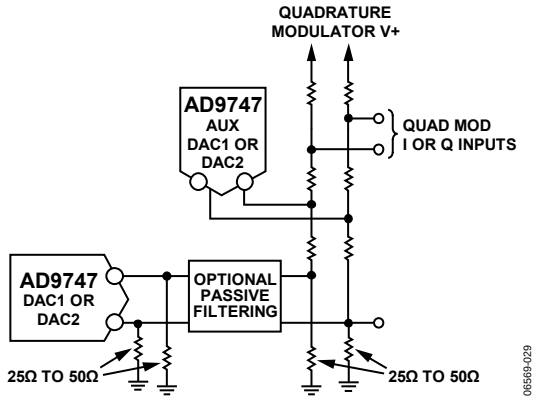


Figure 38. DAC DC Coupled to Quadrature Modulator with Passive DC Shift

POWER DISSIPATION

Figure 39 shows the power dissipation and current draw of the AD9741/AD9743/AD9745/AD9746/AD9747. It shows that the devices have a quiescent power dissipation of about 190 mW. Most of this comes from the AVDD33 supply. Total power dissipation increases about 50% as the clock rate is increased to the maximum clock rate of 250 MHz.

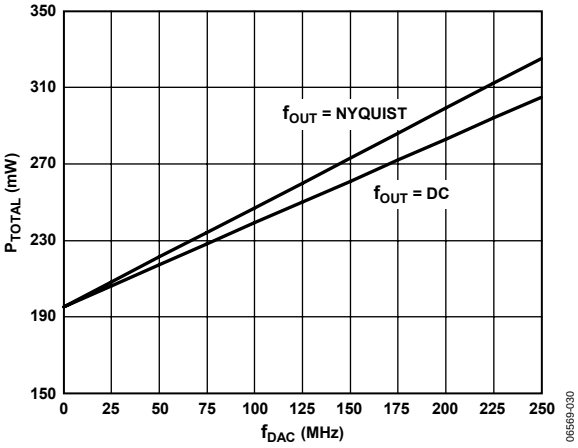


Figure 39. AD9747 Power Dissipation vs. f_{DAC}

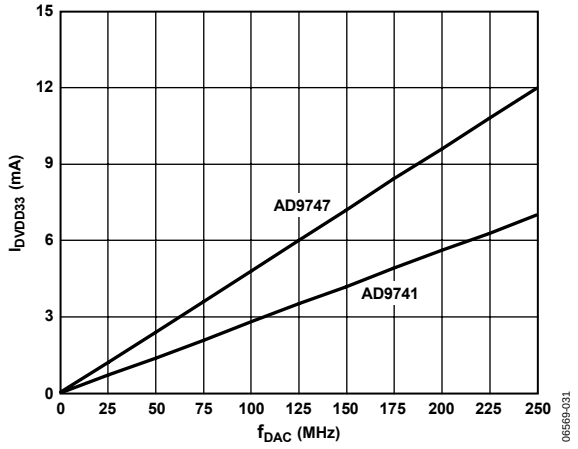


Figure 40. DVDD33 Current vs. f_{DAC}

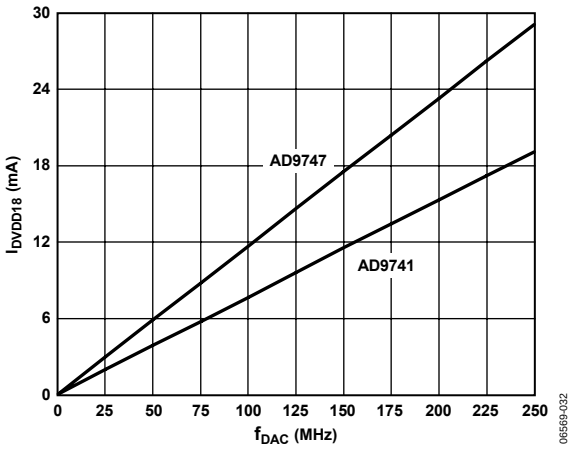


Figure 41. DVDD18 Current vs. f_{DAC}

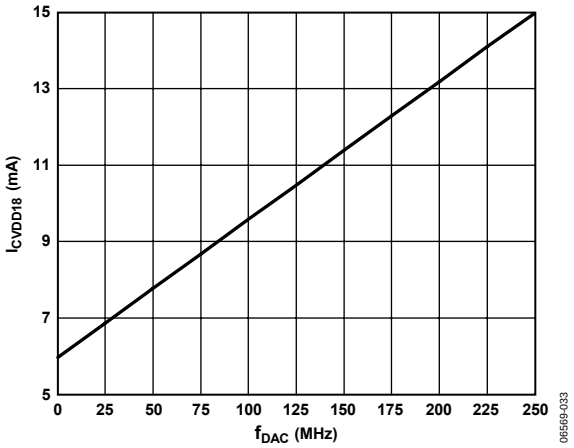


Figure 42. CVDD18 Current vs. f_{DAC}

Figure 43 shows the power consumption for each power supply domain as well as the total power consumption. Individual bars within each group display the power in full active mode (blue) vs. power for five increasing levels of power-down.

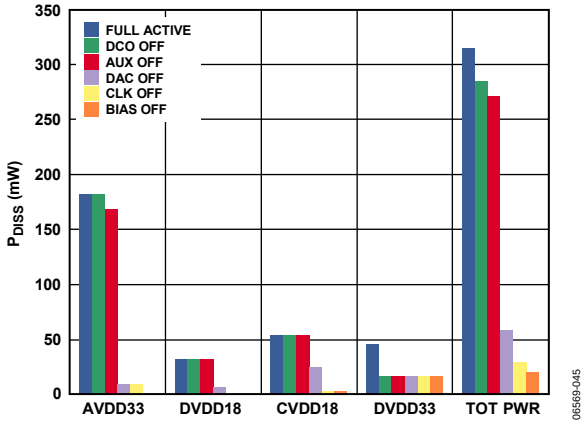


Figure 43. Power Dissipation vs. Power-Down Mode

The overall power consumption is dominated by AVDD33 and significant power savings can be achieved simply by disabling the DAC outputs. Also, disabling the DAC outputs is a significant way to conserve power and still maintain a fast wake-up time. Full power-down disables all circuitry for minimum power consumption. Note, however, that even in full power-down, there is a small power draw (25 mW) due to incoming data activity. To lower power consumption to near zero, all incoming data activity must be halted.

OUTLINE DIMENSIONS

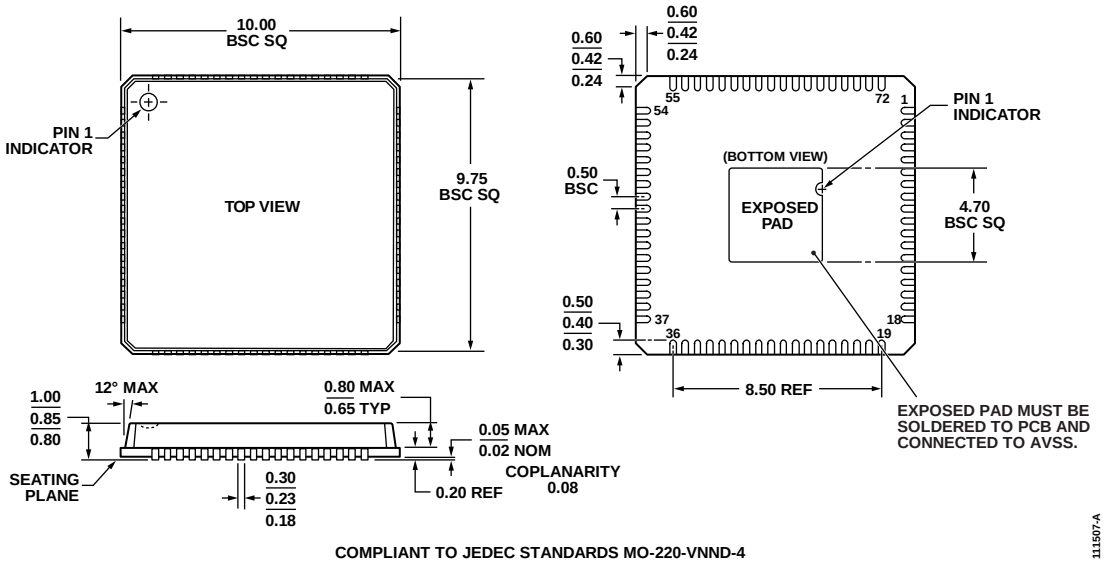


Figure 44. 72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
10 mm × 10 mm, Very Thin Quad
(CP-72-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9741BCPZ[1]	−40°C to +85°C	72-Lead LFCSP_VQ	CP-72-1
AD9741BCPZRL[1]	−40°C to +85°C	72-Lead LFCSP_VQ	CP-72-1
AD9743BCPZ[1]	−40°C to +85°C	72-Lead LFCSP_VQ	CP-72-1
AD9743BCPZRL[1]	−40°C to +85°C	72-Lead LFCSP_VQ	CP-72-1
AD9745BCPZ[1]	−40°C to +85°C	72-Lead LFCSP_VQ	CP-72-1
AD9745BCPZRL[1]	−40°C to +85°C	72-Lead LFCSP_VQ	CP-72-1
AD9746BCPZ[1]	−40°C to +85°C	72-Lead LFCSP_VQ	CP-72-1
AD9746BCPZRL[1]	−40°C to +85°C	72-Lead LFCSP_VQ	CP-72-1
AD9747BCPZ[1]	−40°C to +85°C	72-Lead LFCSP_VQ	CP-72-1
AD9747BCPZRL[1]	−40°C to +85°C	72-Lead LFCSP_VQ	CP-72-1
AD9741-EBZ[1]		Evaluation Board	
AD9743-EBZ[1]		Evaluation Board	
AD9745-EBZ[1]		Evaluation Board	
AD9746-EBZ[1]		Evaluation Board	
AD9747-EBZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

D06569-0-5/07(0)

National Semiconductor

April 8, 2009

ADC16V130

16-Bit, 130 MSPS A/D Converter with LVDS Outputs

General Description

The ADC16V130 is a monolithic high performance CMOS analog-to-digital converter capable of converting analog input signals into 16-bit digital words at rates up to 130 Mega Samples Per Second (MSPS). This converter uses a differential, pipelined architecture with digital error correction and an on-chip sample-and-hold circuit to minimize power consumption and external component count while providing excellent dynamic performance. Automatic power-up calibration enables excellent dynamic performance and reduces part-to-part variation, and the ADC16V130 could be re-calibrated at any time by asserting and then de-asserting power-down. An integrated low noise and stable voltage reference and differential reference buffer amplifier easies board level design. On-chip duty cycle stabilizer with low additive jitter allows wide duty cycle range of input clock without compromising its dynamic performance. A unique sample-and-hold stage yields a full-power bandwidth of 1.4 GHz. The digital data is provided via full data rate LVDS outputs – making possible the 64-pin, 9mm x 9mm LLP package. The ADC16V130 operates on dual power supplies +1.8V and +3.0V with a power-down feature to reduce the power consumption to very low levels while allowing fast recovery to full operation.

Features

- Dual Supplies: 1.8V and 3.0V operation
- On chip automatic calibration during power-up
- Low power consumption
- Multi-level multi-function pins for CLK/DF and PD
- Power-down and sleep modes
- On chip precision reference and sample-and-hold circuit
- On chip low jitter duty-cycle stabilizer
- Offset binary or 2's complement data format
- Full data rate LVDS output port
- 64-pin LLP package (9x9x0.8, 0.5mm pin-pitch)

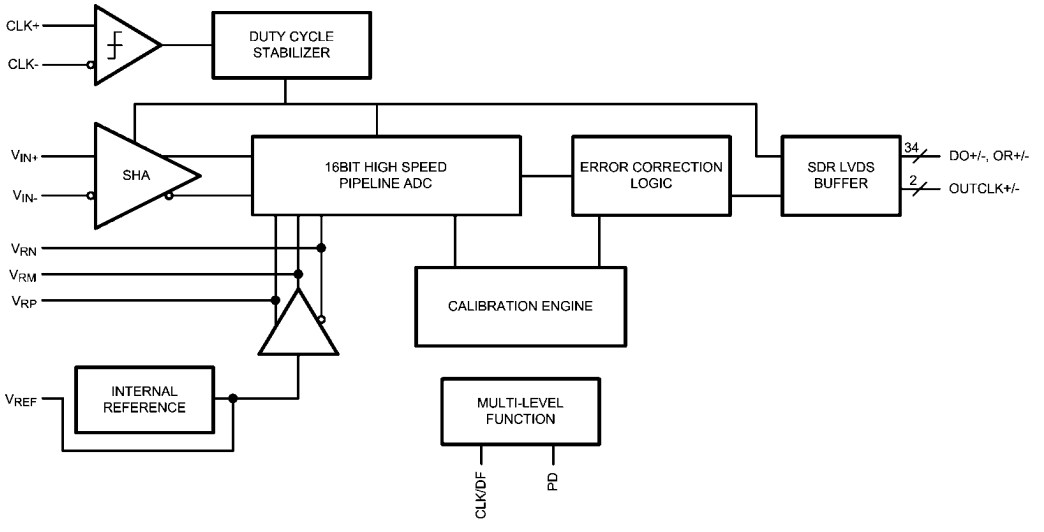
Key Specifications

■ Resolution	16 Bits
■ Conversion Rate	130 MSPS
■ SNR	
(f_{IN} = 10MHz)	78.5 dBFS (typ)
(f_{IN} = 70MHz)	77.8 dBFS (typ)
(f_{IN} = 160MHz)	76.7 dBFS (typ)
■ SFDR	
(f_{IN} = 10 MHz)	95.5 dBFS (typ)
(f_{IN} = 70MHz)	92.0 dBFS (typ)
(f_{IN} = 160MHz)	90.6 dBFS (typ)
■ Full Power Bandwidth	1.4 GHz (typ)
■ Power Consumption	
Core	650 mW (typ)
LVDS Driver	105 mW (typ)
Total	755 mW (typ)
■ Operating Temperature Range	-40°C ~ 85°C

Applications

- High IF Sampling Receivers
- Multi-carrier Base Station Receivers
  GSM/EDGE, CDMA2000, UMTS, LTE and WiMax
- Test and Measurement Equipment
- Communications Instrumentation
- Data Acquisition
- Portable Instrumentation

Block Diagram



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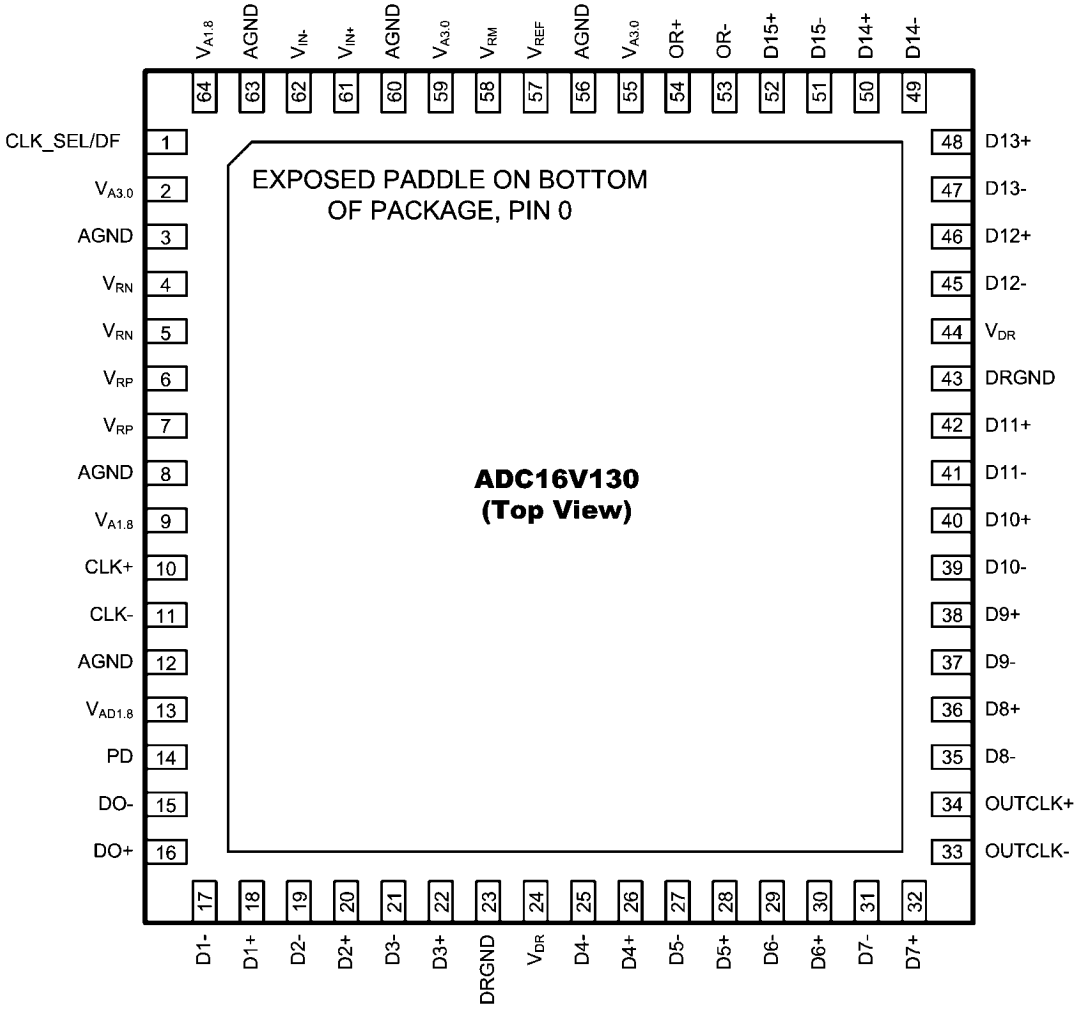
Connection Diagram



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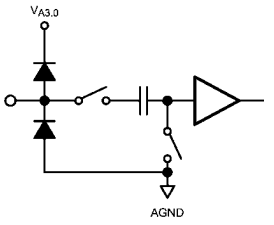
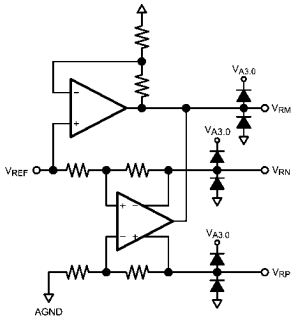
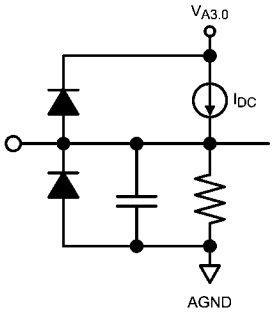
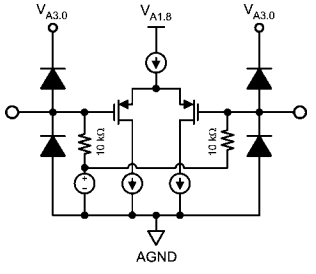
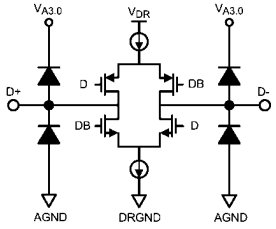
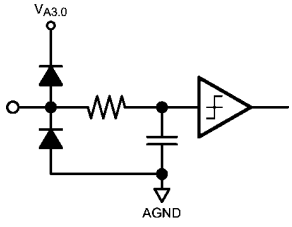
Ordering Information

Industrial (−40°C ≤ T_A ≤ +85°C)	Package
ADC16V130CISQ	64 Pin LLP
ADC16V130EB	Evaluation Board

Pin Descriptions

Pin No.	Symbol	Equivalent Circuit	Function and Connection
ANALOG I/O			
61	V_{IN+}		Differential analog input pins. The differential full-scale input signal level is 2.4Vpp as default. Each input pin signal centered on a common mode voltage, V_{CM}.
62	V_{IN-}		
6,7	V_{RP}		Upper reference voltage. This pin should not be used to source or sink current. The decoupling capacitor to AGND (low ESL 0.1µF) should be placed very close to the pin to minimize stray inductance. V_{RP} needs to be connected to V_{RN} through a low ESL 0.1µF and a low ESR 10µF capacitors in parallel.
4,5	V_{RN}		Lower reference voltage. This pin should not be used to source or sink current. The decoupling capacitor to AGND (low ESL 0.1µF) should be placed very close to the pin to minimize stray inductance. V_{RN} needs to be connected to V_{RP} through a low ESL 0.1µF and a low ESR 10µF capacitors in parallel.
58	V_{RM}		Common mode voltage The decoupling capacitor to AGND (low ESL 0.1µF) should be placed as close to the pin as possible to minimize stray inductance. It is recommended to use V_{RM} to provide the common mode voltage for the differential analog inputs.
57	V_{REF}		Internal reference voltage output / External reference voltage input. By default, this pin is the output for the internal 1.2V voltage reference. This pin should not be used to sink or source current and should be decoupled to AGND with a 0.1µF, low ESL capacitor. The decoupling capacitors should be placed as close to the pins as possible to minimize inductance and optimize ADC performance. The size of decoupling capacitor should not be larger than 0.1µF, otherwise dynamic performance after power-up calibration can drop due to the long V_{REF} settling. This pin can also be used as the input for a low noise external reference voltage. The output impedance for the internal reference at this pin is 9 kΩ and this can be overdriven provided the impedance of the external source is <<9 kΩ. Careful decoupling is just as essential when an external reference is used. The 0.1µF low ESL decoupling capacitor should be placed as close to this pin as possible. The Input differential voltage swing is equal to 2 * V_{REF}.
10	CLK+		Differential clock input pins. DC biasing is provided internally. For single-ended clock mode, drive CLK+ through AC coupling while decoupling CLK- pin to AGND.
11	CLK–		

Pin No.	Symbol	Equivalent Circuit	Function and Connection
DIGITAL I/O			
15 – 22 25 – 32 35 – 42 45 – 52	D0+/- to D3+/- D4+/- to D7+/- D8+/- to D11+/- D12+/- to D15 +/-		LVDS Data Output. The 16-bit digital output of the data converter is provided on these ports in a full data rate manner. A 100 Ω termination resistor must be placed between each pair of differential signals at the far end of the transmission line.
53, 54	OR+/-		Over-Range Indicator. Active High. This output is set High when analog input signal exceeds full scale of 16 bit conversion range (<0,> 65535). This signal is asserted coincidently with the over-range data word. A 100 Ω termination resistor must be placed between the differential signals at the far end of the transmission.
33, 34	OUTCLK+/-		Output Clock. This pin is used to clock the output data. It has the same frequency as the sampling clock. One word of data is output in each cycle of this signal. A 100 Ω termination resistor must be placed between the differential clock signals at the far end of the transmission line. The rising edge of this signal should be used to capture the output data. See the detail Section on *Timing Diagrams* .
14	PD		This is a three-state pin. **PD = $V_{A3.0}$**, then Power Down is enabled. In the Power Down state, only the reference voltage circuitry remains active and power dissipation is reduced. **PD =$V_{A3.0}$ * (2/3)**, then Sleep mode is enabled. In Sleep mode is similar to Power Down mode - it consumes more power but has a faster recovery time. **PD = AGND**, then Normal operation mode is turned on.
1	CLK_SEL/DF		This is a four-state pin controlling two parameters: input clock selection and output data format. **CLK_SEL/DF = $V_{A3.0}$**, then CLK+ and CLK– are configured as a differential clock input and the output data format is 2's complement. **CLK_SEL/DF = $V_{A3.0}$ * (2/3)**, then CLK+ and CLK– are configured as a differential clock input and the output data format is offset binary. **CLK_SEL/DF = $V_{A3.0}$ * (1/3)**, then CLK+ is configured as a single-ended clock input and CLK– should be tied to AGND. The output data format is 2's complement. **CLK_SEL/DF = AGND**, then CLK+ is configured as a single-ended clock input and CLK– should be tied to AGND. The output data format is offset binary.
POWER SUPPLIES			
2, 55, 59	$V_{A3.0}$	Analog Power	3.0V Analog Power Supply. These pins should be connected to a quiet source and should be decoupled to AGND with 0.1µF capacitors located close to the power pins.
9, 64	$V_{A1.8}$	Analog Power	1.8V Analog Power Supply. These pins should be connected to a quiet source and should be decoupled to AGND with 0.1µF capacitors located close to the power pins.
13	$V_{AD1.8}$	Analog/Digital Power	1.8V Analog/Digital Power Supply. These pins should be connected to a quiet source and should be decoupled to AGND with 0.1µF capacitors located close to the power pins.
0, 3, 8, 12, 56, 60, 63	AGND	Analog Ground	Analog Ground Return. The exposed pad (Pin 0) on back of the package must be soldered to ground plane to ensure rated performance.

Pin No.	Symbol	Equivalent Circuit	Function and Connection
24, 44	V_{DR}	Power	Output Driver Power Supply. This pin should be connected to a quiet voltage source and be decoupled to DRGND with a 0.1µF capacitor close to the power pins.
23, 43	DRGND	Ground	Output Driver Ground Return.

Absolute Maximum Ratings (Notes , 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ($V_{A3.0}$)	−0.3V to 4.2V
Supply Voltage ($V_{A1.8}$, $V_{AD1.8}$, V_{DR})	−0.3V to 2.35V
Voltage at any Pin except D0-D15, OVR, OUTCLK, CLK, V_{IN}	−0.3V to ($V_{A3.0}$ +0.3V) (Not to exceed 4.2V)
Voltage at CLK, V_{IN} Pins	-0.3V to (V_{DR} +0.3V) (Not to exceed 2.35V)
Voltage at D0-D15, OR, OUTCLK Pins	0.3V to (V_{DR} + 0.3V) (Not to exceed 2.35V)
Input Current at any pin (Note 3)	5 mA
Storage Temperature Range	-65°C to +150°C
ESD Rating(Note 4)	
Machine Model	200 V
Human Body Model	2000 V
Soldering process must comply with National Semiconductor's Reflow Temperature Profile specifications. Refer to www.national.com/packaging. (Note 5)	

Operating Ratings (Notes 1,)

Specified Temperature Range:	-40°C to +85°C
3.0V Analog Supply Voltage Range: ($V_{A3.0}$)	+2.7V to +3.6V
1.8V Supply Voltage Range: $V_{A1.8}$, $V_{AD1.8}$, V_{DR}	+1.7V to +1.9V
Clock Duty Cycle	30/70 %

Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply: $V_{A3.0}$ = +3.0V, $V_{A1.8}$ = $V_{AD1.8}$ = V_{DR} = +1.8V, f_{CLK} = 130 MSPS, A_{IN} = -1dBFS, LVDS Rterm = 100 Ω, C_L = 5 pF. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Typical (Note 6)	Limits	Units (Limits)
STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes			**16**	Bits (min)
INL	Integral Non Linearity		±1.5		LSB
DNL	Differential Non Linearity		±0.45		LSB
PGE	Positive Gain Error		-4.2		%FS
NGE	Negative Gain Error		3.7		%FS
V_{OFF}	Offset Error (V_{IN}+ = V_{IN}−)		0.12		%FS
	Under Range Output Code		0	**0**	
	Over Range Output Code		65535	**65535**	
REFERENCE AND ANALOG INPUT CHARACTERISTICS					
V_{CM}	Common Mode Input Voltage	V_{RM} is the common mode reference voltage	V_{RM} ±0.05		V
V_{RM}	Reference Ladder Midpoint Output Voltage		1.15		V
V_{REF}	Internal Reference Voltage		1.20		V
	Differential Analog Input Range	Internal Reference	2.4		V_{PP}

Dynamic Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply: $V_{A3.0}$ = +3.0V, $V_{A1.8}$ = $V_{AD1.8}$ = V_{DR} = +1.8V, f_{CLK} = 130 MSPS, A_{IN} = -1dBFS, LVDS Rterm = 100 Ω, C_L = 5 pF. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \leq T_A \leq T_{MAX}$.** All other limits apply for T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Typ	Limits	Units
	Resolution with no missing codes			**16**	Bits
DR	Dynamic Range	0V analog input is applied	79		dBFS
SNR	Signal-to-Noise Ratio (Note 9)	Fin = 10 MHz	78.5		dBFS
		Fin = 40 MHz	78.2		dBFS
		Fin = 70 MHz	77.8		dBFS
		Fin = 160 MHz	76.7	**75.5**	dBFS
		Fin = 240 MHz	75.6		dBFS
SFDR	Single-tone Spurious Free Dynamic Range (Note 9)	Fin = 10 MHz	95.5		dBFS
		Fin = 40 MHz	91		dBFS
		Fin = 70 MHz	92		dBFS
		Fin = 160 MHz	90.6	**87**	dBFS
		Fin = 240 MHz	85.3		dBFS
THD	Total Harmonic Distortion (Note 9)	Fin = 10 MHz	-91.5		dBFS
		Fin = 40 MHz	-88.4		dBFS
		Fin = 70 MHz	-89.4		dBFS
		Fin = 160 MHz	-87.1	**-81**	dBFS
		Fin = 240 MHz	-82.8		dBFS
H2	Second-order Harmonic(Note 9)	Fin = 10 MHz	-95.5		dBFS
		Fin = 40 MHz	-104.1		dBFS
		Fin = 70 MHz	-95.6		dBFS
		Fin = 160 MHz	-91.5	**-88**	dBFS
		Fin = 240 MHz	-85.3		dBFS
H3	Third-order Harmonic (Note 9)	Fin = 10 MHz	-98.3		dBFS
		Fin = 40 MHz	-89.4		dBFS
		Fin = 70 MHz	-92		dBFS
		Fin = 160 MHz	-90.6	**-87**	dBFS
		Fin = 240 MHz	-87.8		dBFS
Spur-H2/3	Worst Harmonic or Spurious Tone excluding H2 and H3(Note 9)	Fin = 10 MHz	106		dBFS
		Fin = 40 MHz	103.2		dBFS
		Fin = 70 MHz	104.1		dBFS
		Fin = 160 MHz	101.5	**94**	dBFS
		Fin = 240 MHz	98.4		dBFS
SINAD	Signal-to-Noise and Distortion Ratio (Note 9)	Fin = 10 MHz	78.3		dBFS
		Fin = 40 MHz	77.8		dBFS
		Fin = 70 MHz	77.5		dBFS
		Fin = 160 MHz	76.3		dBFS
		Fin = 240 MHz	74.8		dBFS
ENOB	Effective Number of Bits	Fin = 10 MHz	12.7		Bits
		Fin = 40 MHz	12.6		Bits
		Fin = 70 MHz	12.6		Bits
		Fin = 160 MHz	12.4		Bits
		Fin = 240 MHz	12.1		Bits
	Full Power Bandwidth	-3dB Compression Point	1.4		GHz

Power Supply Electrical Characteristics

Unless otherwise specified, the following specifications apply: $V_{A3.0}$ = +3.0V, $V_{A1.8}$ = $V_{AD1.8}$ = V_{DR} = +1.8V, f_{CLK} = 130 MSPS, A_{IN} = -1dBFS, LVDS Rterm = 100 Ω, C_L = 5 pF. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Typical	Limits	Units (Limits)
$I_{A3.0}$	Analog 3.0V Supply Current	Full Operation(Note 12)	174.5	208	mA (max)
$I_{A1.8}$	Analog 1.8V Supply Current	Full Operation(Note 12)	36	42	mA (max)
$I_{AD1.8R}$	Digital 1.8V Supply Current	Full Operation (Note 12)	34	41	mA (max)
I_{DR}	Output Driver Supply Current	Full Operation	58.3		mA
	Core Power Consumption	Excludes I_{DR} (Note 12)	650	773	mW (max)
	Driver Power Consumption	Current drawn from the V_{DR} supply; Fin = 10 MHz Rterm = 100Ω	105		mW
	Total Power Consumption	Normal operation; Fin = 10 MHz	755		mW
		Power down state, with external clock	3		mW
		Sleep state, with external clock	30		mW

LVDS Electrical Characteristics

Unless otherwise specified, the following specifications apply: $V_{A3.0}$ = +3.0V, $V_{A1.8}$ = $V_{AD1.8}$ = V_{DR} = +1.8V, f_{CLK} = 130 MSPS, A_{IN} = -1dBFS, LVDS Rterm = 100 Ω, C_L = 5 pF. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVDS DC SPECIFICATIONS (apply to pins DO to D15, OR)						
V_{OD}	Output Differential Voltage	100 Ω Differential Load	175	250	325	mV
V_{OS}	Output Offset Voltage	100 Ω Differential Load	1.15	1.2	1.25	V
I_{OS}	Output Short Circuit Current	0 Ω Differential Load		2.5		mA
I_{OZ}	Output Open Circuit Current	Termination is open	-20	± 1	20	µA

Timing Specifications

Unless otherwise specified, the following specifications apply: V_{IN} = -1dBFS, AGND = DRGND = 0V, $V_{A3.0}$= +3.0V, $V_{A1.8}$ = $V_{AD1.8}$ = V_{DR} = +1.8V, Internal V_{REF} = +1.2V, f_{CLK} = 130 MHz, V_{CM} = V_{RM}, C_L = 5 pF, Single-Ended Clock Mode, Offset Binary Format. Typical values are for T_A = 25°C. Timing measurements are taken at 50% of the signal amplitude. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C, unless otherwise noted.

Parameter	Conditions	Typ	Limits	Units
Input Clock Frequency			**130**	MHz (max)
Minimum Clock Frequency		1		MHz (min)
Data Output Setup Time (Tsu) (Note 10)	Measured @ Vdr/2; Fclk = 130 MHz.	3.3	**2.5**	nS (min)
Data Output Hold Time (Th) (Note 10)	Measured @ Vdr/2; Fclk = 130 MHz.	3.3	**2.5**	nS (min)
Pipeline Latency(Note 11)		11		Clock Cycles
Aperture Jitter		80		fS rms
Power-Up Time	From assertion of Power to specified level of performance.	0.5+ 10^3*(2^{22}+2^{16})/FCLK		mS
Power-Down Recovery Time	From de-assertion of power down mode to output data available.	0.1+ 10^3*(2^{19}+2^{16})/FCLK		mS
Sleep Recovery Time	From de-assertion of sleep mode to output data available.	100		µS

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is guaranteed to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.

Note 2: All voltages are measured with respect to GND = AGND = DRGND = 0V, unless otherwise specified.

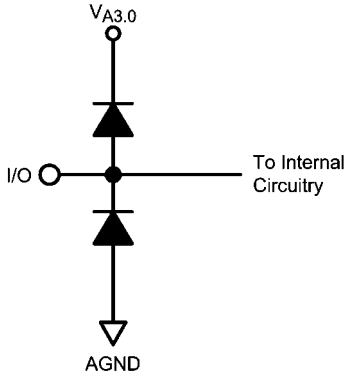
Note 3: When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or V_{IN} > V_A), the current at that pin should be limited to ±5 mA. The ±50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of ±5 mA to 10.

Note 4: Human Body Model is 100 pF discharged through a 1.5 kΩ resistor. Machine Model is 220 pF discharged through 0 Ω.

Note 5: Reflow temperature profiles are different for lead-free and non-lead-free packages.

Note 6: Typical figures are at T_A = 25°C and represent most likely parametric norms at the time of product characterization. The typical specifications are not guaranteed.

Note 7: The inputs are protected as shown below. Input voltage magnitudes above $V_{A3.0}$ or below GND will not damage this device, provided current is limited per (Note 3). However, errors in the A/D conversion can occur if the input goes above 2.6V or below GND as described in the Operating Ratings section.



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Note 8: The input capacitance is the sum of the package/pin capacitance and the sample and hold circuit capacitance.

Note 9: This parameter is specified in units of dBFS – indicating the equivalent value that would be attained with a full-scale input signal.

Note 10:) This parameter is a function of the CLK frequency - increasing directly as the frequency is lowered. At frequencies less than 130 MHz, use the following formulae to calculate the setup and hold times:

For Data and OR+/- Outputs: Tsu = ½*Tp – 0.5 ns (typical)

For Data and OR+/- Outputs: Th = ½*Tp – 0.5 ns (typical)

where Tp = CLK input period = OUTCLK period

Note 11: Input signal is sampled with the falling edge of the CLK input.

Note 12: This parameter is guaranteed only at 25°C. For power dissipation over temperature range, refer to Core Power vs. Temperature plot in *Typical Performance Characteristics, Dynamic Performance*

Specification Definitions

APERTURE DELAY is the time after the falling edge of the clock to when the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

CLOCK DUTY CYCLE is the ratio of the time during one cycle that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

COMMON MODE VOLTAGE (V_{CM}) is the common DC voltage applied to both input terminals of the ADC.

CONVERSION LATENCY is the number of clock cycles between initiation of conversion and the time when data is presented to the output driver stage. Data for any given sample is available at the output pins the Pipeline Delay plus the Output Delay after the sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated as:

Gain Error = Positive Full Scale Error – Negative Full Scale Error

It can also be expressed as Positive Gain Error and Negative Gain Error, which are calculated as:

PGE = Positive Full Scale Error - Offset Error
NGE = Offset Error - Negative Full Scale Error

INTEGRAL NON LINEARITY (INL) is a measure of the deviation of each individual code from a best fit straight line. The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the intermodulation products to the total power in the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is $V_{FS}/2^n$, where "V_{FS}" is the full scale input voltage and "n" is the ADC resolution in bits.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC16V130 is guaranteed not to have any missing codes.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL SCALE ERROR is the difference between the actual first code transition and its ideal value of ½ LSB above negative full scale.

OFFSET ERROR is the difference between the two input voltages ($V_{IN+} - V_{IN-}$) required to cause a transition from code 32767LSB and 32768LSB with offset binary data format.

PIPELINE DELAY (LATENCY) See CONVERSION LATENCY.

POSITIVE FULL SCALE ERROR is the difference between the actual last code transition and its ideal value of 1½ LSB below positive full scale.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the power of input signal to the total power of all other spectral components below one-half the sampling frequency, not including harmonics and DC.

SIGNAL TO NOISE AND DISTORTION (SINAD) Is the ratio, expressed in dB, of the power of the input signal to the total power of all of the other spectral components below half the clock frequency, including harmonics but excluding DC.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the power of input signal and the peak spurious signal power, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB, of the total power of the first seven harmonic to the input signal power. THD is calculated as:

$$THD = 20\log_{10}\sqrt{\frac{f_2^2 + f_3^2 + \ldots + f_8^2}{f_1^2}}$$

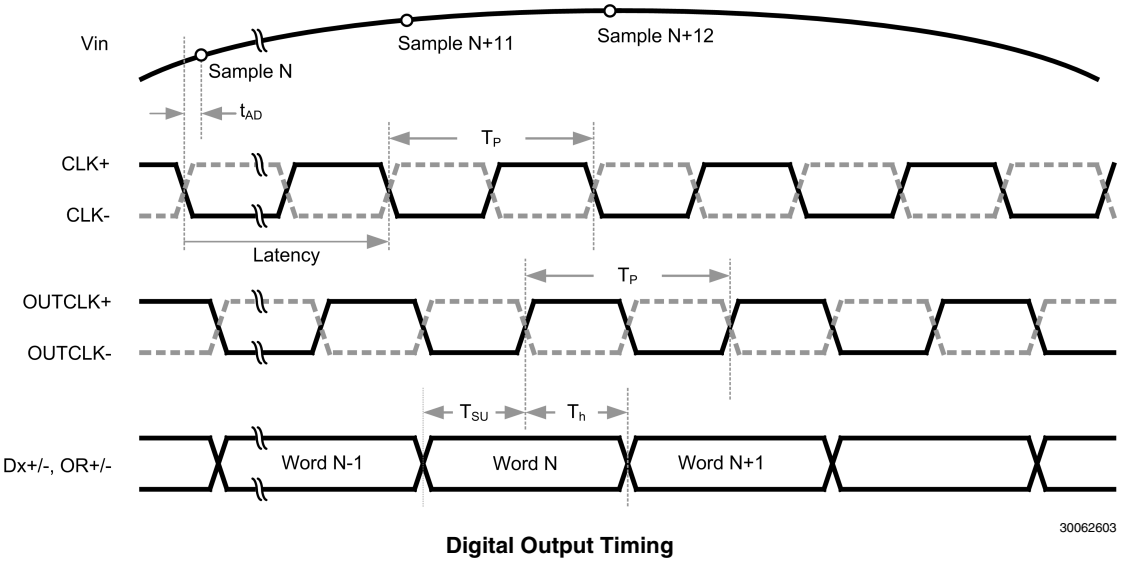
where f_1^2 is the power of the fundamental frequency and f_2^2 through f_8^2 are the powers of the first seven harmonics in the output spectrum.

SECOND HARMONIC DISTORTION (2ND HARM or H2) is the difference expressed in dB, from the power of its 2nd harmonic level to the power of the input signal.

THIRD HARMONIC DISTORTION (3RD HARM or H3) is the difference expressed in dB, from the power of the 3nd harmonic level to the power of the input signal.

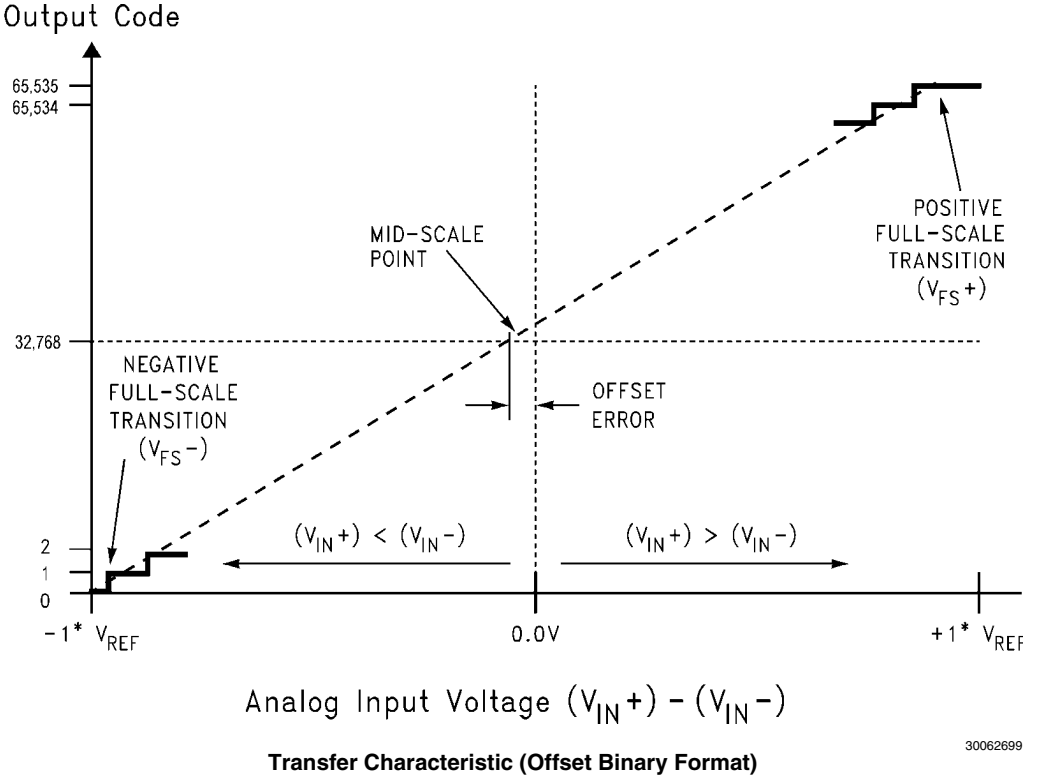
HIGHEST SPURIOUS EXCEPT H2 and H3 (Spur-H2/3) is the difference, expressed in dB, between the power of input signal and the peak spurious signal power except H2 and H3, where a spurious signal is any signal present in the output spectrum that is not present at the input.

Timing Diagrams



Digital Output Timing

Transfer Characteristic

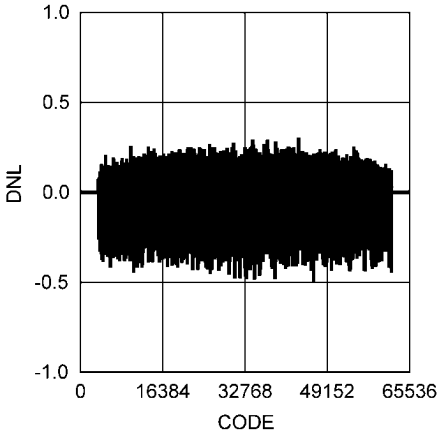


Transfer Characteristic (Offset Binary Format)

Typical Performance Characteristics, DNL, INL

Unless otherwise noted, these specifications apply: $V_{A3.0}$= +3.0V, $V_{A1.8}$, $V_{AD1.8}$, V_{DR} = 1.8V, f_{CLK} = 130 MSPS. Differential Clock Mode, Offset Binary Format. LVDS Rterm = 100 Ω. C_L = 5 pF. Typical values are at T_A = +25°C. Fin = 10MHz with –1dBFS.

DNL



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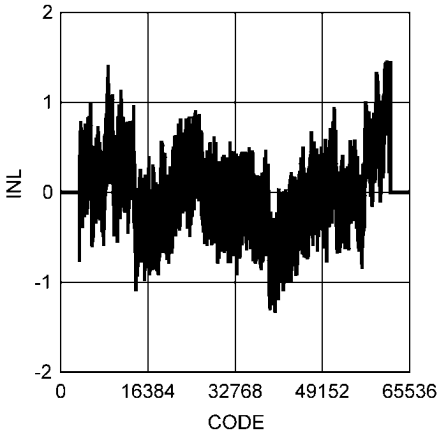
INL



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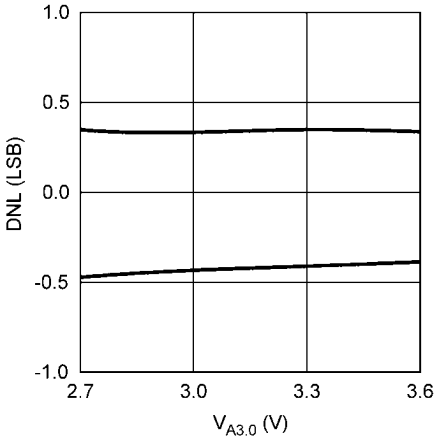
DNL vs.$V_{A3.0}$



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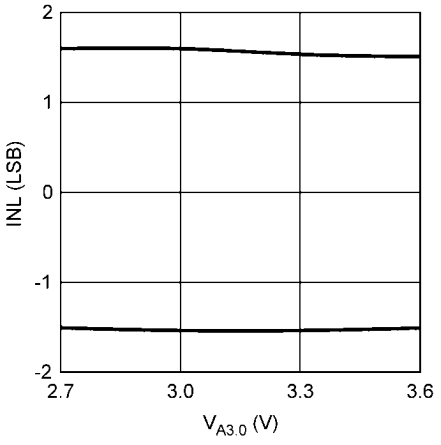
INL vs .$V_{A3.0}$



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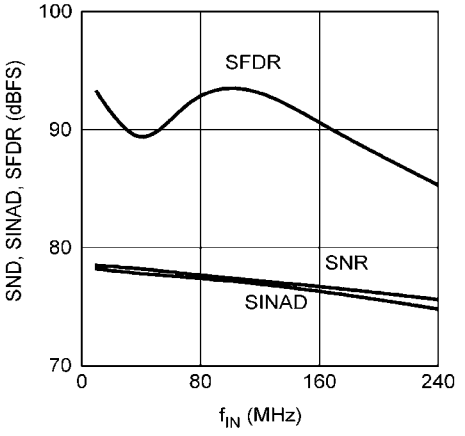
Typical Performance Characteristics, Dynamic Performance

Unless otherwise noted, these specifications apply: $V_{A3.0}$= +3.0V, $V_{A1.8}$, $V_{AD1.8}$, V_{DR} = 1.8V, f_{CLK} = 130 MSPS. Differential Clock Mode, Offset Binary Format. LVDS Rterm = 100 Ω. C_L = 5 pF. Typical values are at T_A = +25°C. Fin = 160MHz with –1dBFS..

SNR, SINAD, SFDR vs. f_{IN}



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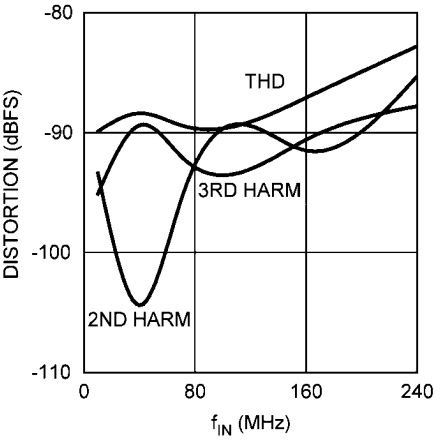
DISTORTION vs. f_{IN}



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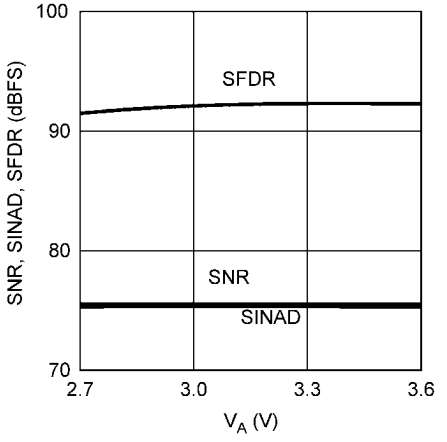
SNR, SINAD, SFDR vs. $V_{A3.0}$



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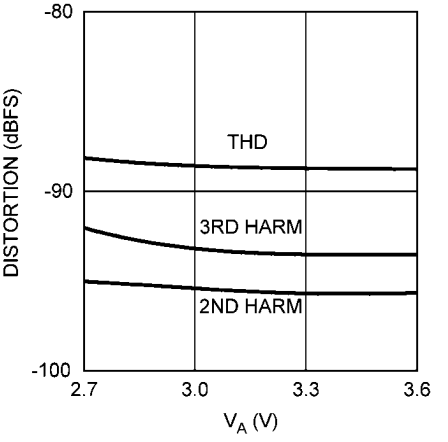
DISTORTION vs. $V_{A3.0}$



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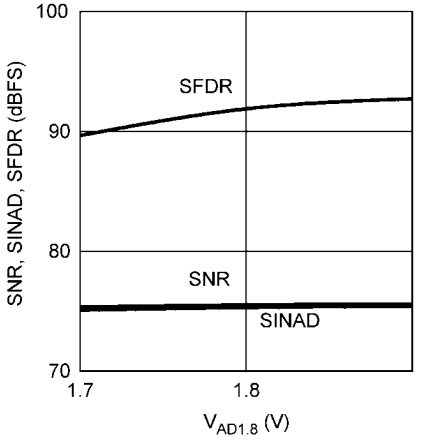
SNR, SINAD, SFDR vs. $V_{AD1.8}$



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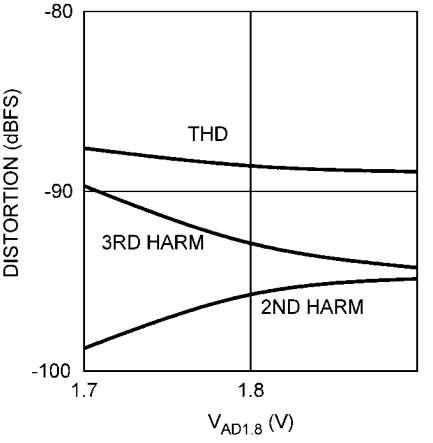
DISTORTION vs. $V_{AD1.8}$



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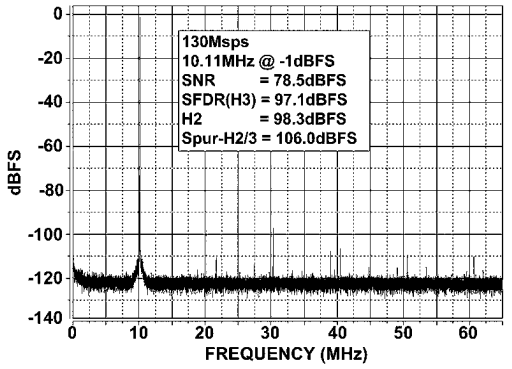
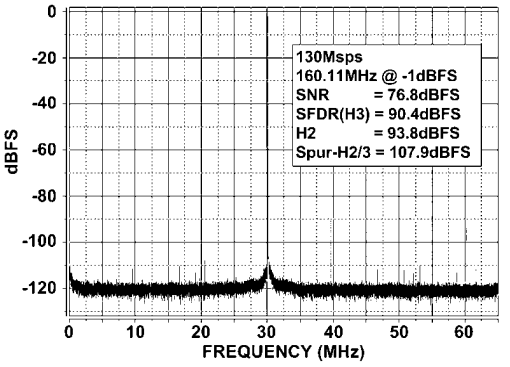
Spectral Response @ 10.11 MHz



30062619

Spectral Response @ 160.11 MHz



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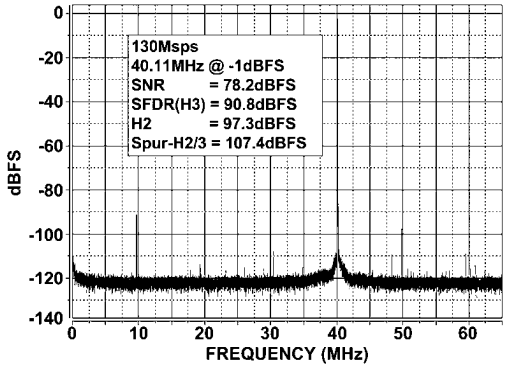
Spectral Response @ 40.11 MHz



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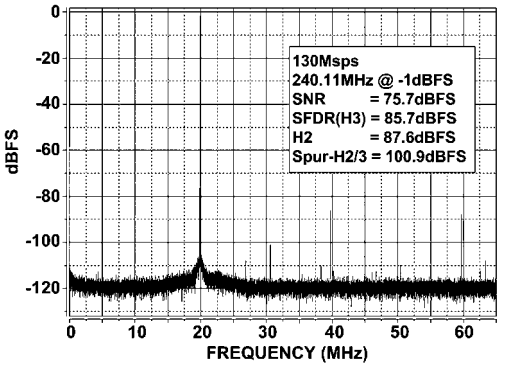
Spectral Response @ 240.11 MHz



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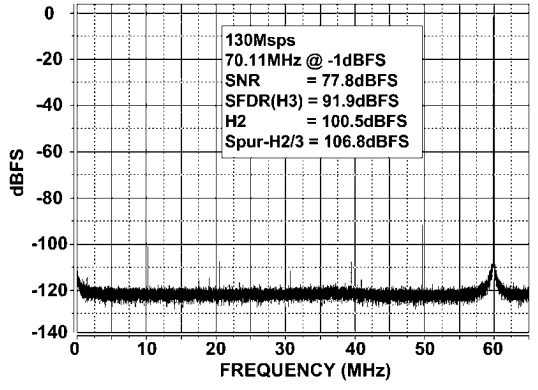
Spectral Response @ 70.11 MHz



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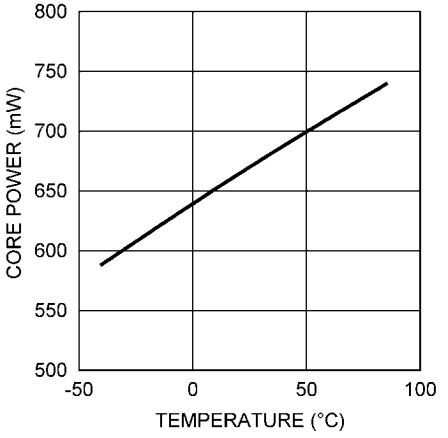
Core Power vs. Temperature (Excludes I_{DR})



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Functional Description

Operating on dual +1.8 and +3.0V supplies, the ADC16V130 digitizes a differential analog input signals to 16 bits, using a differential pipelined architecture with error correction circuitry and an on-chip sample-and-hold circuit to ensure maximum performance. The user has the choice of using an internal 1.2V stable reference, or using an external 1.2V reference. Internal 1.2V reference has high output impedance of > 9 kΩ and can be easily over-driven by external reference. Two multi-level multi-function pins can program data format, clock mode, power down and sleep mode.

ADC Architecture

The ADC16V130 architecture consists of a highly linear and wide bandwidth sample-and-hold circuit, followed by a switched capacitor pipeline ADC. Each stage of the pipeline ADC consists of low resolution flash sub-ADC and an inter-stage multiplying digital-to-analog converter (MDAC), which is a switched capacitor amplifier with a fixed stage signal gain and DC level shifting circuits. The amount of DC level shifting is dependent on sub-ADC digital output code. 16bit final digital output is the result of the digital error correction logic, which receives digital output of each stage including redundant bits to correct offset error of each sub-ADC.

Applications Information

1.0 OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC16V130:

$2.7V \le V_{A3.0} \le 3.6V$

$1.7V \le V_{A1.8} \le 1.9V$

$1.7V \le V_{AD1.8} \le 1.9V$

$1.7V \le V_{DR} \le 1.9V$

$5\ MSPS \le F_{CLK} \le 130\ MSPS$

$V_{REF} \le 1.2V$

$V_{CM} = 1.15V$ (from V_{RM})

2.0 ANALOG INPUTS

Analog input circuit of the ADC16V130 is a differential switched capacitor sample-and-hold circuit (see *Figure 1*) that provides optimum dynamic performance wide input frequency range with minimum power consumption. The clock signal alternates sample mode (Q_S) and hold mode (Q_H). An integrated low jitter duty cycle stabilizer ensures constant optimal sample and hold time over wide range of input clock duty cycle. The duty cycle stabilizer is always turned on during normal operation.

During sample mode, analog signals (V_{IN+}, V_{IN-}) are sampled across two sampling capacitor (C_S) while the amplifier in the sample-and-hold circuit is idle. The dynamic performance of the ADC16V130 is likely determined during sampling mode. The sampled analog inputs (V_{IN+}, V_{IN-}) are held during hold mode by connecting input side of the sampling capacitors to output of the amplifier in the sample-and-hold circuit while driving pipeline ADC core.

The signal source, which drives the ADC16V130, is recommended to have source impedance less than 100 Ω over wide frequency range for optimal dynamic performance.

A shunt capacitor can be placed across the inputs to provide high frequency dynamic charging current during sample mode and also absorb any switching charge coming from the ADC16V130. A shunt capacitor can be placed across each input to GND for similar purpose. Smaller physical size and low ESR and ESL shunt capacitor is recommended.

The value of shunt capacitor should be carefully chosen to optimize the dynamic performance at certain input frequency range. Larger value shunt capacitors can be used for low input frequency range, but the value has to be reduced at high input frequency range.

Balancing impedance at positive and negative input pin over entire signal path must be ensured for optimal dynamic performance.

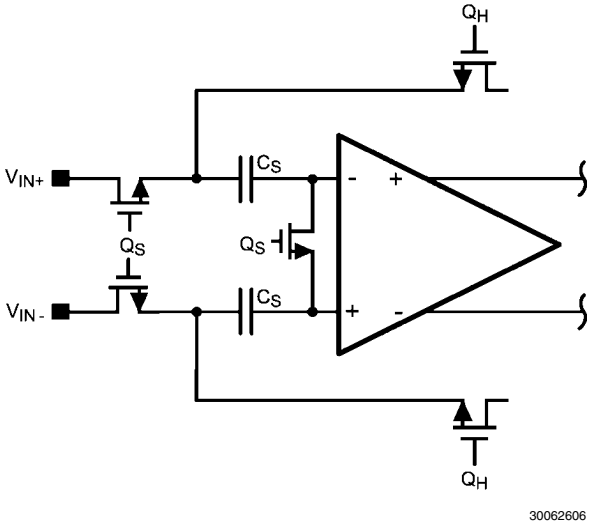

FIGURE 1. Simplified Switched-Capacitor Sample-and-hold Circuit

2.1 Input Common Mode

The analog inputs of the ADC16V130 are not internally dc biased and the range of input common mode is very narrow. Hence it is highly recommended to use the common mode voltage (V_{RM}, typically 1.15V) as input common mode for optimal dynamic performance regardless of DC and AC coupling applications. Input common mode signal must be decoupled with low ESL 0.1µF at the far end of load point to minimize

noise performance degradation due to any coupling or switching noise between the ADC16V130 and input driving circuit.

2.2 Driving Analog Inputs

For low frequency applications, either a flux or balun transformer can convert single-ended input signal into differential and drive the ADC16V130 without additive noise. An example is shown in *Figure 2*. V_{RM} pin is used to bias the input common mode by connecting the center tap of the transformer's secondary ports. Flux transformer is used for this example, but AC coupling capacitors should be added once balun type transformer is used.

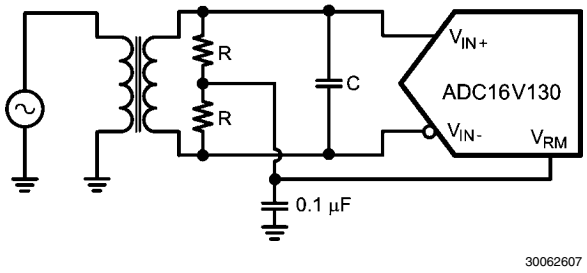

FIGURE 2. Transformer Drive Circuit for Low Input Frequency

Transformer has a characteristic of band pass filtering. It sets lower band limit by being saturated at frequencies below a few MHz and sets upper frequency limit due to its parasitic resistance and capacitance. The transformer core will be saturated with excessive signal power and it causes distortion as equivalent load termination becomes heavier at high input frequencies. This is a reason to reduce shunt capacitors for high IF sampling application to balance the amount of distortion caused by transformer and charge kick-back noise from the device.

As input frequency goes higher with the input network in *Figure 3*, amplitude and phase unbalance increase between positive and negative inputs (V_{IN+} and V_{IN-}) due to the inherent impedance mismatch between the two primary ports of the transformer while one is connected to the signal source and the other is connected to GND. Distortion increases as the result.

Cascaded transmission line transformers can be used for high frequency applications like high IF sampling base station receiver channel. Transmission line transformer has less stray capacitance between primary and secondary ports and so the amount of impedance at secondary ports is effectively less even with the given inherent impedance mismatch on the primary ports. Cascading two transmission line transformers further reduces the effective stray capacitance from the secondary of ports of the secondary transformer to primary ports of first transformer, where impedance is mismatched. A transmission line transformer, for instance MABACT0040 from M/A-COM, with center tap on secondary port could further reduce amplitude and phase mismatch.

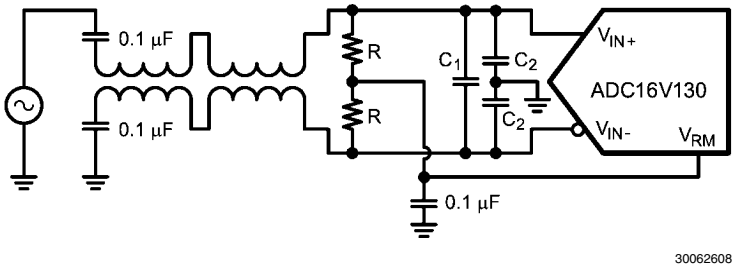

FIGURE 3. Transformer Drive Circuit for High Input Frequency

2.3 Equivalent Input Circuit and Its S11

Input circuit of the ADC16V130 during sample mode is a differential switched capacitor as shown in *Figure 4*. Bottom plate sampling switch is bootstrapped in order to reduce its turn on impedance and its variation across input signal amplitude. Bottom plate sampling switches and top plate sampling switch are all turned off during hold mode. The sampled analog input signal is processed throughout the following pipeline ADC core. Equivalent impedance changes drastically between sample and hold mode while significant amount of charge injection occurs during the transition between the two operating modes.

Distortion and SNR heavily rely on the signal integrity, impedance matching during sample mode and charge injection while switching sampling switches.

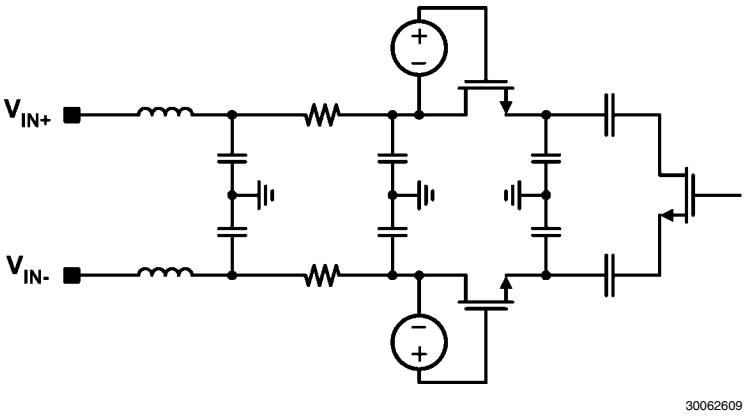

FIGURE 4. Input Equivalent Circuit

A measured S11 of the input circuit of the ADC16V130 is shown in *Figure 5* (Currently the figure is a simulated one. It is subject to be changed later. Note that the simulated S11 closely matches with the measured S11). Up to 500 MHz, it is predominantly capacitive loading with small stray resistance and inductance as shown in *Figure 5*. An appropriate resistive termination at a given input frequency band has to be added to improve signal integrity. Any shunt capacitor on analog input pin deteriorates signal integrity but it provides high frequency charge to absorb the charge inject generated while sampling switches are toggling. A optimal shunt capacitor is dependent on input signal frequency as well as impedance characteristic of analog input signal path including components like transformer, termination resistor, DC coupling capacitors.

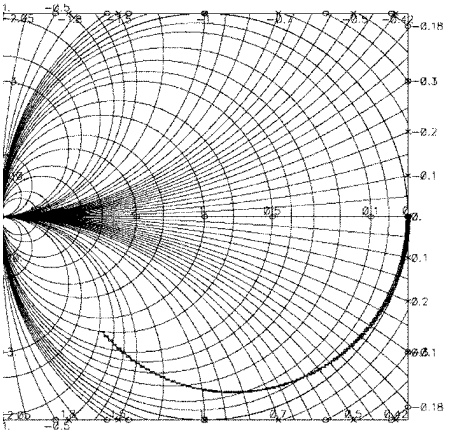

FIGURE 5. S11 Curve of Input Circuit

3.0 CLOCK INPUT CONSIDERATIONS

3.1 Clock Input Modes

The ADC16V130 provides a low additive jitter differential clock receiver for optimal dynamic performance at wide input frequency range. Input common mode of the clock receiver is internally biased at $V_{A1.8}/2$ through a 10 kΩ each to be driven by DC coupled clock input as shown in *Figure 6*. However while DC coupled clock input drives CLK+ and CLK-, it is recommend the common mode (average voltage of CLK+ and CLK-) not to be higher than $V_{A1.8}/2$ in order to prevent substantial tail current reduction, which might cause lowered jitter performance. Meanwhile, CLK+ and CLK- should not become lower than AGND. A high speed back-to-back diode connected between CLK+ and CLK- could limit the maximum swing, but this could cause signal integrity concerns when the diode turns on and reduce load impedance instantaneously.

A preferred differential clocking through a transformer coupled is shown in *Figure 7*. A 0.1µF decoupling capacitor on the center tap of the secondary ports of a flux type transformer stabilizes clock input common mode. Differential clocking increases the maximum amplitude of the clock input at the pins twice as large as that with singled-ended mode as shown in *Figure 8*. Clock amplitude is recommended to be as large as possible while CLK+ and CLK- both never exceed supply rails of $V_{A1.8}$ and AGND. With a given equivalent input noise of the differential clock receiver shown in *Figure 6*, larger clock amplitude at CLK+ and CLK- pins increases its slope around zero-crossing point so that higher signal-to-noise could be obtained by reducing the noise contributed by clock signal path.

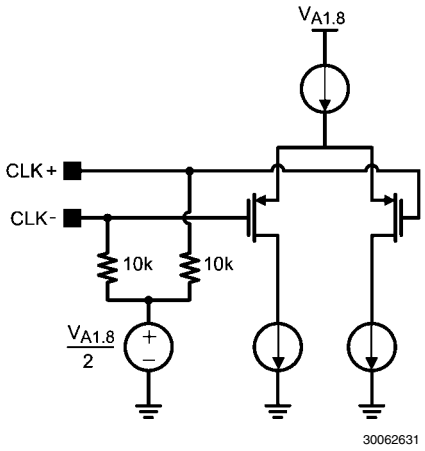

FIGURE 6. Equivalent Clock Receiver

The differential receiver of the ADC16V130 has excellent low noise floor but its bandwidth is wide as multiple times of clock rate. The wide band noise folds back to nyquist frequency band in frequency domain at ADC output. Increased slope of the input clock lowers the equivalent noise contributed by the differential receiver.

A band-pass filter (BPF) with narrow pass band and low insertion loss could be added on the clock input signal path when wide band noise of clock source is noticeably large compared to the input equivalent noise of the differential clock receiver.

Load termination could be a combination of R and C instead of a pure R. This RC termination could improve noise performance of clock signal path by filtering out high frequency noise through a low pass filter. The size of R and C is dependent on the clock rate and slope of the clock input.

A LVPECL and/or LVDS driver could also drive the ADC16V130. However the full dynamic performance of the ADC16V130 might not be achieved due to the high noise floor of the driving circuit itself especially in high IF sampling application.

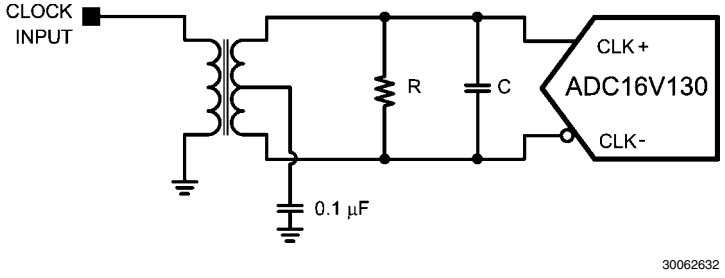

FIGURE 7. Differential Clocking, Transformer Coupled

Singled-ended clock can drive CLK+ pin through a 0.1µF AC coupling capacitor while CLK- is decoupled to AGND through a 0.1µF capacitor as shown in *Figure 8*.

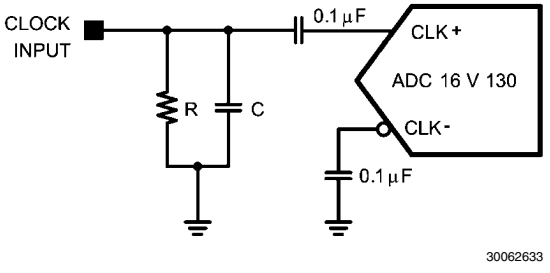

FIGURE 8. Singled-Ended 1.8V Clocking, Capacitive AC Coupled

3.2 Duty Cycle Stabilizer

Highest operating speed with optimal performance could be only achieved with 50% of clock duty cycle because the switched-capacitor circuit of the ADC16V130 is designed to have equal amount of settling time between each stage. The maximum operating frequency could be reduced accordingly while clock duty cycle departs from 50%.

The ADC16V130 contains a duty cycle stabilizer that adjusts non-sampling (rising) clock edge to make the duty cycle of the internal clock over 30 to 70% of input clock duty cycle. The duty cycle stabilizer is always on because the noise and distortion performance are not affected at all. It is not recommended to use the ADC16V130 at the clock frequencies less than 5 MSPS, at which the feedback loop in the duty cycle stabilizer becomes unstable.

3.3 Clock Jitter vs. Dynamic Performance

High speed and high resolution ADCs require low noise clock input to ensure its full dynamic performance over wide input frequency range. SNR (SNR_{Fin}) at a given input frequency (Fin) can be calculated by:

$$SNR_{Fin} = 10\log_{10}\left[\frac{A^2/2}{V_N^2 + (2\pi Fin \times Tj)^2/2}\right]$$

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with a given total noise power (V_N^2) of an ADC, total rms jitter (Tj), and input amplitude (A) in dBFS.

Clock signal path must be treated as an analog signal whenever aperture jitter affects the dynamic performance of the ADC16V130. Power supplies for the clock drivers has to be separated from the ADC output drive supplies to prevent modulated clock signal with the ADC digital output signals. Higher noise floor and/or increased distortion/spur might result from any coupling noise from ADC digital output signals to analog input and clock signals.

In IF sampling applications, the signal-to-noise ratio is particularly affected by clock jitter as shown in *Figure 9*. *Tj* is the integrated noise power of the clock signal divided by the slope of clock signal around tripping point. Upper limit of the noise integration is independent of applications and set by the bandwidth of the clock signal path. However lower limit of the noise integration highly relies on the applications. In base station receiver channel applications, the lower limit is determined by channel bandwidth and space from an adjacent channel.

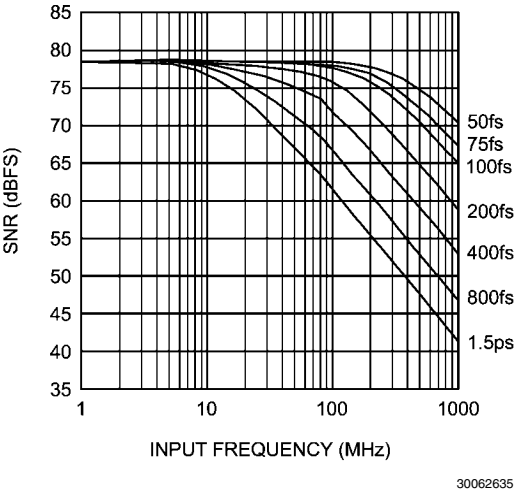


FIGURE 9. SNR with given Jitter vs. Input Frequency

4.0 CALIBRATION

Automatic calibration engine contained within the ADC16V130 improves dynamic performance and reduces its part-to-part variation. Digital output signals including output clock (OUTCLK+/-) are all logic low while calibrating. The ADC16V130 is automatically calibrated when the device is powered up. Optimal dynamic performance might not be obtained if power-up time is longer than internal delay time (~32mS @ 130 MSPS clock rate). In this case, the ADC16V130 could be re-calibrated by asserting and then de-asserting power down mode. Re-calibration is recommended whenever operating clock rate changes.

5.0 VOLTAGE REFERENCE

A stable and low noise voltage reference and its buffer amplifier are built into the ADC16V130. The input full scale is two times of V_{REF}, which is same as VBG (On-chip bandgap output having 9 kΩ output impedance) as well as V_{RP} - V_{RN} as shown in *Figure 10*. The input range can be adjusted by changing V_{REF} either internally or externally. An external reference with low output impedance can easily over-drive V_{REF} pin. Default V_{REF} is 1.2V. Input common mode voltage (V_{RM}) is a fixed voltage level of 1.15V. Maximum SNR can be achieved at maximum input range of 1.2V V_{REF}. Although the ADC16V130 dynamic and static performance is optimized at V_{REF} of 1.2V, reducing V_{REF} can improve SFDR performance with sacrificing SNR of the ADC16V130.

5.1 Reference Decoupling

It is highly recommended to place external decoupling capacitors connected to V_{RP}, V_{RN}, V_{RM} and V_{REF} pins as close to pins as possible. The external decoupling capacitor should have minimal ESL and ESR. During normal operation, inappropriate external decoupling with large ESL and/or ESR capacitors increase settling time of ADC core and results in lower SFDR and SNR performance. V_{RM} pin may be loaded up to 1mA for setting input common mode. The remaining pins should not be loaded. Smaller capacitor values might result in degraded noise performance. Decoupling capacitor on V_{REF} pin must not exceed 0.1µF, heavier decoupling on this pin will cause improper calibration during power-up. All reference pins except V_{REF} have very low output impedance. Driving these pins via low output impedance external circuit for long time period might damage the device.

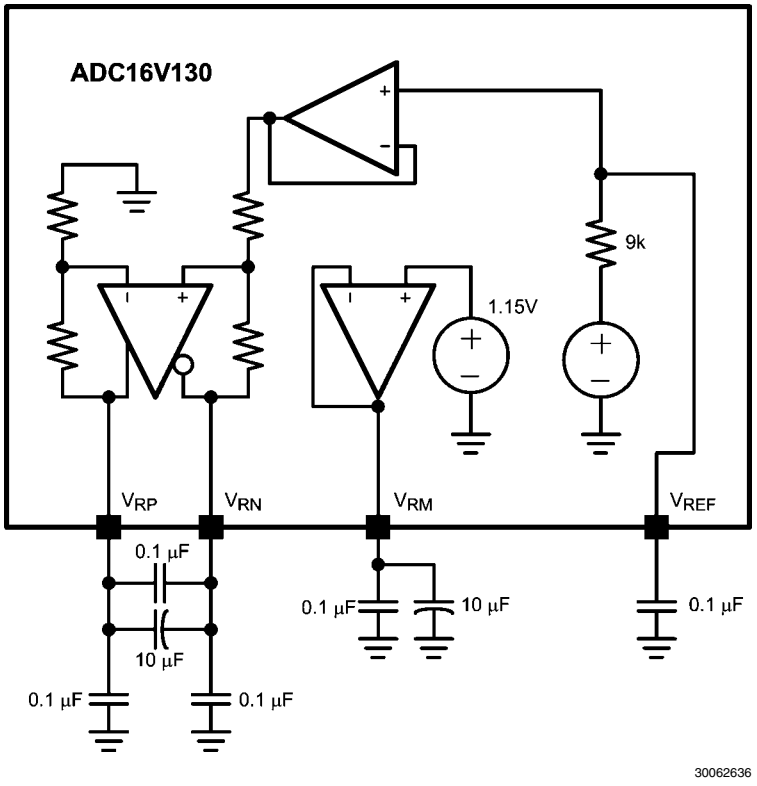


FIGURE 10. Internal References and their Decoupling

While V_{RM} pin is used to set input common mode level via transformer, a smaller serial resistor could be placed on the signal path to isolate any switching noise interfering between ADC core and input signal. The serial resistor introduces voltage error between V_{RM} and V_{CM} due to charge injection while sampling switches toggling. The serial resistance should not be larger than 50 Ω.

All grounds associated with each reference and analog input pins should be connected to a solid and quite ground on PC board. Coupling noise from digital outputs and their supplies to the reference pins and their ground can cause degraded SNR and SFDR performance.

6.0 LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. Maintaining separate analog and digital areas of the board, with the ADC16V130 between these areas, is required to achieve specified performance.

Even though LVDS output reduces ground bounding during its transition, the positive and negative signal path has to be well matched and their trace should be kept as short as possible. It is recommend to place LVDS repeater between the ADC16V130 and digital data receiver block to isolate coupling noise from receiving block while the length of the traces are long or the noise level of the receiving block is high.

Capacitive coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry, and to keep the clock line as short as possible.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than its total ground plane area.

Generally, analog and digital lines should not be crossing each. However whenever it is inevitable, make sure that these lines are crossing each other at 90° to minimize cross talk. Digital output and output clock signals must be separated from analog input, references and clock signals unconditionally to ensure the maximum performance from ADC16V130. Any coupling might result degraded SNR and SFDR performance especially at high IF applications.

Be especially careful with the layout of inductors and transformers. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors and transformers should not be placed side by side, even with just a small part of their bodies beside each other. For instance, place transformers for the analog input and the clock input at 90° to one another to avoid magnetic coupling. It is recommended to place the transformers of input signal path on the top plate, but the transformer of clock signal path on the bottom plate. Every critical analog signal path like analog inputs and clock inputs must be treated as a transmission line and should have a solid ground return path with a small loop.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference pins and ground should be connected to a very clean point in the ground plane. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed in the analog area of the board. All digital circuitry and dynamic I/O lines should be placed in the digital area of the board. The ADC16V130 should be between these two areas. Furthermore, all compo-

nents in the reference circuitry and the input signal chain that are connected to ground should be connected together with short traces and enter the ground plane at a single, quiet point. All ground connections should have a low inductance path to ground.

Ground return current path can be well managed when supply current path is precisely controlled and ground layer is continuous and placed next to the supply layer. This is because of the proximity effect. Ground return current path with a large loop will cause electro-magnetic coupling and results in poor noise performance. Not that even if there is a large plane for a current path, high frequency current path is not spread evenly over the large plane, but only takes a path with lowest impedance. Instead of large plane, using thick trace for supplies makes it easy to control return current path. It is recommended to place supply next to GND layer with thin dielectric for smaller ground return loop. Proper location and size of decoupling capacitors provide short and clean return current path.

7.0 SUPPLIES AND THEIR SEQUENCE

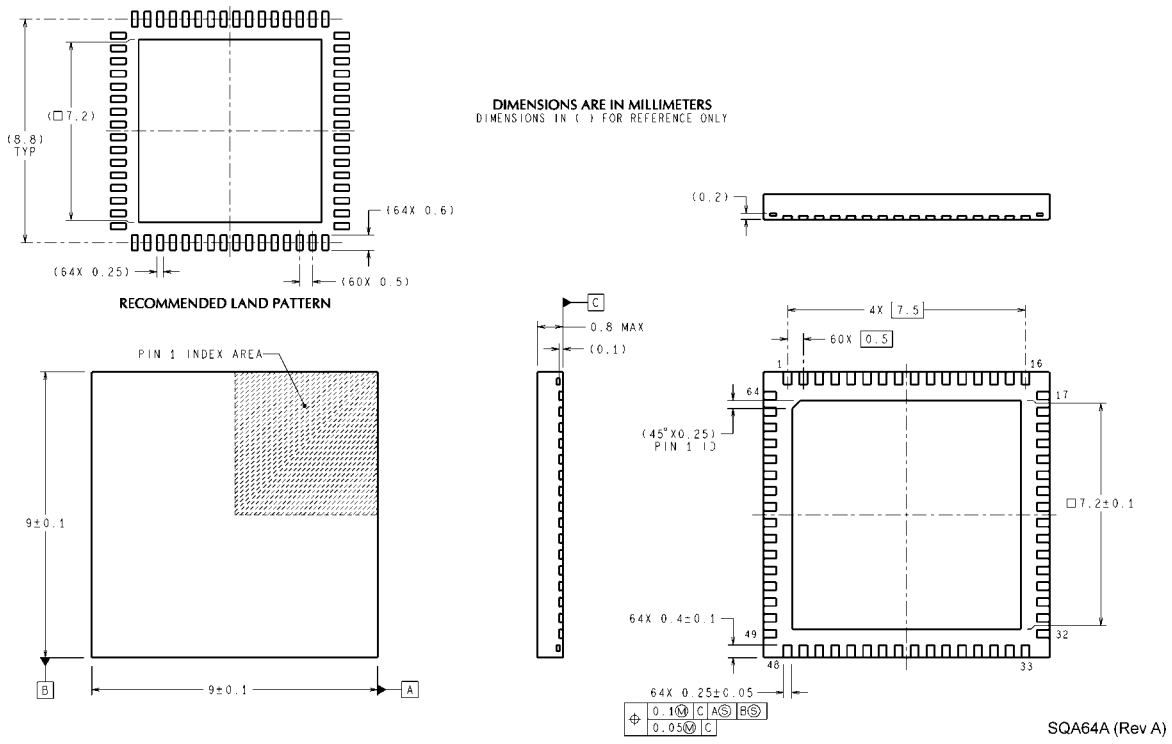
There are four supplies for the ADC16V130; one 3.0V supply $V_{A3.0}$ and three 1.8V supplies $V_{A1.8}$, $V_{AD1.8}$ and V_{DR}. It is recommended to separate V_{DR} from $V_{A1.8}$ supplies, any coupling from V_{DR} to rest of supplies and analog signals could cause lower SFDR and noise performance. When $V_{A1.8}$ and V_{DR} are both from same supply source, coupling noise can be mitigated by adding ferrite-bead on V_{DR} supply path.

The user can use different decoupling capacitors to provide current over wide frequency range. The decoupling capacitors should be located close to the point of entry and close to the supply pins with minimal trace length. A single ground plane is recommended because separating ground under the ADC16V130 could cause unexpected long return current path.

$V_{A3.0}$ supply must turn on before $V_{A1.8}$ and/or V_{DR} reaches single diode turn-on voltage level. If this supply sequence is reversed, excessive amount of current will flow through $V_{A3.0}$ supply. Ramp rate of $V_{A3.0}$ supply must be kept less than 60V/mS (i.e., 60µS for 3.0V supply) in order to prevent excessive surge current through ESD protection devices.

The exposed pad (Pin #0) on the bottom of the package should be soldered to AGND in order to get optimal noise performance. The exposed pad is a solid ground for the device and also is heat sinking path.

Physical Dimensions inches (millimeters) unless otherwise noted



SQA64A (Rev A)

64-Lead LLP Package
Ordering Number ADC16V130CISQ
NS Package Number SQA64A

Notes

Notes

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Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
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3.3 GHz Ultralow Distortion RF/IF Differential Amplifier

ADL5562

FEATURES

–3 dB bandwidth of 3.3 GHz (A_V = 6 dB)
Pin-strappable gain adjust: 6 dB, 12 dB, 15.5 dB
Differential or single-ended input to differential output
Low noise input stage: 2.1 nV/√Hz RTI @ A_V = 12 dB
Low broadband distortion (Av = 6 dB)
10 MHz: –91 dBc HD2, –98 dBc HD3
70 MHz: –102 dBc HD2, –90 dBc HD3
140 MHz: –104 dBc HD2, –87 dBc HD3
250 MHz: –80 dBc HD2, –94 dBc HD3
IMD3s of –94 dBc at 250 MHz center
Slew rate: 9.8 V/ns
Fast settling of 2 ns and overdrive recovery of 3 ns
Single-supply operation: 3 V to 3.6 V
Power-down control
Fabricated using the high speed XFCB3 SiGe process

FUNCTIONAL BLOCK DIAGRAM

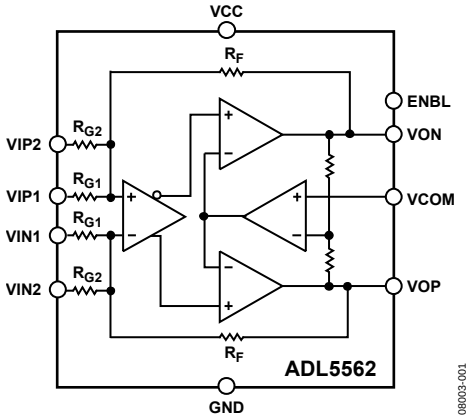

Figure 1.

APPLICATIONS

Differential ADC drivers
Single-ended to differential conversion
RF/IF gain blocks
SAW filter interfacing

GENERAL DESCRIPTION

The ADL5562 is a high performance differential amplifier optimized for RF and IF applications. The amplifier offers low noise of 2.1 nV/√Hz and excellent distortion performance over a wide frequency range, making it an ideal driver for high speed 8-bit to 16-bit ADCs.

The ADL5562 provides three gain levels of 6 dB, 12 dB, and 15.5 dB through a pin-strappable configuration. For the single-ended input configuration, the gains are reduced to 5.6 dB, 11.1 dB, and 14.1 dB. Using an external series input resistor expands the amplifier gain flexibility and allows for any gain selection from 0 dB to 15.5 dB.

The quiescent current of the ADL5562 is typically 80 mA and, when disabled, consumes less than 3 mA, offering excellent input-to-output isolation.

The device is optimized for wideband, low distortion performance. These attributes, together with its adjustable gain capability, make this device the amplifier of choice for general-purpose IF and broadband applications where low distortion, noise, and power are critical. This device is optimized for the best combination of slew speed, bandwidth, and broadband distortion. These attributes allow it to drive a wide variety of ADCs and make it ideally suited for driving mixers, pin diode attenuators, SAW filters, and multi-element discrete devices.

Fabricated on an Analog Devices, Inc., high speed SiGe process, the ADL5562 is supplied in a compact 3 mm × 3 mm, 16-lead LFCSP package and operates over the temperature range of −40°C to + 85°C.

Rev. B

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5/09—Revision 0: Initial Version

SPECIFICATIONS

VCC = 3.3 V, VCOM = 1.65 V, R_L = 200 Ω differential, A_V = 6 dB, C_L = 1 pF differential, f = 140 MHz, T_A = 25°C.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	A_V = 6 dB, V_{OUT} ≤ 1.0 V p-p		3300		MHz
	A_V = 12 dB, V_{OUT} ≤ 1.0 V p-p		3900		MHz
	A_V = 15.5 dB, V_{OUT} ≤ 1.0 V p-p		1900		MHz
Bandwidth for 0.1 dB Flatness	A_V = 6 dB, V_{OUT} ≤ 1.0 V p-p		220		MHz
	A_V = 12 dB, V_{OUT} ≤ 1.0 V p-p		270		MHz
	A_V = 15.5 dB, V_{OUT} ≤ 1.0 V p-p		270		MHz
Gain Accuracy	A_V = 6 dB, R_L = open		0.17		dB
	A_V = 12 dB, R_L = open		0.05		dB
	A_V = 15.5 dB, R_L = open		0.06		dB
Gain Supply Sensitivity	VCC ± 5%		−0.005		dB/V
Gain Temperature Sensitivity	−40°C to +85°C, A_V = 15.5 dB		0.32		mdB/°C
Slew Rate	Rise, A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 2 V step		9.8		V/ns
	Fall, A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 2 V step		10.1		V/ns
Settling Time	2 V step to 1%		2		ns
Overdrive Recovery Time	V_{IN} = 4 V to 0 V step, V_{OUT} ≤ ±10 mV		3		ns
Reverse Isolation (S12)			60		dB
INPUT/OUTPUT CHARACTERISTICS					
Output Common Mode			VCC/2		V
Voltage Adjustment Range			1.4 to 1.8		V
Maximum Output Voltage Swing	1 dB compressed		4.9		V p-p
Output Common-Mode Offset	Referenced to VCC/2		60		mV
Output Common-Mode Drift	−40°C to +85°C		285		µV/°C
Output Differential Offset Voltage			1		mV
CMRR			65		dB
Output Differential Offset Drift	−40°C to +85°C		15		µV/°C
Input Bias Current			3		µA
Input Resistance (Differential)	A_V = 6 dB		400		Ω
	A_V = 12 dB		200		Ω
	A_V = 15.5 dB		133		Ω
Input Resistance (Single-Ended)[1]	A_V = 5.6 dB, R_S = 50 Ω		307		Ω
	A_V = 11.1 dB, R_S = 50 Ω		179		Ω
	A_V = 14.1 dB, R_S = 50 Ω		132		Ω
Input Capacitance (Single-Ended)			0.3		pF
Output Resistance (Differential)			12		Ω
POWER INTERFACE					
Supply Voltage		3	3.3	3.6	V
ENBL Threshold	Device disabled, ENBL low		0.6		V
	Device enabled, ENBL high		1.3		V
ENBL Input Bias Current	ENBL high		−27		µA
	ENBL low		−300		µA
Quiescent Current	ENBL high	75.5	80	84.5	mA
	ENBL low		3.5		mA

Parameter	Conditions	Min	Typ	Max	Unit
10 MHz NOISE/HARMONIC PERFORMANCE					
Second/Third Harmonic Distortion	A_V = 6 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−91/−98		dBc
	A_V = 12 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−95/−98		dBc
	A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−96/−92		dBc
Output Third-Order Intercept/Third-Order Intermodulation Distortion	A_V = 6 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+42/−97		dBm/dBc
	A_V = 12 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+43/−93		dBm/dBc
	A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+43/−91		dBm/dBc
Noise Spectral Density (RTI)	A_V = 6 dB		3		nV/√Hz
	A_V = 12 dB		2.1		nV/√Hz
	A_V = 15.5 dB		1.6		nV/√Hz
1 dB Compression Point (RTO)	A_V = 6 dB		19.7		dBm
	A_V = 12 dB		19.6		dBm
	A_V = 15.5 dB		18.2		dBm
70 MHz NOISE/HARMONIC PERFORMANCE					
Second/Third Harmonic Distortion	A_V = 6 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−102/−90		dBc
	A_V = 12 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−97/−85		dBc
	A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−93/−83		dBc
Output Third-Order Intercept/Third-Order Intermodulation Distortion	A_V = 6 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+46/−96		dBm/dBc
	A_V = 12 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+44/−93		dBm/dBc
	A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+43/−91		dBm/dBc
Noise Spectral Density (RTI)	A_V = 6 dB		3		nV/√Hz
	A_V = 12 dB		2.1		nV/√Hz
	A_V = 15.5 dB		1.6		nV/√Hz
1 dB Compression Point (RTO)	A_V = 6 dB		19.6		dBm
	A_V = 12 dB		19.6		dBm
	A_V = 15.5 dB		18.2		dBm
140 MHz NOISE/HARMONIC PERFORMANCE					
Second/Third Harmonic Distortion	A_V = 6 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−104/−87		dBc
	A_V = 12 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−82/−81		dBc
	A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−80/−80		dBc
Output Third-Order Intercept/Third-Order Intermodulation Distortion	A_V = 6 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+47/−100		dBm/dBc
	A_V = 12 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+45/−95		dBm/dBc
	A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+43/−92		dBm/dBc
Noise Spectral Density (RTI)	A_V = 6 dB		3		nV/√Hz
	A_V = 12 dB		2.1		nV/√Hz
	A_V = 15.5 dB		1.6		nV/√Hz
1 dB Compression Point (RTO)	A_V = 6 dB		19.6		dBm
	A_V = 12 dB		19.4		dBm
	A_V = 15.5 dB		18.1		dBm

Parameter	Conditions	Min	Typ	Max	Unit
250 MHz NOISE/HARMONIC PERFORMANCE					
Second/Third Harmonic Distortion	A_V = 6 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−80/−94		dBc
	A_V = 12 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−74/−86		dBc
	A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−74/−84		dBc
Output Third-Order Intercept/Third-Order Intermodulation Distortion	A_V = 6 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+43/−94		dBm/dBc
	A_V = 12 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+41/−87		dBm/dBc
	A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+40/−86		dBm/dBc
Noise Spectral Density (RTI)	A_V = 6 dB		3.2		nV/√Hz
	A_V = 12 dB		2.2		nV/√Hz
	A_V = 15.5 dB		1.6		nV/√Hz
1 dB Compression Point (RTO)	A_V = 6 dB		19.8		dBm
	A_V = 12 dB		19.3		dBm
	A_V = 15.5 dB		19.1		dBm
500 MHz NOISE/HARMONIC PERFORMANCE					
Second/Third Harmonic Distortion	A_V = 6 dB, R_L = 200 Ω, V_{OUT} = 1 V p-p		−75/−69		dBc
	A_V = 12 dB, R_L = 200 Ω, V_{OUT} = 1 V p-p		−69/−73		dBc
	A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 1 V p-p		−72/−75		dBc
Output Third-Order Intercept/Third-Order Intermodulation Distortion	A_V = 6 dB, R_L = 200 Ω, V_{OUT} = 1 V p-p composite (2 MHz spacing)		+40/−98		dBm/dBc
	A_V = 12 dB, R_L = 200 Ω, V_{OUT} = 1 V p-p composite (2 MHz spacing)		+39/−97		dBm/dBc
	A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 1 V p-p composite (2 MHz spacing)		+38/−93		dBm/dBc
Noise Spectral Density (RTI)	A_V = 6 dB		3.7		nV/√Hz
	A_V = 12 dB		2.2		nV/√Hz
	A_V = 15.5 dB		1.6		nV/√Hz
1 dB Compression Point (RTO)	A_V = 6 dB		18.1		dBm
	A_V = 12 dB		18.1		dBm
	A_V = 15.5 dB		18.1		dBm
1000 MHz NOISE/HARMONIC PERFORMANCE					
Second/Third Harmonic Distortion	A_V = 6 dB, R_L = 200 Ω, V_{OUT} = 1 V p-p		−70/−60		dBc
	A_V = 12 dB, R_L = 200 Ω, V_{OUT} = 1 V p-p		−69/−61		dBc
	A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 1 V p-p		−66/−59		dBc
Output Third-Order Intercept/Third-Order Intermodulation Distortion	A_V = 6 dB, R_L = 200 Ω, V_{OUT} = 1 V p-p composite (2 MHz spacing)		+24/−65		dBm/dBc
	A_V = 12 dB, R_L = 200 Ω, V_{OUT} = 1 V p-p composite (2 MHz spacing)		+24/−66		dBm/dBc
	A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 1 V p-p composite (2 MHz spacing)		+25/−66		dBm/dBc
Noise Spectral Density (RTI)	A_V = 6 dB		4.7		nV/√Hz
	A_V = 12 dB		2.2		nV/√Hz
	A_V = 15.5 dB		1.6		nV/√Hz
1 dB Compression Point (RTO)	A_V = 6 dB		15		dBm
	A_V = 12 dB		15.1		dBm
	A_V = 15.5 dB		15.1		dBm

[1] See the Applications Information section for a discussion of single-ended input, dc-coupled operation.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (VCC)	3.6 V
VIP1, VIP2, VIN1, VIN2	VCC + 0.5 V
Internal Power Dissipation	310 mW
θ_{JA}	98.3°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

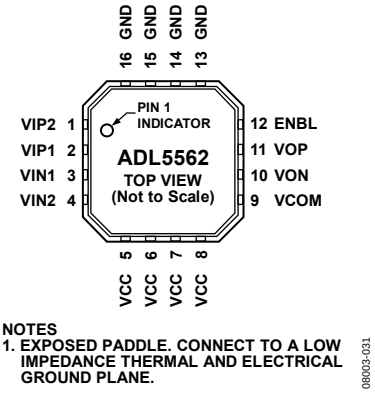


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VIP2	Balanced Differential Input. Biased to VCOM, typically ac-coupled. Input for A_V = 12 dB gain, strapped to VIP1 for A_V = 15.5 dB.
2	VIP1	Balanced Differential Input. Biased to VCOM, typically ac-coupled. Input for A_V = 6 dB gain, strapped to VIP2 for A_V = 15.5 dB.
3	VIN1	Balanced Differential Input. Biased to VCOM, typically ac-coupled. Input for A_V = 6 dB gain, strapped to VIN2 for A_V = 15.5 dB.
4	VIN2	Balanced Differential Input. Biased to VCOM, typically ac-coupled. Input for A_V = 12 dB gain, strapped to VIN1 for A_V = 15.5 dB.
5, 6, 7, 8	VCC	Positive Supply.
9	VCOM	Common-Mode Voltage. A voltage applied to this pin sets the common-mode voltage of the input and output. Typically decoupled to ground with a 0.1 µF capacitor. With no reference applied, input and output common mode floats to midsupply (VCC/2).
10	VON	Balanced Differential Output. Biased to VCOM, typically ac-coupled.
11	VOP	Balanced Differential Output. Biased to VCOM, typically ac-coupled.
12	ENBL	Enable. Apply positive voltage (1.0 V < ENBL < VCC) to activate device.
13, 14, 15, 16	GND	Ground. Connect to low impedance ground.
	EP	Exposed Pad. Connect to a low impedance thermal and electrical ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

VCC = 3.3 V, VCOM = 1.65 V, R_L = 200 Ω differential, A_V = 6 dB, C_L = 1 pF differential, f = 140 MHz, T = 25°C.

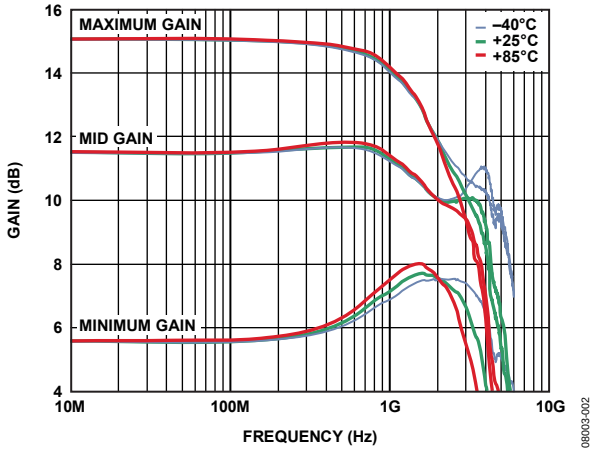


Figure 3. Gain vs. Frequency Response for 200 Ω Differential Load, A_V = 6 dB, A_V = 12 dB, and A_V = 15.5 dB over Temperature

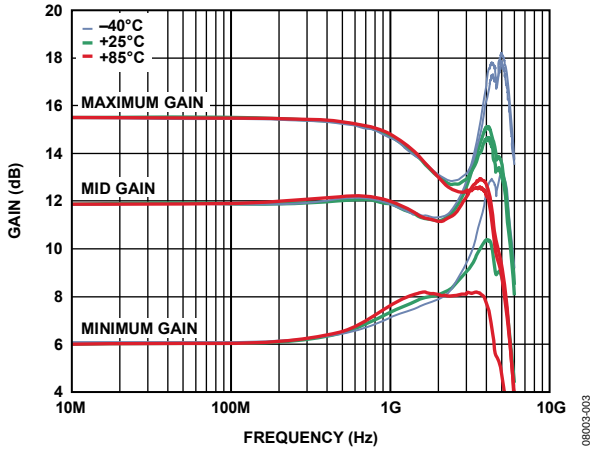


Figure 4. Gain vs. Frequency Response for 1 kΩ Differential Load, A_V = 6 dB, A_V = 12 dB, and A_V = 15.5 dB over Temperature

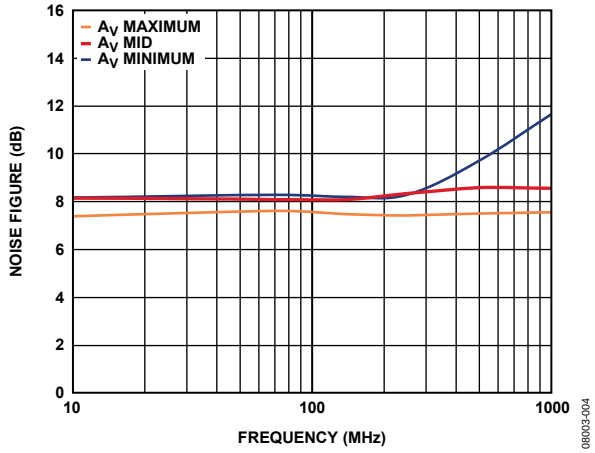


Figure 5. Noise Figure vs. Frequency at A_V = 6 dB, A_V = 12 dB, and A_V = 15.5 dB

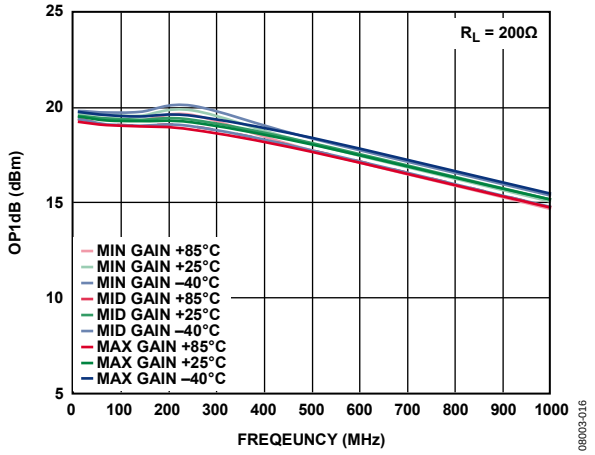


Figure 6. Output P1dB (OP1dB) vs. Frequency at A_V = 6 dB, A_V = 12 dB, and A_V = 15.5 dB over Temperature, 200 Ω Differential Load

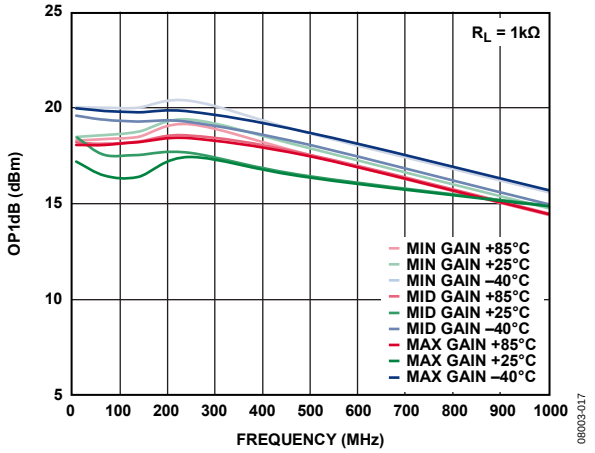


Figure 7. Output P1dB (OP1dB) vs. Frequency at A_V = 6 dB, A_V = 12 dB, and A_V = 15.5 dB over Temperature, 1 kΩ Differential Load

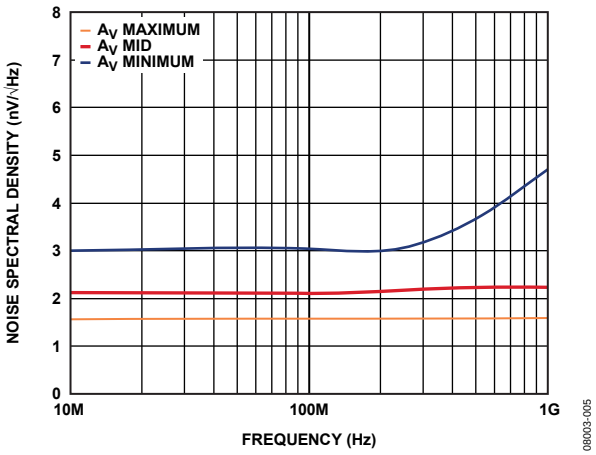


Figure 8. Noise Spectral Density vs. Frequency at A_V = 6 dB, A_V = 12 dB, and A_V = 15.5 dB

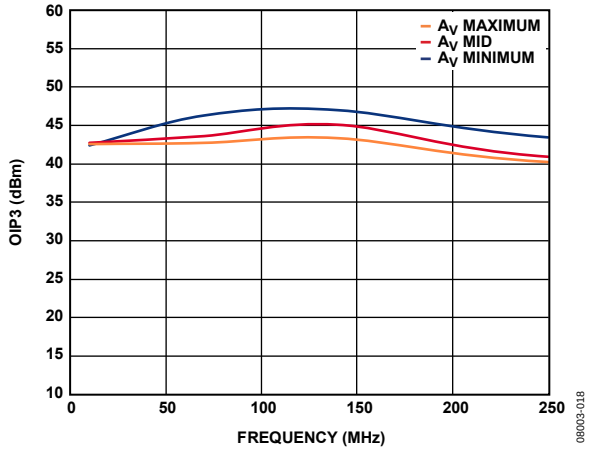


Figure 9. Output Third-Order Intercept at Three Gains, Output Level at 2 V p-p Composite, R_L = 200 Ω

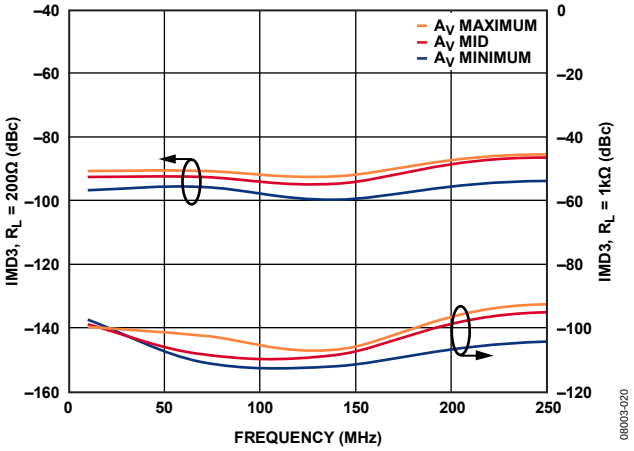


Figure 12. Two-Tone Output IMD vs. Frequency, Output Level at 2 V p-p Composite, R_L = 200 Ω and R_L = 1 kΩ

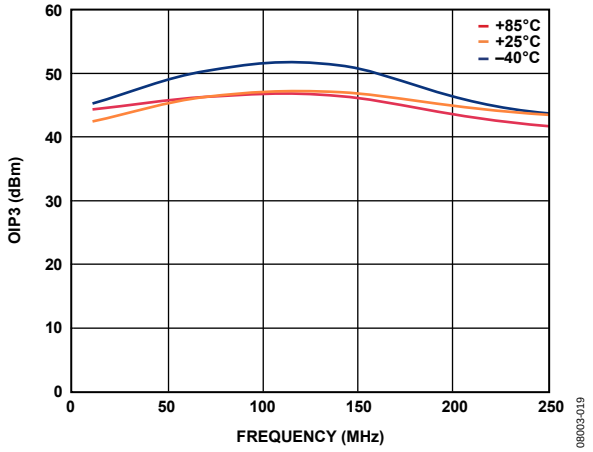


Figure 10. Output Third-Order Intercept vs. Frequency, Over Temperature, Output Level at 2 V p-p Composite, R_L = 200 Ω

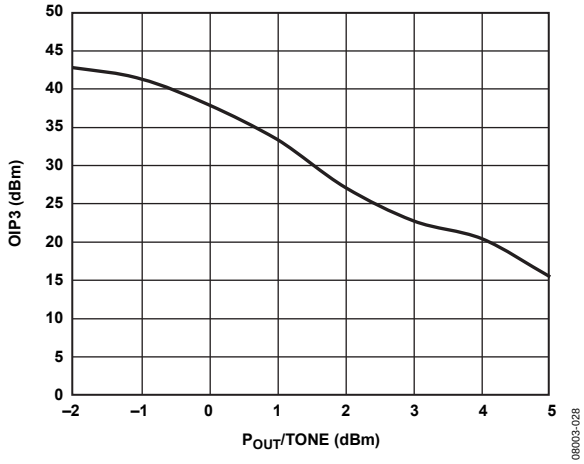


Figure 13. Output Third-Order Intercept (OIP3) vs. Power (P_{OUT}), Frequency 140 MHz, A_V = 15.5 dB

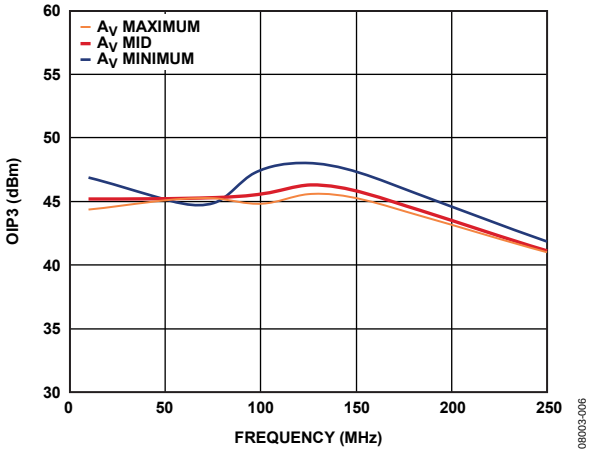


Figure 11. OIP3 vs. Frequency (Single-Ended Input)

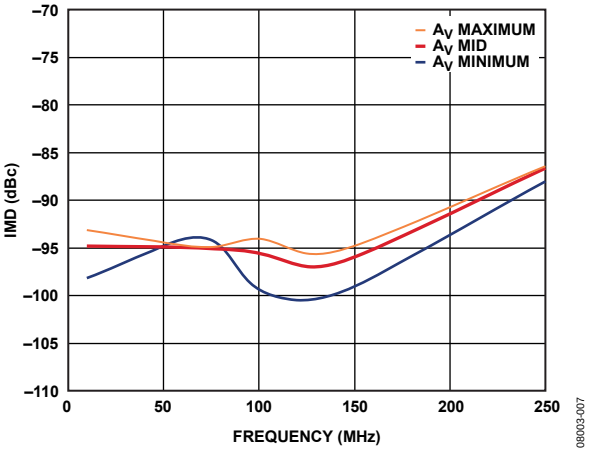


Figure 14. IMD vs. Frequency (Single-Ended Input)

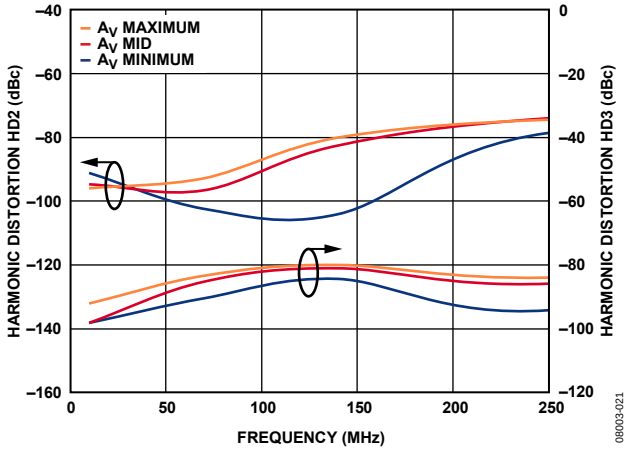


Figure 15. Harmonic Distortion (HD2/HD3) vs. Frequency at A_V = 6 dB, A_V = 12 dB, and A_V = 15.5 dB, Output Level at 2 V p-p, R_L = 200 Ω

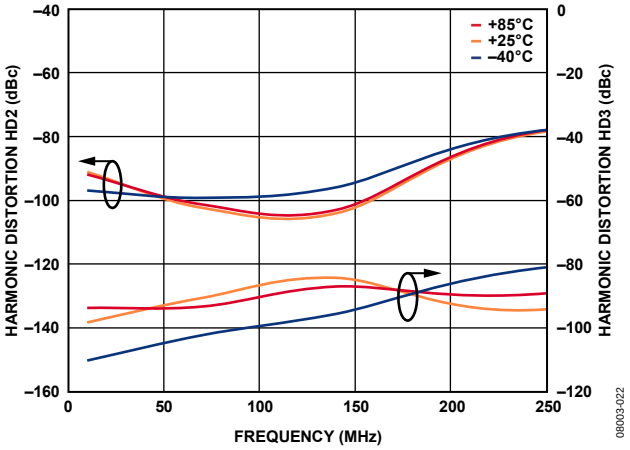


Figure 16. Harmonic Distortion (HD2/HD3) vs. Frequency, Three Temperatures, Output Level at 2 V p-p, R_L = 200 Ω

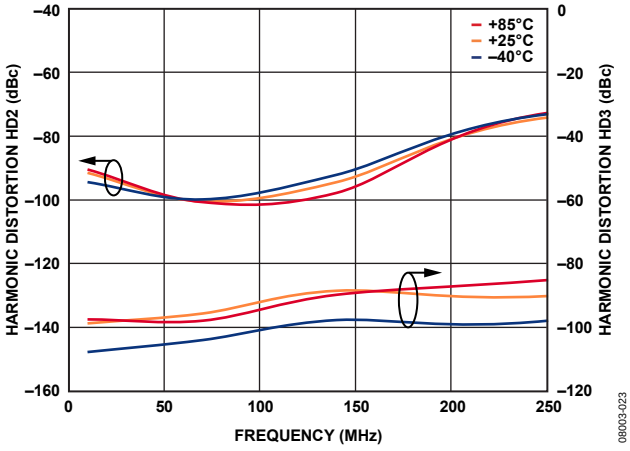


Figure 17. Harmonic Distortion (HD2/HD3) vs. Frequency, Over Temperature, Output Level at 2 V p-p, R_L = 1 kΩ

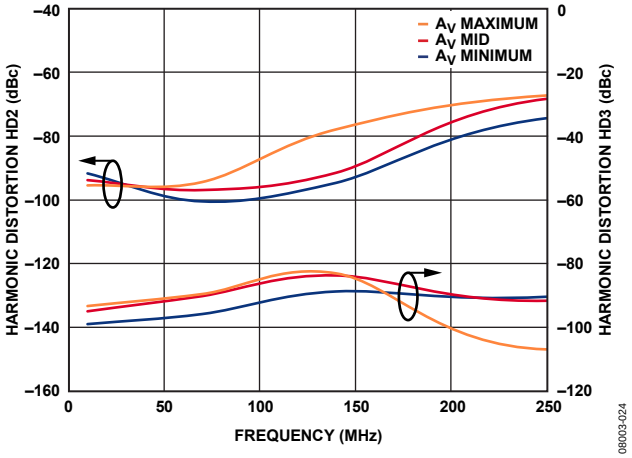


Figure 18. Harmonic Distortion (HD2/HD3) vs. Frequency at A_V = 6 dB, A_V = 12 dB, and A_V = 15.5 dB, Output Level at 2 V p-p, R_L = 1 kΩ

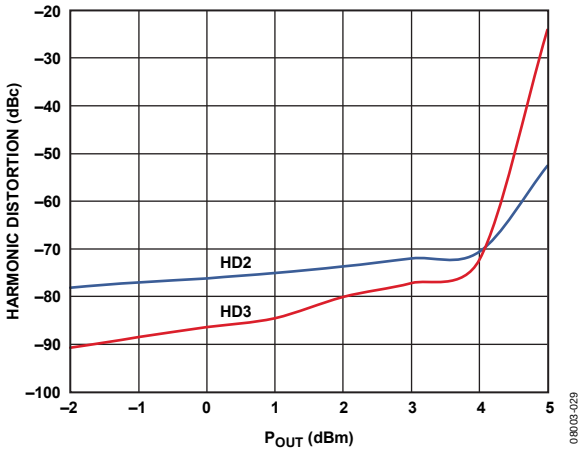


Figure 19. Harmonic Distortion (HD2/HD3) vs. Power (P_{OUT}), Frequency 140 MHz, A_V = 15.5 dB

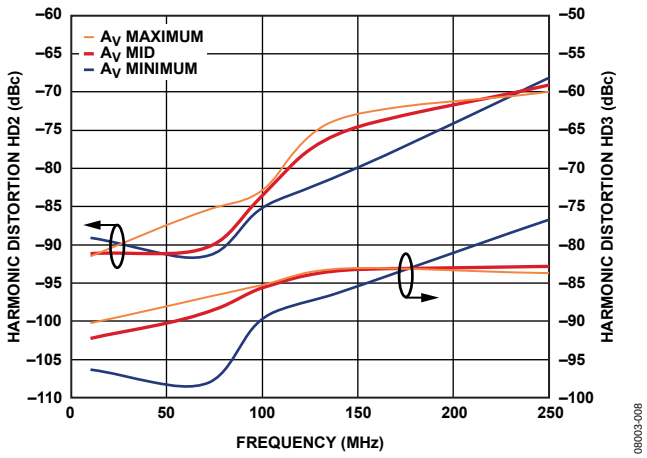


Figure 20. Harmonic Distortion (HD2/HD3) vs. Frequency (Single-Ended Input)

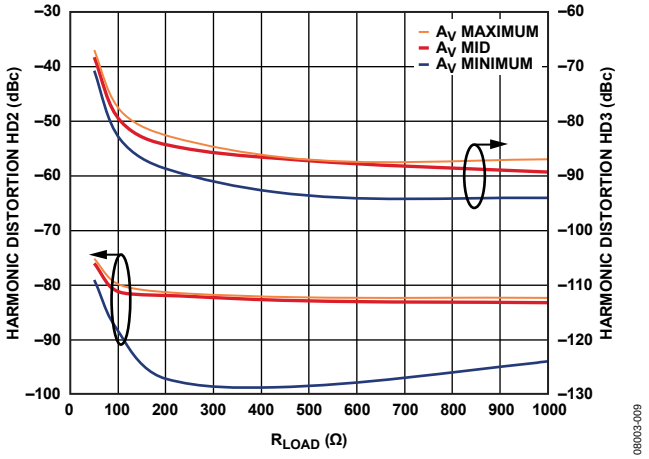


Figure 21. Harmonic Distortion (HD2/HD3) vs. R_{LOAD}

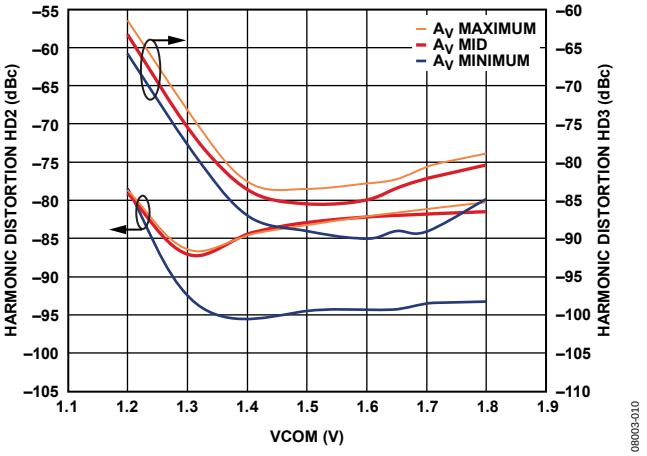


Figure 24. Harmonic Distortion (HD2/HD3) vs. VCOM

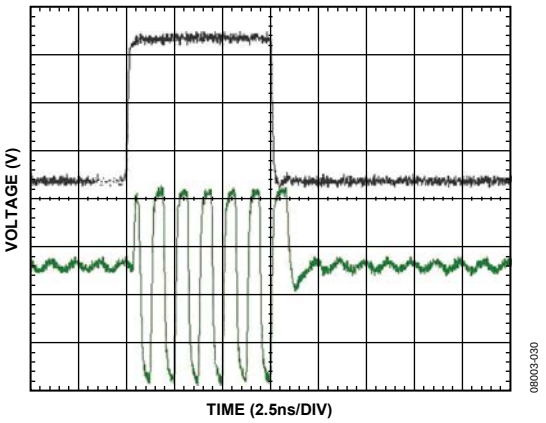


Figure 22. ENBL Time Domain Response

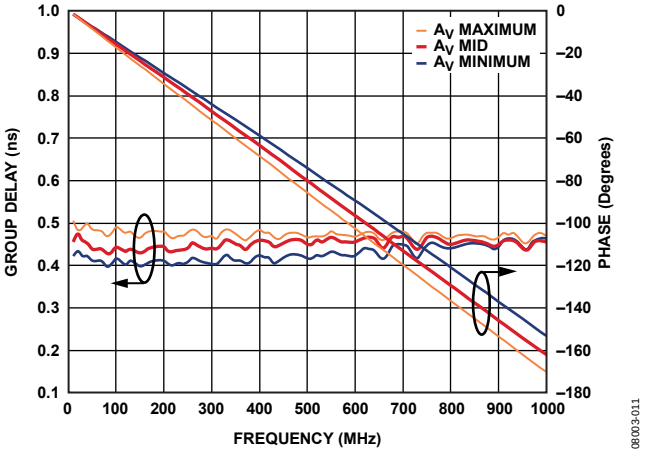


Figure 25. Group Delay and Phase vs. Frequency

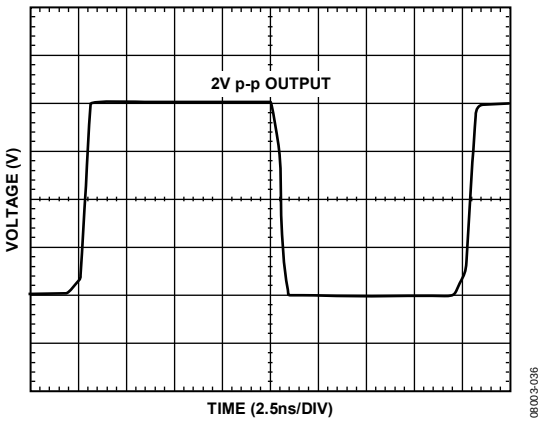


Figure 23. Large Signal Pulse Response, A_V = 15.5 dB

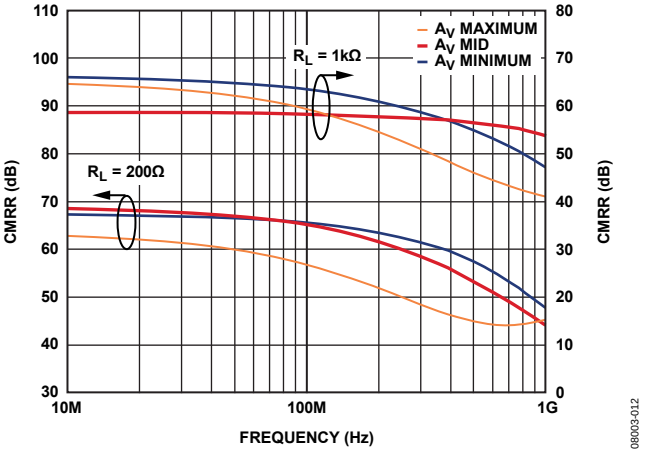


Figure 26. Common-Mode Rejection Ratio (CMRR) vs. Frequency

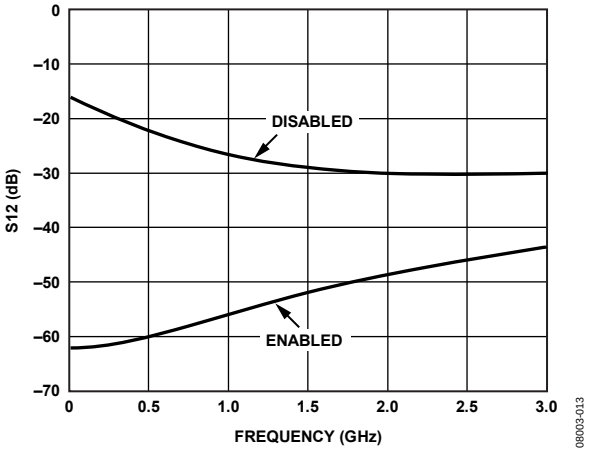


Figure 27. Reverse Isolation (S12) vs. Frequency

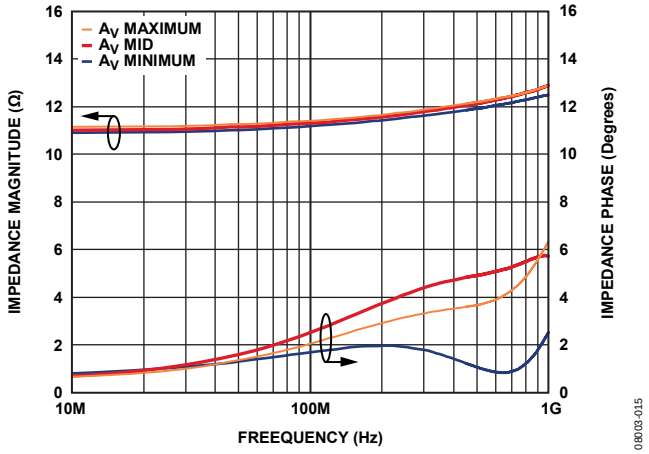


Figure 29. Output Impedance vs. Frequency

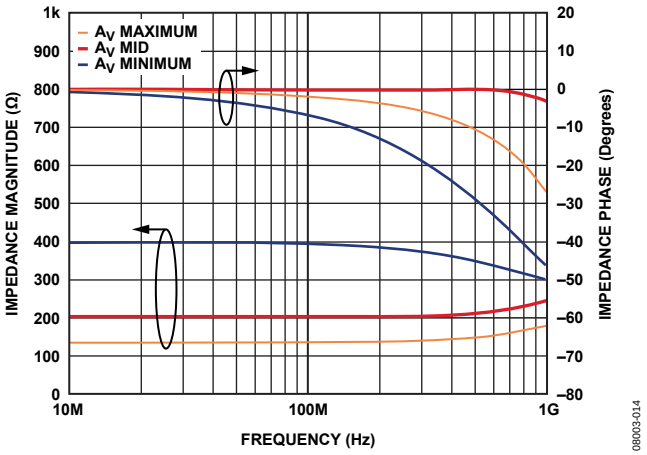


Figure 28. Input Impedance vs. Frequency

CIRCUIT DESCRIPTION

BASIC STRUCTURE

The ADL5562 is a low noise, fully differential amplifier/ADC driver that uses a 3.3 V supply. It provides three gain options (6 dB, 12 dB, and 15.5 dB) without the need for external resistors and has wide bandwidths of 2.6 GHz for 6 dB, 2.3 GHz for 12 dB, and 2.1 GHz for 15.5 dB. Differential input impedance is 400 Ω for 6 dB, 200 Ω for 12 dB, and 133 Ω for 15.5 dB. It has a differential output impedance of 10 Ω and a common-mode adjust voltage of 1.25 V to 1.85 V.

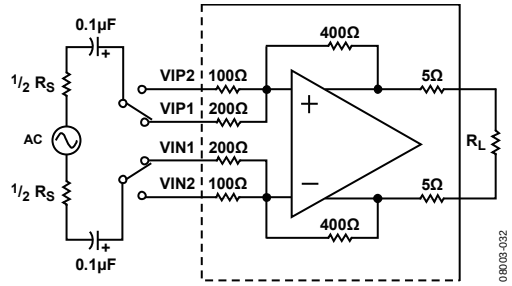


Figure 30. Basic Structure

The ADL5562 is composed of a fully differential amplifier with on-chip feedback and feed-forward resistors. The two feed-forward resistors on each input set this pin-strappable amplifier in three different gain configurations of 6 dB, 12 dB, and 15.5 dB. The amplifier is designed to provide high differential open-loop gain and an output common-mode circuit that enables the user to change the common-mode voltage from a VCOM pin. The amplifier is designed to provide superior low distortion at frequencies up to and beyond 300 MHz with low noise and low power consumption. The low distortion and noise are realized with a 3.3 V power supply at 80 mA.

The ADL5562 is very flexible in terms of I/O coupling. It can be ac-coupled or dc-coupled at the inputs and/or the outputs within the specified input and output common-mode levels. The input of the device can be configured as single-ended or differential with similar distortion performance. Due to the internal connections between the inputs and outputs, keep the output common-mode voltage between 1.25 V and 1.85 V for the best distortion. For a dc-coupled input, the input common mode should be between 1 V and 2.3 V for the best distortion. The device has been characterized using 2 V p-p into 200 Ω. If the inputs are ac-coupled, the input and output common-mode voltages are set by VCC/2 when no external circuitry is used. The ADL5562 provides an output common-mode voltage set by VCOM, which allows driving an ADC directly without external components, such as a transformer or ac coupling capacitors, provided the VCOM of the amplifier is within the VCOM of the ADC. For dc-coupled requirements, the input VCM must be set by the VCOM pin in all three gain settings.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 31 shows the basic connections for operating the ADL5562. VCC should be 3.3 V with each supply pin decoupled with at least one low inductance surface-mount ceramic capacitor of 0.1 µF placed as close as possible to the device. The VCOM pin (Pin 9) should also be decoupled using a 0.1 µF capacitor.

The gain of the part is determined by the pin-strappable input configuration. When Input A is applied to VIP1 and Input B is applied to VIN1, the gain is 6 dB (minimum gain, see Equation 1 and Equation 2). When Input A is applied to VIP2 and Input B is applied to VIN2, the gain is 12 dB (middle gain). When Input A is applied to VIP1 and VIP2 and Input B is applied to VIN1 and VIN2, the gain is 15.5 dB (maximum gain).

Pin 1 to Pin 4, Pin 10, and Pin 11 are biased at 1/2 VCC above ground and can be dc-coupled (if within the specified input or output common-mode voltage levels) or ac-coupled as shown in Figure 31.

To enable the ADL5562, the ENBL pin must be pulled high. Pulling the ENBL pin low puts the ADL5562 in sleep mode, reducing the current consumption to 3 mA at ambient.

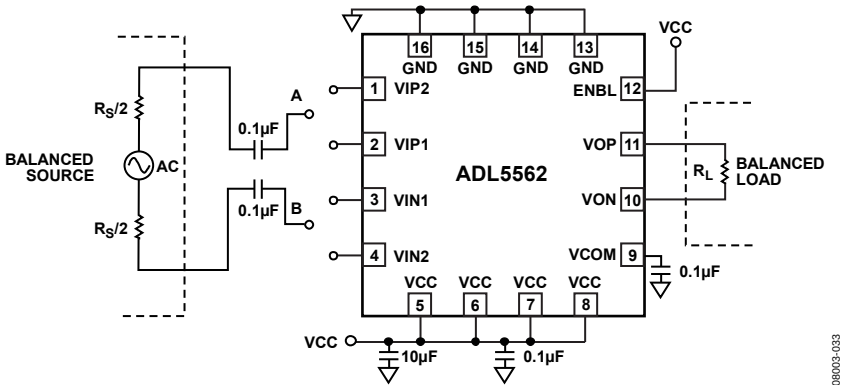


Figure 31. Basic Connections

INPUT AND OUTPUT INTERFACING

The ADL5562 can be configured as a differential-input to differential-output driver, as shown in Figure 32. The differential broadband input is provided by the ETC1-1-13 balun transformer, and the two 34.8 Ω resistors provide a 50 Ω input match for the three input impedances that change with the variable gain strapping. The input and output 0.1 µF capacitors isolate the VCC/2 bias from the source and balanced load. The load should equal 200 Ω to provide the expected ac performance (see the Specifications section and the Typical Performance Characteristics section).

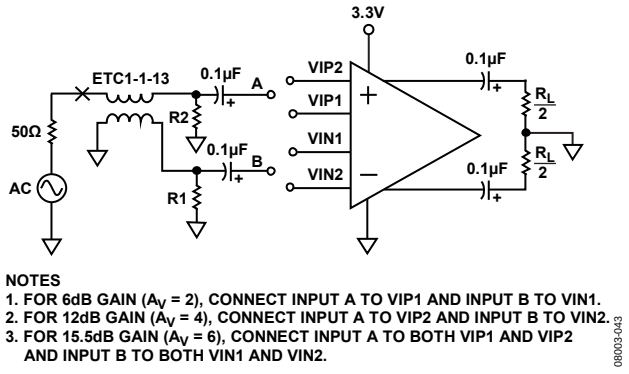


Figure 32. Differential-Input to Differential-Output Configuration

Table 4. Differential Termination Values for Figure 32

Gain (dB)	R1 (Ω)	R2 (Ω)
6	28.7	28.7
12	33.2	33.2
15.5	40.2	40.2

The differential gain of the ADL5562 is dependent on the source impedance and load, as shown in Figure 33.

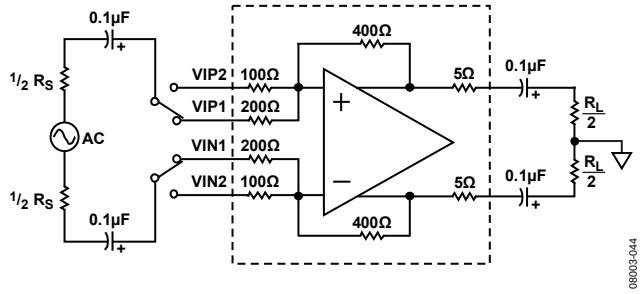


Figure 33. Differential Input Loading Circuit

The differential gain can be determined using the following formula. The values of R_{IN} for each gain configuration are shown in Table 5.

$$A_V = \frac{400}{R_{IN}} \times \frac{R_L}{10 + R_L} \quad (1)$$

Table 5. Values of R_{IN} for Differential Gain

Gain (dB)	R_{IN} (Ω)
6	200
12	100
15.5	66.7

Single-Ended Input to Differential Output

The ADL5562 can also be configured in a single-ended input to differential output driver, as shown in Figure 34. In this configuration, the gain of the part is reduced due to the application of the signal to only one side of the amplifier. The strappable gain values are listed in Table 6 with the required terminations to match to a 50 Ω source using R1 and R2. Note that R1 must equal the parallel value of the source and R2. The input and output 0.1 µF capacitors isolate the VCC/2 bias from the source and the balanced load. The performance for this configuration is shown in Figure 11, Figure 14, and Figure 20.

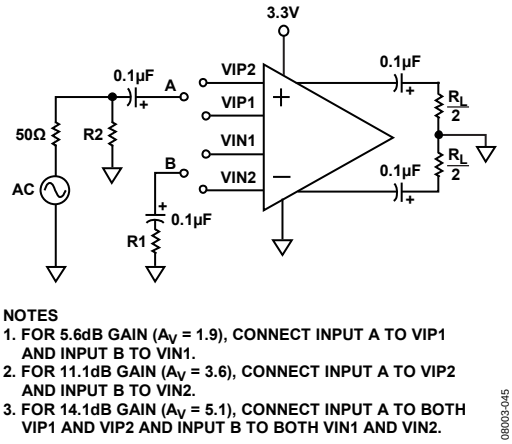


Figure 34. Single-Ended Input to Differential Output Configuration

Table 6. Single-Ended Termination Values for Figure 34

Gain (dB)	R1 (Ω)	R2 (Ω)
5.6	27	60
11.1	29	69
14.1	30	77

The single-ended gain configuration of the ADL5562 is dependent on the source impedance and load, as shown in Figure 35.

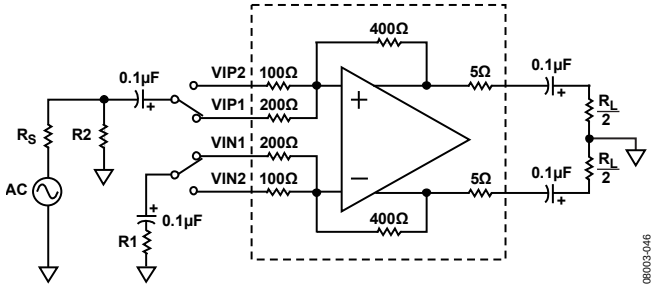


Figure 35. Single-Ended Input Loading Circuit

The single-ended gain can be determined using the following formula. The values of R_{IN} and R_X for each gain configuration are shown in Table 7.

$$A_{V1} = \frac{400}{R_{IN} + \left(\frac{R_S \times R2}{R_S + R2}\right)} \times \frac{R2}{R_S + R2} \times \frac{R_X + R_S}{R_X} \times \frac{R_L}{10 + R_L} \quad (2)$$

Table 7. Values of R_{IN} and R_X for Single-Ended Gain

Gain (dB)	R_{IN} (Ω)	R_X (Ω)
5.6	200	R2 || 307[1]
11.1	100	R2 || 179[1]
14.1	66.7	R2 || 132[1]

[1] These values based on a 50 Ω input match.

GAIN ADJUSTMENT AND INTERFACING

The effective gain of the ADL5562 can be reduced using a number of techniques. A matched attenuator network can reduce the effective gain; however, this requires the addition of a separate component that can be prohibitive in size and cost. Instead, a simple voltage divider can be implemented using the combination of additional series resistors at the amplifier input and the input impedance of the ADL5562, as shown in Figure 36. A shunt resistor is used to match to the impedance of the previous stage.

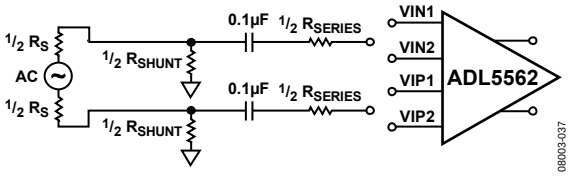


Figure 36. Gain Adjustment Using a Series Resistor

Figure 36 shows a typical implementation of the divider concept that effectively reduces the gain by adding attenuation at the input. For frequencies less than 100 MHz, the input impedance of the ADL5562 can be modeled as a real 133 Ω, 200 Ω, or 400 Ω resistance (differential) for maximum, middle, and minimum gains, respectively. Assuming that the frequency is low enough to ignore the shunt reactance of the input and high enough so that the reactance of moderately sized ac coupling capacitors can be considered negligible, the insertion loss, Il, due to the shunt divider can be expressed as

$$Il(dB) = 20\log\left(\frac{R_{IN}}{R_{SERIES} + R_{IN}}\right) \quad (3)$$

The necessary shunt component, R_{SHUNT}, to match to the source impedance, R_S, can be expressed as

$$R_{SHUNT} = \frac{1}{\frac{1}{R_S} - \frac{1}{R_{SERIES} + R_{IN}}} \quad (4)$$

The insertion loss and the resultant power gain for multiple shunt resistor values are summarized in Table 8. The source resistance and input impedance need careful attention when using Equation 3 and Equation 4. The reactance of the input impedance of the ADL5562 and the ac coupling capacitors must be considered before assuming that they make a negligible contribution.

Table 8. Gain Adjustment Using Series Resistor

Il (dB)	R_{IN} (Ω)	R_S (Ω)	R_{SERIES} (Ω)	R_{SHUNT} (Ω)
2	400	50	105	54.9
4	400	50	232	54.9
2	200	50	51.1	61.9
4	200	50	115	59
2	133	50	34.8	71.5
2	400	200	102	332
4	400	200	232	294
2	200	200	51.1	976
4	200	200	115	549
2	400	50	105	54.9
4	400	50	232	54.9
2	200	50	51.1	61.9

ADC INTERFACING

The ADL5562 is a high output linearity amplifier that is optimized for ADC interfacing. There are several options available to the designer when using the ADL5562. Figure 37 shows a simplified wideband interface with the ADL5562 driving the AD9445. The AD9445 is a 14-bit, 125 MSPS ADC with a buffered wideband input.

For optimum performance, the ADL5562 should be driven differentially using an input balun. Figure 37 uses a wideband 1:1 transmission line balun followed by two 34.8 Ω resistors in parallel with the three input impedances (which change with the gain selection of the AD55L62) to provide a 50 Ω differential input impedance. This provides a wideband match to a 50 Ω source. The ADL5562 is ac-coupled from the AD9445 to avoid common-mode dc loading. The 33 Ω series resistors help to improve the isolation between the ADL5562 and any switching currents present at the analog-to-digital sample-and-hold input circuitry. The AD9445 input presents a 2 kΩ differential load impedance and requires a 2 V p-p differential input swing to reach full scale (VREF = 1 V).

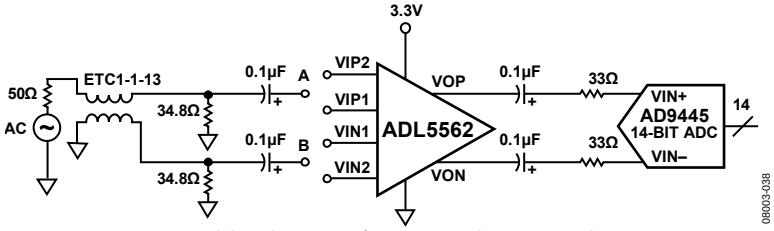


Figure 37. Wideband ADC Interfacing Example Featuring the AD9445

This circuit provides variable gain, isolation, and source matching for the AD9445. Using this circuit with the ADL5562 in a gain of 6 dB, an SFDR performance of 87 dBc is achieved at 140 MHz, and a −3 dB bandwidth of 760 MHz, as indicated in Figure 38 and Figure 39.

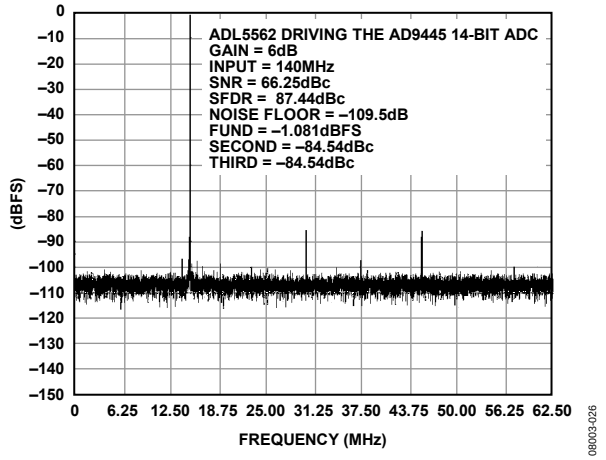


Figure 38. Measured Single-Tone Performance of the Circuit in Figure 37 for a 100 MHz Input Signal

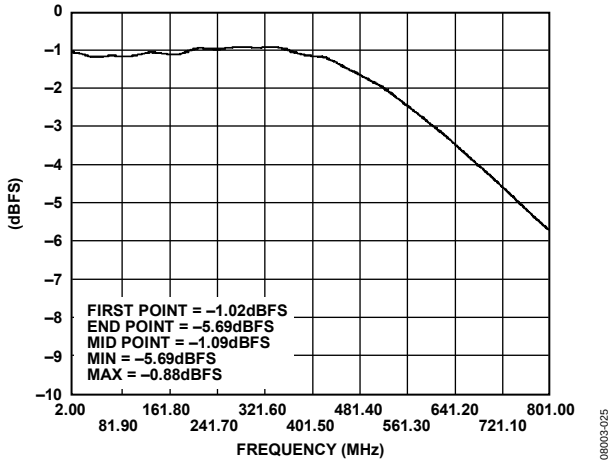


Figure 39. Measured Frequency Response of the Wideband ADC Interface Depicted in Figure 37

The wideband frequency response is an advantage in broadband applications, such as predistortion receiver designs and instrumentation applications. However, by designing for a wide analog input frequency range, the cascaded SNR performance is somewhat degraded due to high frequency noise aliasing into the wanted Nyquist zone.

An alternative narrow-band approach is presented in Figure 40. By designing a narrow band-pass antialiasing filter between the ADL5562 and the target ADC, the output noise of the ADL5562 outside of the intended Nyquist zone can be attenuated, helping to preserve the available SNR of the ADC. In general, the SNR improves several decibels when including a reasonable order antialiasing filter. In this example, a low loss 1:1 input transformer is used to match the ADL5562 balanced input to a 50 Ω unbalanced source, resulting in minimum insertion loss at the input.

Figure 40 is optimized for driving some of the Analog Devices popular unbuffered ADCs, such as the AD9246, AD9640, and AD6655. Table 9 includes antialiasing filter component recommendations for popular IF sampling center frequencies. Inductor L5 works in parallel with the on-chip ADC input capacitance and a portion of the capacitance presented by C4 to form a resonant tank circuit. The resonant tank helps to ensure that the ADC input looks like a real resistance at the target center frequency. The L5 inductor shorts the ADC inputs at dc, which introduces a zero into the transfer function. In addition, the ac coupling capacitors introduce additional zeros into the transfer function. The final overall frequency response takes on a band-pass characteristic, helping to reject noise outside of the intended Nyquist zone. Table 9 provides initial suggestions for prototyping purposes. Some empirical optimization may be needed to help compensate for actual PCB parasitics.

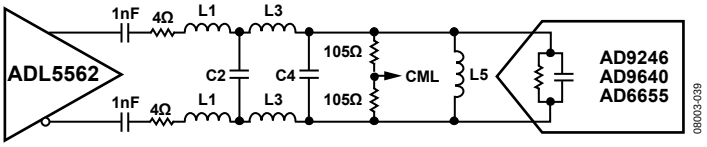


Figure 40. Narrow-Band IF Sampling Solution for an Unbuffered ADC Application

Table 9. Interface Filter Recommendations for Various IF Sampling Frequencies

Center Frequency (MHz)	1 dB Bandwidth (MHz)	L1 (nH)	C2 (pF)	L3 (nH)	C4 (pF)	L5 (nH)
96	30	3.3	47	27	75	100
140	33	3.3	47	27	33	120
170	32	3.3	56	27	22	110
211	33	3.3	47	27	18	56

LAYOUT CONSIDERATIONS

High-Q inductive drives and loads, as well as stray transmission line capacitance in combination with package parasitics, can potentially form a resonant circuit at high frequencies, resulting in excessive gain peaking or possible oscillation. If RF transmission lines connecting the input or output are used, they should be designed such that stray capacitance at the input/output pins is minimized. In many board designs, the signal trace widths should be minimal where the driver/receiver is more than one-eighth of the wavelength from the amplifier. This nontransmission line configuration requires that underlying and adjacent ground and low impedance planes be dropped from the signal lines

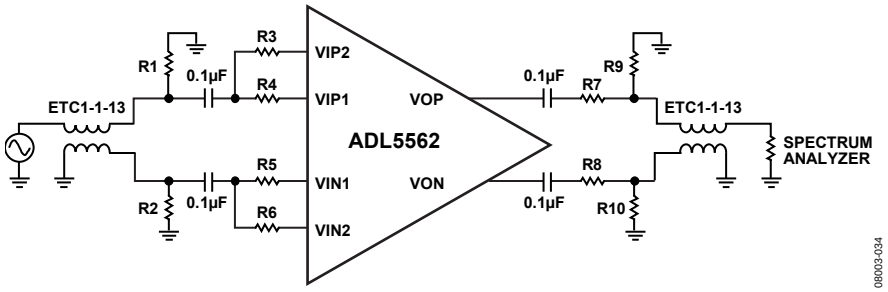


Figure 41. General Purpose Characterization Circuit

Table 10. Gain Setting and Input Termination Components for Figure 41

A_V (dB)	R1 (Ω)	R2 (Ω)	R3 (Ω)	R4 (Ω)	R5 (Ω)	R6 (Ω)
6	29	29	Open	0	0	Open
12	33	33	0	Open	Open	0
15.5	40.2	40.2	0	0	0	0

Table 11. Output Matching Network for Figure 41

R_L (Ω)	R7 (Ω)	R8 (Ω)	R9 (Ω)	R10 (Ω)
200	84.5	84.5	34.8	34.8
1 k	487	487	25	25

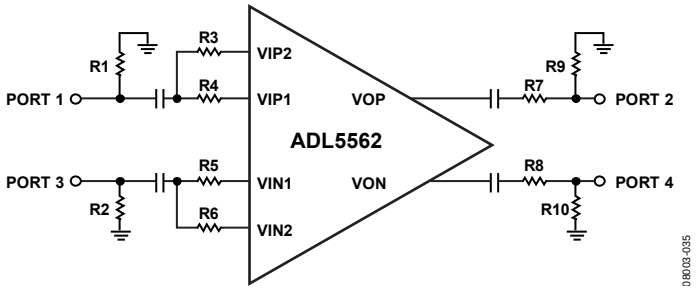


Figure 42. Differential Characterization Circuit Using Agilent E8357A 4-Port PNA

Table 12. Gain Setting and Input Termination Components for Figure 42

A_V (dB)	R1 (Ω)	R2 (Ω)	R3 (Ω)	R4 (Ω)	R5 (Ω)	R6 (Ω)
6	67	67	Open	0	0	Open
12	100	100	0	Open	Open	0
15.5	200	200	0	0	0	0

Table 13. Output Matching Network for Figure 42

R_L (Ω)	R7 (Ω)	R8 (Ω)	R9 (Ω)	R10 (Ω)
200	50	50	Open	Open
1 k	475	475	61.9	61.9

SOLDERING INFORMATION

On the underside of the chip scale package, there is an exposed compressed paddle. This paddle is internally connected to the ground of the chip. Solder the paddle to the low impedance ground plane on the PCB to ensure the specified electrical performance and to provide thermal relief. To further reduce thermal impedance, it is recommended that the ground planes on all layers under the paddle be stitched together with vias.

EVALUATION BOARD

Figure 43 shows the schematic of the ADL5562 evaluation board. The board is powered by a single supply in the 3 V to 3.6 V range. The power supply is decoupled by 10 µF and 0.1 µF capacitors.

Table 14 details the various configuration options of the evaluation board. Figure 44 and Figure 45 show the component and circuit layouts of the evaluation board.

To realize the minimum gain (6 dB into a 200 Ω load), Input 1 (VIN1 and VIP1) must be used by installing 0 Ω resistors at R3 and R4, leaving R5 and R6 open. R1 and R2 must be 33 Ω for a 50 Ω input impedance.

Likewise, driving Input 2 (VIN2 and VIP2) realizes the middle gain (12 dB into a 200 Ω load) by installing 0 Ω at R5 and R6 and leaving R3 and R4 open. R1 and R2 must be 29 Ω for a 50 Ω input impedance.

For the maximum gain (15.5 dB into a 200 Ω load), both inputs are driven by installing 0 Ω resistors at R3, R4, R5, and R6. R1 and R2 must be 40.2 Ω for a 50 Ω input impedance.

The balanced input and output interfaces are converted to single ended with a pair of baluns (M/A-COM ETC1-1-13). The balun at the input, T1, provides a 50 Ω single-ended-to-differential transformation. The output balun, T2, and the matching components are configured to provide a 200 Ω to 50 Ω impedance transformation with an insertion loss of about 17 dB.

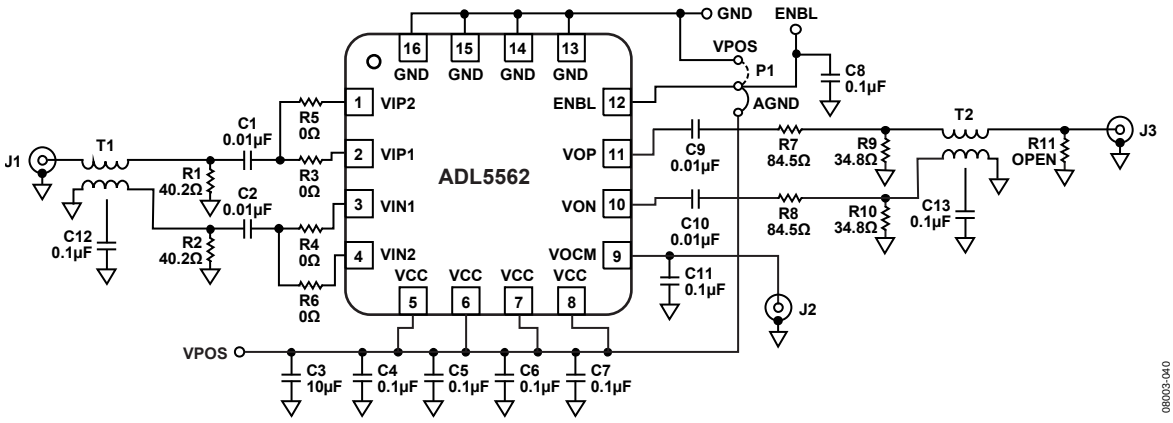


Figure 43. Evaluation Board Schematic

Table 14. Evaluation Board Configuration Options

Component	Description	Default Condition
VPOS, GND	Ground and supply vector pins.	VPOS, GND = installed
C3, C4, C5, C6, C7, C11	Power supply decoupling. The supply decoupling consists of a 10 µF capacitor (C3) to ground. C4 to C7 are bypass capacitors. C11 ac couples VREF to ground.	C3 = 10 µF (Size D), C4, C5, C6, C7, C11 = 0.1 µF (Size 0402)
J1, R1, R2, R3, R4, R5, R6, C1, C2, C12, T1	Input interface. The SMA labeled J1 is the input. T1 is a 1-to-1 impedance ratio balun to transform a single-ended input into a balanced differential signal. C1 and C2 provide ac coupling. C12 is a bypass capacitor. R1 and R2 provide a differential 50 Ω input termination. R3 to R6 are used to select the input for the pin-strappable gain. Maximum gain: R3, R4, R5, R6 = 0 Ω; and R1, R2 = 40.2 Ω. Middle gain: R5, R6 = 0 Ω; and R3, R4 = open; R1, R2 = 33 Ω. Minimum gain: R3, R4 = 0 Ω; and R5, R6 = open; R1, R2 = 29 Ω.	J1 = installed, R1, R2 = 40.2 Ω (Size 0402), R3, R4, R5, R6 = 0 Ω (Size 0402), C1, C2 = 0.01 µF (Size 0402), C12 = 0.1 µF (Size 0402) T1 = ETC1-1-13 (M/A-COM)
J3, R7, R8, R9, R10, R11, C9, C10, C13, T2	Output interface. The SMA labeled J3 is the output. T2 is a 1-to-1 impedance ratio balun to transform a balanced differential signal to a single-ended signal. C13 is a bypass capacitor. R7, R8, R9, and R10 are provided for generic placement of matching components. The evaluation board is configured to provide a 200 Ω to 50 Ω impedance transformation with an insertion loss of 17 dB. C9 and C10 provide ac coupling.	J3 = installed, R7, R8 = 84.5 Ω (Size 0402), R9, R10 = 34.8 Ω (Size 0402), R11 = open (Size 0402), C9, C10 = 0.01 µF (Size 0402), C13 = 0.1 µF (Size 0402) T2 = ETC1-1-13 (M/A-COM)
ENBL, P1, C8	Device enable. C8 is a bypass capacitor. When the P1 jumper is set toward the VPOS label, the ENBL pin is connected to the supply, enabling the device. In the opposite direction, toward the GND label, the ENBL pin is grounded, putting the device in power-down mode.	ENBL, P1= installed, C8 = 0.1 µF (Size 0402)

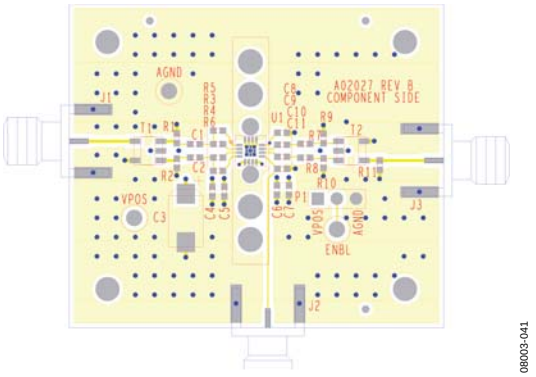


Figure 44. Layout of Evaluation Board, Component Side

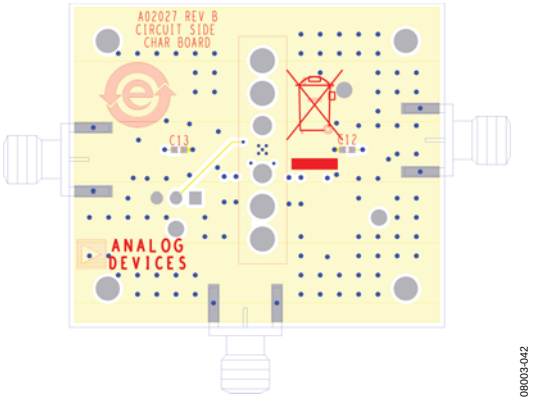


Figure 45. Layout of Evaluation Board, Circuit Side

OUTLINE DIMENSIONS

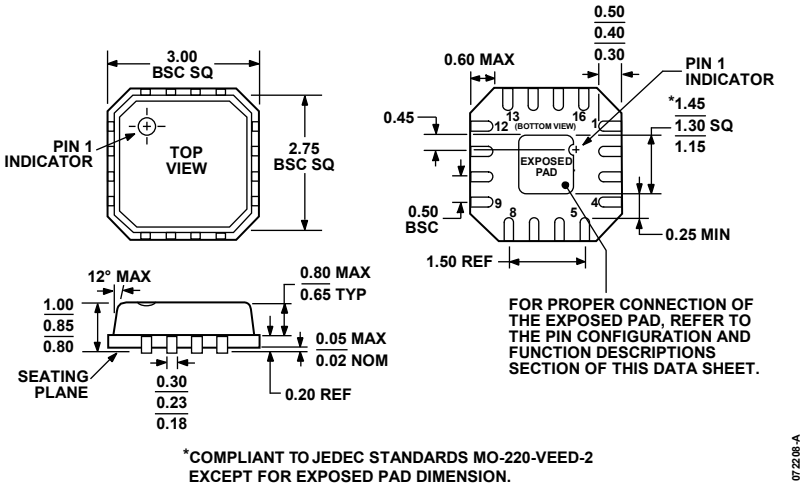


Figure 46. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
3 mm × 3 mm Body, Very Thin Quad
(CP-16-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding	Ordering Quantity
ADL5562ACPZ-R7	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ], 7″ Reel	CP-16-2	Q1Q	1,500
ADL5562ACPZ-WP	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ], Waffle Pack	CP-16-2	Q1Q	50
ADL5562-EVALZ		Evaluation Board			

[1] Z = RoHS Compliant Part.

NOTES

NOTES

NOTES

D08003-0-3/10(B)

SAW Components

SAW IF filter

TD-SCDMA

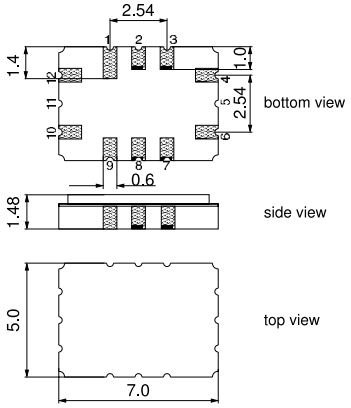
Series/type:	**B5207**
Ordering code:	**B39141B5207H310**
Date:	March 05, 2009
Version:	2.0

Application

- Low-loss IF filter for TD-SCDMA base station
- Usable passband 20.0 MHz
- Balanced or unbalanced operation

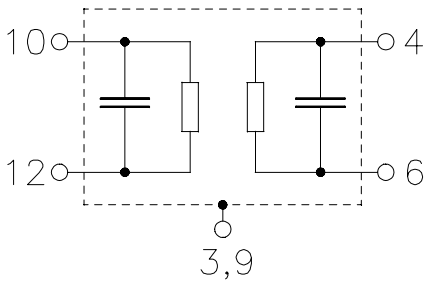
Features

- Package size 7.0 x 5.0 x 1.48 mm^3
- Package code QCC12C
- RoHS compatible
- Approximate weight 0.25 g
- Ceramic Package for **S**urface **M**ount **T**echnology (**SMT**)
- Ni, gold-plated terminals
- **E**lectrostatic **S**ensitive **D**evice (**ESD**)
- Filter surface passivated



Pin configuration

■	10	Input
■	12	Input ground
■	4	Output
■	6	Output ground
■	1, 2, 7, 8	To be grounded
■	3, 9	Case ground

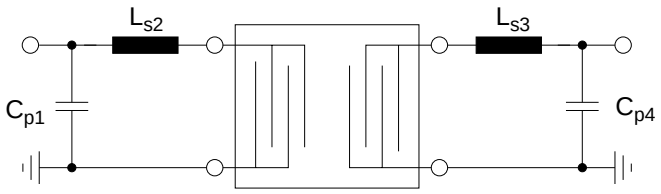


Characteristics

Temperature range for specification: T = –40 ˚C to +85 ˚C
Terminating source impedance: Z_S = 50 Ω and matching network
Terminating load impedance: Z_L = 50 Ω and matching network

		min.	typ. @ 25 ˚C	max.	
Nominal frequency	f_N	—	138.24	—	MHz
Minimum insertion attenuation (including matching network)	α_{min}	—	8.5	10.0	dB
Passband width $\alpha_{rel} \leq$ 1.0 dB	$B_{1.0dB}$	20	23.1	—	MHz
Amplitude ripple (p-p)	$\Delta\alpha$				
$f_N \pm$ 10.0 MHz		—	0.4	1.0	dB
Group delay ripple (p-p)	$\Delta\tau$				
$f_N \pm$ 10.0 MHz		—	40	60	ns
Absolute group delay (mean)	$\bar{\tau}$				
$f_N \pm$ 10.0 MHz		—	665	—	ns
Relative attenuation (relative to α_{min})	α_{rel}				
10.00 MHz ... 90.00 MHz		55	62	—	dB
90.00 MHz ... 108.24 MHz		50	57	—	dB
108.24 MHz ... 117.52 MHz		50	57	—	dB
122.88 MHz		45	52	—	dB
220.40 MHz ... 271.12 MHz		58	75	—	dB
271.12 MHz ... 1000.00 MHz		40	75	—	dB
1dB compression point		12	—	—	dBm
Input IP3		35	—	—	dBm
Temperature coefficient of frequency	TC_f	—	–87	—	ppm/K

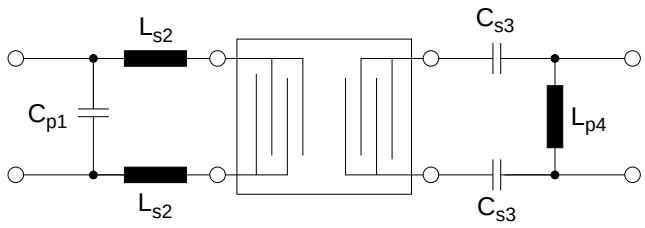
Matching network to 50 Ω



C_{p1} = 27 || 2.2 pF
L_{s2} = 82 nH
L_{s3} = 33 nH
C_{p4} = 47 || 2.2 pF

Element values depend upon board layout and properties.

Matching network to 200 Ω balanced input and 200 Ω balanced output



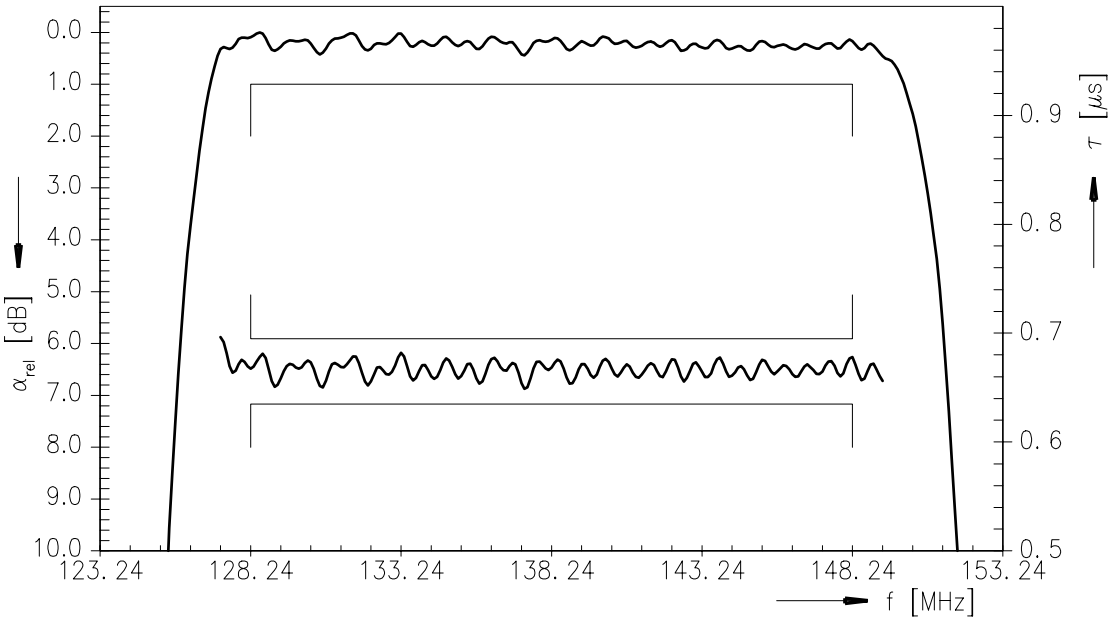
C_{p1} = 18 pF
L_{s2} = 62 nH
C_{s3} = 100 pF
L_{p4} = 47 nH

Element values depend upon board layout and properties.

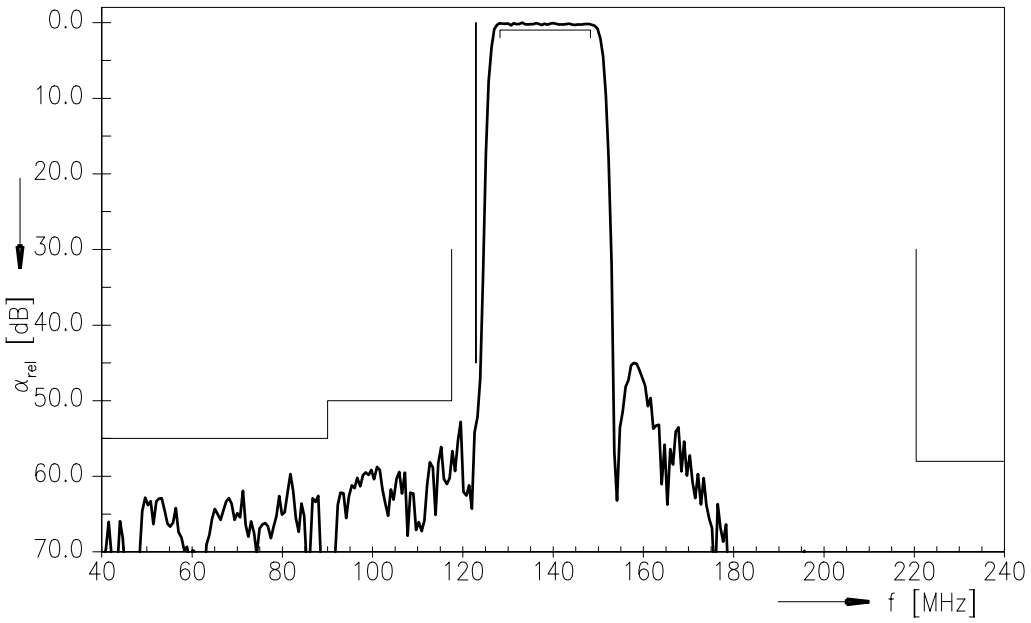
Maximum ratings

Operable temperature range	T	–40/+85	°C	
Storage temperature range	T_{stg}	–40/+85	°C	
DC voltage	V_{DC}	0	V	
Input Power	P_{IN}	10	dBm	

Transfer function (S21, Narrowband)



Transfer function (S21, Wideband)



References

Type	B5207
Ordering code	B39141B5207H310
Marking and package	C61157-A7-A95
Packaging	F61074-V8170-Z000
Date codes	L_1126
S-parameters	
Soldering profile	S_6001
RoHS compatible	defined as compatible with the following documents: "DIRECTIVE 2002/95/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment. 2005/618/EC from April 18th, 2005, amending Directive 2002/95/EC of the European Parliament and of the Council for the purposes of establishing the maximum concentration values for certain hazardous substances in electrical and electronic equipment."

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HMC473MS8 / 473MS8E

v01.1105

GaAs MMIC VOLTAGE VARIABLE ATTENUATOR, 0.45 - 2.2 GHz

Typical Applications

The HMC473MS8 / HMC473MS8E is ideal for:

- Cellular, UMTS/3G Infrastructure
- Portable Wireless
- GPS

Features

RoHS Compliant Product

Single Positive Voltage Control: 0 to +3V

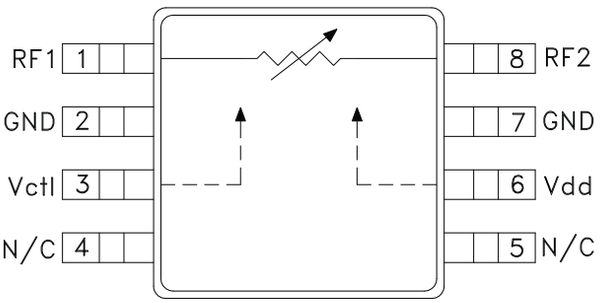
High Attenuation Range: 48 dB @ 0.9 GHz

High P1dB Compression Point: +15 dBm

Ultra Small Package: MSOP8

Replaces HMC173MS8

Functional Diagram



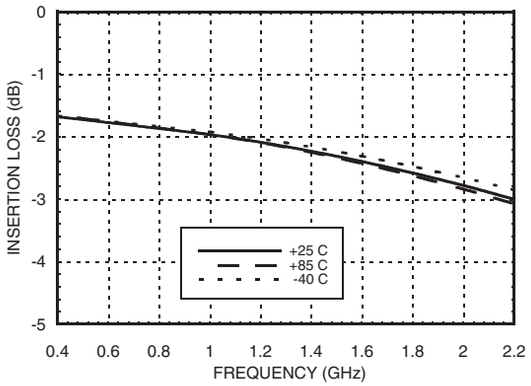
General Description

The HMC473MS8 & HMC473MS8E are general purpose absorptive voltage variable attenuators in 8-lead MSOP packages. The devices operate with a +3.3V supply voltage and a 0 to +3V control voltage. Unique features include a high dynamic attenuation range of up to 48 dB and excellent power handling performance through all attenuation states. The HMC473MS8 & HMC473MS8E are ideal for operation in wireless applications from 0.45 to 1.6 GHz. Operation from 1.7 to 2.2 GHz is possible with a reduced maximum attenuation of 29 to 32 dB. Improved control voltage linearity vs. attenuation can be achieved with an external driver circuit.

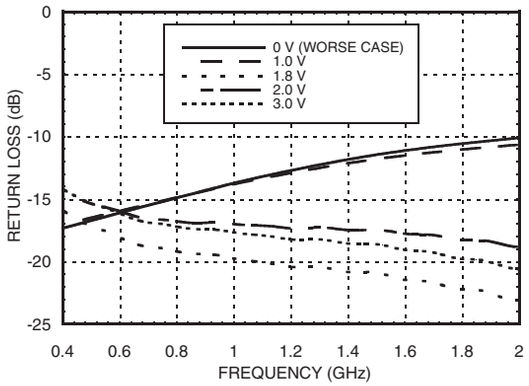
Electrical Specifications, T_A = +25° C, Vdd = +3.3 Vdc, 50 Ohm System

Parameter		Min.	Typ.	Max.	Units
Insertion Loss (Min. Atten.) (Vctl = 0.0 Vdc)	0.45 - 0.8 GHz 0.8 - 1.0 GHz 1.0 - 1.6 GHz 1.6 - 2.0 GHz 2.0 - 2.2 GHz		1.8 1.9 2.4 2.8 3.0	2.2 2.3 2.9 3.3 3.5	dB dB dB dB dB
Attenuation Range (Vctl = 0 to +3 V)	0.45 - 0.8 GHz 0.8 - 1.0 GHz 1.0 - 1.6 GHz 1.6 - 2.0 GHz 2.0 - 2.2 GHz	34 43 32 27 24	39 48 37 32 29		dB dB dB dB dB
Return Loss (Vctl = 0 to +3 V)	0.45 - 0.8 GHz 0.8 - 1.0 GHz 1.0 - 1.6 GHz 1.6 - 2.0 GHz 2.0 - 2.2 GHz		15 14 11 10 9		 dB dB dB
Input Power for 0.1 dB Compression (0.9 GHz)	Min Atten. Atten. >2.0		20 5.5		dBm dBm
Input Power for 1.0 dB Compression (0.9 GHz)	Min Atten. Atten. >2.0	24 11	28 15		dBm dBm
Input Third Order Intercept (0.9 GHz, Two-tone Input Power = +5.0 dBm Each Tone)	Min Atten. Atten. >2.0		47 20		dBm dBm
Switching Characteristics tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)	0.45 - 2.2 GHz		1.3 1.5		 µS µS

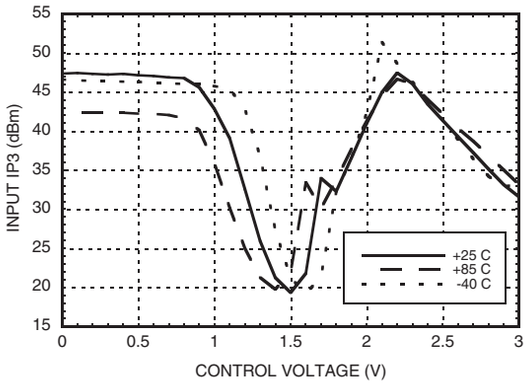
Insertion Loss vs. Temperature



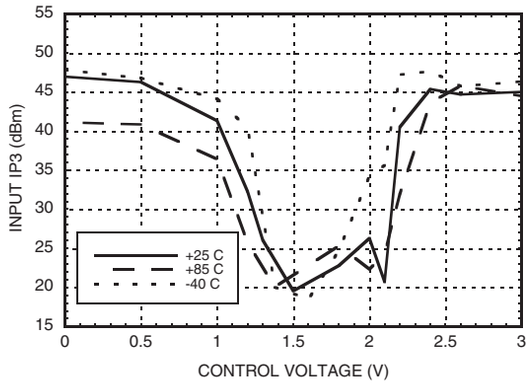
Return Loss vs. Control Voltage



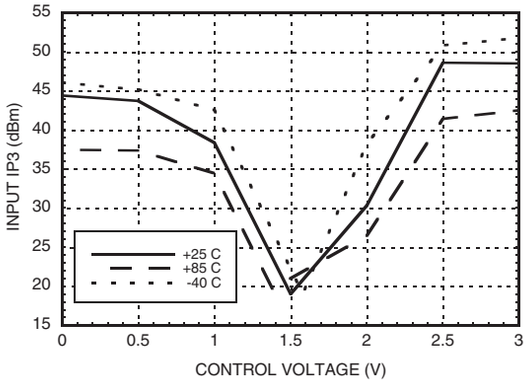
Input IP3 vs. Control Voltage @ 0.45 GHz



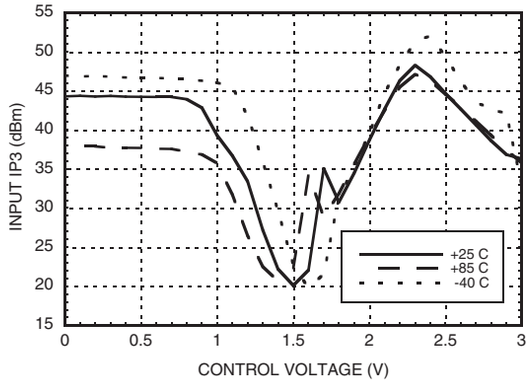
Input IP3 vs. Control Voltage @ 0.9 GHz



Input IP3 vs. Control Voltage @ 1.9 GHz



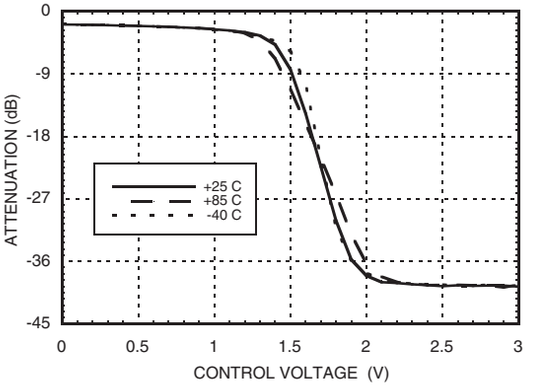
Input IP3 vs. Control Voltage @ 2.1 GHz



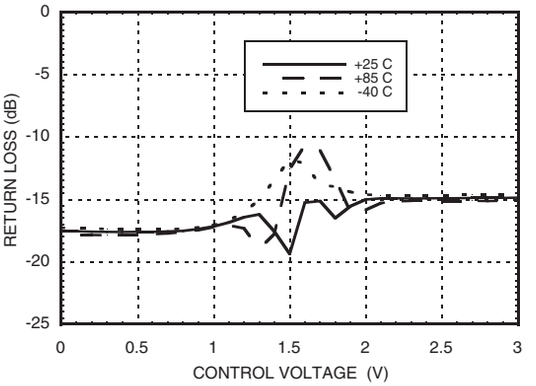
HMC473MS8 / 473MS8E

GaAs MMIC VOLTAGE VARIABLE ATTENUATOR, 0.45 - 2.2 GHz

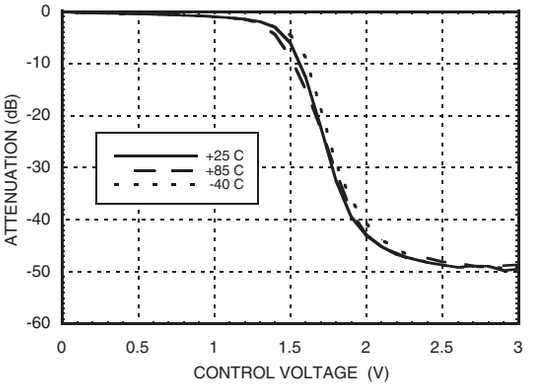
Relative Attenuation vs. Control Voltage @ 0.45 GHz



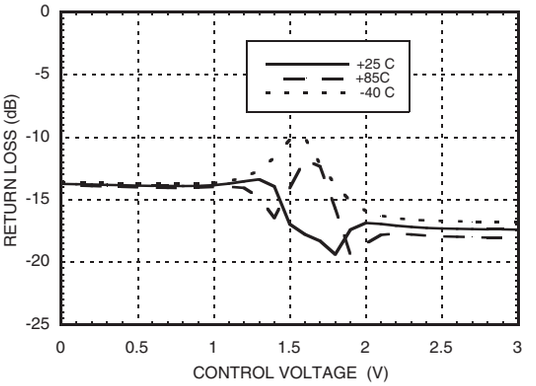
Return Loss vs. Control Voltage @ 0.45 GHz



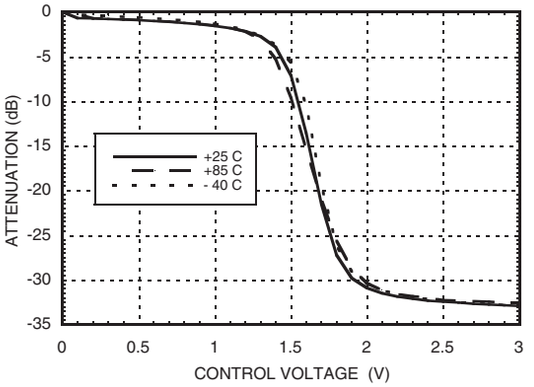
Relative Attenuation vs. Control Voltage @ 0.9 GHz



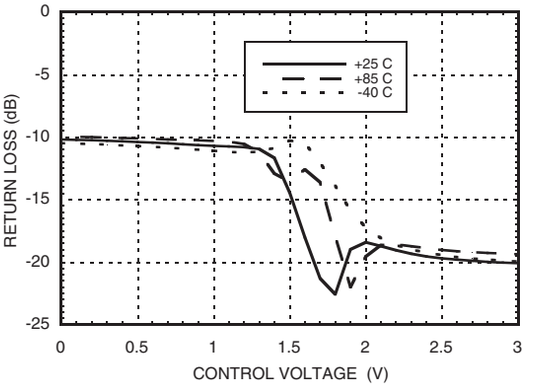
Return Loss vs. Control Voltage @ 0.9 GHz



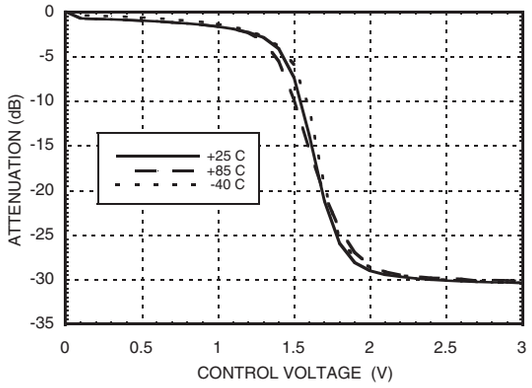
Relative Attenuation vs. Control Voltage @ 1.9 GHz



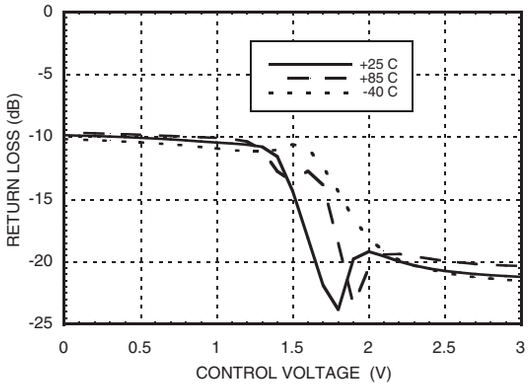
Return Loss vs. Control Voltage @ 1.9 GHz



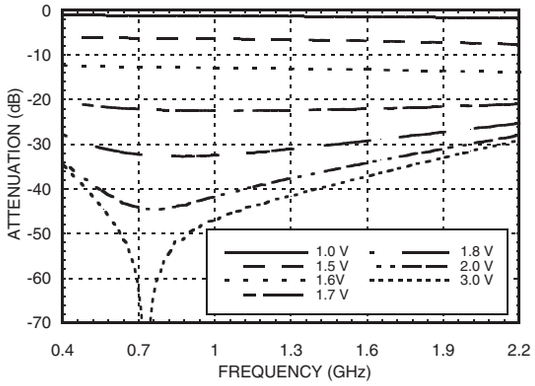
Relative Attenuation vs. Control Voltage @ 2.1 GHz



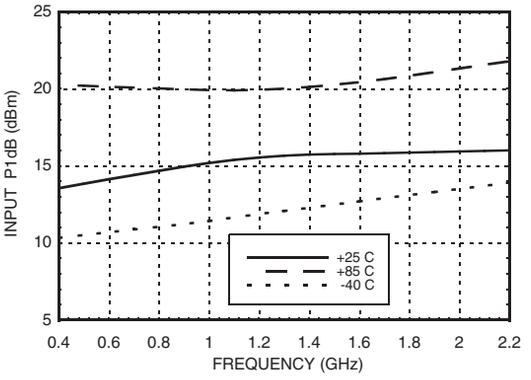
Return Loss vs. Control Voltage @ 2.1 GHz



Relative Attenuation vs. Control Voltage



Worse Case Input P1dB vs. Temperature



MICROWAVE CORPORATION v01.1105

HMC473MS8 / 473MS8E

GaAs MMIC VOLTAGE VARIABLE ATTENUATOR, 0.45 - 2.2 GHz

Absolute Maximum Ratings

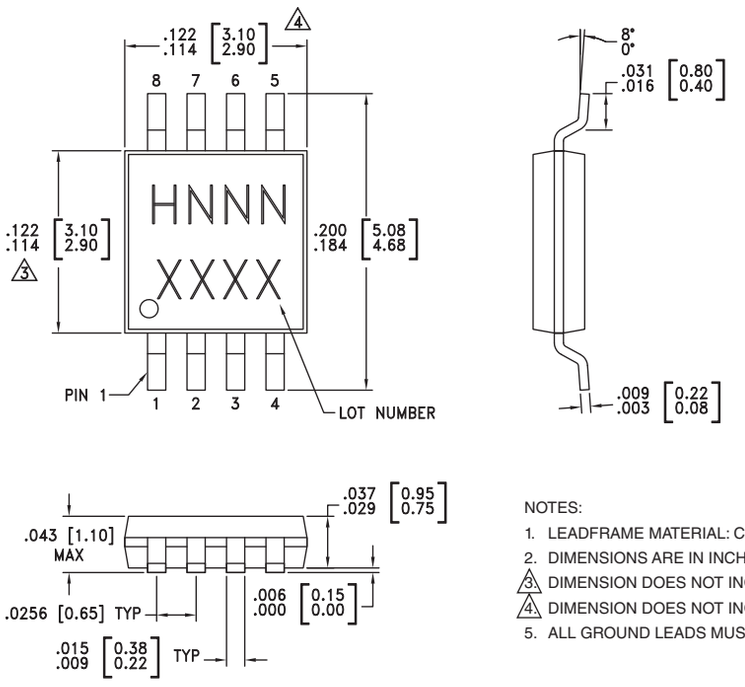
V_{CTL}	-0.2 Vdc to Vdd
Vdd	+8 Vdc
Maximum Input Power Vdd = +3.3 Vdc	+29 dBm Min. Atten. +21 dBm Attenuation >2 dB
Channel Temperature (Tc)	150 °C
Thermal Resistance (R_{TH}) (junction to lead)	92 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

Control and Bias Voltage

V_{CTL}	0 to +3 Vdc @ 1 µA
Vdd	+3.3 Vdc ± 0.1 Vdc @ 10 µA

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

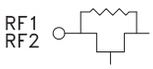
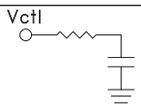
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
4. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
5. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC473MS8	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H473 XXXX
HMC473MS8E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H473 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 8	RF1, RF2	These pins are DC coupled and matched to 50 Ohms. DC blocking capacitors are required. 330pF capacitors are supplied on evaluation board.	
2, 7	GND	Pins must connect to RF ground.	
3	Vctl	Control voltage	
4, 5	N/C	No Connection. These pins may be connected to RF ground. Performance will not be affected.	
6	Vdd	Supply Voltage.	

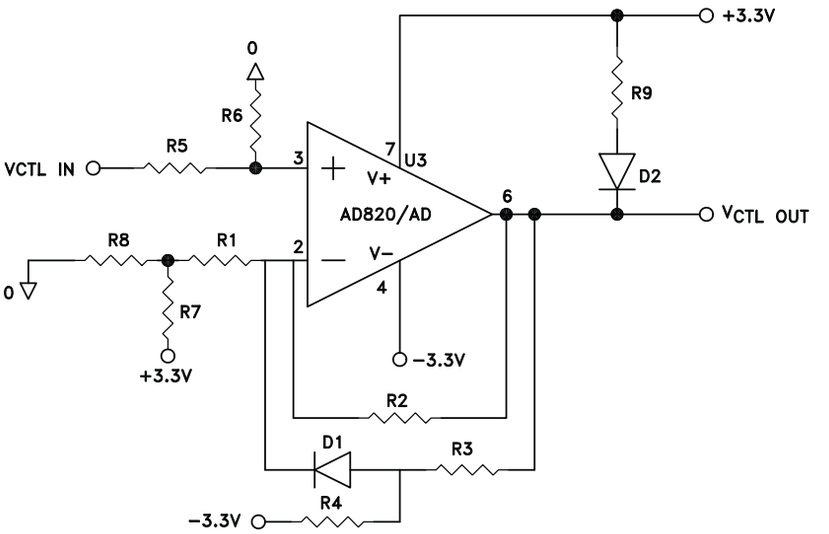
Attenuation Linearizing Control Circuit For The HMC473MS8 / HMC473MS8E Voltage Variable Attenuator

A driver circuit to improve the attenuation linearity of the HMC473MS8 & HMC473MS8E can be implemented with a simple op-amp configuration. A *breakpoint* linearization circuit will scale the voltage supplied to the control line of the HMC473MS8 & HMC473MS8E, so that a more linear attenuation vs. control voltage slope can be achieved. A -3.3V and +3.3V supply is required.

Diode and resistor values which define the op-amp gain, and breakpoint were selected to optimize a measured production lot of attenuators at 0.9 GHz. R7 may be varied to optimize the performance of any given attenuator. If the input voltage to the linearizing circuit will not drop below 1.0V, the R9 and D2 may be omitted, and this will greatly reduce the overall power consumption of the driver circuit.

The linearizing circuit has been optimized for 0.9 GHz attenuation applications. A similar approach may be used at other frequencies by adjusting R1 - R9 resistor values.

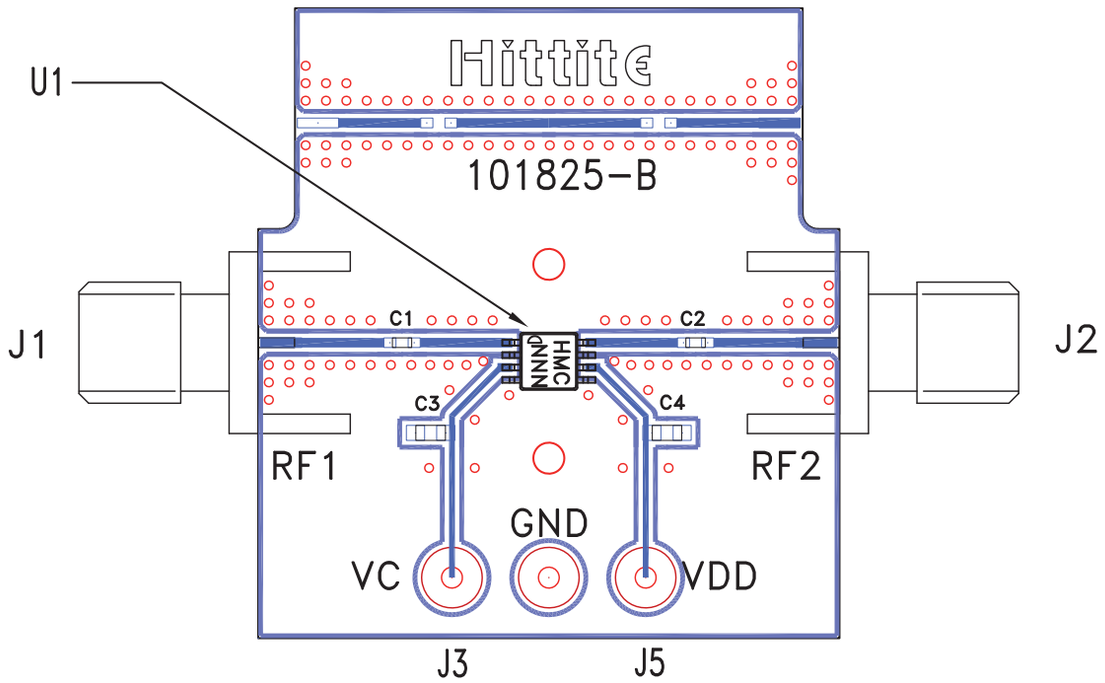
Application Circuit



Required Parts List

Part	Description	Manufacturer
AD822	Op-Amp	Analog Devices
R1	10K ohms	Panasonic
R2	200K ohms	Panasonic
R3	7.5K ohms	Panasonic
R4	39K ohms	Panasonic
R5	220K ohms	Panasonic
R6	91K ohms	Panasonic
R7	910 ohms	Panasonic
R8	51 ohms	Panasonic
R9	100 ohms	Panasonic
D1, D2	LL4148 D-35	Digi-Key

Evaluation PCB



List of Materials for Evaluation PCB 101827 [1]

Item	Description
J1 - J2	PCB Mount SMA RF Connector
J3 - J5	DC PIN
C1, C2	330pF capacitor, 0402 Pkg.
C3, C4	10KpF capacitor, 0603 Pkg.
U1	HMC473MS8 / HMC473MS8E
PCB [2]	101825 Eval Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should be generated with proper RF circuit design techniques. Signal lines at the RF ports should be 50 ohm impedance and the package ground leads should be connected directly to the PCB RF ground plane, similar to that shown above. The evaluation circuit board shown above is available from Hittite Microwave Corporation upon request.

HMC624LP4 / 624LP4E

0.5 dB LSB GaAs MMIC 6-BIT DIGITAL ATTENUATOR, DC - 6 GHz

Typical Applications

The HMC624LP4(E) is ideal for:

- Cellular/3G Infrastructure
- WiBro / WiMAX / 4G
- Microwave Radio & VSAT
- Test Equipment and Sensors
- IF & RF Applications

Features

0.5 dB LSB Steps to 31.5 dB

Power-Up State Selection

High Input IP3: +55 dBm

Low Insertion Loss: 2.2 dB @ 3.5 GHz

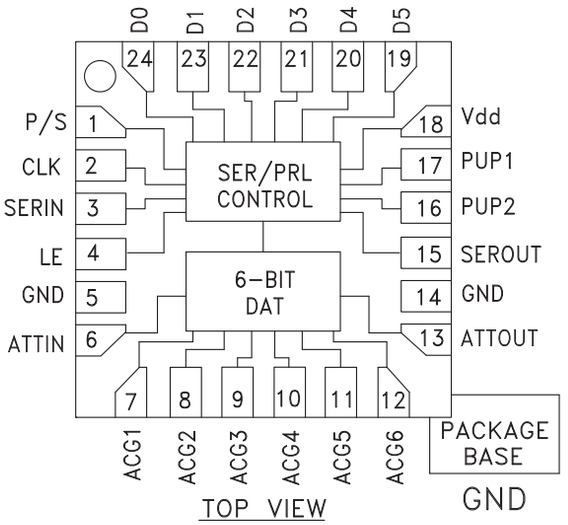
TTL/CMOS Compatible, Serial, Parallel or Latched Parallel Control

±0.25 dB Typical Step Error

Single +3V or +5V Supply

24 Lead 4x4mm SMT Package: $16mm^2$

Functional Diagram



General Description

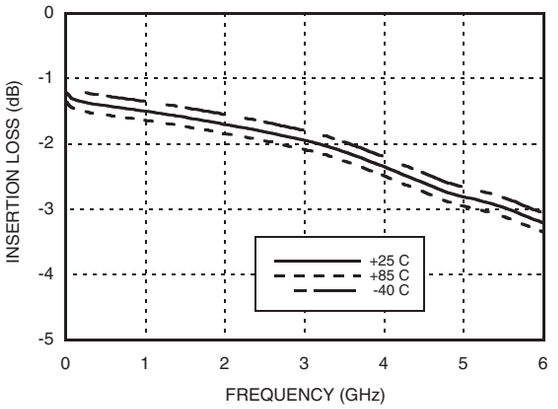
The HMC624LP4(E) is a broadband 6-bit GaAs IC Digital Attenuator in a low cost leadless SMT package. This versatile digital attenuator incorporates off-chip AC ground capacitors for near DC operation, making it suitable for a wide variety of RF and IF applications. The dual mode control interface is CMOS/TTL compatible, and accepts either a three wire serial input or a 6 bit parallel word. The HMC624LP4(E) also features a user selectable power up state and a serial output port for cascading other Hittite serial controlled components. The HMC624LP4(E) is housed in a RoHS compliant 4x4 mm QFN leadless package, and requires no external matching components.

Electrical Specifications, T_A = +25° C, 50 Ohm System, with Vdd = +5V & Vctl = 0/+5V (Unless Otherwise Noted)

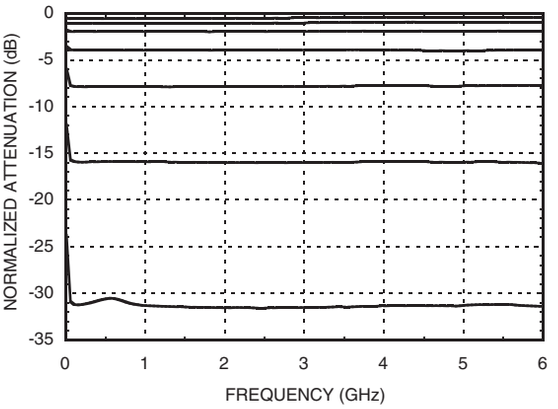
Parameter	Frequency (GHz)	Min.	Typ.	Max.	Units
Insertion Loss	DC - 3 GHz 3.0 - 6.0 GHz		1.8 2.8	2.4 3.8	dB dB
Attenuation Range			31.5		dB
Return Loss (ATTIN, ATTOUT, All Atten. States)	DC - 6 GHz		15		dB
Attenuation Accuracy: (Referenced to Insertion Loss) All Attenuation States	DC - 0.8 GHz 0.8 - 6.0 GHz	± (0.10 + 5% of Atten. Setting) Max. ± (0.30 + 3% of Atten. Setting) Max.			dB dB
Input Power for 0.1 dB Compression	DC - 6 GHz		30		dBm
Input Third Order Intercept Point (Two-Tone Input Power= 10 dBm Each Tone)	DC - 6 GHz		55		dBm

0.5 dB LSB GaAs MMIC 6-BIT DIGITAL ATTENUATOR, DC - 6 GHz

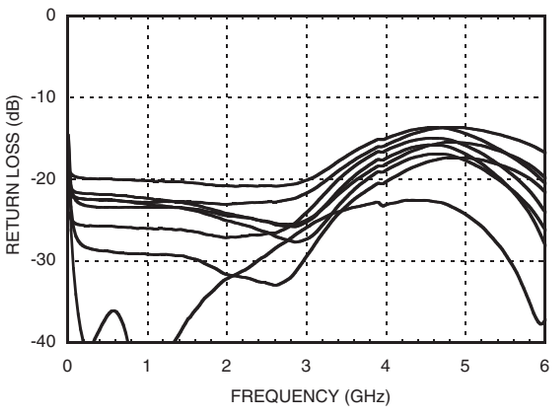
Insertion Loss vs. Temperature [1]



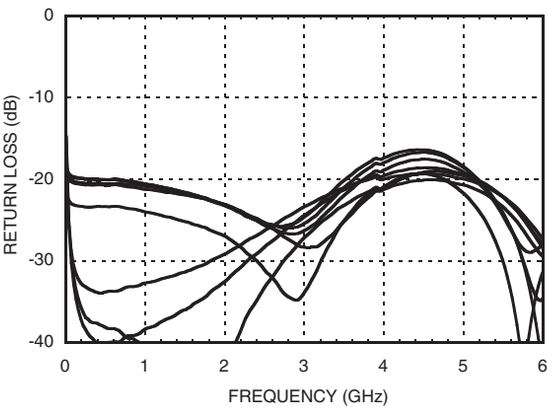
Normalized Attenuation [1]
(Only Major States are Shown)



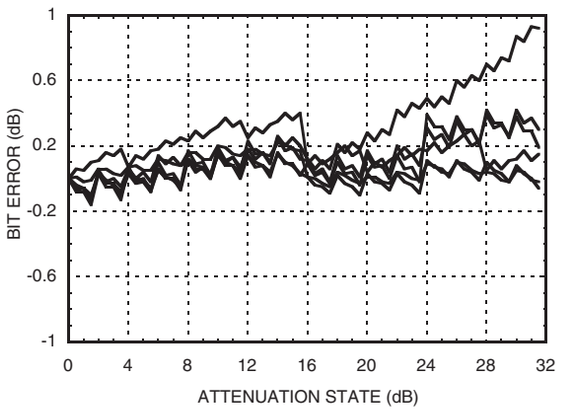
Input Return Loss [1]
(Only Major States are Shown)



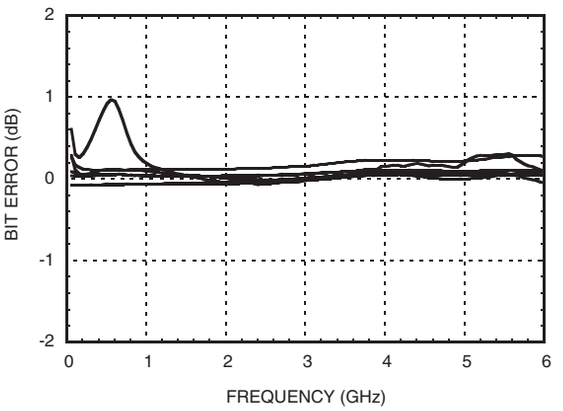
Output Return Loss [1]
(Only Major States are Shown)



Bit Error vs. Attenuation State [2]

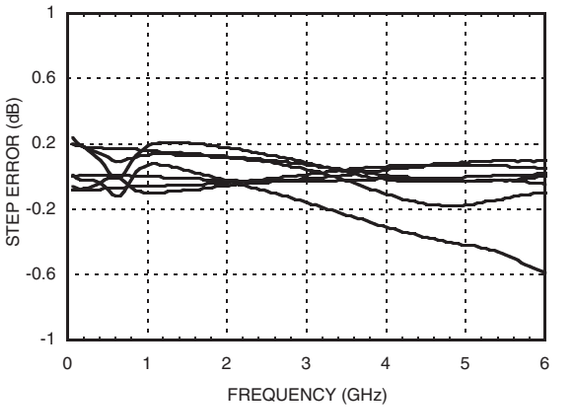


Bit Error vs. Frequency [2]
(Only Major States are Shown)

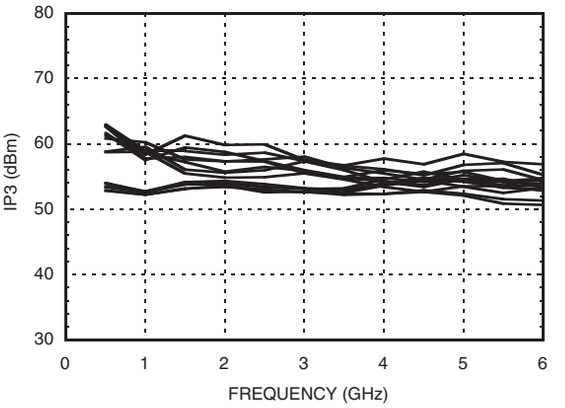


[1] Data taken with bias tees on input and output RF ports.
[2] C1, C6 = 330pF

Worst Case Step Error Between Successive Attenuation States [2]



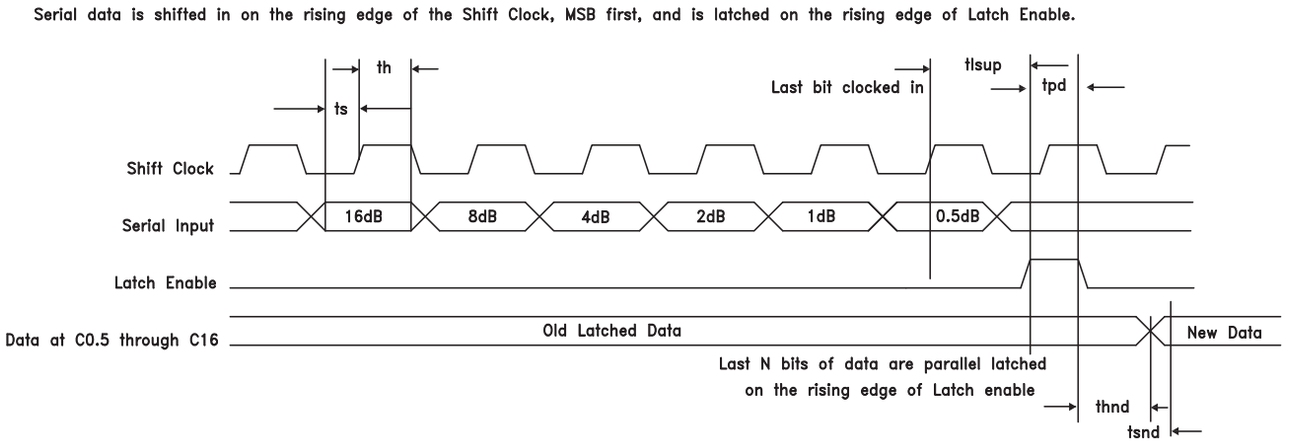
IP3 vs. Temperature [2]



Serial Mode

The serial mode is enabled when P/S is set to high. Data is entered MSB first and after the 6th shift clock cycle the LE (Latch Enable) is pulsed High and then Low. See timing diagram below for reference.

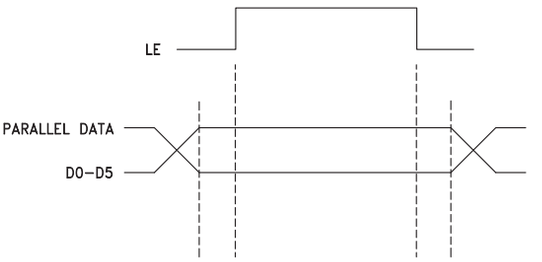
Timing Diagram



Timing

Parameter	Symbol	Vdd = +5V (Typ.)	Units
Serial Input Setup Time	ts	20	ns
Hold Time from Serial Input to Shift Clock	th	20	ns
Setup Time from Shift Clock to Latch Enable	tlsup	40	ns
Propagation Delay	tpd	10	ns
Setup Time for New Data	tsnd	10	ns

Timing Diagram *(Latched Parallel Mode)*



Parallel Mode *(Direct Parallel Mode & Latched Parallel Mode)*

Note: The parallel mode is enabled when P/S is set to low.

Direct Parallel Mode - The attenuation state is changed by the Control Voltage Inputs directly. The LE (Latch Enable) must be at a logic high to control the attenuator in this manner.

Latched Parallel Mode - The attenuation state is selected using the Control Voltage Inputs and set while the LE is in the Low state. The attenuator will not change state while LE is Low. Once all Control Voltage Inputs are at the desired states the LE is pulsed. See timing diagram below for reference.

HMC624LP4 / 624LP4E

0.5 dB LSB GaAs MMIC 6-BIT DIGITAL ATTENUATOR, DC - 6 GHz

Power-Up States

Using the Parallel PUP truth table the attenuator can be turned on at a specific attenuation state. By using the PUP1 and PUP2 line four different attenuation states can be selected. It can also be used in the Direct Parallel Mode using the Control Voltage Inputs to select attenuation values.

Parallel PUP Truth Table

P/S	LE	PUP1	PUP2	Attenuation State
0	0	0	0	31.5 dB
0	0	1	0	24 dB
0	0	0	1	16 dB
0	0	1	1	Insertion Loss
0	1	X	X	0.5 to 31.5 dB

Note: Power-Up with LE= 1 provides normal parallel operation with D0 - D5, and PUP1 and PUP2 are not active.

Absolute Maximum Ratings

RF Input Power (DC - 6 GHz)	28 dBm (T = +85 °C)
Digital Inputs ($\overline{\text{Reset}}$, Shift Clock, Latch Enable & Serial Input)	-1.5V to (Vdd +1.5V) Vdc
Bias Voltage (Vdd)	5.6 Vdc
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 9.8 mW/°C above 85 °C) [1]	0.635 W
Thermal Resistance	102 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

Truth Table

Control Voltage Input						Attenuation State
D5	D4	D3	D2	D1	D0	
High	High	High	High	High	High	Reference I.L.
High	High	High	High	High	Low	0.5 dB
High	High	High	High	Low	High	1 dB
High	High	High	Low	High	High	2 dB
High	High	Low	High	High	High	4 dB
High	Low	High	High	High	High	8 dB
Low	High	High	High	High	High	16 dB
Low	Low	Low	Low	Low	Low	31.5 dB
Any combination of the above states will provide an attenuation approximately equal to the sum of the bits selected.						

Bias Voltage

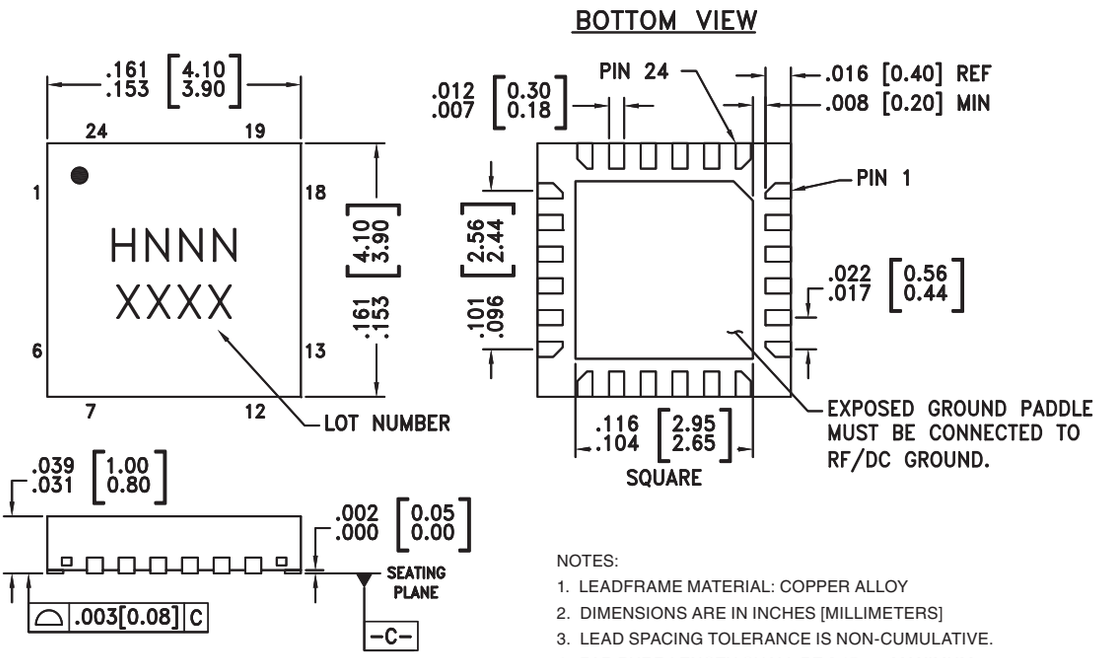
Vdd (Vdc)	Idd (Typ.) (mA)
3	1.8
5	2.0

TTL/CMOS Control Voltage

State	Vdd= +3V or +5V
Low	0 to 0.8V
High	2.0V to Vdd

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

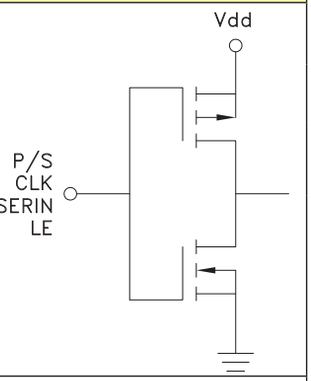
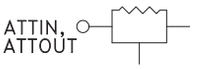
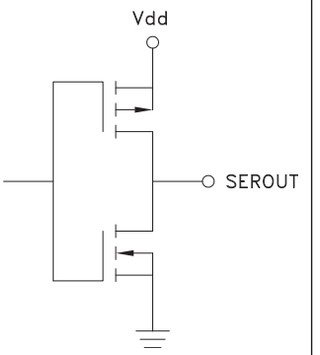
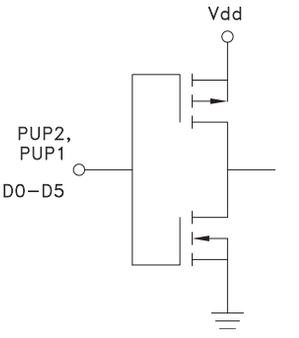
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

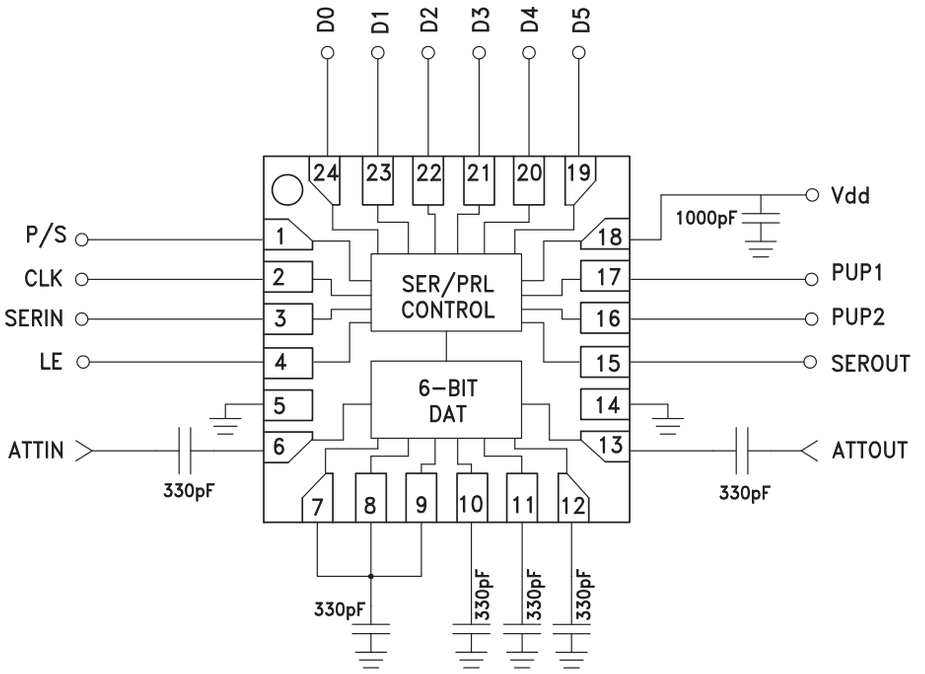
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC624LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H624 XXXX
HMC624LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H624 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

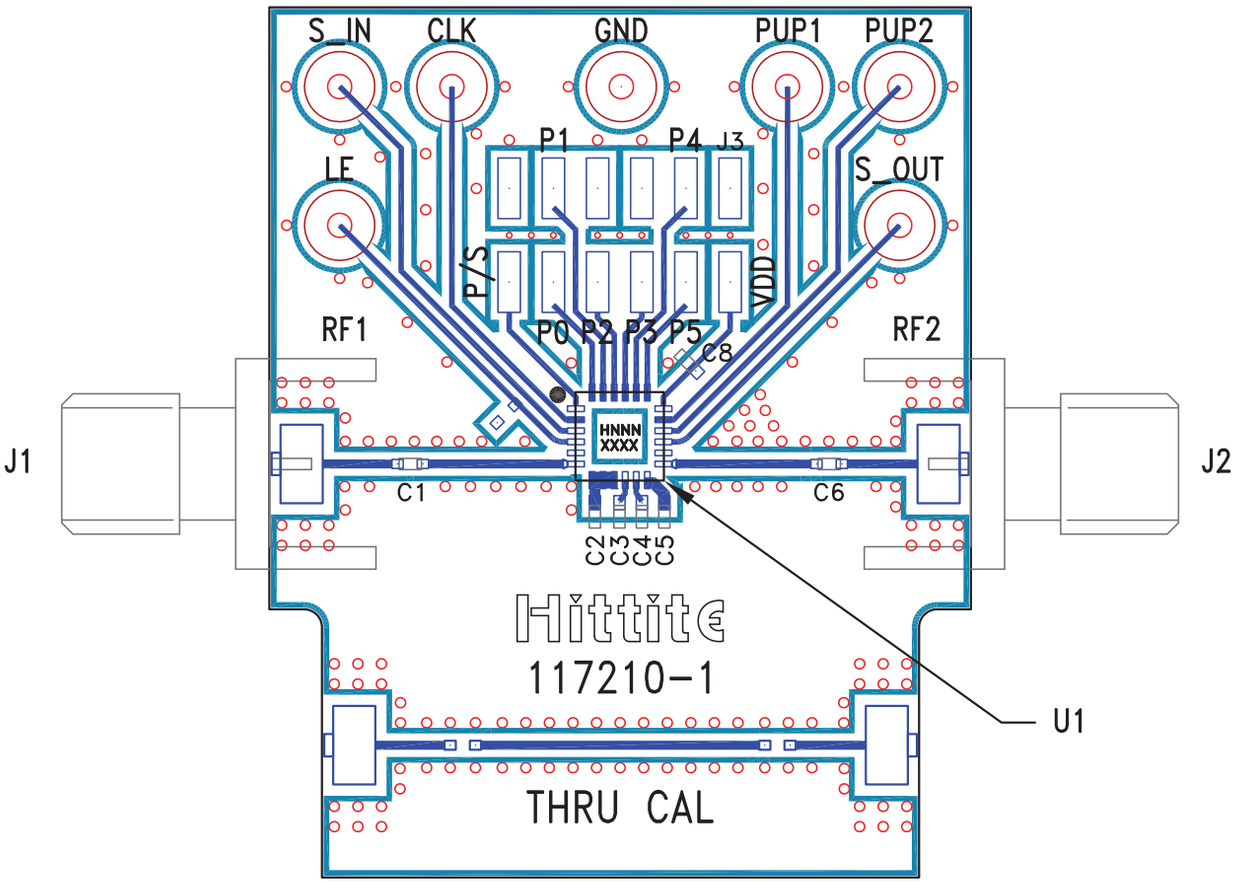
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	P/S	See truth table, control voltage table and timing diagram.	
2	CLK		
3	SERIN		
4	LE		
5, 14	GND	These pins and package bottom must be connected to RF/DC ground.	
6, 13	ATTIN, ATTOUT	These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required. Select value based on lowest frequency of operation.	
7 - 12	ACG1 - ACG6	External capacitors to ground is required. Select value for lowest frequency of operation. Place capacitor as close to pins as possible.	
15	SEROUT	Serial input data delayed by 6 clock cycles.	
16, 17 19 - 24	PUP2, PUP1 D5, D4, D3, D2, D1, D0	See truth table, control voltage table and timing diagram.	
18	Vdd	Supply voltage	

Application Circuit



Evaluation PCB



List of Materials for Evaluation PCB 117212 [1]

Item	Description
J1 - J2	PCB Mount SMA Connector
J3	14 Pin DC Connector
C1, C6	330 pF Capacitor, 0402 Pkg.
C7, C8	1000 pF Capacitor, 0402 Pkg.
U1	HMC624LP4(E) Digital Attenuator
PCB [2]	117210 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Notes:

HMC668LP3 / 668LP3E

v01.0808

GaAs PHEMT MMIC LNA w/ FAILSAFE BYPASS MODE, 700 - 1200 MHz

Typical Applications

The HMC668LP3(E) is ideal for:

- Cellular/3G and LTE/WiMAX/4G
- BTS & Infrastructure
- Repeaters and Femtocells
- Tower Mounted Amplifiers
- Test & Measurement Equipment

Features

Noise Figure: 0.9 dB

Output IP3: +33 dBm

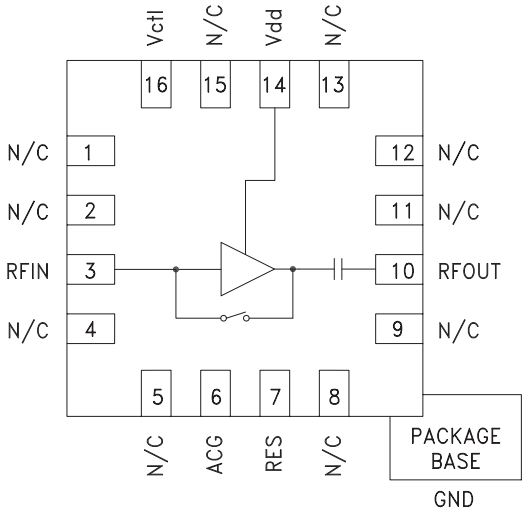
Gain: 16 dB

Failsafe Operation:
Bypass is enabled when LNA is unpowered

Single Supply: +3V or +5V

16 Lead 3x3mm QFN Package: 9 mm^2

Functional Diagram



General Description

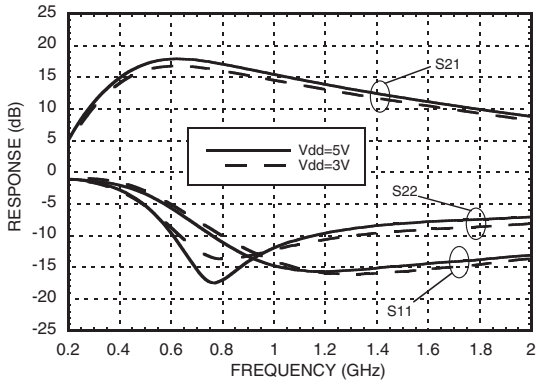
The HMC668LP3(E) is a versatile, high dynamic range GaAs MMIC Low Noise Amplifier that integrates a low loss LNA bypass mode on the IC. The amplifier is ideal for receivers and LNA modules operating between 0.7 and 1.2 GHz and provides 0.9 dB noise figure, 16 dB of gain and +33 dBm IP3 from a single supply of +5V @ 57mA. Input and output return losses are excellent and no external matching components are required. A single control line is used to switch between LNA mode and a low loss bypass mode. The failsafe topology enables the LNA bypass path, when no DC power is available.

Electrical Specifications, T_A = +25° C, Rbias = 0 Ohm

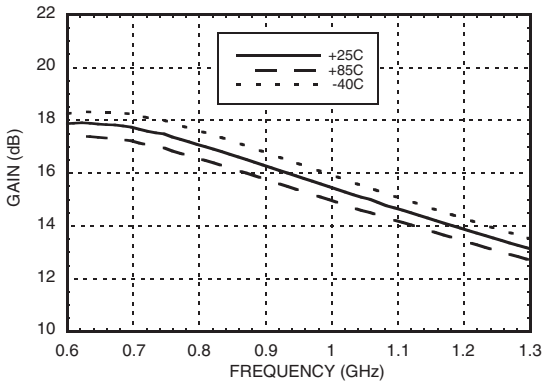
Parameter	LNA Mode						Bypass Mode			Failsafe Mode			Units
	Vdd = +3V			Vdd = +5V									
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	0.7 - 1.2			0.7 - 1.2			0.7 - 1.2			0.7 - 1.2			GHz
Gain	12	15		13	16		-2.5	-1.5		-2.5	-1.5		dB
Gain Variation Over Temperature		0.03			0.016			0.0008			0.0008		dB / °C
Noise Figure		0.85	1.1		0.9	1.1							dB
Input Return Loss		12			13			12			12		dB
Output Return Loss		13			14			13			13		dB
Reverse Isolation		22			23			-			-		dB
Power for 1dB Compression (P1dB)[1]		13			13			22			24		dBm
Third Order Intercept (IP3)[2]		27			33			26			26		dBm
Supply Current (Idd)		32	40		57	70		0.05			-		mA
Switching Speed (90% -10%) LNA Mode to Bypass Mode Bypass Mode to LNA Mode		 85			 85			200			-		 ns ns

[1] P1dB for LNA Mode is referenced to RFOUT while P1dB for Bypass and Failsafe Modes are referenced to RFIN.
[2] IP3 for LNA Mode is referenced to RFOUT while IP3 for Bypass and Failsafe Modes are referenced to RFIN.

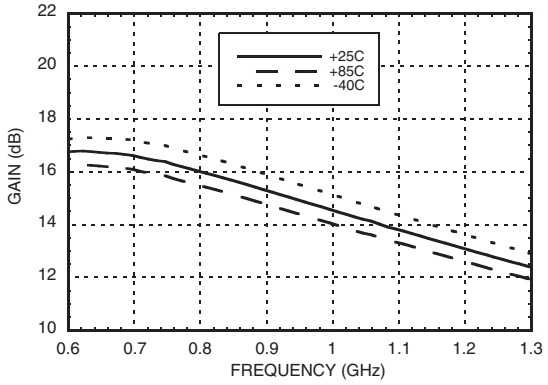
LNA - Broadband Gain & Return Loss



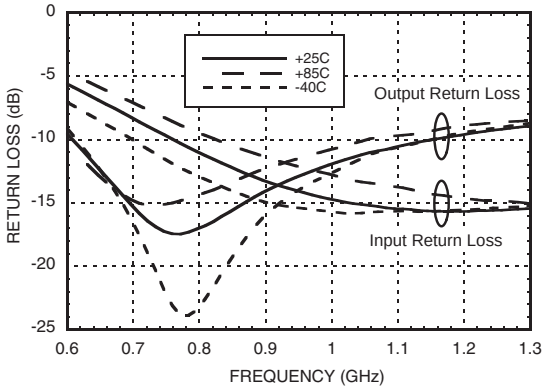
LNA - Gain vs. Temperature [1]



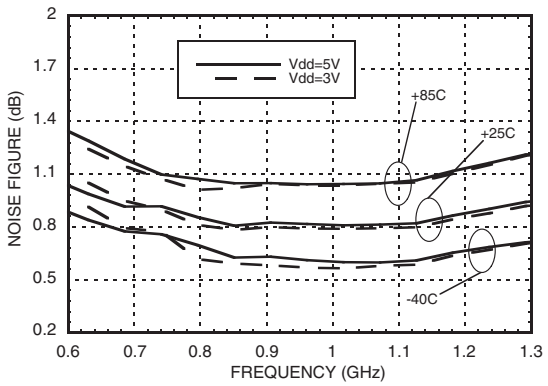
LNA - Gain vs. Temperature [2]



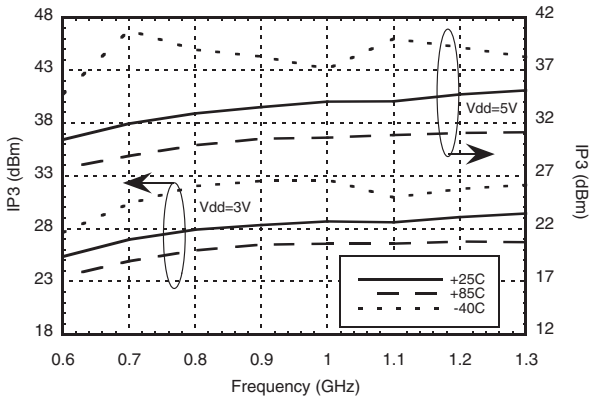
LNA - Return Loss vs. Temperature [1]



LNA - Noise Figure vs. Temperature [3]



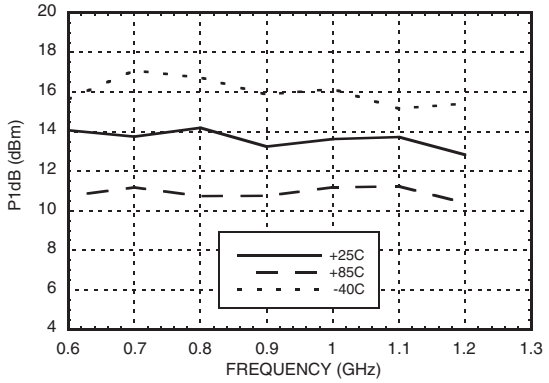
LNA - Output IP3 vs. Temperature, Output Power @ 0 dBm



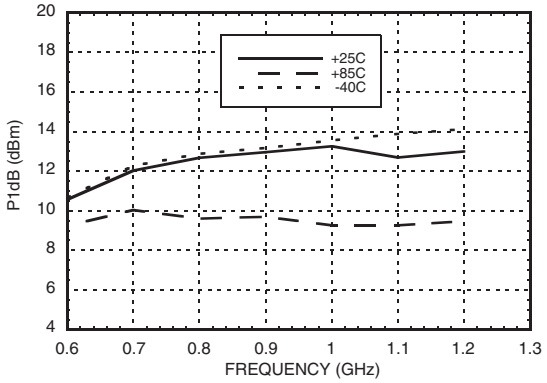
[1] Vdd = 5V [2] Vdd = 3V [3] Measurement reference plane shown on evaluation PCB drawing.

GaAs PHEMT MMIC LNA w/ FAILSAFE BYPASS MODE, 700 - 1200 MHz

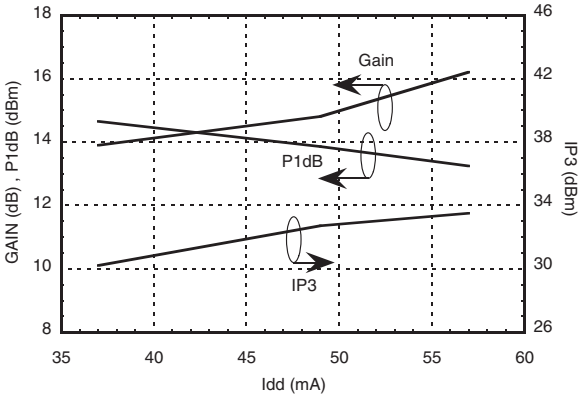
LNA - Output P1dB vs. Temperature [1]



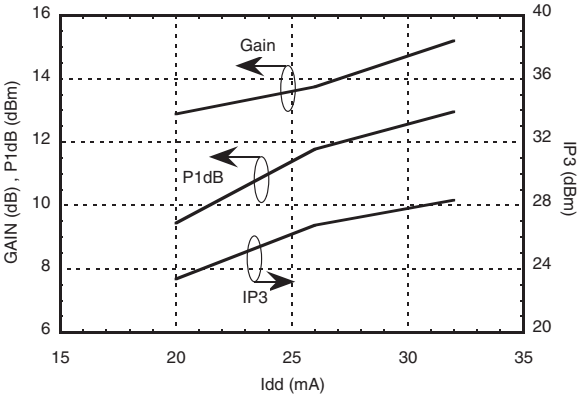
LNA - Output P1dB vs. Temperature [2]



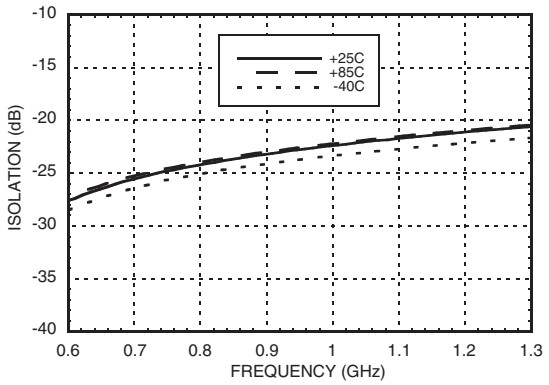
LNA - Gain, P1dB, Output IP3 vs. Current [1] @ 900 MHz



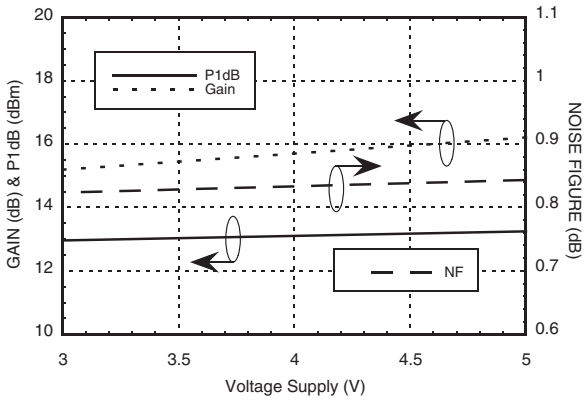
LNA - Gain, P1dB, Output IP3 vs. Current [2] @ 900 MHz



LNA - Reverse Isolation vs. Temperature [1]

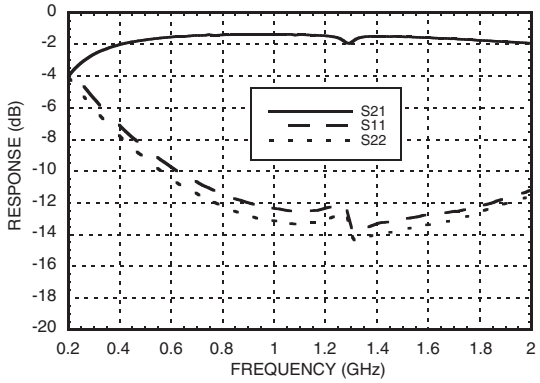


LNA - Output P1dB, Gain & Noise Figure [3] vs. Vdd @ 900 MHz

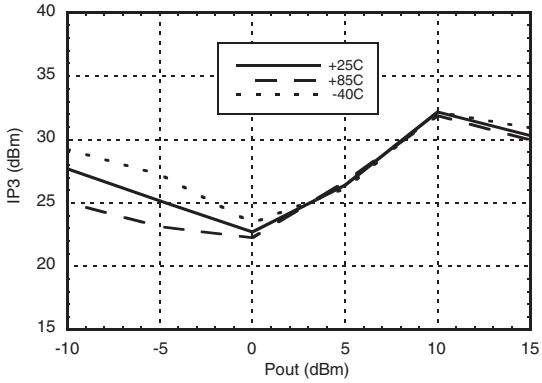


[1] Vdd = 5V [2] Vdd = 3V [3] Measurement reference plane shown on evaluation PCB drawing.

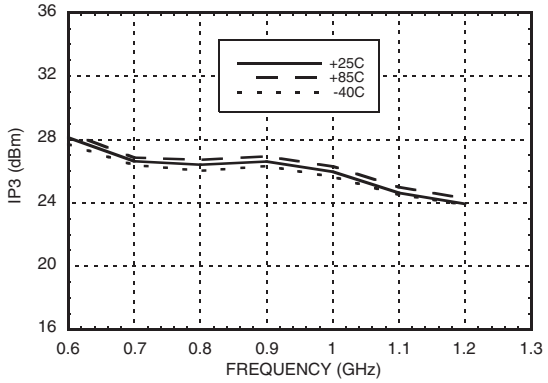
Bypass Mode - Broadband Gain & Return Loss



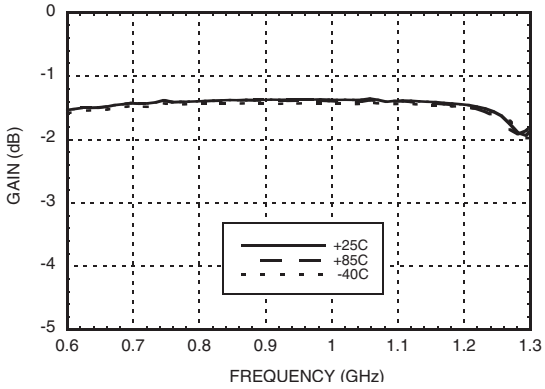
Bypass Mode - Input IP3 vs. Output Power @ 900 MHz



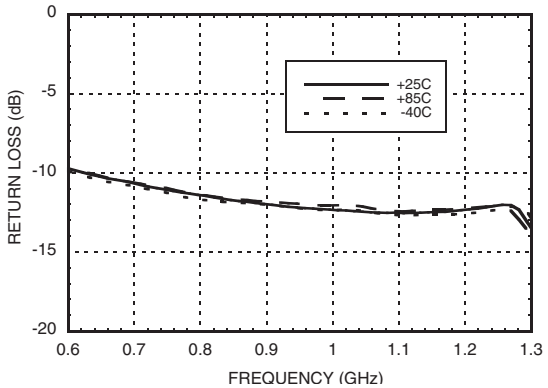
Bypass Mode - Input IP3 vs. Temperature, Output Power @ 5 dBm



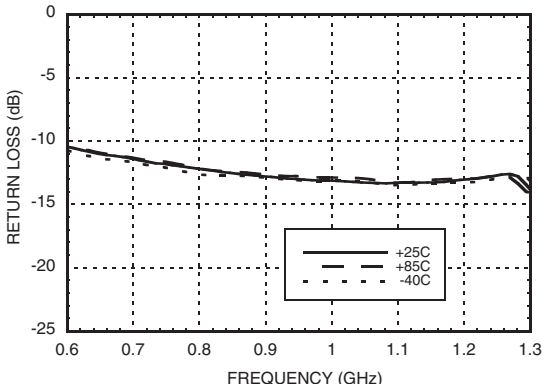
Bypass Mode - Insertion Loss vs. Temperature



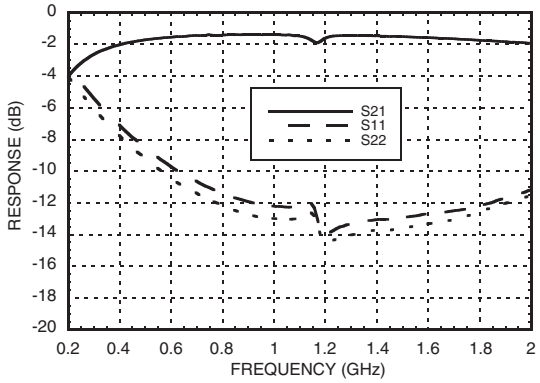
Bypass Mode - Input Return Loss vs. Temperature



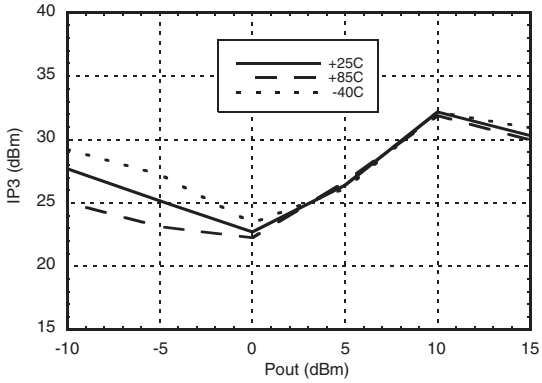
Bypass Mode - Output Return Loss vs. Temperature



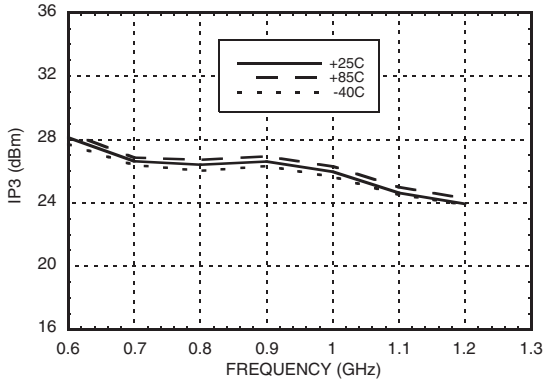
Failsafe Mode - Broadband Gain & Return Loss



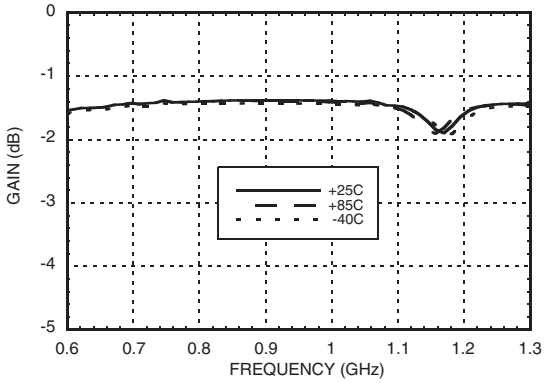
Failsafe Mode - Input IP3 vs. Output Power @ 900 MHz



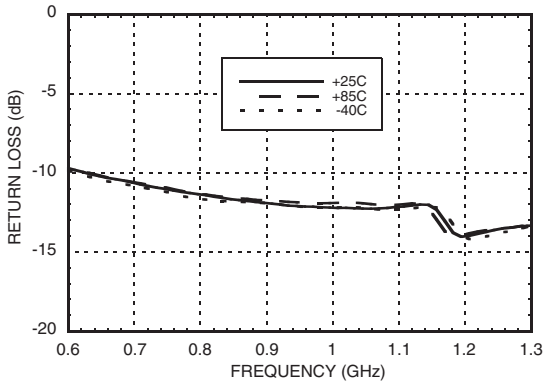
Failsafe Mode - Input IP3 vs. Temperature, Output Power @ 5 dBm



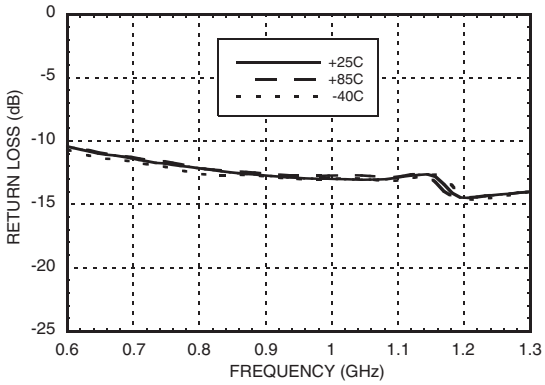
Failsafe Mode - Insertion Loss vs. Temperature



Failsafe Mode - Input Return Loss vs. Temperature



Failsafe Mode - Output Return Loss vs. Temperature



Absolute Maximum Ratings

Drain Bias Voltage (Vdd)	+6 Vdc
Control Voltage (Vctl)	+6 Vdc
RF Input Power (RFIN) LNA Mode / Bypass / Failsafe Mode	+5 dBm / +20 dBm
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 10.71 mW/°C above 85 °C)	0.70 W
Thermal Resistance (channel to ground paddle)	93.33 °C/W
Storage Temperature	-65 to +150° C
Operating Temperature	-40 to +85° C
ESD Sensitivity (HBM)	Class 1A

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Typical Supply Current vs. Vdd

Rbias Ω	Idd (mA)	
	Vdd= 3V	Vdd= 5V
0	32	57
15	26	49
47	20	37
180 [1]	10	20

[1] Recommended maximum Rbias

Truth Table

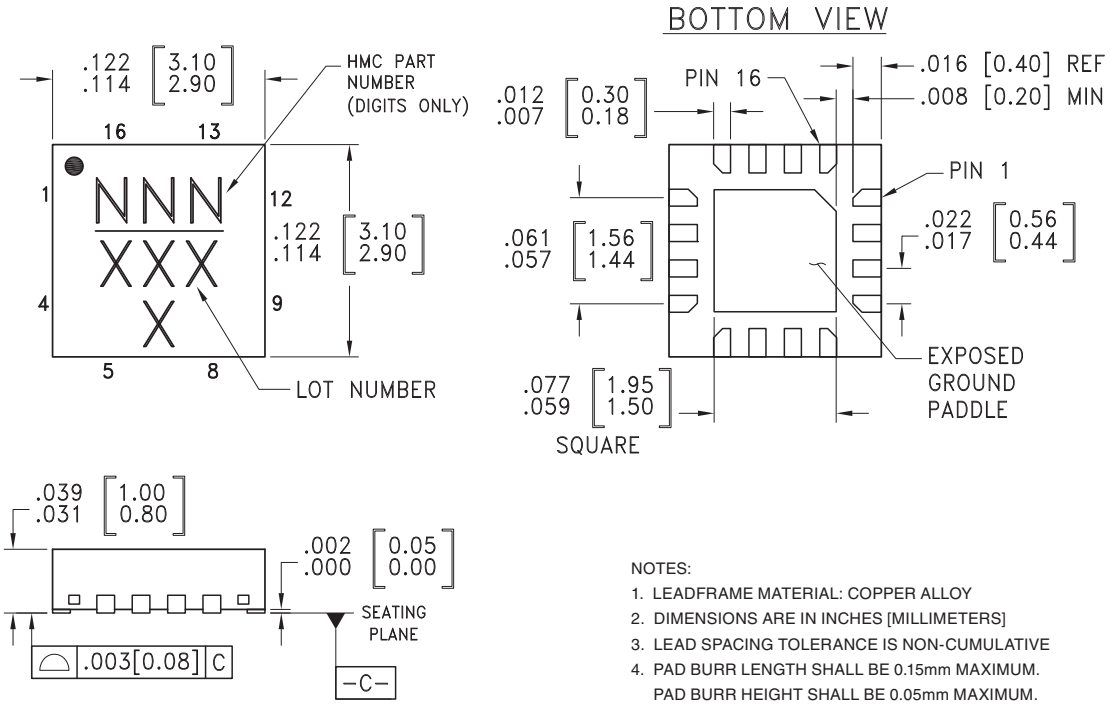
LNA Mode	Vctl = Vdd = 3 to 5V
Bypass Mode	Vctl= 0V, Vdd = 3 to 5V
Failsafe Mode	Vctl = Vdd = N/C

HMC668LP3 / 668LP3E

v01.0808

GaAs PHEMT MMIC LNA w/ FAILSAFE BYPASS MODE, 700 - 1200 MHz

Outline Drawing



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6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

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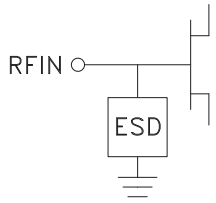
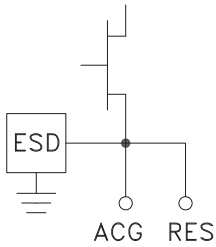
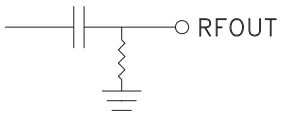
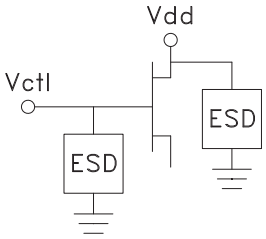
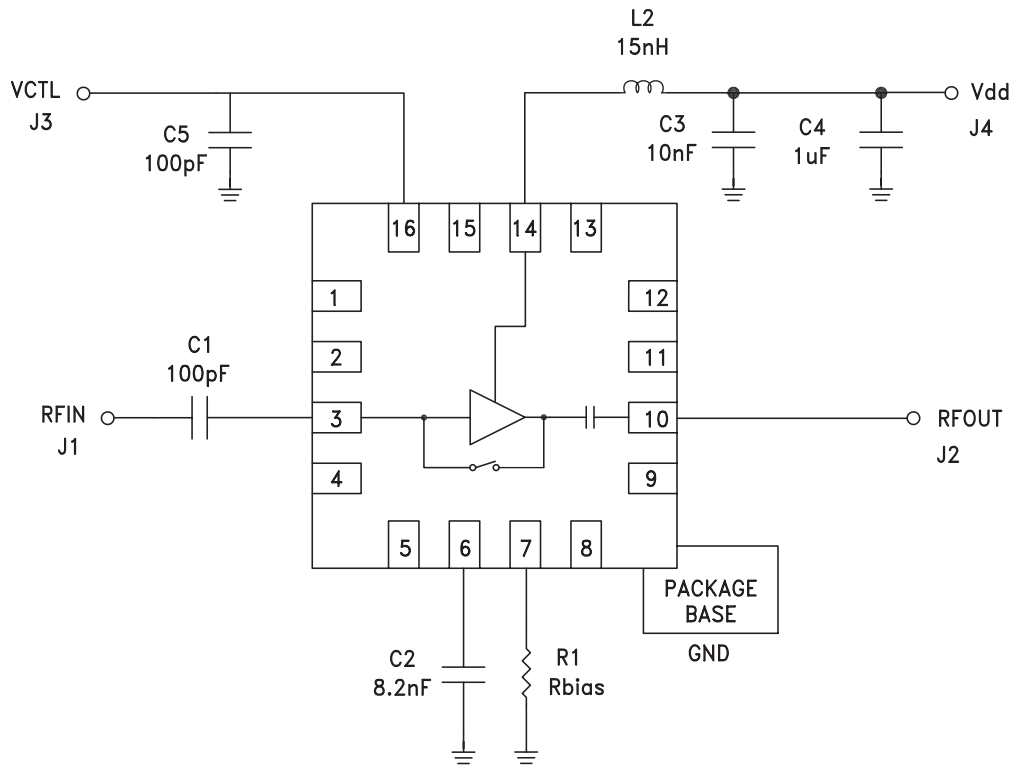
HMC668LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	668 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

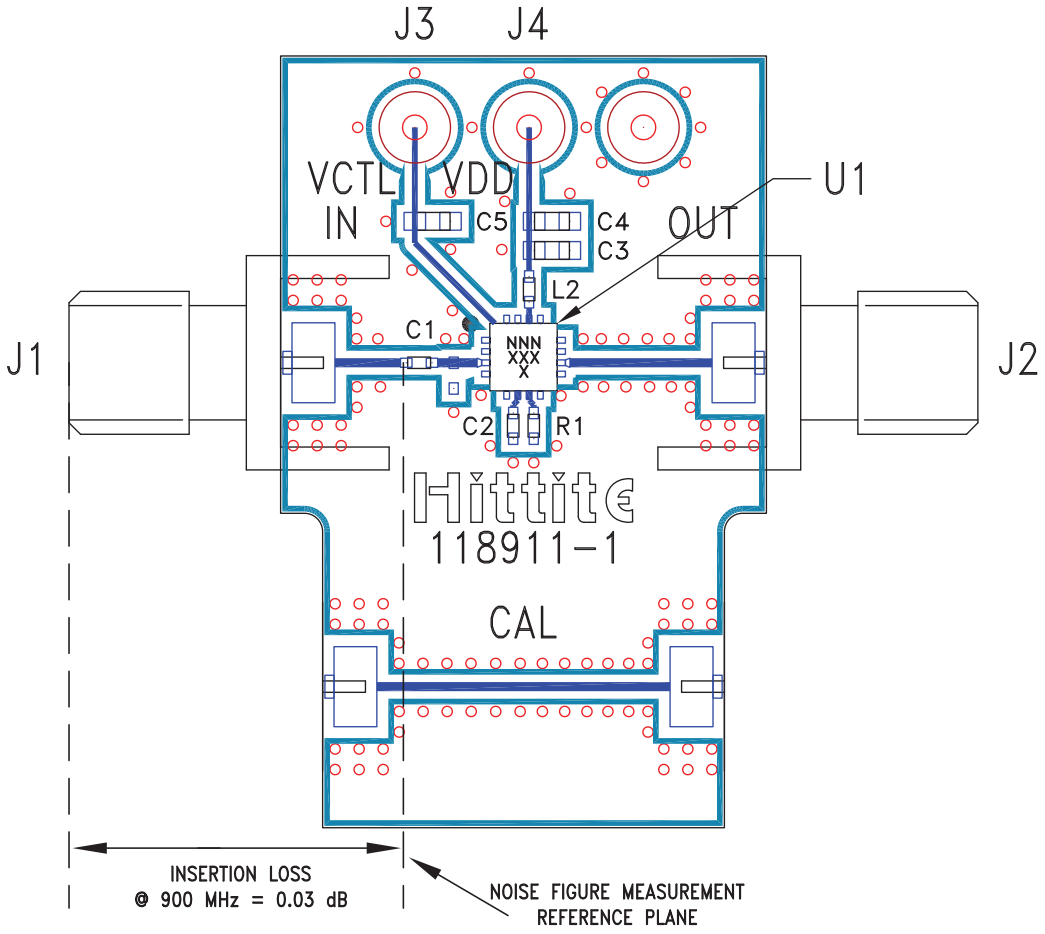
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 2, 4, 5, 8, 9, 11, 12, 13, 15	N/C	No connection required. These pins may be connected to RF GND. Performance will not be affected.	
3	RFIN	This pin is DC coupled. Off-chip DC blocking capacitor required.	
6	ACG	AC Ground. Attach bypass capacitor per application circuit.	
7	RES	External resistor pin for current control. See table for external resistor value vs. bias current data.	
10	RFOUT	This pin is matched to 50 Ohms	
14	Vdd	Power Supply voltage pin. External bypass capacitors required.	
16	Vctl	Control voltage pin for LNA / Bypass Modes. Setting voltage equal to VDD enables LNA Mode. External Bypass capacitor required.	

Application Circuit



Evaluation PCB



List of Materials for Evaluation PCB 121922 [1]

Item	Description
J1 - J2	PCB Mount SMA Connector
J3 - J4	DC Pin
C1	100 pF Capacitor, 0402 Pkg.
C2	8200 pF Capacitor, 0402 Pkg.
C3	10 nF Capacitor, 0603 Pkg.
C4	1 µF Capacitor, 0603 Pkg.
C5	100 pF Capacitor, 0603 Pkg.
L2	15 nH Inductor, 0402 Pkg.
R1	0 Ohm Resistor, 0402 Pkg.
U1	HMC668LP3(E) Amplifier
PCB [2]	118911 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

400MHz to 3.8GHz 3.3V High Signal Level Downconverting Mixer

FEATURES

- **3.3V Operation for Reduced Power**
- **50Ω Single-Ended RF and LO Ports**
- **Wide RF Frequency Range: 400MHz to 3.8GHz***
- **High Input IP3: 25.6dBm at 900MHz**
  24.7dBm at 1950MHz
  23.7dBm at 2.6GHz
- **Conversion Gain: 3.3dB at 900MHz**
  2.9dB at 1950MHz
- **–3dBm LO Drive Level**
- **Low LO Leakage**
- **Low Noise Figure: 10.6dB at 900MHz**
  11.7dB at 1950MHz
- Very Few External Components
- 16-Lead (4mm × 4mm) QFN Package

APPLICATIONS

- Cellular, CDMA, WCDMA, TD-SCDMA and UMTS Infrastructure
- WiMAX
- Wireless Infrastructure Receiver
- Wireless Infrastructure PA Linearization
- 900MHz/2.4GHz/3.5GHz WLAN

DESCRIPTION

The LT®5557 active mixer is optimized for high linearity, wide dynamic range downconverter applications. The IC includes a high speed differential LO buffer amplifier driving a double-balanced mixer. Broadband, integrated transformers on the RF and LO inputs provide single-ended 50Ω interfaces. The differential IF output allows convenient interfacing to differential IF filters and amplifiers, or is easily matched to drive a single-ended 50Ω load, with or without an external transformer.

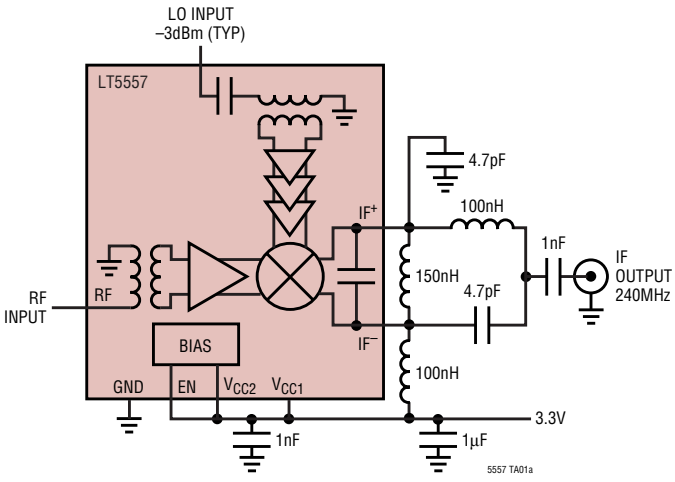
The RF input is internally matched to 50Ω from 1.6GHz to 2.3GHz, and the LO input is internally matched to 50Ω from 1GHz to 5GHz. The frequency range of both ports is easily extended with simple external matching. The IF output is partially matched and usable for IF frequencies up to 600MHz.

The LT5557's high level of integration minimizes the total solution cost, board space and system-level variation.

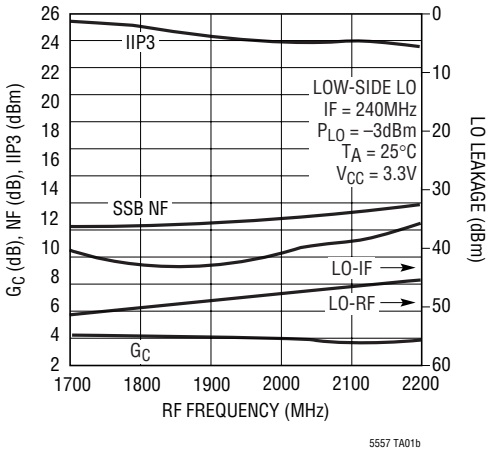
*Operation over a wider frequency range is possible with reduced performance. Consult factory for information and assistance.

TYPICAL APPLICATION

High Signal Level Downmixer for Multi-Carrier Wireless Infrastructure



Conversion Gain, IIP3, SSB NF and LO Leakage vs RF Frequency



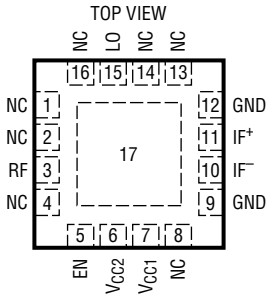
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC1}, V_{CC2}, IF^+, IF^-) 4V
Enable Voltage ..... –0.3V to V_{CC} + 0.3V
LO Input Power (380MHz to 4.2GHz) ..... +10dBm
LO Input DC Voltage ..... –1V to V_{CC} + 1V
RF Input Power (400MHz to 3.8GHz) ..... +12dBm
RF Input DC Voltage ..... ±0.1V
Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C
Junction Temperature (T_J) ..... 125°C

CAUTION: This part is sensitive to electrostatic discharge (ESD). It is very important that proper ESD precautions be observed when handling the LT5557.

PACKAGE/ORDER INFORMATION



UF PACKAGE
16-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 17) IS GND
MUST BE SOLDERED TO PCB

ORDER PART NUMBER
LT5557EUF#PBF
UF PART MARKING
5557

Order Options Tape and Reel: Add #TR
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, EN = High, T_A = 25°C, unless otherwise specified. Test circuit shown in Figure 1. (Note 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Requirements (V_{CC})						
Supply Voltage			2.9	3.3	3.9	V
Supply Current	V_{CC1} (Pin 7)			25.1		mA
	V_{CC2} (Pin 6)			3.3		mA
	$IF^+ + IF^-$ (Pin 11 + Pin 10)			53.2	60	mA
	Total Supply Current			81.6	92	mA
Enable (EN) Low = Off, High = On						
Shutdown Current		EN = Low			100	µA
Input High Voltage (On)			2.7			V
Input Low Voltage (Off)					0.3	V
EN Pin Input Current		EN = 3.3V DC		53	90	µA
Turn-ON Time				2.8		µs
Turn-OFF Time				2.9		µs

AC ELECTRICAL CHARACTERISTICS

Test circuit shown in Figure 1. (Notes 2, 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RF Input Frequency Range	No External Matching (Midband)		1600 to 2300		MHz
	With External Matching (Low Band or High Band)	400		3800	MHz
LO Input Frequency Range	No External Matching		1000 to 4200		MHz
	With External Matching	380			MHz
IF Output Frequency Range	Requires Appropriate IF Matching		0.1 to 600		MHz
RF Input Return Loss	Z_0 = 50Ω, 1600MHz to 2300MHz (No External Matching)		>12		dB
LO Input Return Loss	Z_0 = 50Ω, 1000MHz to 5000MHz (No External Matching)		>10		dB
IF Output Impedance	Differential at 240MHz		529Ω||2.6pF		R||C
LO Input Power	1200MHz to 4200MHz	–8	–3	2	dBm
	380MHz to 1200MHz	–5	0	5	dBm

AC ELECTRICAL CHARACTERISTICS

Standard Downmixer Application: V_{CC} = 3.3V, EN = High, T_A = 25°C, P_{RF} = –6dBm (–6dBm/tone for 2-tone IIP3 tests, Δf = 1MHz), $f_{LO} = f_{RF} – f_{IF}$, P_{LO} = –3dBm (0dBm for 450MHz and 900MHz tests), IF output measured at 240MHz, unless otherwise noted. Test circuit shown in Figure 1. (Notes 2, 3, 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Gain	RF = 450MHz, IF = 70MHz, High Side LO		2.9		dB
	RF = 900MHz, IF = 140MHz		3.3		dB
	RF = 1750MHz		3.0		dB
	RF = 1950MHz		2.9		dB
	RF = 2150MHz		2.9		dB
	RF = 2600MHz, IF = 360MHz		2.5		dB
	RF = 3600MHz, IF = 450MHz		1.7		dB
Conversion Gain vs Temperature	T_A = –40°C to 85°C, RF = 1950MHz		–0.0217		dB/°C
Input 3rd Order Intercept	RF = 450MHz, IF = 70MHz, High Side LO		24.1		dBm
	RF = 900MHz, IF = 140MHz		25.6		dBm
	RF = 1750MHz		25.5		dBm
	RF = 1950MHz		24.7		dBm
	RF = 2150MHz		24.3		dBm
	RF = 2600MHz, IF = 360MHz		23.7		dBm
	RF = 3600MHz, IF = 450MHz		23.5		dBm
Single-Sideband Noise Figure	RF = 450MHz, IF = 70MHz, High Side LO		12.7		dB
	RF = 900MHz, IF = 140MHz		10.6		dB
	RF = 1750MHz		11.3		dB
	RF = 1950MHz		11.7		dB
	RF = 2150MHz		12.8		dB
	RF = 2600MHz, IF = 360MHz		13.2		dB
	RF = 3600MHz, IF = 450MHz		15.4		dB
LO to RF Leakage	f_{LO} = 380MHz to 1600MHz		<–50		dBm
	f_{LO} = 1600MHz to 4000MHz		<–45		dBm
LO to IF Leakage	f_{LO} = 380MHz to 2200MHz		<–42		dBm
	f_{LO} = 2200MHz to 4000MHz		<–38		dBm
RF to LO Isolation	f_{RF} = 400MHz to 1700MHz		>50		dB
	f_{RF} = 1700MHz to 3800MHz		>42		dB
RF to IF Isolation	f_{RF} = 400MHz to 2300MHz		>41		dB
	f_{RF} = 2300MHz to 3800MHz		>37		dB
2RF-2LO Output Spurious Product ($f_{RF} = f_{LO} + f_{IF}/2$)	900MHz: f_{RF} = 830MHz at –6dBm, f_{IF} = 140MHz		–61		dBc
	1950MHz: f_{RF} = 1830MHz at –6dBm, f_{IF} = 240MHz		–53		dBc
3RF-3LO Output Spurious Product ($f_{RF} = f_{LO} + f_{IF}/3$)	900MHz: f_{RF} = 806.67MHz at –6dBm, f_{IF} = 140MHz		–83		dBc
	1950MHz: f_{RF} = 1790MHz at –6dBm, f_{IF} = 240MHz		–70		dBc
Input 1dB Compression	RF = 450MHz, IF = 70MHz, High Side LO		10.0		dBm
	RF = 900MHz, IF = 140MHz		8.8		dBm
	RF = 1950MHz		8.8		dBm
	RF = 2600MHz, IF = 360MHz		8.6		dBm
	RF = 3600MHz, IF = 450MHz		9.1		dBm

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: 450MHz and 900MHz performance measured with external LO and RF matching. 2600MHz and 3600MHz performance measured with external RF matching. See Figure 1 and Applications Information.

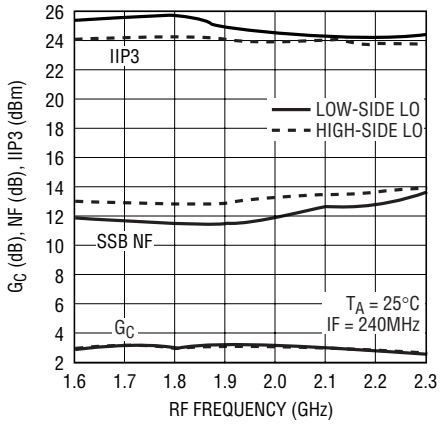
Note 3: Specifications over the –40°C to 85°C temperature range are assured by design, characterization and correlation with statistical process controls.

Note 4: SSB Noise Figure measurements performed with a small-signal noise source and bandpass filter on RF input, and no other RF signal applied.

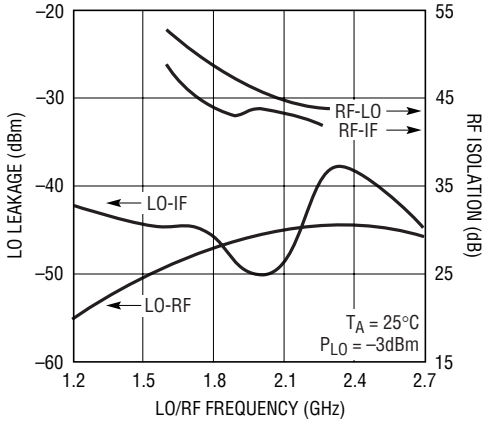
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, Test circuit shown in Figure 1. Midband (No external RF/LO matching) 240MHz IF output, P_{RF} = –6dBm (–6dBm/tone for 2-tone IIP3 tests, Δf = 1MHz), P_{LO} = –3dBm, unless otherwise noted.

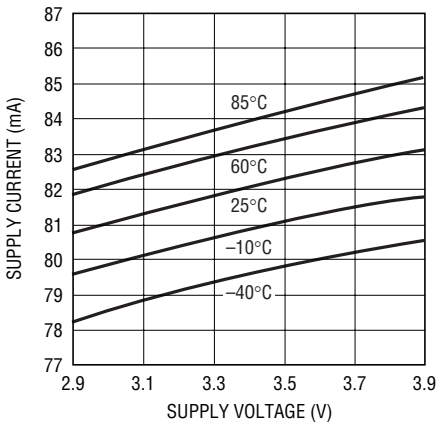
Conversion Gain, IIP3 and NF vs RF Frequency



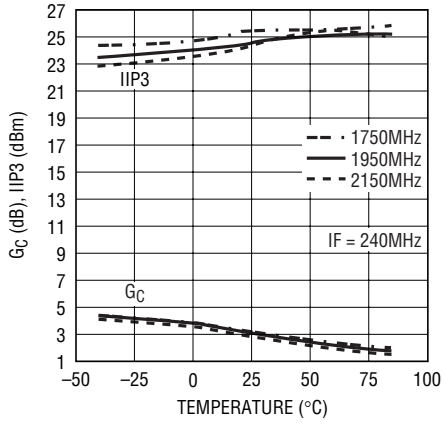
LO Leakage and RF Isolation vs LO and RF Frequency



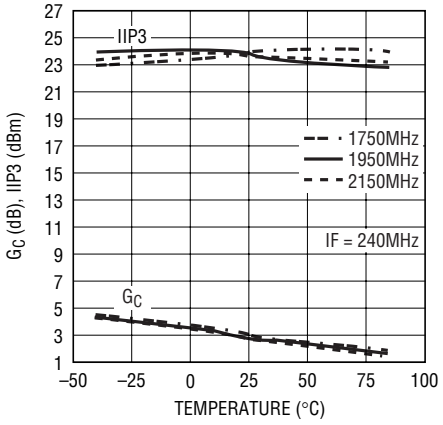
Supply Current vs Supply Voltage



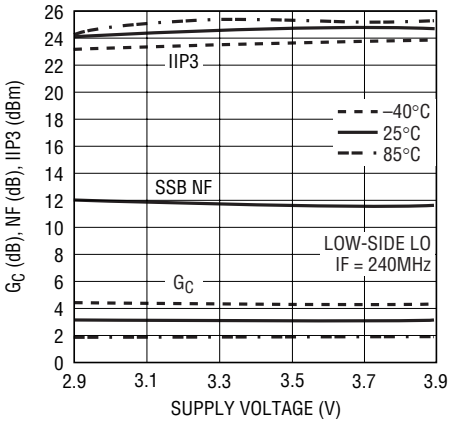
Conversion Gain and IIP3 vs Temperature (Low-Side LO)



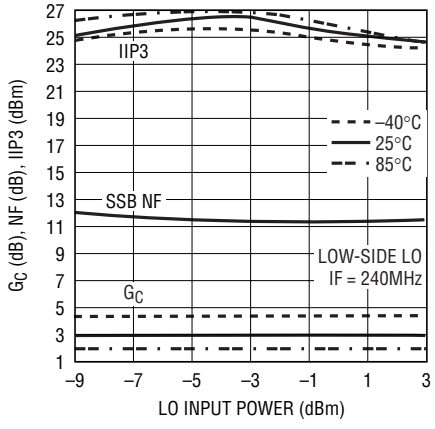
Conversion Gain and IIP3 vs Temperature (High-Side LO)



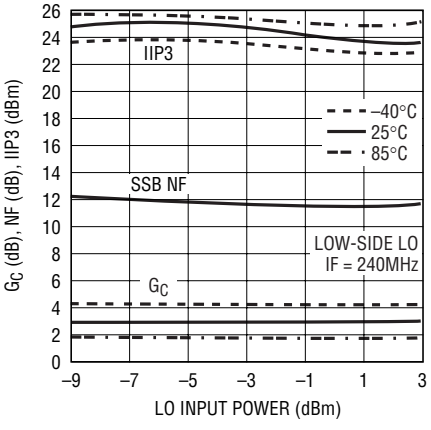
1950MHz Conversion Gain, IIP3 and NF vs Supply Voltage



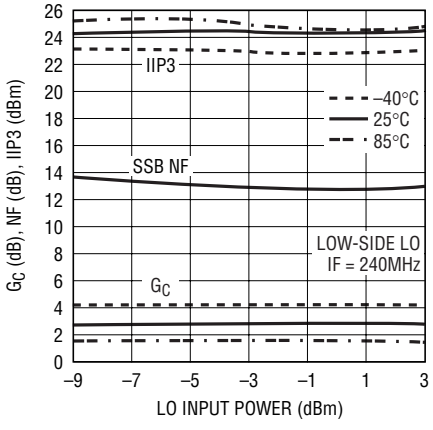
1750MHz Conversion Gain, IIP3 and NF vs LO Power



1950MHz Conversion Gain, IIP3 and NF vs LO Power



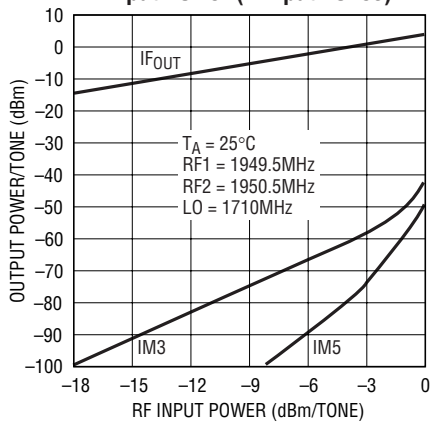
2150MHz Conversion Gain, IIP3 and NF vs LO Power



TYPICAL PERFORMANCE CHARACTERISTICS

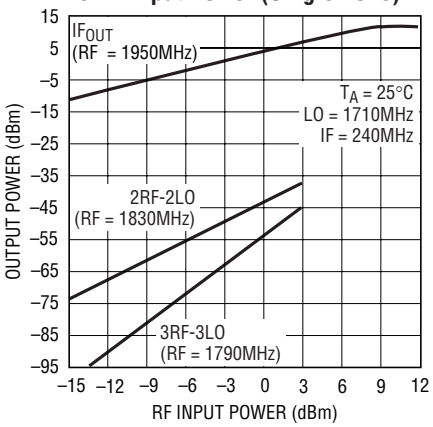
V_{CC} = 3.3V, Test circuit shown in Figure 1. Midband (No external RF/LO matching) 240MHz IF output, P_{RF} = –6dBm (–6dBm/tone for 2-tone IIP3 tests, Δf = 1MHz), P_{LO} = –3dBm, unless otherwise noted.

IF Output Power, IM3 and IM5 vs RF Input Power (2 Input Tones)



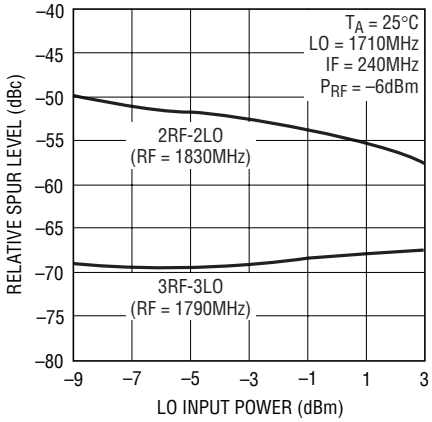
5557 G10

IF_{OUT}, 2 × 2 and 3 × 3 Spurs vs RF Input Power (Single Tone)



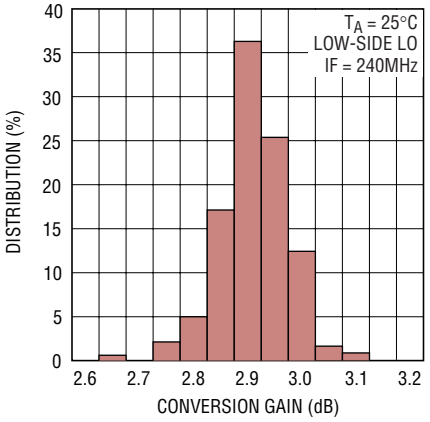
5557 G11

2 × 2 and 3 × 3 Spurs vs LO Power (Single Tone)



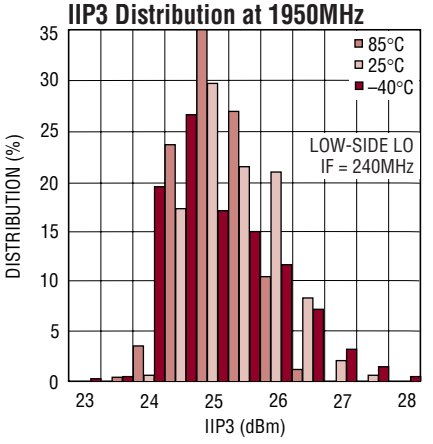
5557 G12

Conversion Gain Distribution at 1950MHz



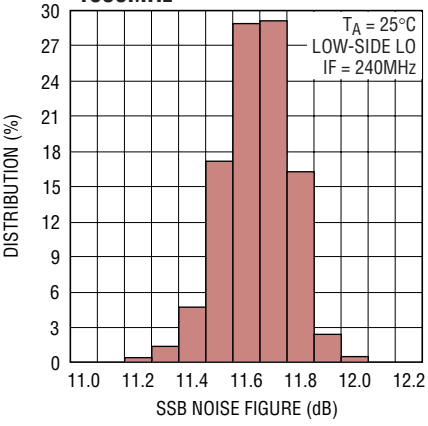
5557 G25

IIP3 Distribution at 1950MHz



5557 G26

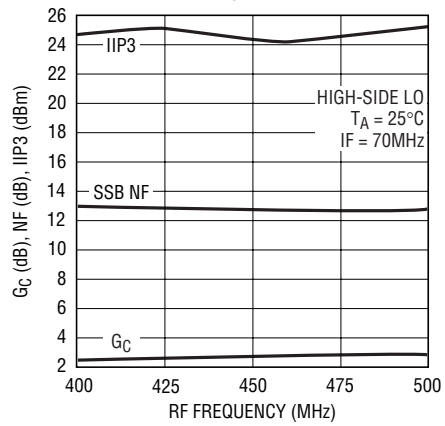
SSB Noise Figure Distribution at 1950MHz



5557 G27

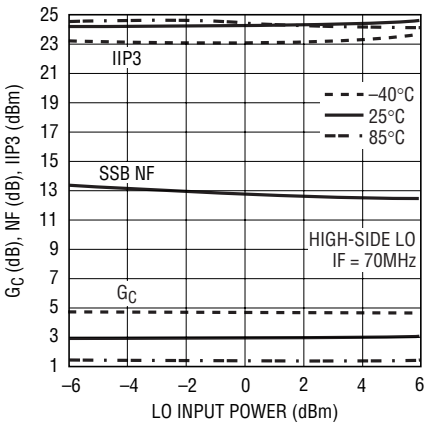
450MHz application (with external RF/LO matching) 70MHz IF output, P_{RF} = –6dBm (–6dBm/tone for 2-tone IIP3 tests, Δf = 1MHz), high-side LO at 0dBm, unless otherwise noted.

Conversion Gain, IIP3 and NF vs RF Frequency



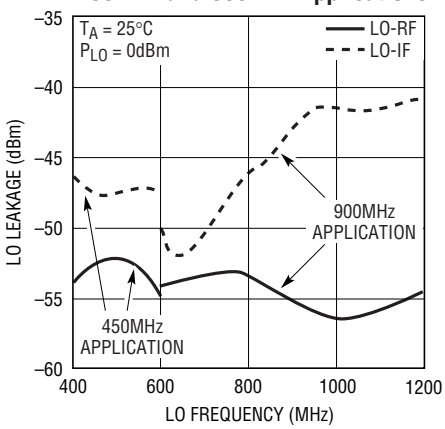
5557 G13

450MHz Conversion Gain, IIP3 and NF vs LO Power



5557 G14

LO Leakage vs LO Frequency 450MHz and 900MHz Applications

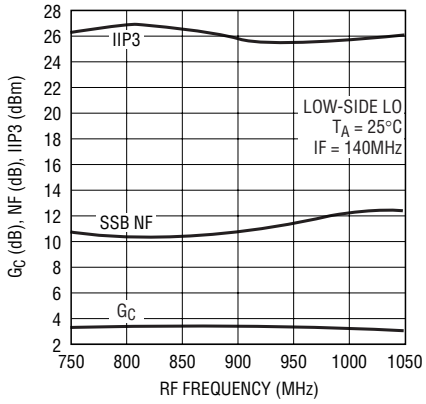


5557 G15

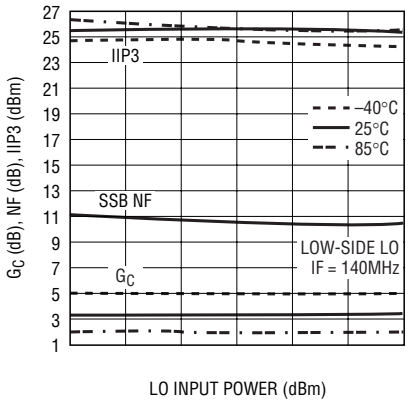
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, Test circuit shown in Figure 1. 900MHz application (with external RF/LO matching), 140MHz IF output, P_{RF} = –6dBm (–6dBm/tone for 2-tone IIP3 tests, Δf = 1MHz), low-side LO at 0dBm, unless otherwise noted.

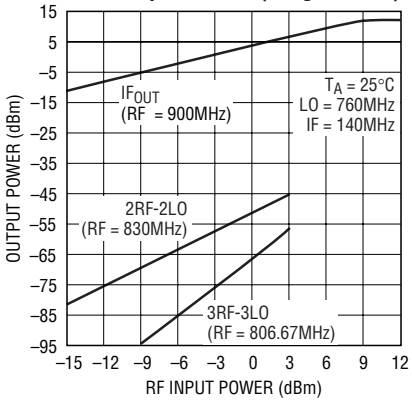
Conversion Gain, IIP3 and NF vs RF Frequency



900MHz Conversion Gain, IIP3 and NF vs LO Power

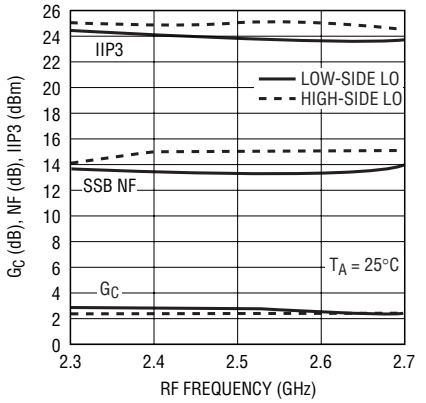


IF_{OUT}, 2 × 2 and 3 × 3 Spurs vs RF Input Power (Single-Tone)

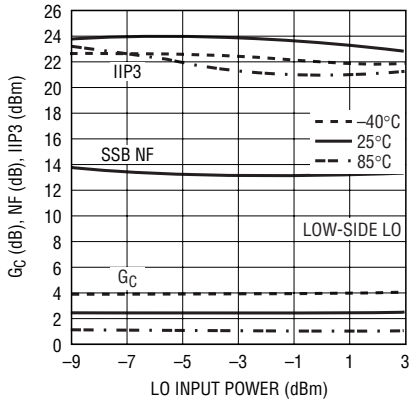


2.3-2.7GHz application (with external RF matching) 360MHz IF output, P_{RF} = –6dBm (–6dBm/tone for 2-tone IIP3 tests, Δf = 1MHz), P_{LO} = –3dBm, unless otherwise noted.

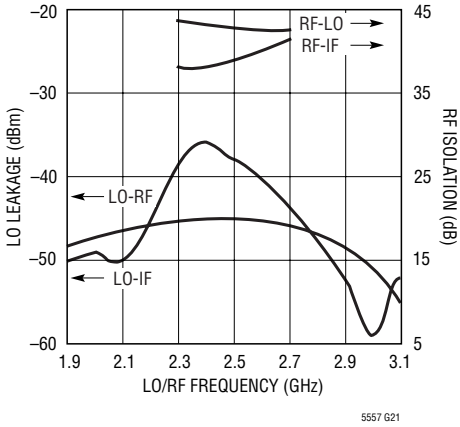
Conversion Gain, IIP3 and SSB NF vs RF Frequency



2.6GHz Conversion Gain, IIP3 and NF vs LO Power

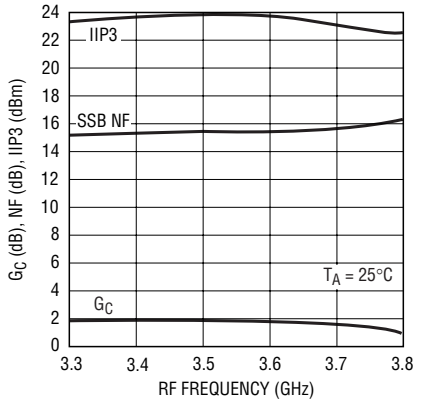


LO Leakage and RF Isolation vs LO and RF Frequency

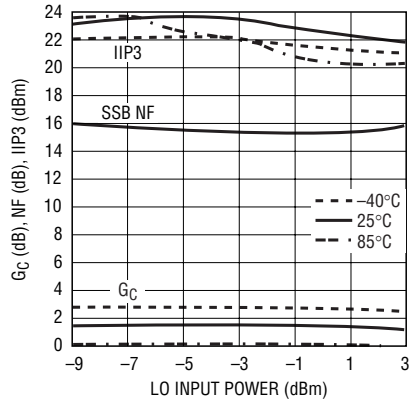


3.3-3.8GHz application (with external RF matching) 450MHz IF output, P_{RF} = –6dBm (–6dBm/tone for 2-tone IIP3 tests, Δf = 1MHz), low-side LO at –3dBm, unless otherwise noted.

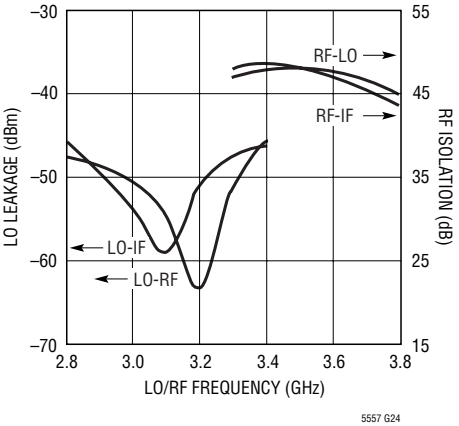
Conversion Gain, IIP3 and SSB NF vs RF Frequency



3.6GHz Conversion Gain, IIP3 and SSB NF vs LO Power



LO Leakage and RF Isolation vs LO and RF Frequency



PIN FUNCTIONS

NC (Pins 1, 2, 4, 8, 13, 14, 16): Not Connected Internally. These pins should be grounded on the circuit board for the best LO-to-RF and LO-to-IF isolation.

RF (Pin 3): Single-Ended Input for the RF Signal. This pin is internally connected to the primary side of the RF input transformer, which has low DC resistance to ground. **If the RF source is not DC blocked, then a series blocking capacitor must be used**. The RF input is internally matched from 1.6GHz to 2.3GHz. Operation down to 400MHz or up to 3.8GHz is possible with simple external matching.

EN (Pin 5): Enable Pin. When the input enable voltage is higher than 2.7V, the mixer circuits supplied through Pins 6, 7, 10 and 11 are enabled. When the input voltage is less than 0.3V, all circuits are disabled. Typical input current is 53µA for EN = 3.3V and 0µA when EN = 0V. The EN pin should not be left floating. Under no conditions should the EN pin voltage exceed V_{CC} + 0.3V, even at start-up.

V_{CC2} (Pin 6): Power Supply Pin for the Bias Circuits. Typical current consumption is 3.3mA. This pin should be externally connected to the V_{CC1} pin and decoupled with 1000pF and 1µF capacitors.

V_{CC1} (Pin 7): Power Supply Pin for the LO Buffer Circuits. Typical current consumption is 25.1mA. This pin should be externally connected to the V_{CC2} pin and decoupled with 1000pF and 1µF capacitors.

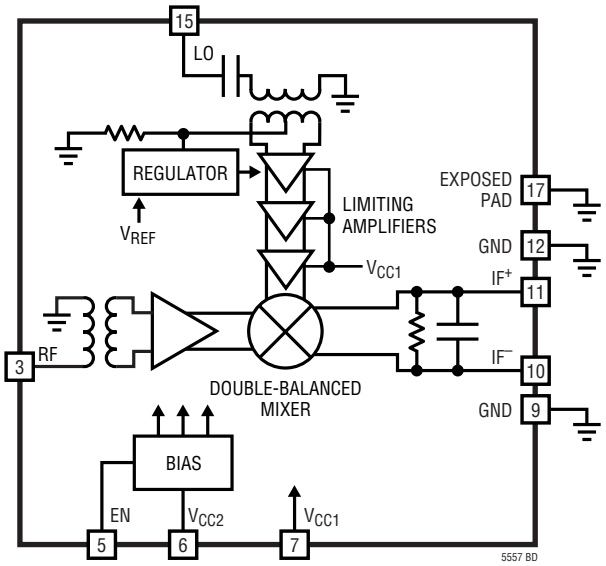
GND (Pins 9, 12): Ground. These pins are internally connected to the backside ground for improved isolation. They should be connected to the RF ground on the circuit board, although they are not intended to replace the primary grounding through the backside contact of the package.

IF^-, IF^+ (Pins 10, 11): Differential Outputs for the IF Signal. An impedance transformation may be required to match the outputs. These pins must be connected to V_{CC} through impedance matching inductors, RF chokes or a transformer center tap. Typical current consumption is 26.6mA each (53.2mA total).

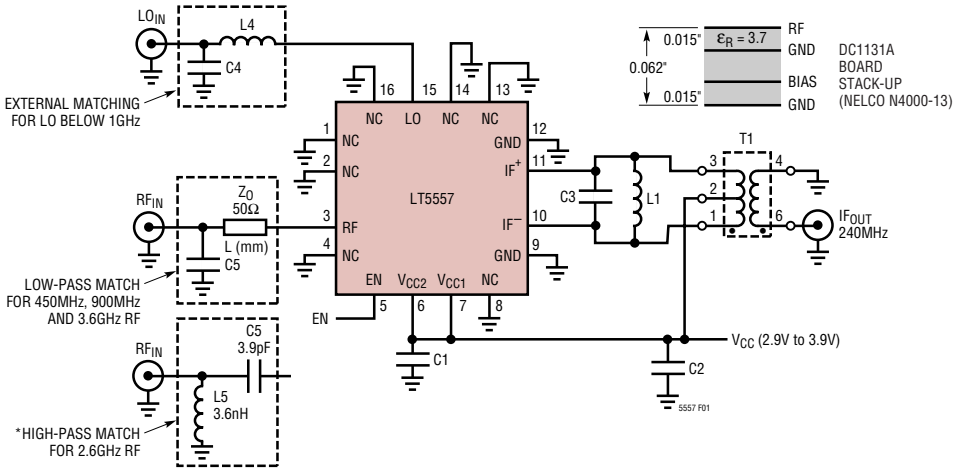
LO (Pin 15): Single-Ended Input for the Local Oscillator Signal. This pin is internally connected to the primary side of the LO transformer, which is internally DC blocked. An external blocking capacitor is not required. The LO input is internally matched from 1GHz to 5GHz. Operation down to 380MHz is possible with simple external matching.

Exposed Pad (Pin 17): Circuit Ground Return for the Entire IC. This must be soldered to the printed circuit board ground plane.

BLOCK DIAGRAM



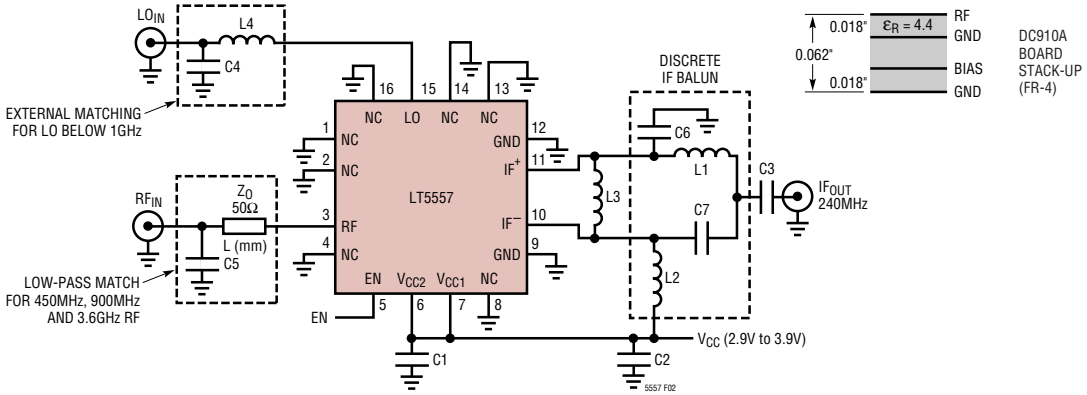
TEST CIRCUITS



APPLICATION			RF MATCH		LO MATCH		IF MATCH	
RF	LO	IF	L	C5	L4	C4	L1	C3
450MHz	High Side	70MHz	6.5mm	12pF	10nH	8.2pF	270nH	15pF
900MHz	Low Side	140MHz	1.7mm	3.9pF	2.7nH	3.9pF	180nH	3.9pF
2.6GHz		360MHz	HIGH-PASS*		–	–	47nH	1.2pF
3.6GHz		450MHz	2.9mm	1pF	–	–	39nH	–

REF DES	VALUE	SIZE	PART NUMBER	REF DES	VALUE	SIZE	PART NUMBER
C1	1000pF	0402	AVX 04025C102JAT	L4, C4, C5		0402	See Applications Information
C2	1µF	0603	AVX 0603ZD105KAT	L1	82nH	0603	Toko LLQ1608-F82NG
C3	2.2pF	0402	AVX 04025A2R2BAT	T1	8:1		Mini-Circuits TC8-1+

Figure 1. Standard Downmixer Test Schematic—Transformer-Based Bandpass IF Matching (240MHz IF)



REF DES	VALUE	SIZE	PART NUMBER	REF DES	VALUE	SIZE	PART NUMBER
C1, C3	1000pF	0402	AVX 04025C102JAT	L4, C4, C5		0402	See Applications Information
C2	1µF	0603	AVX 0603ZD105KAT	L1, L2	100nH	0603	Toko LL1608-FSLR10J
C6, C7	4.7pF	0402	AVX 04025A4R7CAT	L3	150nH	0603	Toko LL1608-FSLR15J

Figure 2. Downmixer Test Schematic—Discrete IF Balun Matching (240MHz IF)

APPLICATIONS INFORMATION

Introduction

The LT5557 consists of a high linearity double-balanced mixer, RF buffer amplifier, high speed limiting LO buffer amplifier and bias/enable circuits. The RF and LO inputs are both single ended. The IF output is differential. Low side or high side LO injection can be used.

Two evaluation circuits are available. The standard evaluation circuit, shown in Figure 1, incorporates transformer-based IF matching and is intended for applications that require the highest dynamic range and the widest IF bandwidth. The second evaluation circuit, shown in Figure 2, replaces the IF transformer with a discrete IF balun for reduced solution cost and size. The discrete IF balun delivers higher conversion gain, but slightly degraded IIP3 and noise figure, and reduced IF bandwidth.

RF Input Port

The mixer's RF input, shown in Figure 3, consists of an integrated transformer and a high linearity differential amplifier. The primary terminals of the transformer are connected to the RF input (Pin 3) and ground. The secondary side of the transformer is internally connected to the amplifier's differential inputs. The DC resistance of the primary is 4.2Ω. **If the RF source has DC voltage present, then a coupling capacitor must be used in series with the RF input pin.**

The RF input is internally matched from 1.6GHz to 2.3GHz, requiring no external components over this frequency range. The input return loss, shown in Figure 4a, is typically 12dB at the band edges. The input match at the lower band edge can be optimized with a series 3.9pF capacitor at Pin 3, which improves the 1.6GHz return loss to greater than 25dB. Likewise, the 2.3GHz match can be improved to greater than 25dB with a series 1.5nH inductor. A series 2.7nH/2.2pF network will simultaneously optimize the lower and upper band edges and expand the RF input bandwidth to 1.2GHz-2.5GHz. Measured RF input return losses for these three cases are also plotted in Figure 4a.

Alternatively, the input match can be shifted as low as 400MHz or up to 3800MHz by adding a shunt capacitor (C5) to the RF input. A 450MHz input match is realized with C5 = 12pF, located 6.5mm away from Pin 3 on the evaluation board's 50Ω input transmission line. A 900MHz input match requires C5 = 3.9pF, located at 1.7mm. A 3.6GHz input match is realized with C5 = 1pF, located at 2.9mm. This

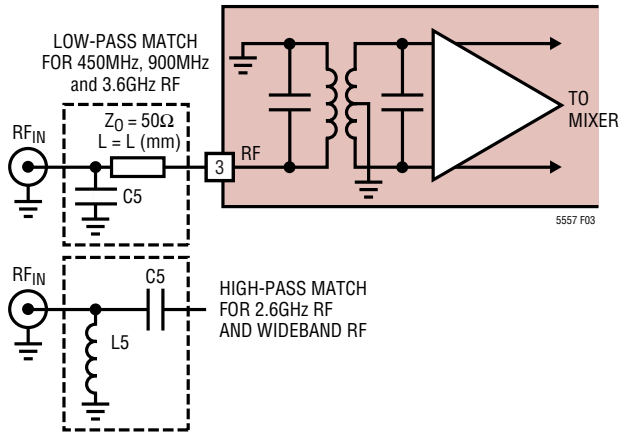
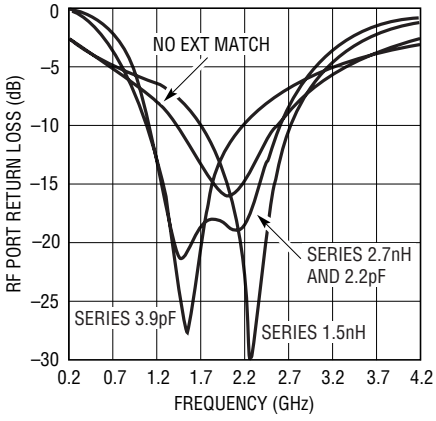
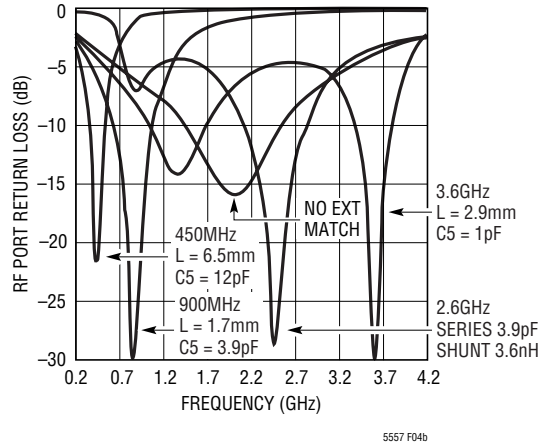


Figure 3. RF Input Schematic



(4a) Series Reactance Matching



(4b) Series Shunt Matching

Figure 4. RF Input Return Loss With and Without External Matching

APPLICATIONS INFORMATION

series transmission line/shunt capacitor matching topology allows the LT5557 to be used for multiple frequency standards without circuit board layout modifications. The series transmission line can also be replaced with a series chip inductor for a more compact layout.

Input return losses for the 450MHz, 900MHz, 2.6GHz and 3.6GHz applications are plotted in Figure 4b. The input return loss with no external matching is repeated in Figure 4b for comparison. The 2.6GHz RF input match uses the high-pass matching network shown in Figures 1 and 3 with C5 = 3.9pF and L5 = 3.6nH. The high-pass input matching network is also used to create a wideband or dual-band input match. For example, with C5 = 3.3pF and L5 = 10nH, the RF input is matched from 800MHz to 2.2GHz, with optimum matching in the 800MHz to 1.1GHz and 1.6GHz to 2.2GHz bands, simultaneously.

RF input impedance and S11 versus frequency (with no external matching) are listed in Table 1 and referenced to Pin 3. The S11 data can be used with a microwave circuit simulator to design custom matching networks and simulate board-level interfacing to the RF input filter.

Table 1. RF Input Impedance vs Frequency

FREQUENCY (MHz)	INPUT IMPEDANCE	S11	
		MAG	ANGLE
50	4.6 + j2.3	0.832	174.7
300	9.1 + j11.2	0.706	153.8
450	12.0 + j14.5	0.639	145.8
600	14.7 + j17.4	0.588	138.7
900	20.5 + j23.3	0.506	123.4
1300	34.4 + j30.3	0.380	97.5
1700	59.6 + j23.8	0.229	55.8
1950	69.2 + j2.8	0.163	6.9
2200	59.2 – j18.1	0.184	–53.5
2450	41.5 – j24.5	0.274	–94.2
2700	28.3 – j21.3	0.374	–120.3
3000	19.0 – j13.5	0.481	–145.5
3300	13.9 – j5.1	0.568	–167.3
3600	10.8 + j3.4	0.645	171.9
3900	9.4 + j12.3	0.700	151.4

LO Input Port

The mixer's LO input, shown in Figure 5, consists of an integrated transformer and high speed limiting differential amplifiers. The amplifiers are designed to precisely drive the mixer for the highest linearity and the lowest noise figure. An internal DC blocking capacitor in series with the transformer's primary eliminates the need for an external blocking capacitor.

The LO input is internally matched from 1 to 5GHz. The input match can be shifted down, as low as 750MHz, with a single shunt capacitor (C4) on Pin 15. One example is plotted in Figure 6 where C4 = 2.7pF produces a 750MHz to 1GHz match.

LO input matching below 750MHz requires the series inductor (L4)/shunt capacitor (C4) network shown in Figure 5. Two examples are plotted in Figure 6 where L4 = 2.7nH/C4 = 3.9pF produces a 650MHz to 830MHz match and L4 = 10nH/C4 = 8.2pF produces a 460MHz to 560MHz match. The evaluation boards do not include pads for L4, so the circuit trace needs to be cut near Pin 15 to insert L4. A low cost multilayer chip inductor is adequate for L4.

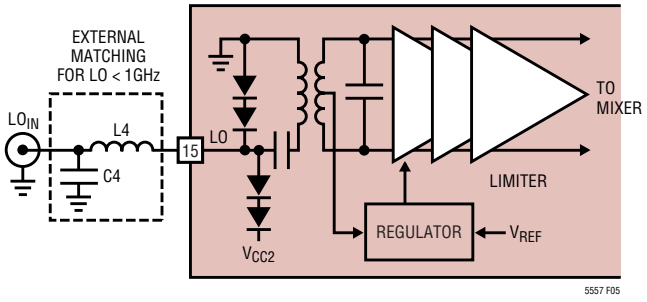


Figure 5. LO Input Schematic

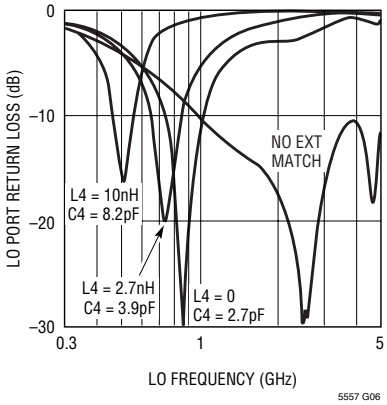


Figure 6. LO Input Return Loss

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The optimum LO drive is –3dBm for LO frequencies above 1.2GHz, although the amplifiers are designed to accommodate several dB of LO input power variation without significant mixer performance variation. Below 1.2GHz, 0dBm LO drive is recommended for optimum noise figure, although –3dBm will still deliver good conversion gain and linearity.

Custom matching networks can be designed using the port impedance data listed in Table 2. This data is referenced to the LO pin with no external matching.

Table 2. LO Input Impedance vs Frequency

FREQUENCY (MHz)	INPUT IMPEDANCE	S11	
		MAG	ANGLE
50	10.0 – j326	0.991	–17.4
300	8.5 – j41.9	0.820	–99.2
500	11.8 – j10.1	0.632	–155.9
700	18.8 + j10.9	0.474	151.8
900	35.0 + j27.4	0.350	100.8
1200	72.9 + j19.3	0.241	31.3
1500	70.0 – j12.6	0.196	–26.1
1800	55.0 – j17.0	0.167	–64.3
2200	47.8 – j9.7	0.102	–97.2
2600	53.6 – j1.9	0.039	–26.8
3000	66.7 + j0.7	0.143	2.1
3500	82.1 – j13.9	0.263	–17.4
4000	69.0 – j30.1	0.290	–43.5
4500	43.7 – j13.2	0.154	–107.5
5000	36.4 + j19.8	0.271	111.6

IF Output Port

The IF outputs, IF^+ and IF^-, are internally connected to the collectors of the mixer switching transistors (see Figure 7). Both pins must be biased at the supply voltage, which can be applied through the center tap of a transformer or through matching inductors. Each IF pin draws 26.6mA of supply current (53.2mA total). For optimum single-ended performance, these differential outputs should be combined externally through an IF transformer or a discrete IF balun circuit. The standard evaluation board (see Figure 1) includes an IF transformer for impedance transformation and differential to single-ended transformation. A second evaluation board (see Figure 2) realizes the same functionality with a discrete IF balun circuit.

The IF output impedance can be modeled as 560Ω in parallel with 2.6pF at low frequencies. An equivalent small-signal model (including bondwire inductance) is shown in Figure 8. Frequency-dependent differential IF output impedance is listed in Table 3. This data is referenced to the package pins (with no external components) and includes the effects of IC and package parasitics. The IF output can be matched for IF frequencies as low as several kHz or as high as 600MHz.

Table 3. IF Output Impedance vs Frequency

FREQUENCY (MHz)	DIFFERENTIAL OUTPUT IMPEDANCE (R_{IF} || X_{IF})
1	560 || – j63.7k (2.6pF)
70	556 || – j870 (2.6pF)
140	551 || – j440 (2.6pF)
190	523 || – j320 (2.6pF)
240	529 || – j254 (2.6pF)
300	509 || – j200 (2.66pF)
360	483 || – j163 (2.7pF)
450	448 || – j125 (2.83pF)
600	396 || – j92 (2.88pF)

Two methods of differential to single-ended IF matching are described:

- Transformer - Based Bandpass
- Discrete IF balun

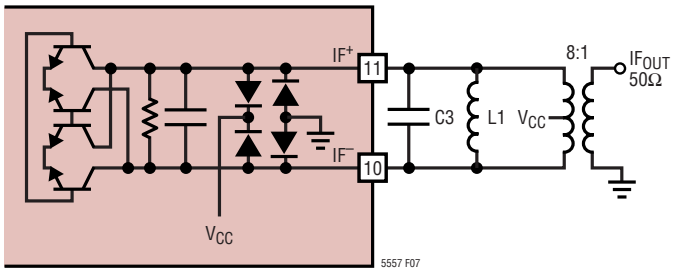


Figure 7. IF Output with External Matching

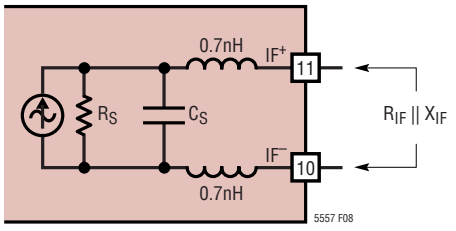


Figure 8. IF Output Small-Signal Model

APPLICATIONS INFORMATION

Transformer-Based Bandpass IF Matching

The standard evaluation board (shown in Figure 1) uses an L-C bandpass IF matching network, with an 8:1 transformer connected across the IF pins. The L-C network maximizes mixer performance at the desired IF frequency. The transformer performs impedance transformation and provides a single-ended 50Ω output.

The value of L1 is calculated as:

$$L1 = 1/[(2\pi f_{IF})^2 \bullet C_{IF}]$$

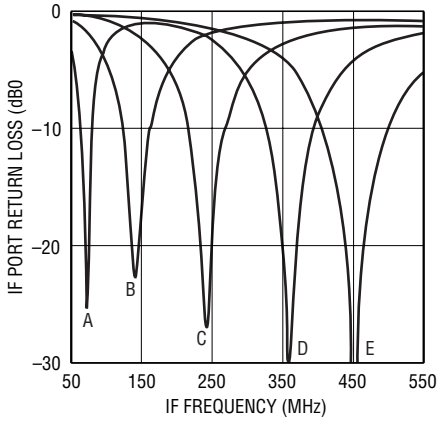
where C_{IF} is the sum of C3 and the internal IF capacitance (listed in Table 3). The value of C3 is selected such that L1 falls on a standard value, while satisfying the desired IF bandwidth. The IF bandwidth can be estimated as:

$$BW_{IF} = 1/(2\pi R_{EFF} C_{IF})$$

where R_{EFF}, the effective IF resistance when loaded with the transformer and inductor loss, is approximately 200Ω.

Below 40MHz, the magnitude of the internal IF reactance is relatively high compared to the internal resistance. In this case, L1 (and C3) can be eliminated, and the 8:1 transformer alone is adequate for IF matching.

The LT5557 was characterized with IF frequencies of 70MHz, 140MHz, 240MHz, 360MHz and 450MHz. The values of L1 and C3 used for these frequencies are tabulated in Figure 1 and repeated in Figure 9. In all cases, L1 is a high-Q 0603 wire-wound chip inductor, for highest conversion gain. Low-cost multi-layer chip inductors can be substituted, with a slight reduction in conversion gain. The measured IF output return losses are plotted in Figure 9.



A: 70MHz, L1 = 270nH, C3 = 15pF
B: 140MHz, L1 = 180nH, C3 = 3.9pF
C: 240MHz, L1 = 82nH, C3 = 2.2pF
D: 360MHz, L1 = 47nH, C3 = 1.2pF
E: 450MHz, L1 = 39nH, C3 = 0pF

Figure 9. IF Output Return Loss with Transformer-Based Bandpass Matching

Discrete IF Balun Matching

For many applications, it is possible to replace the IF transformer with the discrete IF balun shown in Figure 2. The values of L1, L2, C6 and C7 are calculated to realize a 180 degree phase shift at the desired IF frequency and provide a 50Ω single-ended output, using the equations listed below. Inductor L3 is calculated to cancel the internal 2.6pF capacitance. L3 also supplies bias voltage to the IF+ pin. Low cost multilayer chip inductors are adequate for L1, L2 and L3. C3 is a DC blocking capacitor.

$$L1, L2 = \frac{\sqrt{R_{IF} \bullet R_{OUT}}}{\omega_{IF}}$$

$$C6, C7 = \frac{1}{\omega_{IF} \bullet \sqrt{R_{IF} \bullet R_{OUT}}}$$

$$L3 = \frac{|X_{IF}|}{\omega_{IF}}$$

APPLICATIONS INFORMATION

These equations give a good starting point, but it is usually necessary to adjust the component values after building and testing the circuit. The final solution can be achieved with less iteration by considering the parasitics of L3 in the above calculations. Specifically, the effective parallel resistance of L3 (calculated from the manufacturer's Q data) will reduce the value of R_{IF}, which in turn influences the calculated values of L1 (=L2) and C6 (=C7). Also, the effective parallel capacitance of L3 (taken from the manufacturers SRF data) must be considered, since it is in parallel with X_{IF} (from table 3). Frequently, the calculated value for L1 does not fall on a standard value for the desired IF. In this case, a simple solution is to load the IF output with a high-value external chip resistor in parallel with L3, which reduces the value of R_{IF}, until L1 is a standard value.

Discrete IF balun element values for four common IF frequencies (190MHz, 240MHz, 360MHz and 450MHz) are listed in Table 4. The 190MHz application circuit uses a 3.3kΩ resistor in parallel with L3 as described above. The corresponding measured IF output return losses are shown in Figure 10. Typical conversion gain, IIP3 and LO-IF leakage, versus RF input frequency, for all four examples is shown in Figure 11. Typical conversion gain, IIP3 and noise figure versus IF output frequency is shown in Figure 12.

Compared to the transformer-based IF matching technique, this network delivers approximately 1dB higher conversion gain (since the IF transformer loss is eliminated), though noise figure and IIP3 are degraded slightly. The most significant performance difference, as shown in Figure 12, is the limited IF bandwidth available from the discrete approach. For low IF frequencies, the absolute bandwidth is small, whereas higher IF frequencies offer wider bandwidth.

Table 5. Discrete IF Balun Element Values (R_{OUT} = 50Ω)

IF FREQUENCY (MHz)	L1, L2	C6, C7	L3
190	120nH	6.0pF	270nH ‖ 3.3kΩ
240	100nH	4.7pF	150nH
360	56nH	3.0pF	82nH
450	47nH	2.2pF	47nH

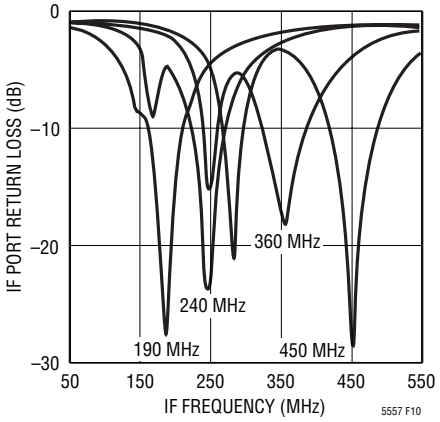


Figure 10. IF Output Return Losses with Discrete Balun Matching

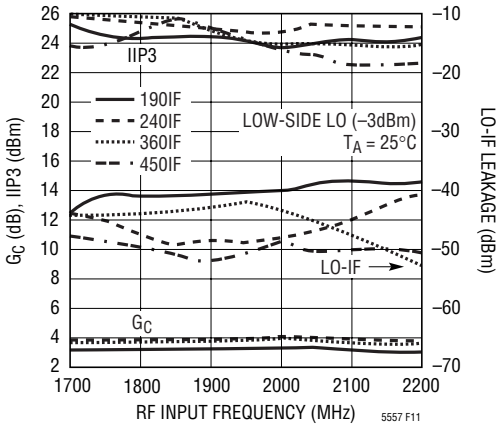


Figure 11. Conversion Gain, IIP3 and LO-IF Leakage vs RF Input Frequency and IF Output Frequency (in MHz) Using Discrete IF Balun Matching

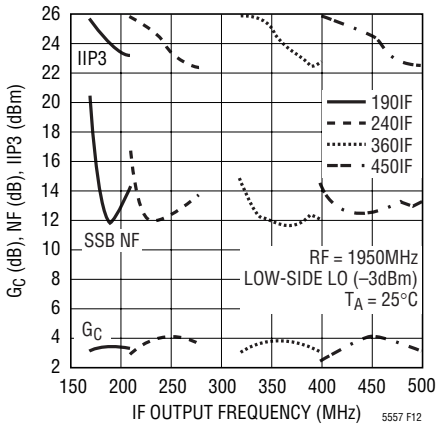


Figure 12. Conversion Gain, IIP3 and SSB NF vs IF Output Frequency Using Discrete IF Balun Matching

APPLICATIONS INFORMATION

Differential IF Output Matching

For fully differential IF architectures, the mixer's IF outputs can be matched directly into a SAW filter or IF amplifier, thus eliminating the IF transformer. One example is shown in Figure 13, where the mixer's 500Ω differential output resistance is matched into a 100Ω differential SAW filter using the tapped-capacitor technique. Inductors L1 and L2 form the inductive portion of the matching network, cancel the internal 2.6pF capacitance, and supply DC bias current to the mixer core. Capacitors C6 through C9 are the capacitive portion of the matching, and perform the impedance step-down.

The calculations for tapped-capacitor matching are covered in the literature, and are not repeated here. Other differential matching options include low-pass, high-pass and band-pass. The choice depends on the system performance goals, IF frequency, IF bandwidth and filter (or amplifier) input impedance. Contact the factory for applications assistance.

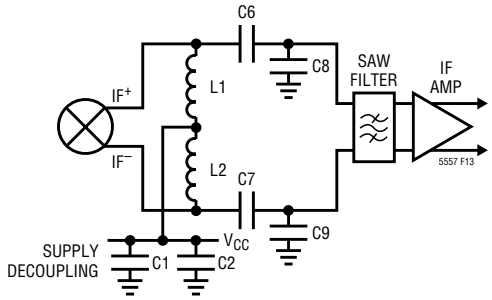


Figure 13. Differential IF Matching Using the Tapped-Capacitor Technique

Enable Interface

Figure 14 shows a simplified schematic of the EN pin interface. The voltage necessary to turn on the LT5557 is 2.7V. To disable the chip, the enable voltage must be less than 0.3V. If the EN pin is allowed to float, the chip will tend to remain in its last operating state. Thus it is not recommended that the enable function be used in this manner. If the shutdown function is not required, then the EN pin should be connected directly to V_{CC}.

The voltage at the EN pin should never exceed the power supply voltage (V_{CC}) by more than 0.3V. If this should occur, the supply current could be sourced through the EN pin ESD diode, potentially damaging the IC.

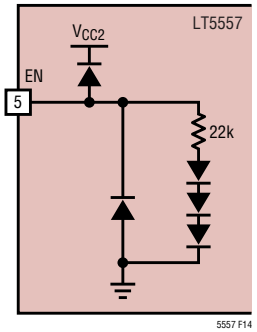
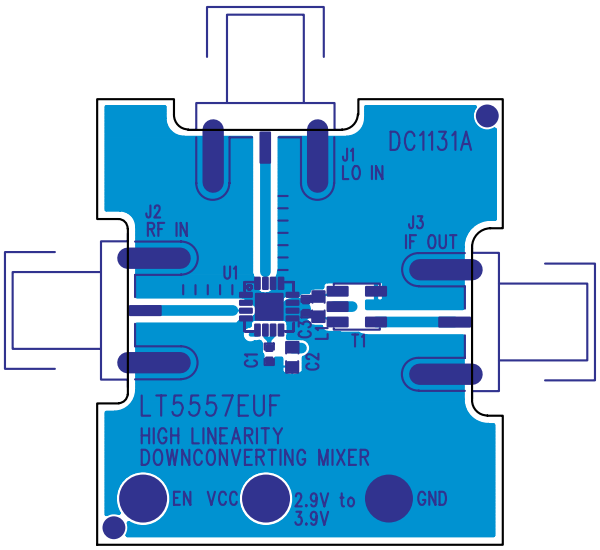
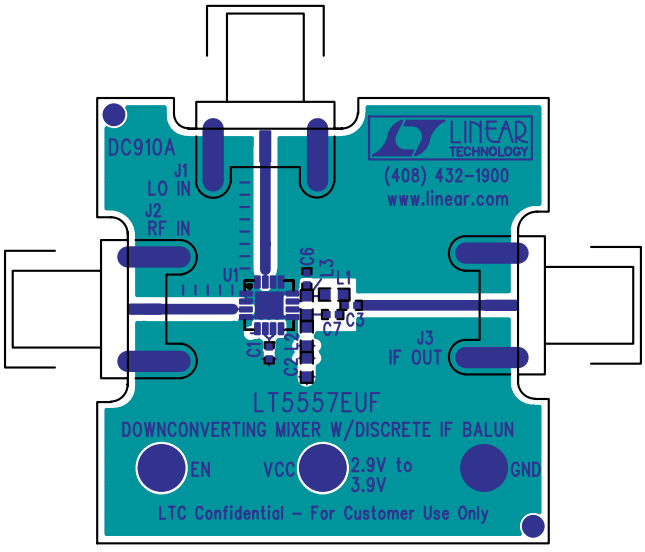


Figure 14. Enable Input Circuit

Standard Evaluation Board Layout (DC1131A)

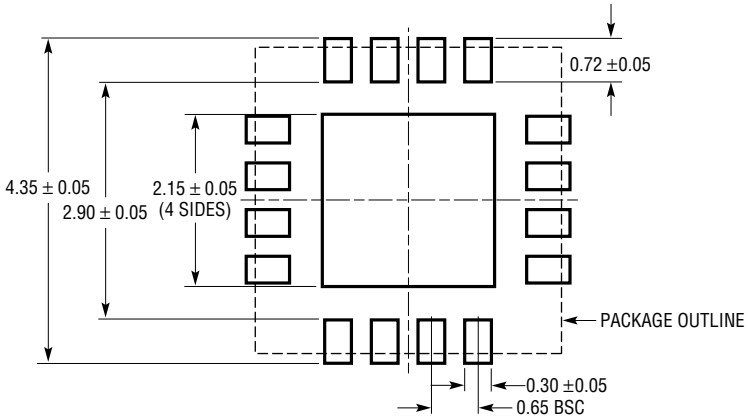


Discrete IF Evaluation Board Layout (DC910A)

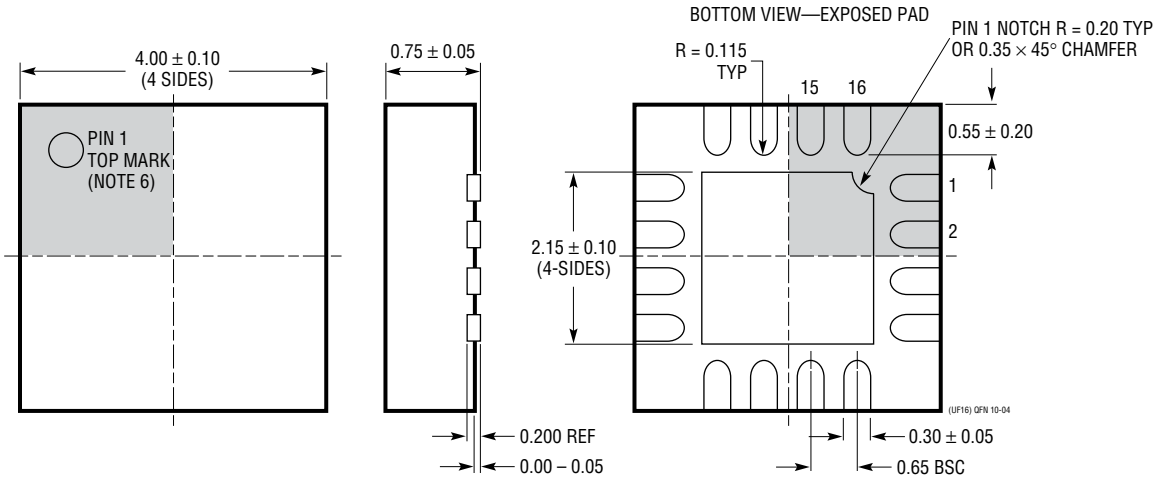


PACKAGE DESCRIPTION

UF Package
16-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1692)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGC)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Infrastructure		
LT5511	High Linearity Upconverting Mixer	RF Output to 3GHz, 17dBm IIP3, Integrated LO Buffer
LT5512	1KHz-3GHz High Signal Level Active Mixer	20dBm IIP3 from 30MHz to 900MHz, Integrated LO Buffer, HF/VHF/UHF Optimized
LT5514	Ultralow Distortion, IF Amplifier/ADC Driver with Digitally Controlled Gain	850MHz Bandwidth, 47dBm OIP3 at 100MHz, 10.5dB to 33dB Gain Control Range
LT5515	1.5GHz to 2.5GHz Direct Conversion Quadrature Demodulator	20dBm IIP3, Integrated LO Quadrature Generator
LT5516	0.8GHz to 1.5GHz Direct Conversion Quadrature Demodulator	21.5dBm IIP3, Integrated LO Quadrature Generator
LT5517	40MHz to 900MHz Quadrature Demodulator	21dBm IIP3, Integrated LO Quadrature Generator
LT5519	0.7GHz to 1.4GHz High Linearity Upconverting Mixer	17.1dBm IIP3 at 1GHz, Integrated RF Output Transformer with 50Ω Matching, Single-Ended LO and RF Ports Operation
LT5520	1.3GHz to 2.3GHz High Linearity Upconverting Mixer	15.9dBm IIP3 at 1.9GHz, Integrated RF Output Transformer with 50Ω Matching, Single-Ended LO and RF Ports Operation
LT5521	10MHz to 3700MHz High Linearity Upconverting Mixer	24.2dBm IIP3 at 1.95GHz, NF = 12.5dB, 3.15V to 5.25V Supply, Single-Ended LO Port Operation
LT5522	400MHz to 2.7GHz High Signal Level Downconverting Mixer	4.5V to 5.25V Supply, 25dBm IIP3 at 900MHz, NF = 12.5dB, 50Ω Single-Ended RF and LO Ports
LT5525	High Linearity, Low Power Downconverting Mixer	Single-Ended 50Ω RF and LO Ports, 17.6dBm IIP3 at 1900MHz, I_{CC} = 28mA
LT5526	High Linearity, Low Power Downconverting Mixer	3V to 5.3V Supply, 16.5dBm IIP3, 100kHz to 2GHz RF, NF = 11dB, I_{CC} = 28mA, –65dBm LO-RF Leakage
LT5527	400MHz to 3.7GHz, 5V High Signal Level Downconverting Mixer	23.5dBm IIP3 at 1.9GHz, NF = 12.5dB, Single-Ended RF and LO Ports
LT5528	1.5GHz to 2.4GHz High Linearity Direct I/Q Modulator	21.8dBm OIP3 at 2GHz, –159dBm/Hz Noise Floor, 50Ω Interface at all Ports
LT5568	600MHz to 1.2GHz High Linearity Direct I/Q Modulator	22.9dBm OIP3, –160.3dBm/Hz Noise Floor, –46dBc Image Rejection, –43dBm Carrier Leakage
RF Power Detectors		
LTC®5505	RF Peak Detectors with >40dB Dynamic Range	300MHz to 3GHz, Temperature Compensated, –32dBm to 12dBm
LTC5507	100kHz to 1000MHz RF Peak Power Detector	100kHz to 1GHz, Temperature Compensated, –34dBm to 14dBm
LTC5508	300MHz to 7GHz RF Peak Power Detector	44dB Dynamic Range, Temperature Compensated, SC70 Package, –32dBm to 12dBm
LTC5509	300MHz to 3GHz RF Peak Power Detector	36dB Dynamic Range, Low Power Consumption, SC70 Package, –30dBm to 6dBm
LTC5530	300MHz to 7GHz Precision RF Peak Power Detector	Precision V_{OUT} Offset Control, Shutdown, Adjustable Gain, –32dBm to 10dBm
LTC5531	300MHz to 7GHz Precision RF Peak Power Detector	Precision V_{OUT} Offset Control, Shutdown, Adjustable Offset, –32dBm to 10dBm
LTC5532	300MHz to 7GHz Precision RF Peak Power Detector	Precision V_{OUT} Offset Control, Adjustable Gain and Offset, ±35mV Offset Voltage Tolerence
LTC5533	300MHz to 11GHz Dual Precision RF Peak Detector	–32dBm to 12dBm, Adjustable Offset, 45dB Ch-Ch Isolation
LT5534	50MHz to 3GHz RF Log Detector with 60dB Dynamic Range	±1dB Output Variation over Temperature, 38ns Response Time
LTC5536	Precision 600MHz to 7GHz RF Peak Detector with Fast Comparator Output	25ns Response Time, Comparator Reference Input, Latch Enable Input, –26dBm to +12dBm Input Range
LT5537	90dB Dynamic Range RF Log Detector	LF to 1GHz, –79dBm to 12dBm, Very Low Tempco
Low Voltage RF Building Block		
LT5546	500MHz Quadrature Demodulator with VGA and 17MHz Baseband Bandwidth	17MHz Baseband Bandwidth, 40MHz to 500MHz IF, 1.8V to 5.25V Supply, –7dB to 56dB Linear Power Gain

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

LT 1206 • PRINTED IN THE USA

5MHz to 1600MHz High Linearity Direct Quadrature Modulator

FEATURES

- **Frequency Range: 5MHz to 1600MHz**
- **High Output IP3: +27.7dBm at 140MHz**
  +22.9dBm at 900MHz
- **Low Output Noise Floor at 6MHz Offset:**
  No Baseband AC Input: –161.2dBm/Hz
  P_{OUT} = 5.5dBm: –160dBm/Hz
- **Low LO Feedthrough: –55dBm at 140MHz**
- **High Image Rejection: –50.4dBc at 140MHz**
- **Integrated LO Buffer and LO Quadrature Phase Generator**
- **50Ω Single-Ended LO and RF Ports**
- **>400MHz Baseband Bandwidth**
- 24-Lead QFN 4mm × 4mm Package
- Pin-Compatible with Industry Standard Pin-Out
- Shut-down Mode

APPLICATIONS

- Point-to-Point Microwave Link
- Military Radio
- Basestation Transmitter GSM/EDGE/CDMA2K
- 700MHz LTE Basestation Transmitter
- Satellite Communication
- CATV/Cable Broadband Modulator
- 13.56MHz/UHF RFID Modulator

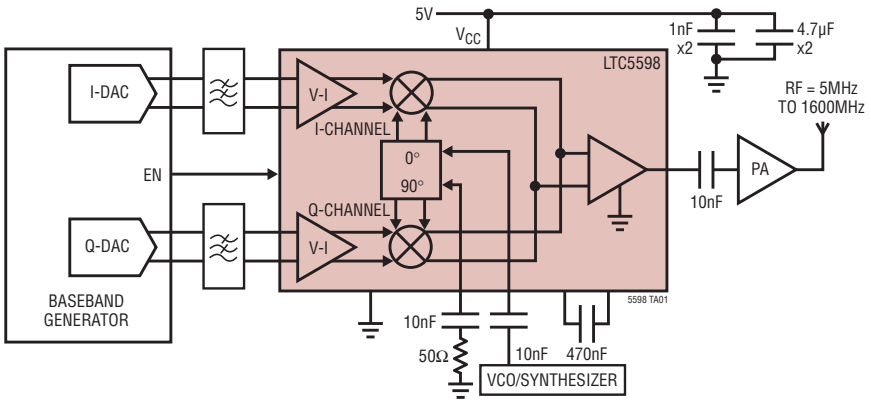
DESCRIPTION

The LTC®5598 is a direct I/Q modulator designed for high performance wireless applications, including wireless infrastructure. It allows direct modulation of an RF signal using differential baseband I and Q signals. It supports point-to-point microwave link, GSM, EDGE, CDMA, 700MHz band LTE, CDMA2000, CATV applications and other systems. It may also be configured as an image reject upconverting mixer, by applying 90° phase-shifted signals to the I and Q inputs.

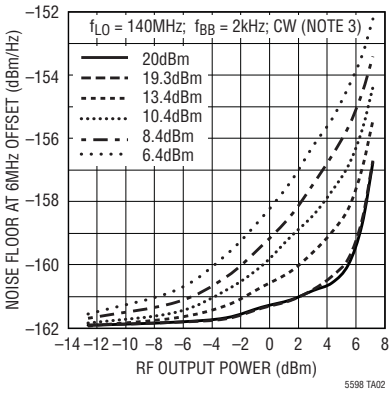
The I/Q baseband inputs consist of voltage-to-current converters that in turn drive double-balanced mixers. The outputs of these mixers are summed and applied to a buffer, which converts the differential mixer signals to a 50Ω single-ended buffered RF output. The four balanced I and Q baseband input ports are intended for DC coupling from a source with a common-mode voltage level of about 0.5V. The LO path consists of an LO buffer with single-ended or differential inputs, and precision quadrature generators that produce the LO drive for the mixers. The supply voltage range is 4.5V to 5.25V, with about 168mA current.

TYPICAL APPLICATION

5MHz to 1600MHz Direct Conversion Transmitter Application



Noise Floor vs RF Output Power and Differential LO Input Power

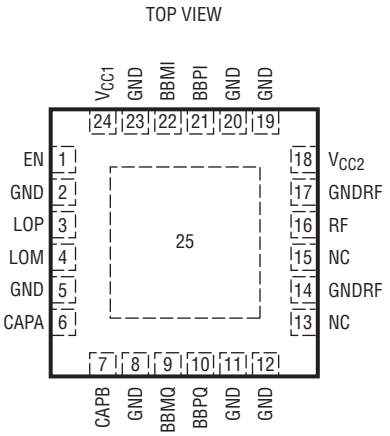


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 5.6V
Common Mode Level of BBPI, BBMI and
BBPQ, BBMQ 0.6V
LOP, LOM Input 20dBm
Voltage on Any Pin
Not to Exceed ..... –0.3V to V_{CC} + 0.3V
T_{JMAX} ..... 150°C
Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC5598IUF#PBF	LTC5598IUF#TRPBF	5598	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, EN = 5V, T_A = 25°C, P_{LO} = 0dBm, single-ended; BBPI, BBMI, BBPQ, BBMQ common-mode DC voltage V_{CMBB} = 0.5V_{DC}, I&Q baseband input signal = 100kHz CW, 0.8$V_{PP,DIFF}$ each, I&Q 90° shifted (lower side-band selection), unless otherwise noted. (Note 11)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RF OUTPUT (RF)						
f_{RF}	RF Frequency Range			5 to 1600		MHz
$S_{22, ON}$	RF Output Return Loss	EN = High, 5MHz to 1600MHz		<–20		dB
f_{LO} = 140MHz, f_{RF} = 139.9MHz						
G_V	Conversion Voltage Gain	20 • Log ($V_{RF, OUT, 50Ω}/V_{IN, DIFF, I or Q}$)		–2		dB
P_{OUT}	Absolute Output Power	1$V_{PP,DIFF}$ on each I&Q Inputs		2		dBm
OP1dB	Output 1dB Compression			8.5		dBm
OIP2	Output 2nd Order Intercept	(Notes 4, 5)		74		dBm
OIP3	Output 3rd Order Intercept	(Notes 4, 6)		27.7		dBm
NFloor	RF Output Noise Floor	No Baseband AC Input Signal (Note 3) P_{OUT} = 4.6dBm (Note 3) $P_{LO, SE}$ = 10dBm P_{OUT} = 5.5dBm (Note 3) $P_{LO, DIFF}$ = 20dBm		–161.2 –154.5 –160		dBm/Hz dBm/Hz dBm/Hz
IR	Image Rejection	(Note 7)		–50.4		dBc
LOFT	LO Feedthrough (Carrier Leakage)	EN = High (Note 7) EN = Low (Note 7)		–55 –78		dBm dBm
f_{LO} = 450MHz, f_{RF} = 449.9MHz						
G_V	Conversion Voltage Gain	20 • Log ($V_{RF, OUT, 50Ω}/V_{IN, DIFF, I or Q}$)	–5.0	–2.1	0.5	dB
P_{OUT}	Absolute Output Power	1$V_{PP,DIFF}$ on each I&Q Inputs		1.9		dBm
OP1dB	Output 1dB Compression			8.4		dBm
OIP2	Output 2nd Order Intercept	(Notes 4, 5)		72		dBm
OIP3	Output 3rd Order Intercept	(Notes 4, 6)		25.5		dBm
NFloor	RF Output Noise Floor	No Baseband AC Input Signal (Note 3)		–160.9		dBm/Hz
IR	Image Rejection	(Note 7)		–55		dBc
LOFT	LO Feedthrough (Carrier Leakage)	EN = High (Note 7) EN = Low (Note 7)		–51 –68		dBm dBm
f_{LO} = 900MHz, f_{RF} = 899.9MHz						
G_V	Conversion Voltage Gain	20 • Log ($V_{RF, OUT, 50Ω}/V_{IN, DIFF, I or Q}$)		–2		dB
P_{OUT}	Absolute Output Power	1$V_{PP,DIFF}$ on each I&Q Inputs		2		dBm
OP1dB	Output 1dB Compression			8.5		dBm
OIP2	Output 2nd Order Intercept	(Notes 4, 5)		69		dBm
OIP3	Output 3rd Order Intercept	(Notes 4, 6)		22.9		dBm
NFloor	RF Output Noise Floor	No Baseband AC Input Signal (Note 3) P_{OUT} = 5.2dBm (Note 3) $P_{LO, SE}$ = 10dBm		–160.3 –154.5		dBm/Hz dBm/Hz
IR	Image Rejection	(Note 7)		–54		dBc
LOFT	LO Feedthrough (Carrier Leakage)	EN = High (Note 7) EN = Low (Note 7)		–48 –54		dBm dBm

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, EN = 5V, T_A = 25°C, P_{LO} = 0dBm, single-ended; BBPI, BBMI, BBPQ, BBMQ common-mode DC voltage V_{CMBB} = 0.5V_{DC}, I&Q baseband input signal = 100kHz CW, 0.8$V_{PP,DIFF}$ each, I&Q 90° shifted (lower side-band selection), unless otherwise noted. (Note 11)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LO INPUT (LOP)						
f_{LO}	LO Frequency Range			5 to 1600		MHz
$P_{LO,DIFF}$	Differential LO Input Power Range			–10 to 20		dBm
$P_{LO, SE}$	Single-Ended LO Input Power Range			–10 to 12		dBm
$S_{11, ON}$	LO Input Return Loss	EN = High		–10.5		dB
$S_{11, OFF}$	LO Input Return Loss	EN = Low		–9.6		dB
BASEBAND INPUTS (BBPI, BBMI, BBPQ, BBMQ)						
BW_{BB}	Baseband Bandwidth	-3dB Bandwidth		>400		MHz
$I_{b,BB}$	Baseband Input Current	Single-Ended		–68		µA
$R_{IN, SE}$	Input Resistance	Single-Ended		–7.4		kΩ
V_{CMBB}	DC Common-Mode Voltage	Externally Applied		0.5		V
V_{SWING}	Amplitude Swing	No Hard Clipping, Single-Ended		0.86		V_{P-P}
POWER SUPPLY (V_{CC1}, V_{CC2})						
V_{CC}	Supply Voltage		4.5	5	5.25	V
$I_{CC(ON)}$	Supply Current	EN = High, I_{CC1}+ I_{CC2}	130	165	200	mA
$I_{CC(OFF)}$	Supply Current, Sleep Mode	EN = 0V, I_{CC1}+ I_{CC2}		0.24	0.9	mA
t_{ON}	Turn-On Time	EN = Low to High (Notes 8, 10)		75		ns
t_{OFF}	Turn-Off Time	EN = High to Low (Notes 9, 10)		10		ns
POWER UP/DOWN						
Enable	Input High Voltage Input High Current	EN = High EN = 5V	2	 43		V µA
Sleep	Input Low Voltage Input Low Current	EN = Low EN = 0V		 –40	1	V µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC5598 is guaranteed functional over the operating temperature range –40°C to 85°C.

Note 3: At 6MHz offset from the LO signal frequency. 100nF between BBPI and BBMI, 100nF between BBPQ and BBMQ.

Note 4: Baseband is driven by 2MHz and 2.1MHz tones with 1$V_{PP,DIFF}$ for two-tone signals at each I or Q input (0.5$V_{PP,DIFF}$ for each tone).

Note 5: IM2 is measured at LO frequency – 4.1MHz.

Note 6: IM3 is measured at LO frequency – 1.9 MHz and LO frequency – 2.2MHz.

Note 7: Amplitude average of the characterization data set without image or LO feedthrough nulling (unadjusted).

Note 8: RF power is within 10% of final value.

Note 9: RF power is at least 30dB lower than in the ON state.

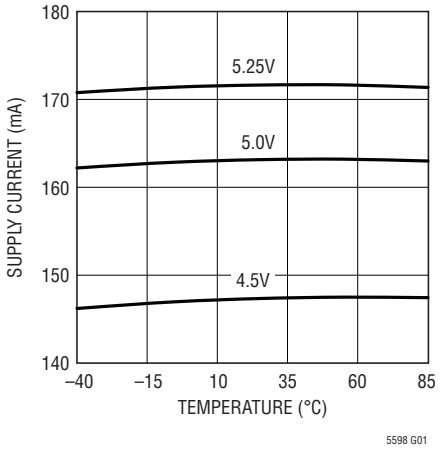
Note 10: External coupling capacitors at pins LOP, LOM and RF are 100pF each.

Note 11: Tests are performed as shown in the configuration of Figure 10. The LO power is applied to J3 while J5 is terminated with 50Ω to ground for single-ended LO drive.

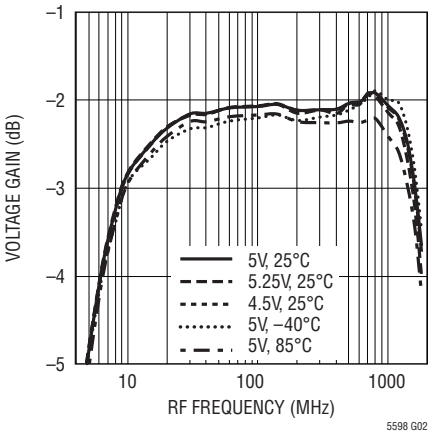
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5V, EN = 5V, T_A = 25°C, $f_{RF} = f_{LO} - f_{BB}$, P_{LO} = 0dBm single-ended, BBPI, BBMI, BBPQ, BBMQ common-mode DC voltage $V_{CMBB} = 0.5V_{DC}$, I&Q baseband input signal = 100kHz, $0.8V_{PP,DIFF}$, two-tone baseband input signal = 2MHz, 2.1MHz, $0.5V_{PP,DIFF}$ each tone, I&Q 90° shifted (lower side-band selection); $f_{NOISE} = f_{LO} - 6MHz$; unless otherwise noted. (Note 11)

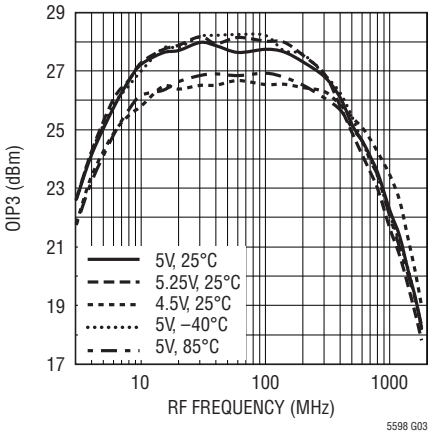
Supply Current vs Temperature



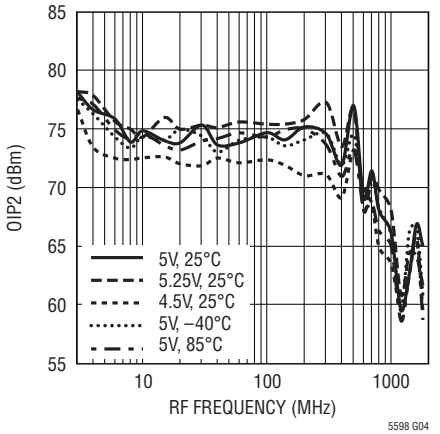
Voltage Gain vs RF Frequency



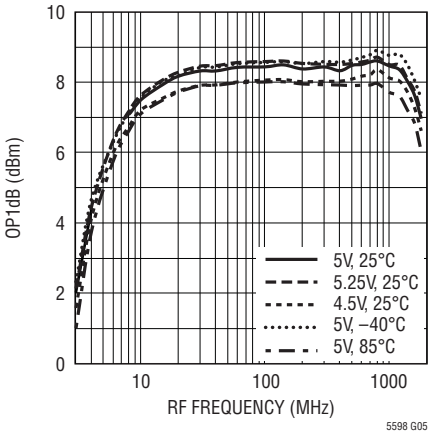
Output IP3 vs RF Frequency



Output IP2 vs RF Frequency



Output 1dB Compression vs RF Frequency



LO Feedthrough to RF Output vs LO Frequency

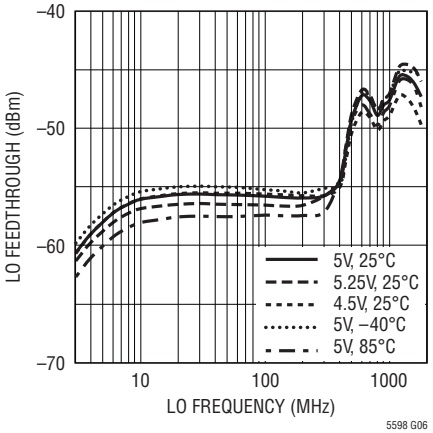
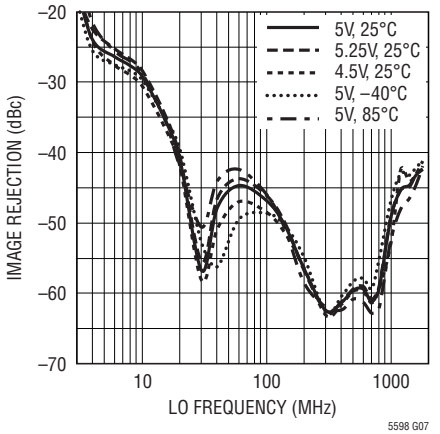
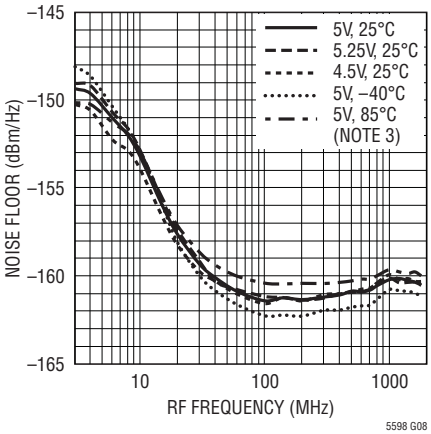


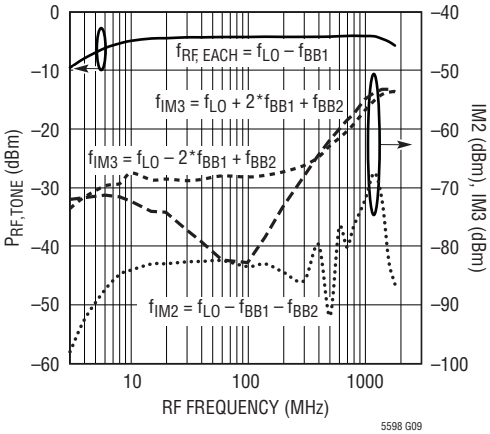
Image Rejection vs LO Frequency



Noise Floor vs RF Frequency (No AC Baseband Input Signal)



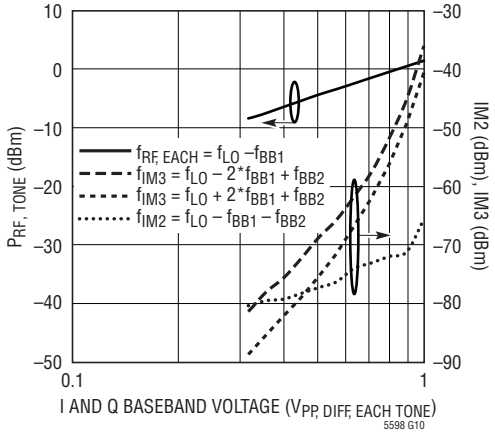
RF Two-Tone Power (Each Tone), IM2 and IM3 vs RF Frequency



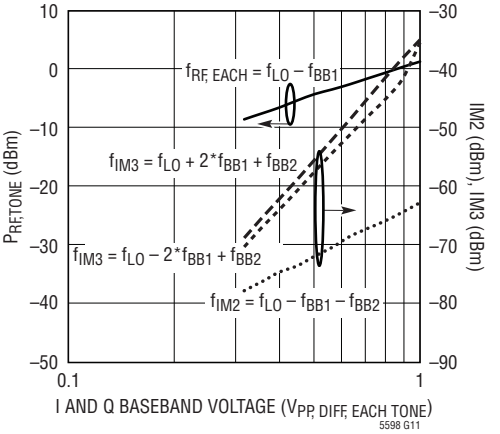
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5V, EN = 5V, T_A = 25°C, $f_{RF} = f_{LO} - f_{BB}$, P_{LO} = 0dBm single-ended, BBPI, BBMI, BBPQ, BBMQ common-mode DC voltage $V_{CMBB} = 0.5V_{DC}$, I&Q baseband input signal = 100kHz, $0.8V_{PP,DIFF}$, two-tone baseband input signal = 2MHz, 2.1MHz, $0.5V_{PP,DIFF}$ each tone, I&Q 90° shifted (lower side-band selection); $f_{NOISE} = f_{LO}$ – 6MHz; unless otherwise noted. (Note 11)

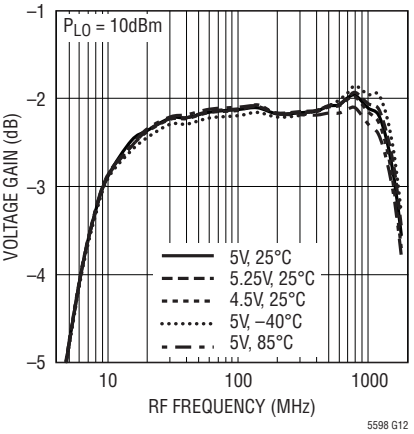
RF Two-Tone Power (Each Tone), IM2 and IM3 vs Baseband Voltage and Temperature (f_{LO} = 140MHz)



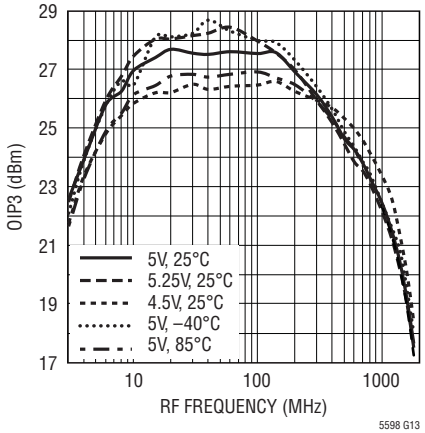
RF Two-Tone Power (Each Tone), IM2 and IM3 vs Baseband Voltage and Temperature (f_{LO} = 900MHz)



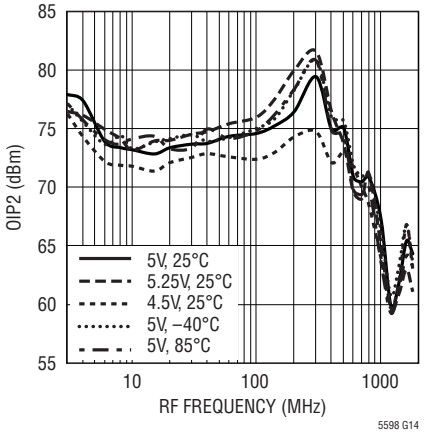
Voltage Gain vs RF Frequency (P_{LO} = 10dBm)



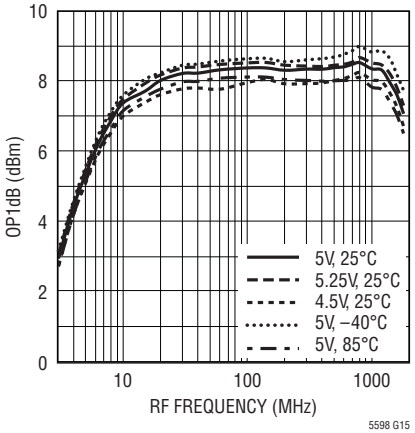
Output IP3 vs RF Frequency (P_{LO} = 10dBm)



Output IP2 vs RF Frequency (P_{LO} = 10dBm)



Output 1dB Compression vs RF Frequency (P_{LO} = 10dBm)



LO Feedthrough to RF Output vs LO Frequency (P_{LO} = 10dBm)

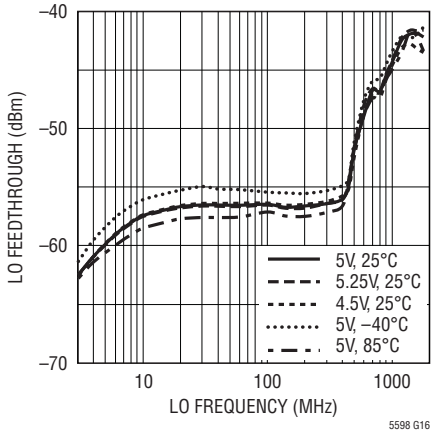
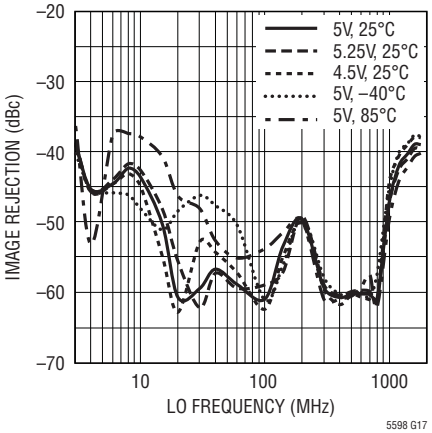
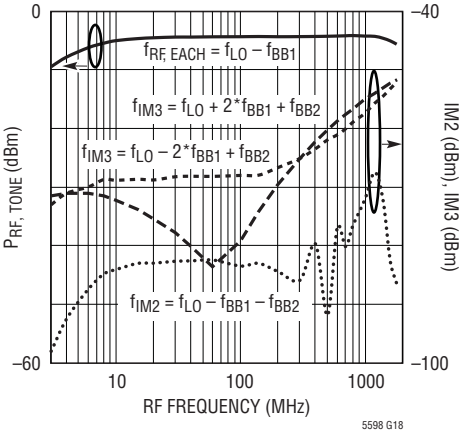


Image Rejection vs LO Frequency (P_{LO} = 10dBm)



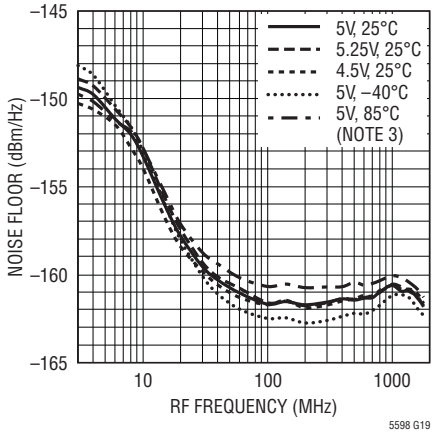
RF Two-Tone Power (Each Tone), IM2 and IM3 vs RF Frequency (P_{LO} = 10dBm)



TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5V, EN = 5V, T_A = 25°C, $f_{RF} = f_{LO} - f_{BB}$, f_{LO} = 450MHz, P_{LO} = 0dBm single-ended, BBPI, BBMI, BBPQ, BBMQ common-mode DC voltage $V_{CMBB} = 0.5V_{DC}$, I&Q baseband input signal = 100kHz, $0.8V_{PP,DIFF}$, two-tone baseband input signal = 2MHz, 2.1MHz, $0.5V_{PP,DIFF}$ each tone, I&Q 90° shifted (lower side-band selection); $f_{NOISE} = f_{LO}$ – 6MHz; unless otherwise noted. (Note 11)

Noise Floor vs RF Frequency (P_{LO} = 10dBm, No AC Baseband Input Signal)



LO Feedthrough to RF Output vs LO Frequency for EN = Low

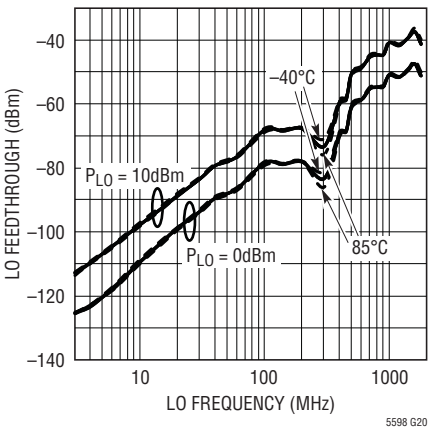
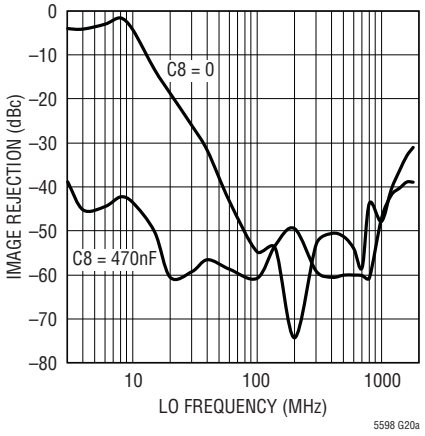
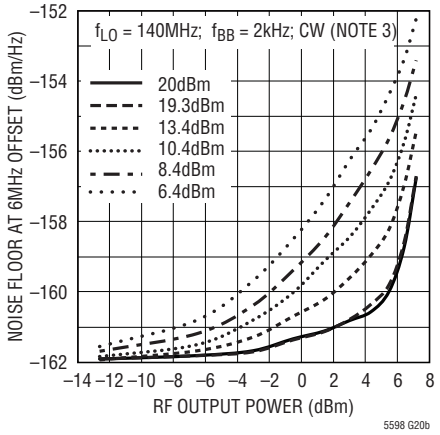


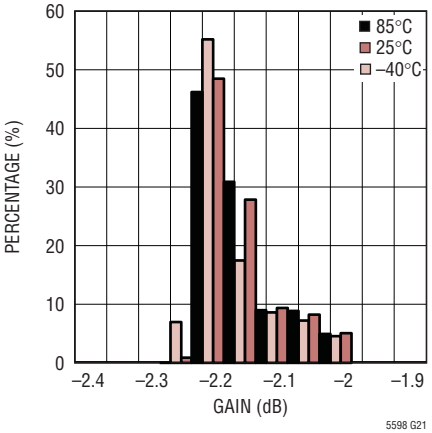
Image Rejection vs LO Frequency (P_{LO} = 10dBm)



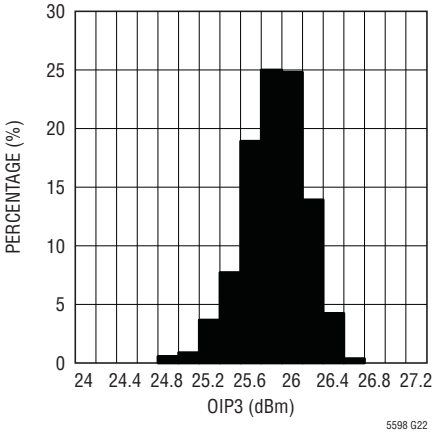
Noise Floor vs RF Output Power and Differential LO Input Power



Gain Distribution



Output IP3 Distribution at 25°C



LO Feedthrough Distribution

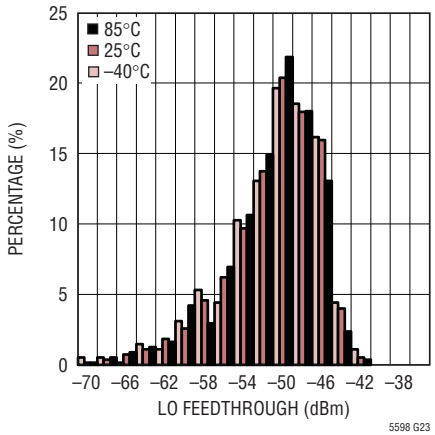
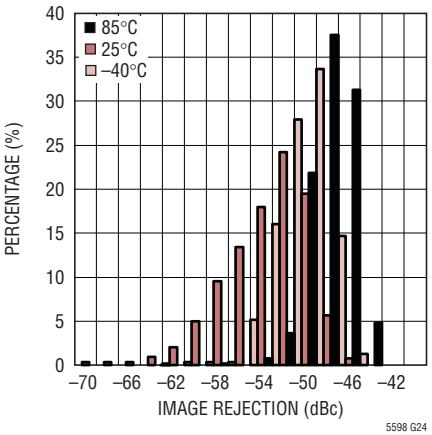
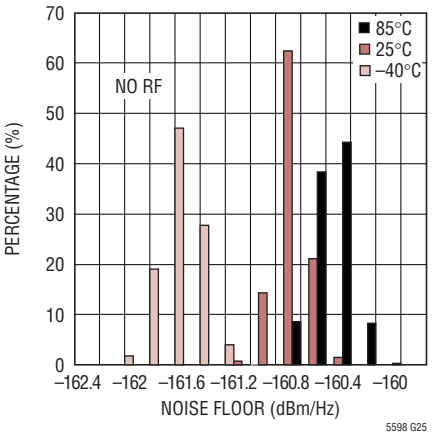


Image Rejection Distribution



Noise Floor Distribution



PIN FUNCTIONS

EN (Pin 1): Enable Input. When the Enable Pin voltage is higher than 2 V, the IC is turned on. When the input voltage is less than 1 V, the IC is turned off. If not connected, the IC is enabled.

GND (Pins 2, 5, 8, 11, 12, 19, 20, 23 and 25): Ground. Pins 2, 5, 8, 11, 12, 19, 20, 23 and exposed pad 25 are connected to each other internally. For best RF performance, pins 2, 5, 8, 11, 12, 19, 20, 23 and the Exposed Pad 25 should be connected to RF ground.

LOP (Pin 3): Positive LO Input. This LO input is internally biased at about 2.3V. An AC de-coupling capacitor should be used at this pin to match to an external 50Ω source.

LOM (Pin 4): Negative LO Input. This input is internally biased at about 2.3V. An AC de-coupling capacitor should be used at this pin via a 50Ω to ground for best OIP2 performance.

CAPA, CAPB (Pins 6, 7): External capacitor pins. A capacitor between the CAPA and the CAPB pin can be used in order to improve the image rejection for frequencies below 100MHz. A capacitor value of 470nF is recommended. These pins are internally biased at about 2.3V.

BBMQ, BBPQ (Pins 9, 10): Baseband Inputs for the Q-channel, each high input impedance. They should be externally biased at 0.5V common-mode level and not be left floating. Applied common-mode voltage must stay below $0.6V_{DC}$.

NC (Pins 13, 15): No Connect. These pins are floating.

GNDRF (Pins 14, 17): Ground. Pins 14 and 17 are connected to each other internally and function as the ground return for the RF output buffer. They are connected via back-to-back diodes to the exposed pad 25. For best LO suppression performance those pins should be grounded separately from the exposed paddle 25. For best RF performance, pins 14 and 17 should be connected to RF ground.

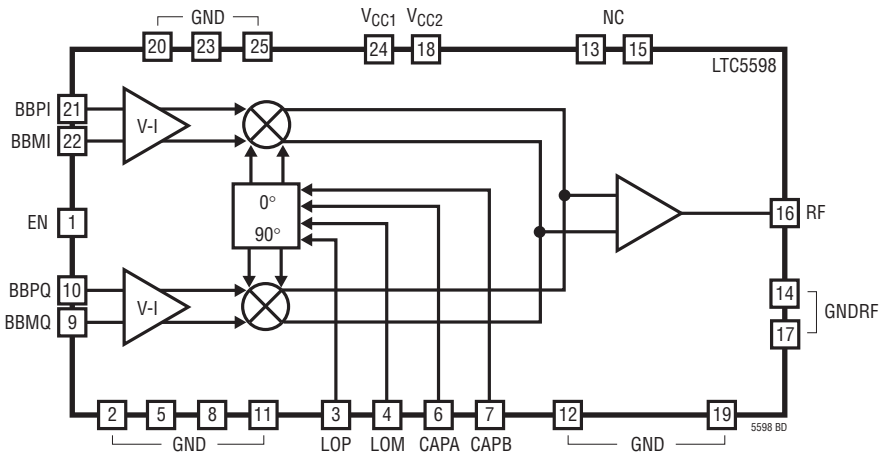
RF (Pin 16): RF Output. The RF output is a DC-coupled single-ended output with approximately 50Ω output impedance at RF frequencies. An AC coupling capacitor should be used at this pin to connect to an external load.

V_{CC} (Pins 18, 24): Power Supply. It is recommended to use 1nF and 4.7µF capacitors for decoupling to ground on each of these pins.

BBPI, BBMI (Pins 21, 22): Baseband Inputs for the Q-channel, each high input impedance. They should be externally biased at 0.5V common-mode level and not be left floating. Applied common-mode voltage must stay below $0.6V_{DC}$.

Exposed Pad (Pin 25): Ground. This pin must be soldered to the printed circuit board ground plane.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LTC5598 consists of I and Q input differential voltage-to-current converters, I and Q up-conversion mixers, an RF output buffer, an LO quadrature phase generator and LO buffers.

External I and Q baseband signals are applied to the differential baseband input pins, BBPI, BBMI, and BBPQ, BBMQ. These voltage signals are converted to currents and translated to RF frequency by means of double-balanced up-converting mixers. The mixer outputs are combined in an RF output buffer, which also transforms the output impedance to 50Ω. The center frequency of the resulting RF signal is equal to the LO signal frequency. The LO input drives a phase shifter which splits the LO signal into in-phase and quadrature LO signals. These LO signals are then applied to on-chip buffers which drive the up-conversion mixers. In most applications, the LOP input is driven by the LO source via an optional matching network, while the LOM input is terminated with 50Ω to RF ground via a similar optional matching network. The RF output is single-ended and internally 50Ω matched.

Baseband Interface

The circuit is optimized for a common mode voltage of 0.5V which should be externally applied. The baseband pins should not be left floating because the internal PNP's base current will pull the common mode voltage higher than the 0.6V limit. This condition may damage the part. In shut-down mode, it is recommended to have a termination to ground or to a 0.5V source with a value lower than 1kΩ. The PNP's base current is about –68µA in normal operation.

The baseband inputs (BBPI, BBMI, BBPQ, BBMQ) present a single-ended input impedance of about –7.4kΩ each. Because of the negative input impedance, it is important to keep the source resistance at each baseband input low enough such that the parallel value remains positive vs baseband frequency. At each of the four baseband inputs, a capacitor of 4pF in series with 30Ω is connected to ground. This is in parallel with a PNP emitter follower (see Figure 1). The baseband bandwidth depends on the source impedance. For a 25Ω source impedance, the baseband bandwidth (–1dB) is about 300MHz. If a 5.6nH series inductor is inserted in each of the four baseband connections, the –1dB baseband bandwidth increases to about 800MHz.

It is recommended to include the baseband input impedance in the baseband lowpass filter design. The input impedance of each baseband input is given in Table 1.

Table 1. Single-Ended BB Port Input Impedance vs Frequency for EN = High and V_{CMBB} = 0.5V_{DC}

FREQUENCY (MHz)	BB INPUT IMPEDANCE	REFLECTION COEFFICIENT	
		MAG	ANGLE
0.1	–10578 – j263	1.01	–0.02
1	–8436 – j1930	1.011	–0.15
2	–6340 – j3143	1.013	–0.36
4	–3672 – j3712	1.014	–0.78
8	–1644 – j2833	1.015	–1.51
16	–527 – j1765	1.016	–2.98
30	–177 – j1015	1.017	–5.48
60	–45.2 – j514	1.017	–11
100	–13.2 – j306	1.014	–18.5
140	–0.2 – j219	1	–25.7
200	4.5 – j151	0.982	–36.6
300	10.4 – j99.4	0.921	–52.9
400	12.3 – j72.4	0.854	–68.2
500	14.7 – j57.5	0.780	–79.9
600	15.5 – j46.3	0.720	–91.4

The baseband inputs should be driven differentially; otherwise, the even-order distortion products may degrade the overall linearity performance. Typically, a DAC will

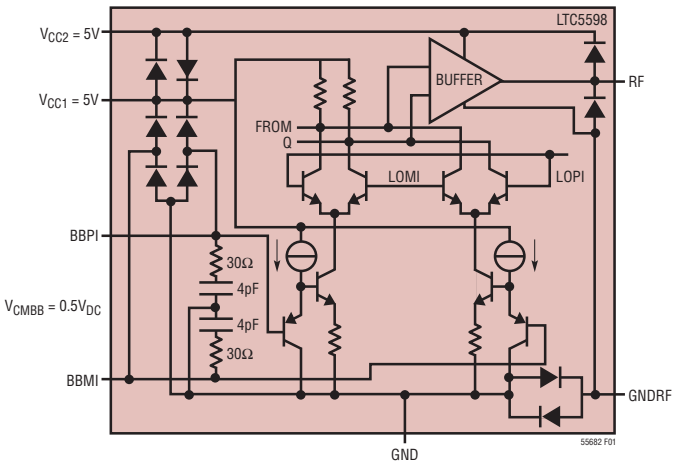


Figure 1. Simplified Circuit Schematic of the LTC5598 (Only I-Half is Drawn)

APPLICATIONS INFORMATION

be the signal source for the LTC5598. A reconstruction filter should be placed between the DAC output and the LTC5598's baseband inputs.

In Figure 2 a typical baseband interface is shown, using a fifth-order lowpass ladder filter.

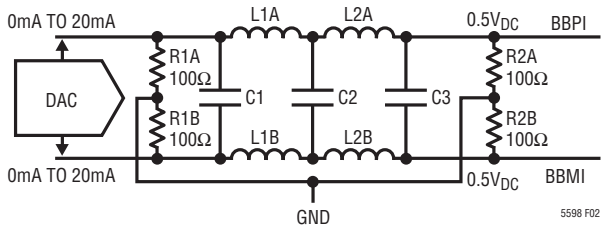


Figure 2. Baseband Interface with 5th Order Filter and $0.5V_{CM}$ DAC (Only I Channel is Shown)

For each baseband pin, a 0 to 1V swing is developed corresponding to a DAC output current of 0mA to 20mA. The maximum sinusoidal single side-band RF output power is about +7.3dBm for full 0V to 1V swing on each I- and Q- channel baseband input ($2V_{PP, DIFF}$).

LO Section

The internal LO chain consists of poly-phase phase shifters followed by LO buffers. The LOP input is designed as a single-ended input with about 50Ω input impedance. The LOM input should be terminated with 50Ω through a DC blocking capacitor.

The LOP and LOM inputs can be driven differentially in case an exceptionally low large-signal output noise floor is required (see graph 5598 G20b).

A simplified circuit schematic for the LOP, LOM, CAPA and CAPB inputs is given in Figure 3. A feedback path is implemented from the LO buffer outputs to the LO inputs in order to minimize offsets in the LO chain by storing the offsets on C5, C7 and C8 (see Figure 10). Optional capacitor C8 improves the image rejection below 100MHz (see graph 5598 G20a). Because of the feedback path, the input impedance for P_{LO} = 0dBm is somewhat different than for P_{LO} = 10dBm for the lower part of the operating frequency range. In Table 2, the LOP port input impedance vs frequency is given for EN = High and P_{LO} = 0dBm. For EN = Low and P_{LO} = 0dBm, the input impedance is given in Table 3. In Table 4 and 5, the LOP port input impedance is given for EN = High and Low under the condition of P_{LO} = 10dBm. Figure 4 shows the LOP port return loss for the standard demo board (schematic is shown in Figure 10) when the LOM port is terminated with 50Ω to GND. The values of L1, L2, C9 and C10 are chosen such that the bandwidth for the LOP port of the standard demo board is maximized while meeting the LO input return loss $S_{11, ON}$ < –10dB.

Table 2. LOP Port Input Impedance vs Frequency for EN = High and P_{LO} = 0dBm (LOM AC Coupled With 50Ω to Ground).

FREQUENCY (MHz)	LO INPUT IMPEDANCE	REFLECTION COEFFICIENT	
		MAG	ANGLE
0.1	333 – j10.0	0.739	–0.5
1	318 – j59.9	0.737	–3.3
2	285 – j94.7	0.728	–6.1
4	227 – j120	0.708	–10.6
8	154 – j124	0.678	–18.7
16	89.9 – j95.4	0.611	–33.0
30	60.4 – j60.6	0.420	–41.3
60	54.8 – j35.8	0.489	–51.5
100	43.6 – j24.4	0.261	–89.9
200	37.9 – j17.3	0.235	–113
400	31.8 – j12.4	0.266	–137
800	23.6 – j8.2	0.374	–156
1000	19.8 – j5.5	0.437	–165
1250	16.0 – j1.8	0.515	–175
1500	13.6 + j2.4	0.574	174
1800	12.1 + j7.3	0.618	162

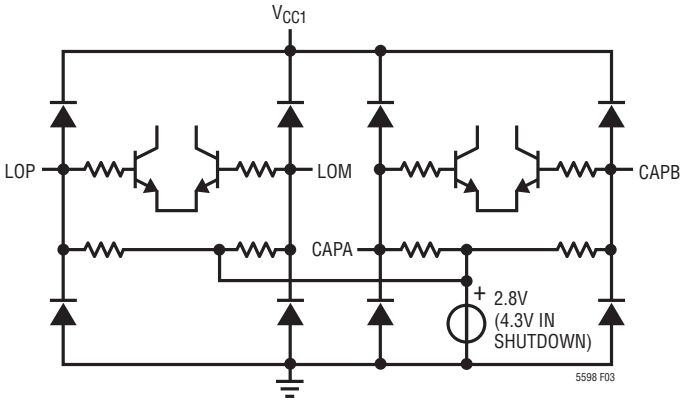


Figure 3. Simplified Circuit Schematic for the LOP, LOM, CAPA and CAPB Inputs.

APPLICATIONS INFORMATION

Table 3. LOP Port Input Impedance vs Frequency for EN = Low and P_{LO} = 0dBm (LOM AC Coupled with 50Ω to Ground).

FREQUENCY (MHz)	LO INPUT IMPEDANCE	REFLECTION COEFFICIENT	
		MAG	ANGLE
0.1	1376 – j84.4	0.930	–0.3
1	541 – j1593	0.980	–3.2
2	177 – j877	0.977	–6.2
4	75.3 – j452	0.965	–12.2
8	49.2 – j228	0.918	–23.6
16	43.3 – j117	0.784	–41.8
30	40.7 – j64.1	0.585	–62.7
60	39.1 – j34.6	0.382	–86
100	37.6 – j23.8	0.296	–102
200	33.4 – j16.4	0.275	–124
400	27.5 – j11.1	0.320	–145
800	20.1 – j4.9	0.430	–167
1000	17.5 – j1.6	0.479	–176
1250	15.3 + j2.1	0.532	175
1500	13.8 + j5.6	0.571	167
1800	12.8 + j9.7	0.605	157

Table 4. LOP Port Input Impedance vs Frequency for EN = High and P_{LO} = 10dBm (LOM AC Coupled with 50Ω to Ground).

FREQUENCY (MHz)	LO INPUT IMPEDANCE	REFLECTION COEFFICIENT	
		MAG	ANGLE
0.1	360-j14.8	0.756	–0.7
1	349-j70.5	0.758	–3.2
2	311-j113	0.752	–6.0
4	240-j148	0.739	–10.9
8	148-j146	0.715	–19.7
16	81.3-j102	0.641	–35.2
30	55.4-j61.6	0.506	–54.7
60	45.7-j34.4	0.341	–77.4
100	43.0-j24.1	0.261	–91.6
200	38.0-j17.1	0.234	–114
400	32.0-j12.5	0.265	–137
800	23.6-j8.3	0.374	–156
1000	19.8-j5.6	0.438	–165
1250	15.8-j1.7	0.520	–176
1500	13.5+j2.4	0.575	174
1800	12.0+j7.3	0.619	162

Table 5. LOP Port Input Impedance vs Frequency for EN = Low and P_{LO} = 10dBm (LOM AC Coupled with 50Ω to Ground).

FREQUENCY (MHz)	LO INPUT IMPEDANCE	REFLECTION COEFFICIENT	
		MAG	ANGLE
0.1	454 – j30.5	0.802	–0.9
1	423 – j102	0.780	–3.2
2	365 – j165	0.796	–5.9
4	249 – j219	0.798	–11.4
8	117 – j179	0.781	–22.4
16	60.7 – j106	0.697	–40.3
30	43.1 – j62.0	0.559	–62.4
60	38.6 – j34.6	0.386	–86.7
100	37.6 – j23.9	0.297	–102
200	33.5 – j16.5	0.274	–124
400	27.6 – j11.3	0.319	–145
800	20.2 – j5.1	0.429	–166
1000	17.7 – j1.7	0.478	–175
1250	15.2 + j2.0	0.533	175
1500	13.9 + j5.4	0.570	167
1800	12.9 + j9.5	0.604	158

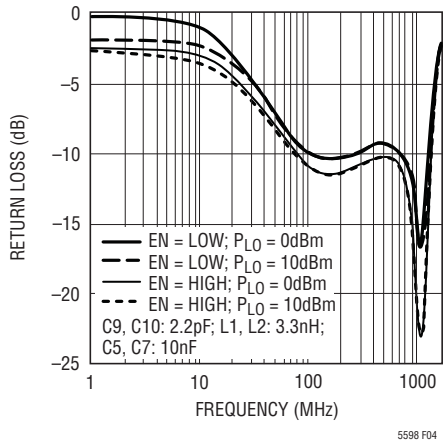


Figure 4. LOP Port Return Loss vs Frequency for Standard Board (See Figure 10)

APPLICATIONS INFORMATION

The LOP port return loss for the low end of the operating frequency range can be optimized using extra 120Ω terminations at the LO inputs (replace C9 and C10 with 120Ω resistors, see Figure 10), and is shown in Figure 5.

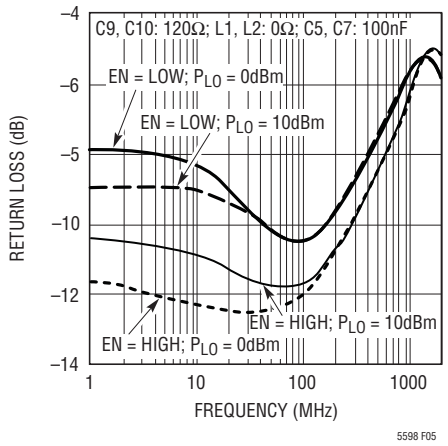


Figure 5. LO Port Return Loss vs Frequency Optimized for Low Frequency (See Figure 10)

The LOP port return loss for the high end of the operating frequency range can be optimized using slightly different values for C9, C10 and L1, L2 (see Figure 6).

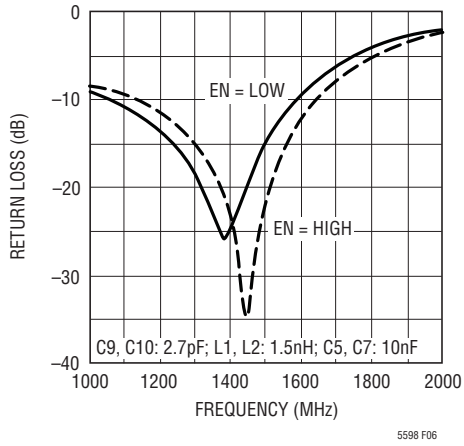


Figure 6. LO Port Return Loss vs Frequency Optimized for High Frequency (See Figure 10)

The third-harmonic rejection on the applied LO signal is recommended to be equal or better than the desired image rejection performance since third-harmonic LO content can degrade the image rejection severely. Image rejection is not sensitive to second-harmonic LO content.

The large-signal noise figure can be improved with a higher LO input power. However, if the LO input power is too large and causes internal clipping in the phase shifter section, the image rejection can be degraded rapidly. This clipping point depends on the supply voltage, LO frequency, temperature and single-ended vs differential LO drive. At f_{LO} = 140MHz, V_{CC} = 5V, T = 25°C and single-ended LO drive, this clipping point is at about 16.6dBm. For 4.5V it lowers to 14.6dBm. For differential drive with V_{CC} = 5V it is about 20dBm.

The differential LO port input impedance for EN = High and P_{LO} = 10dBm is given in Table 6.

Table 6. LOP - LOM Port Differential Input Impedance vs Frequency for EN = High and P_{LO} = 10dBm

FREQUENCY (MHz)	LO DIFFERENTIAL INPUT IMPEDANCE
0.1	642 – j25.7
1.0	626 – j112
2.0	572 – j204
4.0	429 – j305
8.0	222 – j287
16	102 – j181
30	64.2 – j104
60	50.9 – j58.9
100	46.2 – j40.2
200	37.4 – j28.6
400	28.3 – j19.4
800	20.0 – j10.6
1000	17.5 – j7.9
1250	16.6 – j2.7
1500	17.3 + j3.3
1800	20.6 + j10.2

RF Section

After upconversion, the RF outputs of the I and Q mixers are combined. An on-chip buffer performs internal differential to single-ended conversion, while transforming the output impedance to 50Ω. Table 7 shows the RF port output impedance vs frequency for EN = High.

APPLICATIONS INFORMATION

Table 7. RF Output Impedance vs Frequency for EN = High

FREQUENCY (MHz)	RF OUTPUT IMPEDANCE	REFLECTION COEFFICIENT	
		MAG	ANGLE
0.1	59.0 – j0.6	0.083	–3.6
1	58.5 – j2.1	0.081	–12.7
2	57.3 – j3.5	0.076	–23.6
4	54.6 – j4.5	0.061	–41.6
8	51.9 – j3.6	0.040	–60.8
16	50.5 – j2.1	0.022	–74.8
30	50.2 – j1.1	0.011	–80
60	50 – j0.5	0.005	–86.5
100	50 – j0.2	0.002	–84.9
200	49.7 + j0	0.003	177.4
400	48.9 + j0.3	0.011	162
800	46.1 + j0.4	0.041	173.3
1000	44.5 + j0.2	0.058	178
1250	42.8 + j0	0.077	–179.7
1500	41.2 – j0.1	0.097	–179.4
1800	39.9 + j0.4	0.113	177.4

The RF port output impedance for EN = Low is given in Table 8. It is roughly equivalent to a 1.3pF capacitor to ground.

Table 8. RF Output Impedance vs Frequency for EN = Low

FREQUENCY (MHz)	LO INPUT IMPEDANCE	REFLECTION COEFFICIENT	
		MAG	ANGLE
100	82.3 – j1223	0.995	–4.6
200	51.1 – j618	0.987	–9.2
400	35.3 – j310	0.965	–18.1
800	24.4 – j148	0.906	–36.6
1000	20.4 – j114	0.878	–46.4
1250	17 – j87	0.847	–58.4
1500	14.7 – j68	0.818	–70.7
1800	13.1 – j54	0.785	–84.3

In Figure 7 the simplified circuit schematic of the RF output buffer is drawn. A plot of the RF port return loss vs frequency is drawn in Figure 8 for EN = High and Low.

Enable Interface

Figure 9 shows a simplified schematic of the EN pin interface. The voltage necessary to turn on the LTC5598 is 2V. To disable (shut down) the chip, the enable voltage must be below 1V. If the EN pin is not connected, the chip is enabled. This EN = High condition is assured by the 125k on-chip pull-up resistor. It is important that the voltage at the EN pin does not exceed V_{CC} by more than 0.3V. Should

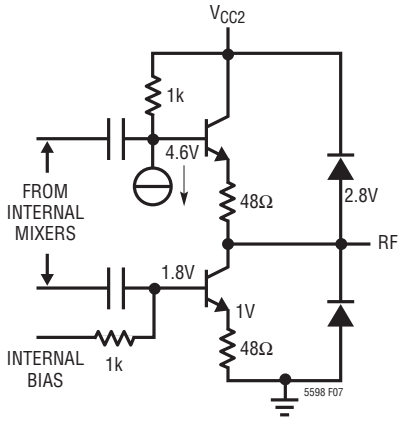


Figure 7. Simplified Circuit Schematic of the RF Output

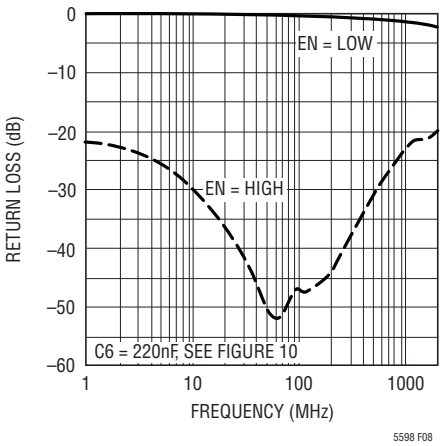


Figure 8. RF Port Return Loss vs Frequency

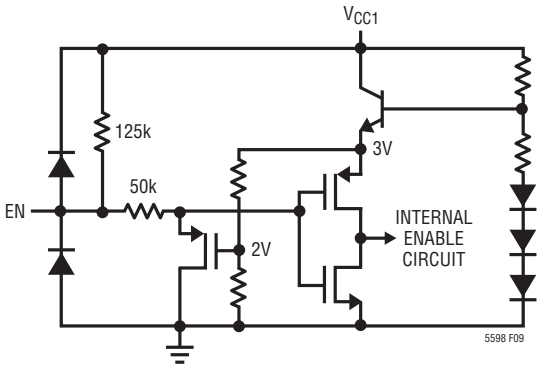


Figure 9: EN Pin Interface

APPLICATIONS INFORMATION

this occur, the supply current could be sourced through the EN pin ESD protection diodes, which are not designed to carry the full supply current, and damage may result.

Evaluation Board

Figure 10 shows the evaluation board schematic. A good ground connection is required for the exposed pad. If this is not done properly, the RF performance will degrade. Additionally, the exposed pad provides heat sinking for the part and minimizes the possibility of the chip overheating. Resistors R1 and R2 reduce the charging current in capacitors C1 and C4 (see Figure 10) and will reduce supply ringing during a fast power supply ramp-up in case an inductive cable is connected to the V_{CC} and GND turrets. For EN = High, the voltage drop over R1 and R2 is about 0.15V. If a power supply is used that ramps up slower than 10V/µs and limits the overshoot on the supply below 5.6V, R1 and R2 can be omitted.

The LTC5598 can be used for base-station applications with various modulation formats. Figure 13 shows a typical application.

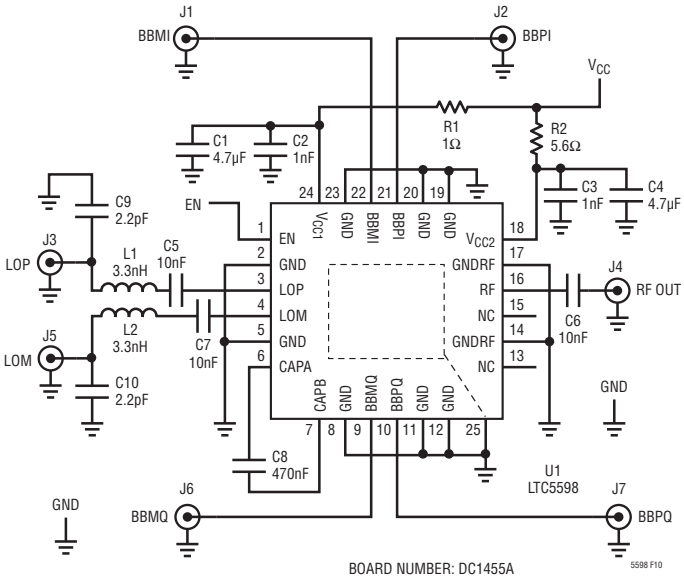


Figure 10. Evaluation Circuit Schematic

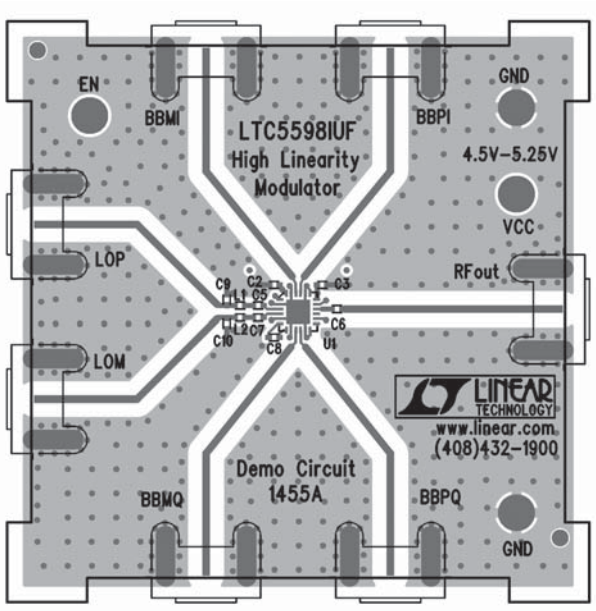


Figure 11. Component Side of Evaluation Board

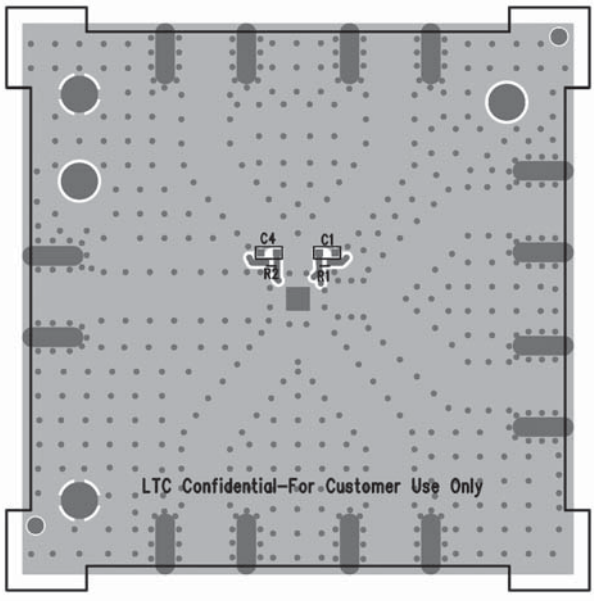


Figure 12. Bottom Side of Evaluation Board

APPLICATIONS INFORMATION

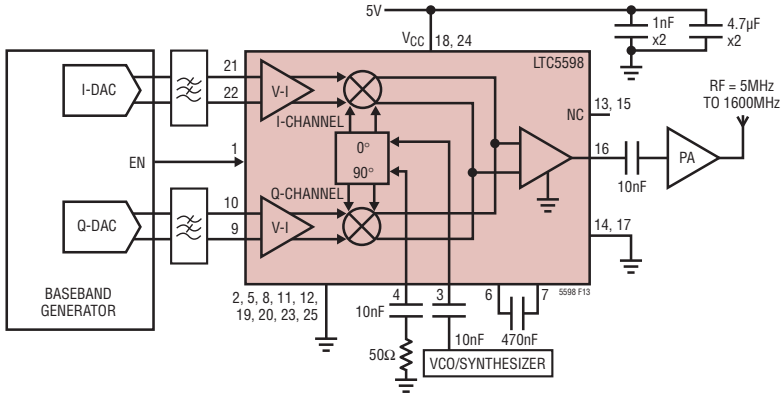
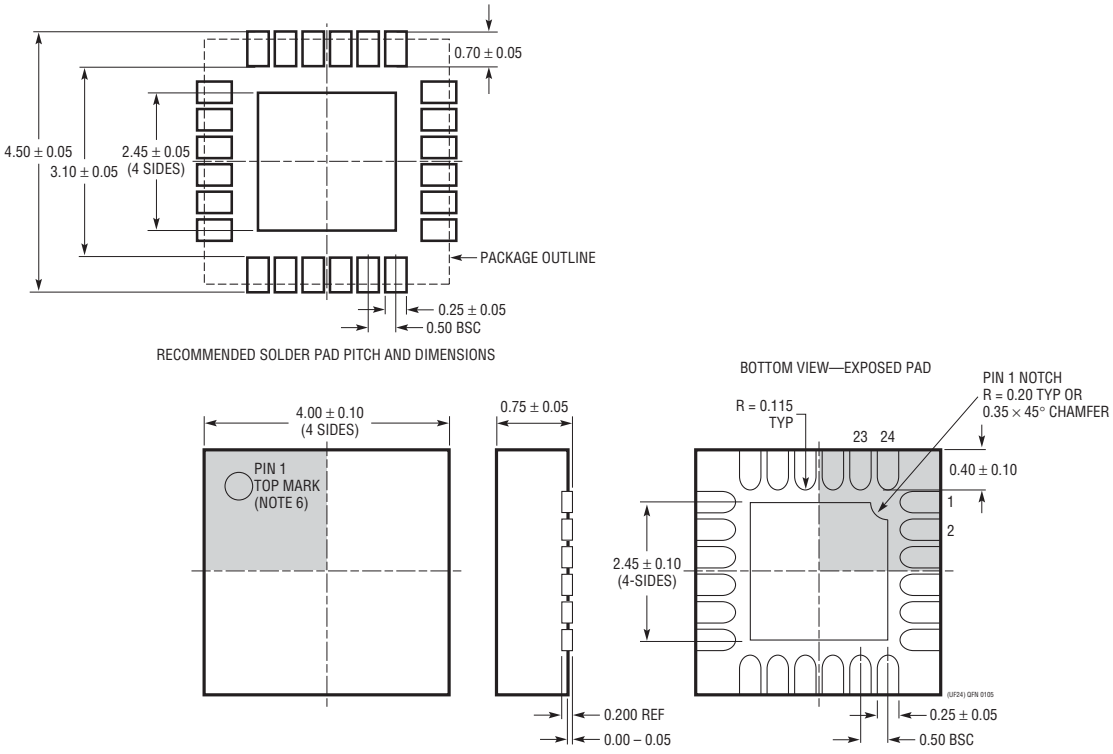


Figure 13: 5MHz to 1600MHz Direct Conversion Transmitter Application

PACKAGE DESCRIPTION

UF Package
24-Lead (4mm × 4mm) Plastic QFN
(Reference LTC DWG # 05-08-1697)



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Infrastructure		
LT5514	Ultralow Distortion, IF Amplifier/ADC Driver with Digitally Controlled Gain	850MHz Bandwidth, 47dBm OIP3 at 100MHz, 10.5dB to 33dB Gain Control Range
LT5517	40MHz to 900MHz Quadrature Demodulator	21dBm IIP3, Integrated LO Quadrature Generator
LT5518	1.5GHz to 2.4GHz High Linearity Direct Quadrature Modulator	22.8dBm OIP3 at 2GHz, –158.2dBm/Hz Noise Floor, 50Ω Single-Ended RF and LO Ports, 4-Channel W-CDMA ACPR = –64dBc at 2.14GHz
LT5519	0.7GHz to 1.4GHz High Linearity Upconverting Mixer	17.1dBm IIP3 at 1GHz, Integrated RF Output Transformer with 50Ω Matching, Single-Ended LO and RF Ports Operation
LT5520	1.3GHz to 2.3GHz High Linearity Upconverting Mixer	15.9dBm IIP3 at 1.9GHz, Integrated RF Output Transformer with 50Ω Matching, Single-Ended LO and RF Ports Operation
LT5521	10MHz to 3700MHz High Linearity Upconverting Mixer	24.2dBm IIP3 at 1.95GHz, NF = 12.5dB, 3.15V to 5.25V Supply, Single-Ended LO Port Operation
LT5522	600MHz to 2.7GHz High Signal Level Downconverting Mixer	4.5V to 5.25V Supply, 25dBm IIP3 at 900MHz, NF = 12.5dB, 50Ω Single-Ended RF and LO Ports
LT5527	400MHz to 3.7GHz High Signal Level Downconverting Mixer	IIP3 = 23.5dBm and NF = 12.5dBm at 1900MHz, 4.5V to 5.25V Supply, I_{CC} = 78mA, Conversion Gain = 2dB.
LT5528	1.5GHz to 2.4GHz High Linearity Direct Quadrature Modulator	21.8dBm OIP3 at 2GHz, –159.3dBm/Hz Noise Floor, 50Ω, 0.5V_{DC} Baseband Interface, 4-Channel W-CDMA ACPR = –66dBc at 2.14GHz
LT5554	Broadband Ultra Low Distortion 7-Bit Digitally Controlled VGA	48dBm OIP3 at 200MHz, 1.4nV/$\sqrt{Hz}$ Input-Referred Noise, 2dB to 18dB Gain Range, 0.125dB Gain Step Size
LT5557	400MHz to 3.8GHz High Signal Level Downconverting Mixer	IIP3 = 23.7dBm at 2600MHz, 23.5dBm at 3600MHz, I_{CC} = 82mA at 3.3V
LT5560	Ultra-Low Power Active Mixer	10mA Supply Current, 10dBm IIP3, 10dB NF, Usable as Up- or Down-Converter.
LT5568	700MHz to 1050MHz High Linearity Direct Quadrature Modulator	22.9dBm OIP3 at 850MHz, –160.3dBm/Hz Noise Floor, 50Ω, 0.5V_{DC} Baseband Interface, 3-Ch CDMA2000 ACPR = –71.4dBc at 850MHz
LT5571	620MHz - 1100MHz High Linearity Quadrature Modulator	21.7dBm OIP3 at 900MHz, –159dBm/Hz Noise Floor, High-Ohmic 0.5V_{DC} Baseband Interface
LT5572	1.5GHz to 2.5GHz High Linearity Direct Quadrature Modulator	21.6dBm OIP3 at 2GHz, –158.6dBm/Hz Noise Floor, High-Ohmic 0.5V_{DC} Baseband Interface, 4-Ch W-CDMA ACPR = –67.7dBc at 2.14GHz
LT5575	800MHz to 2.7GHz High Linearity Direct Conversion I/Q Demodulator	50Ω, Single-Ended RF and LO Ports, 28dBm IIP3 at 900MHz, 13.2dBm P1dB, 0.04dB I/Q Gain Mismatch, 0.4° I/Q Phase Mismatch
LT5579	1.5GHz to 3.8GHz High Linearity Upconverting Mixer	27.3dBm OIP3 at 2.14GHz, 9.9dB Noise Floor, 2.6dB Conversion Gain, –35dBm LO Leakage
RF Power Detectors		
LTC®5505	RF Power Detectors with >40dB Dynamic Range	300MHz to 3GHz, Temperature Compensated, 2.7V to 6V Supply
LTC5507	100kHz to 1000MHz RF Power Detector	100kHz to 1GHz, Temperature Compensated, 2.7V to 6V Supply
LTC5508	300MHz to 7GHz RF Power Detector	44dB Dynamic Range, Temperature Compensated, SC70 Package
LTC5509	300MHz to 3GHz RF Power Detector	36dB Dynamic Range, Low Power Consumption, SC70 Package
LTC5530	300MHz to 7GHz Precision RF Power Detector	Precision V_{OUT} Offset Control, Shutdown, Adjustable Gain
LTC5531	300MHz to 7GHz Precision RF Power Detector	Precision V_{OUT} Offset Control, Shutdown, Adjustable Offset
LTC5532	300MHz to 7GHz Precision RF Power Detector	Precision V_{OUT} Offset Control, Adjustable Gain and Offset
LT5534	50MHz to 3GHz Log RF Power Detector with 60dB Dynamic Range	±1dB Output Variation over Temperature, 38ns Response Time, Log Linear Response
LTC5536	Precision 600MHz to 7GHz RF Power Detector with Fast Comparator Output	25ns Response Time, Comparator Reference Input, Latch Enable Input, –26dBm to +12dBm Input Range
LT5537	Wide Dynamic Range Log RF/IF Detector	Low Frequency to 1GHz, 83dB Log Linear Dynamic Range
LT5538	3.8GHz Wide Dynamic Range Log Detector	75dB Dynamic Range, ±1dB Output Variation Over Temperature
LT5570	2.7GHz RMS Power Detector	Fast Responding, up to 60dB Dynamic Range, ±0.3dB Accuracy Over Temperature
LT5581	40dB Dynamic Range RMS Detector	10MHz to 6GHz, ±1dB Accuracy Over Temperature, 1.4mA at 3.3V Supply

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

LT 0509 • PRINTED IN USA

1.8GHz Low Noise, Low Distortion Differential ADC Driver for 300MHz IF

FEATURES

- 1.8GHz –3dB Bandwidth
- Fixed Gain of 10V/V (20dB)
- –94dBc IMD_3 at 70MHz (Equivalent OIP3 = 51dBm)
- –65dBc IMD_3 at 300MHz (Equivalent OIP3 = 36.5dBm)
- 1nV/√Hz Internal Op Amp Noise
- 2.1nV/√Hz Total Input Noise
- 6.2dB Noise Figure
- Differential Inputs and Outputs
- 200Ω Input Impedance
- 2.85V to 3.5V Supply Voltage
- 90mA Supply Current (270mW)
- 1V to 1.6V Output Common Mode Voltage, Adjustable
- DC- or AC-Coupled Operation
- Max Differential Output Swing $4.4V_{P-P}$
- Small 16-Lead 3mm × 3mm × 0.75mm QFN Package

APPLICATIONS

- Differential ADC Driver
- Differential Driver/Receiver
- Single Ended to Differential Conversion
- IF Sampling Receivers
- SAW Filter Interfacing

DESCRIPTION

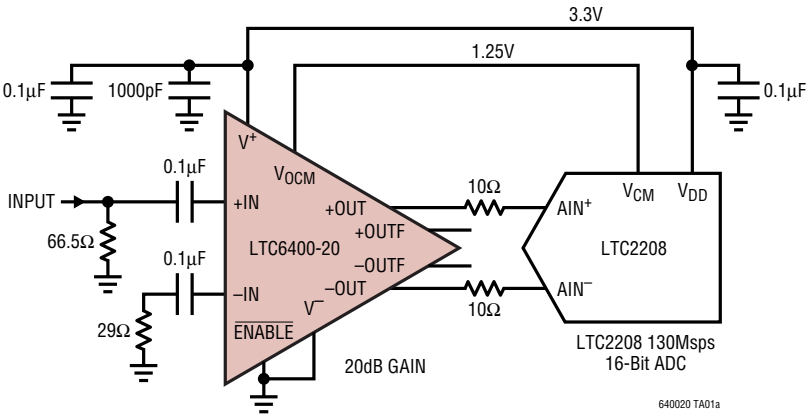
The LTC®6400-20 is a high-speed differential amplifier targeted at processing signals from DC to 300MHz. The part has been specifically designed to drive 12-, 14- and 16-bit ADCs with low noise and low distortion, but can also be used as a general-purpose broadband gain block.

The LTC6400-20 is easy to use, with minimal support circuitry required. The output common mode voltage is set using an external pin, independent of the inputs, which eliminates the need for transformers or AC-coupling capacitors in many applications. The gain is internally fixed at 20dB (10V/V).

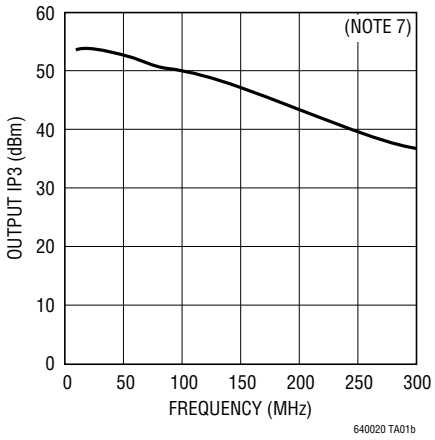
The LTC6400-20 saves space and power compared to alternative solutions using IF gain blocks and transformers. The LTC6400-20 is packaged in a compact 16-lead 3mm × 3mm QFN package and operates over the –40°C to 85°C temperature range.

TYPICAL APPLICATION

Single-Ended to Differential ADC Driver



Equivalent Output IP3 vs Frequency

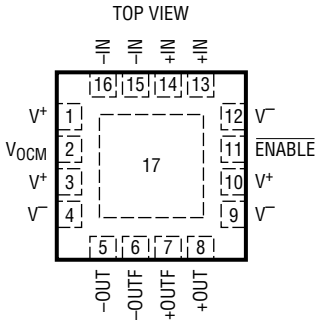


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage ($V^+ – V^–$).....3.6V
Input Current (Note 2).....±10mA
Operating Temperature Range
(Note 3) ..... –40°C to 85°C
Specified Temperature Range
(Note 4) ..... –40°C to 85°C
Storage Temperature Range..... –65°C to 150°C
Maximum Junction Temperature ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 68°C/W, θ_{JC} = 4.2°C/W
EXPOSED PAD (PIN 17) IS $V^–$, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6400CUD-20#PBF	LTC6400CUD-20#TRPBF	LCCS	16-Lead (3mm × 3mm) Plastic QFN	0°C to 70°C
LTC6400IUD-20#PBF	LTC6400IUD-20#TRPBF	LCCS	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

LTC6400 AND LTC6401 SELECTOR GUIDE

Please check each datasheet for complete details.

PART NUMBER	GAIN (dB)	GAIN (V/V)	Z_{IN} (DIFFERENTIAL) (Ω)	I_S (mA)
LTC6400-20	20	10	200	90
LTC6401-20	20	10	200	50

In addition to the LTC6400 family of amplifiers, a lower power LTC6401 family is available. The LTC6401 is pin compatible to the LTC6400, and has the same low noise performance. The lower power consumption of the LTC6401 comes at the expense of slightly higher non-linearity, especially at input frequencies above 140MHz. Please refer to the separate LTC6401 data sheets for complete details. Other gain versions from 8dB to 26dB will follow.

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, +IN = –IN = V_{OCM} = 1.25V, $\overline{ENABLE}$ = 0V, No R_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input/Output Characteristic							
G_{DIFF}	Gain	V_{IN} = ±100mV Differential	●	19.4	20	20.6	dB
TC_{GAIN}	Gain Temperature Drift	V_{IN} = ±100mV Differential	●		–1.5		mdB/°C
$V_{SWINGMIN}$	Output Swing Low	Each Output, V_{IN} = ±600mV Differential	●		80	150	mV
$V_{SWINGMAX}$	Output Swing High	Each Output, V_{IN} = ±600mV Differential	●	2.35	2.46		V
$V_{OUTDIFFMAX}$	Maximum Differential Output Swing	1dB Compressed	●		4.4		V_{P-P}
I_{OUT}	Output Current Drive	Each Output	●	20			mA
V_{OSDIFF}	Input Differential Offset Voltage		●	–2		2	mV
TCV_{OSDIFF}	Input Differential Offset Voltage Drift	T_{MIN} to T_{MAX}	●		1.2		µV/°C
I_{VRMIN}	Input Common Mode Voltage Range, MIN					1	V
I_{VRMAX}	Input Common Mode Voltage Range, MAX			1.6			V
R_{INDIFF}	Input Resistance (+IN, –IN)	Differential	●	170	200	230	Ω
C_{INDIFF}	Input Capacitance (+IN, –IN)	Differential, Includes Parasitic			1		pF
$R_{OUTDIFF}$	Output Resistance (+OUT, –OUT)	Differential	●	18	25	32	Ω
$R_{OUTFDIFF}$	Filtered Output Resistance (+OUTF, –OUTF)	Differential	●	85	100	115	Ω
$C_{OUTFDIFF}$	Filtered Output Capacitance (+OUTF, –OUTF)	Differential, Includes Parasitic			2.7		pF
CMRR	Common Mode Rejection Ratio	Input Common Mode Voltage 1.1V~1.4V	●	45	65		dB
Output Common Mode Voltage Control							
G_{CM}	Common Mode Gain	V_{OCM} = 1V to 1.6V			1		V/V
V_{OCMMIN}	Output Common Mode Range, MIN		 ●			1 1.1	V V
V_{OCMMAX}	Output Common Mode Range, MAX		 ●	1.6 1.5			V V
V_{OSCM}	Common Mode Offset Voltage	V_{OCM} = 1.1V to 1.5V	●	–15		15	mV
TCV_{OSCM}	Common Mode Offset Voltage Drift	T_{MIN} to T_{MAX}	●		16		µV/°C
IV_{OCM}	V_{OCM} Input Current		●		5	15	µA
$\overline{ENABLE}$ Pin							
V_{IL}	$\overline{ENABLE}$ Input Low Voltage		●			0.8	V
V_{IH}	$\overline{ENABLE}$ Input High Voltage		●	2.4			V
I_{IL}	$\overline{ENABLE}$ Input Low Current	$\overline{ENABLE}$ = 0.8V	●			0.5	µA
I_{IH}	$\overline{ENABLE}$ Input High Current	$\overline{ENABLE}$ = 2.4V	●		1.2	3	µA
Power Supply							
V_S	Operating Supply Range		●	2.85	3	3.5	V
I_S	Supply Current	$\overline{ENABLE}$ = 0.8V	●	75	90	105	mA
I_{SHDN}	Shutdown Supply Current	$\overline{ENABLE}$ = 2.4V	●		1	3	mA
PSRR	Power Supply Rejection Ratio (Differential Outputs)	V^+ = 2.85V to 3.5V	●	55	86		dB

AC ELECTRICAL CHARACTERISTICS

Specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, V_{OCM} = 1.25V, $\overline{ENABLE}$ = 0V, No R_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
–3dBBW	–3dB Bandwidth	200mV$_{P-P,OUT}$ (Note 6)		1.84		GHz
0.1dBBW	Bandwidth for 0.1dB Flatness	200mV$_{P-P,OUT}$ (Note 6)		0.3		GHz
0.5dBBW	Bandwidth for 0.5dB Flatness	200mV$_{P-P,OUT}$ (Note 6)		0.7		GHz
1/f	1/f Noise Corner			10.5		kHz
SR	Slew Rate	Differential (Note 6)		4.5		V/ns
$t_{S1\%}$	1% Settling Time	2V$_{P-P,OUT}$ (Note 6)		0.8		ns
t_{OVDR}	Overdrive Recovery Time	1.9V$_{P-P,OUT}$ (Note 6)		4		ns
t_{ON}	Turn-On Time	+OUT, –OUT Within 10% of Final Values		82		ns
t_{OFF}	Turn-Off Time	I_{CC} Falls to 10% of Nominal		190		ns
–3dBBW$_{VOCM}$	V_{OCM} Pin Small Signal –3dB BW	0.1V$_{P-P}$ at V_{OCM}, Measured Single-Ended at Output (Note 6)		15		MHz
10MHz Input Signal						
$HD_{2,10M}/HD_{3,10M}$	Second/Third Order Harmonic Distortion	2V$_{P-P,OUT}$, R_L = 400Ω		–97/–93		dBc
		2V$_{P-P,OUT}$, No R_L		–98/–97		dBc
		2V$_{P-P,OUTFILT}$, No R_L		–100/–98		dBc
$IMD_{3,10M}$	Third-Order Intermodulation (f1 = 9.5MHz f2 = 10.5MHz)	2V$_{P-P,OUT}$ Composite, R_L = 400Ω		–95		dBc
		2V$_{P-P,OUT}$ Composite, No R_L		–99		dBc
		2V$_{P-P,OUTFILT}$ Composite, No R_L		–100		dBc
$OIP_{3,10M}$	Third-Order Output Intercept Point (f1 = 9.5MHz f2 = 10.5MHz)	2V$_{P-P,OUT}$ Composite, No R_L (Note 7)		53.8		dBm
$P_{1dB,10M}$	1dB Compression Point	R_L = 375Ω (Notes 5, 7)		18		dBm
NF_{10M}	Noise Figure	R_L = 375Ω (Note 5)		6.2		dB
$e_{IN,10M}$	Input Referred Voltage Noise Density	Includes Resistors (Short Inputs)		2.2		nV/√Hz
$e_{ON,10M}$	Output Referred Voltage Noise Density	Includes Resistors (Short Inputs)		21.7		nV/√Hz
70MHz Input Signal						
$HD_{2,70M}/HD_{3,70M}$	Second/Third Order Harmonic Distortion	2V$_{P-P,OUT}$, R_L = 400Ω		–86/–85		dBc
		2V$_{P-P,OUT}$, No R_L		–88/–87		dBc
		2V$_{P-P,OUTFILT}$, No R_L		–86/–88		dBc
$IMD_{3,70M}$	Third-Order Intermodulation (f1 = 69.5MHz f2 = 70.5MHz)	2V$_{P-P,OUT}$ Composite, R_L = 400Ω		–93		dBc
		2V$_{P-P,OUT}$ Composite, No R_L		–94		dBc
		2V$_{P-P,OUTFILT}$ Composite, No R_L		–93		dBc
$OIP_{3,70M}$	Third-Order Output Intercept Point (f1 = 69.5MHz f2 = 70.5MHz)	2V$_{P-P,OUT}$ Composite, No R_L (Note 7)		51		dBm
$P_{1dB,70M}$	1dB Compression Point	R_L = 375Ω (Notes 5, 7)		18		dBm
NF_{70M}	Noise Figure	R_L = 375Ω (Note 5)		6.2		dB
$e_{IN,70M}$	Input Referred Voltage Noise Density	Includes Resistors (Short Inputs)		2.1		nV/√Hz
$e_{ON,70M}$	Output Referred Voltage Noise Density	Includes Resistors (Short Inputs)		21		nV/√Hz

AC ELECTRICAL CHARACTERISTICS

Specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, V_{OCM} = 1.25V, $\overline{ENABLE}$ = 0V, No R_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
140MHz Input Signal						
$HD_{2,140M}/HD_{3,140M}$	Second/Third Order Harmonic Distortion	$2V_{P-P,OUT}$, R_L = 400Ω		–74/–74		dBc
		$2V_{P-P,OUT}$, No R_L		–73/–83		dBc
		$2V_{P-P,OUTFILT}$, No R_L		–77/–76		dBc
$IMD_{3,140M}$	Third-Order Intermodulation (f1 = 139.5MHz f2 = 140.5MHz)	$2V_{P-P,OUT}$ Composite, R_L = 400Ω		–93		dBc
		$2V_{P-P,OUT}$ Composite, No R_L		–87		dBc
		$2V_{P-P,OUTFILT}$ Composite, No R_L		–89		dBc
$OIP_{3,140M}$	Third-Order Output Intercept Point (f1 = 139.5MHz f2 = 140.5MHz)	$2V_{P-P,OUT}$ Composite, No R_L (Notes 7)		47.7		dBm
$P_{1dB,140M}$	1dB Compression Point	R_L = 375Ω (Notes 5, 7)		18.4		dBm
NF_{140M}	Noise Figure	R_L = 375Ω (Note 5)		6.5		dB
$e_{IN,140M}$	Input Referred Voltage Noise Density	Includes Resistors (Short Inputs)		2.1		$nV/\sqrt{Hz}$
$e_{ON,140M}$	Output Referred Voltage Noise Density	Includes Resistors (Short Inputs)		21.5		$nV/\sqrt{Hz}$
240MHz Input Signal						
$HD_{2,240M}/HD_{3,240M}$	Second-Order Harmonic Distortion	$2V_{P-P,OUT}$, R_L = 400Ω		–66/–58		dBc
		$2V_{P-P,OUT}$, No R_L		–65/–63		dBc
		$2V_{P-P,OUTFILT}$, No R_L		–65/–58		dBc
$IMD_{3,240M}$	Third-Order Intermodulation (f1 = 239.5MHz f2 = 240.5MHz)	$2V_{P-P,OUT}$ Composite, R_L = 400Ω		–71		dBc
		$2V_{P-P,OUT}$ Composite, No R_L		–74		dBc
		$2V_{P-P,OUTFILT}$ Composite, No R_L		–67		dBc
$OIP_{3,240M}$	Third-Order Output Intercept Point (f1 = 239.5MHz f2 = 240.5MHz)	$2V_{P-P,OUT}$ Composite, No R_L (Note 7)		41		dBm
$P_{1dB,240M}$	1dB Compression Point	R_L = 375Ω (Notes 5, 7)		17.9		dBm
NF_{240M}	Noise Figure	R_L = 375Ω (Note 5)		7.1		dB
$e_{N,\ 240M}$	Input Referred Voltage Noise Density	Includes Resistors (Short Inputs)		1.9		$nV/\sqrt{Hz}$
$e_{ON,240M}$	Output Referred Voltage Noise Density	Includes Resistors (Short Inputs)		21.7		$nV/\sqrt{Hz}$

AC ELECTRICAL CHARACTERISTICS

Specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, V_{OCM} = 1.25V, $\overline{ENABLE}$ = 0V, No R_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
300MHz Input Signal						
$HD_{2,300M}/HD_{3,300M}$	Second-Order Harmonic Distortion	$2V_{P-P,OUT}$, R_L = 400Ω		–61/–53		dBc
		$2V_{P-P,OUT}$, No R_L		–60/–55		dBc
		$2V_{P-P,OUTFILT}$, No R_L		–63/–46		dBc
$IMD_{3,300M}$	Third-Order Intermodulation (f1 = 299.5MHz f2 = 300.5MHz)	$2V_{P-P,OUT}$ Composite, R_L = 400Ω		–64		dBc
		$2V_{P-P,OUT}$ Composite, No R_L		–65		dBc
		$2V_{P-P,OUTFILT}$ Composite, No R_L		–58		dBc
$OIP_{3,300M}$	Third-Order Output Intercept Point (f1 = 299.5MHz f2 = 300.5MHz)	$2V_{P-P,OUT}$ Composite, No R_L (Note 7)		36.6		dBm
$P_{1dB,300M}$	1dB Compression Point	R_L = 375Ω (Notes 5, 7)		17.5		dBm
NF_{300M}	Noise Figure	R_L = 375Ω (Note 5)		7.5		dB
$e_{N,300M}$	Input Referred Voltage Noise Density	Includes Resistors (Short Inputs)		1.8		$nV/\sqrt{Hz}$
$e_{ON,300M}$	Output Referred Voltage Noise Density	Includes Resistors (Short Inputs)		22		$nV/\sqrt{Hz}$
$IMD_{3,280M/320M}$	Third-Order Intermodulation (f1 = 280MHz f2 = 320MHz) Measure at 360MHz	$2V_{P-P,OUT}$ Composite, R_L = 375Ω	–64	–70		dBc

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Input pins (+IN, –IN) are protected by steering diodes to either supply. If the inputs go beyond either supply rail, the input current should be limited to less than 10mA.

Note 3: The LTC6400C and LTC6400I are guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 4: The LTC6400C is guaranteed to meet specified performance from 0°C to 70°C. It is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LTC6400I is guaranteed to meet specified performance from –40°C to 85°C.

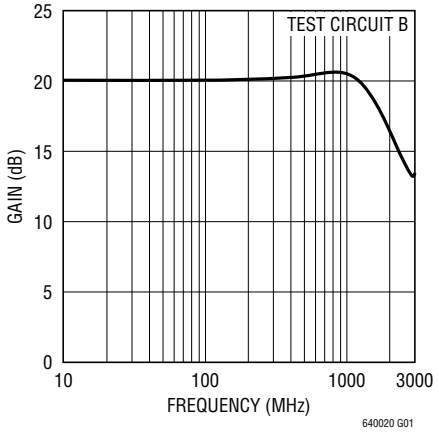
Note 5: Input and output baluns used. See Test Circuit A.

Note 6: Measured using Test Circuit B.

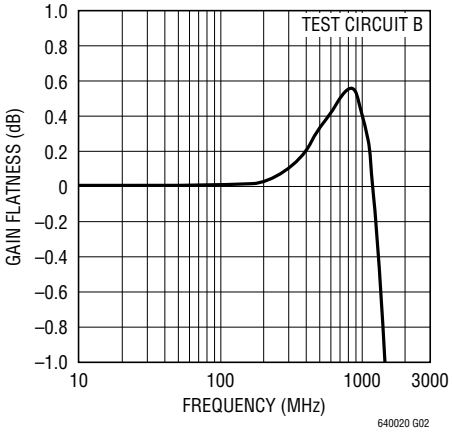
Note 7: Since the LTC6400-20 is a feedback amplifier with low output impedance, a resistive load is not required when driving an AD converter. Therefore, typical output power is very small. In order to compare the LTC6400-20 with amplifiers that require 50Ω output load, the LTC6400-20 output voltage swing driving a given R_L is converted to OIP_3 and P_{1dB} as if it were driving a 50Ω load. Using this modified convention, $2V_{P-P}$ is by definition equal to 10dBm, regardless of actual R_L.

TYPICAL PERFORMANCE CHARACTERISTICS

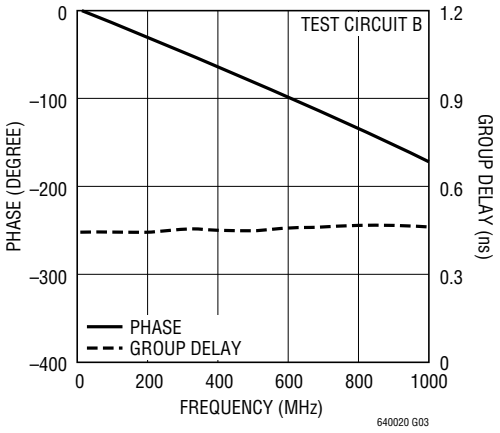
Frequency Response



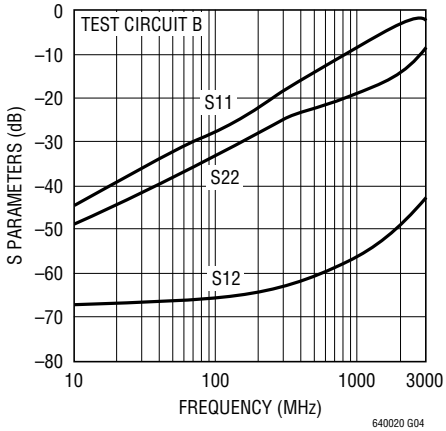
Gain 0.1dB Flatness



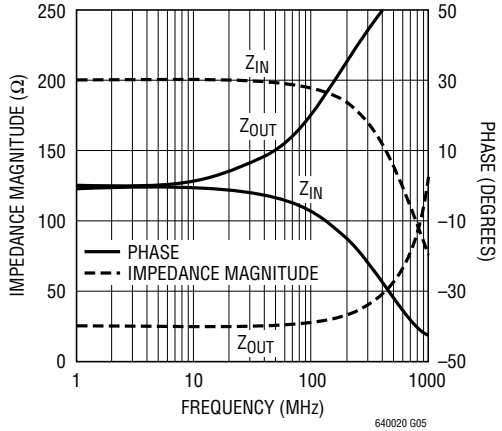
S21 Phase and Group Delay vs Frequency



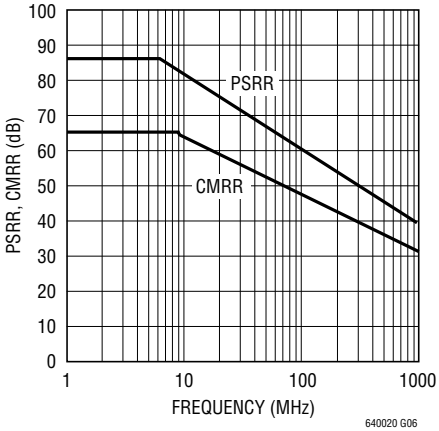
Input and Output Reflection and Reverse Isolation vs Frequency



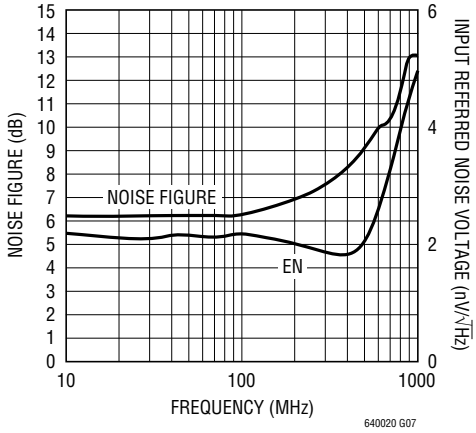
Input and Output Impedance vs Frequency



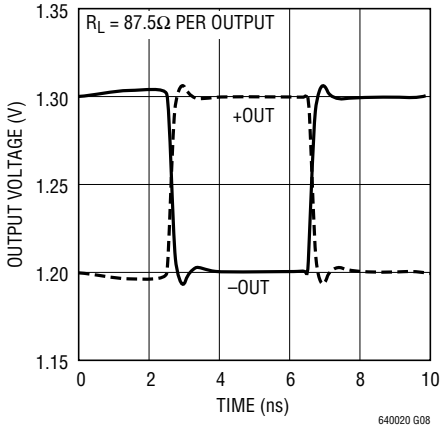
PSRR and CMRR vs Frequency



Noise Figure and Input Referred Noise Voltage vs Frequency



Small Signal Transient Response



Large Signal Transient Response