2.5 Theory of Operation

General Overview

The Link AX is a point to point Wireless ATM-25 Extender operating in the 5.3/5.7 GHz U-NII band as authorized in rule sections 15.401 through 15.407. The unit is enclosed in a weather proof outdoor enclosure and is intended to provide data links over distances up to 15 km. The radio in the unit operates full duplex, transmitting and receiving data at the rate of 8.192 Mbps. The radio is modulated using BPSK.

Circuit Description

The following circuit description is intended to explain the operation of the radio at the block diagram level. This text is written with the idea that the reader has the block diagram readily available, as it will aid in understanding the signal flow in the radio.

2.5.1 Link AX Transmitter

The physical interface to the radio consists of ATM-25 cells that are routed to ATM physical interface (PHY) chip. The PHY chip stores the data cells, and then converts them into a synchronous 8.448 Mbps data stream that is fed into the transmitter. To mark cell boundries, a SYNC byte (01111110) is inserted at the beginning of every cell. Zero insertion circuitry, inserts a zero after five consecutive ones, guaranteeing SYNC byte uniqueness while transmiting the cell's content.

The data is differentially encoded and scrambled before it is routed through the transmit baseband filter to provide spectral shaping. The baseband filter is a five pole low pass filter. After amplification, the baseband signal is fed to the modulator consisting of a doubly balanced mixer. The modulator is running directly at the transmitter frequency of 5.775 GHz $\pm$ 50 MHz. The local oscillator signal of the mixer is supplied from the frequency synthesizer section, with the frequency dependant on the RF channel selected.

From the output of the modulator, the signal is amplified and then passed through a 150 MHz wide bandpass filter to remove any local oscillator products from the output spectrum. After filtering, the signal is passed through a series of amplifier and attenuator stages that are used to control the output power level. With a combination of fixed and variable attenuation the output power can be set to one of four different levels to accommodate different antennas used with the product.

The power setting is maintained by an active ALC circuit that samples the transmitter output power and then adjusts the variable attenuator to keep the output power constant over the operating temperature of the unit. The power level is controlled to within +1/-2 dB of the set point.

Following the attenuators the signal is fed through additional amplification to bring the output level to a maximum of +14 dBm at the output of power amplifier. A lowpass matching section follows the power amplifier to aid in filtering harmonics of the signal. After passing through the duplexer, the power level at the antenna port is a maximum of +12 dBm.

Figure 2.2a - Outdoor Unit, Front View, External Antenna

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Figure 2.2b - Outdoor Unit, Back View, External Antenna

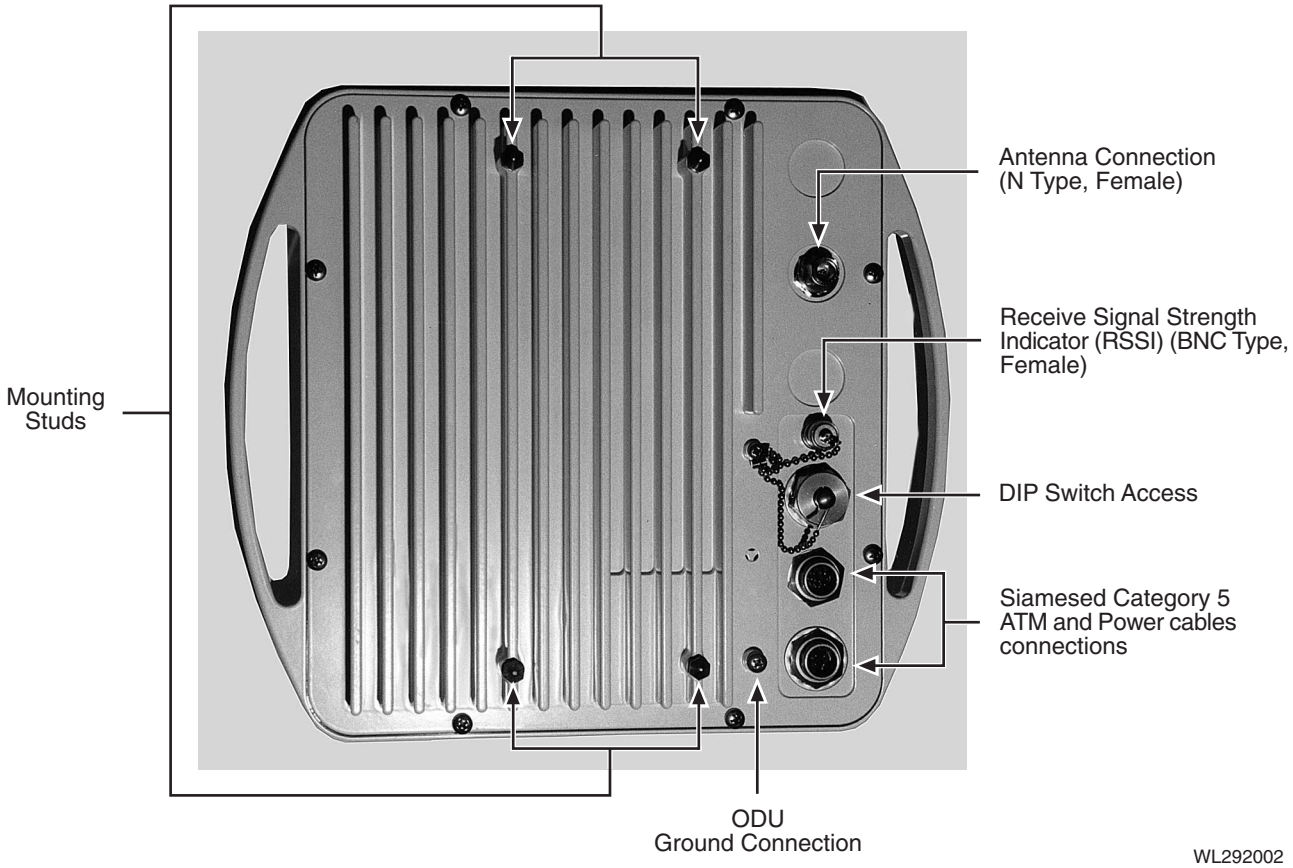

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Figure 2.2c - Outdoor Unit, Front View, Integral Antenna

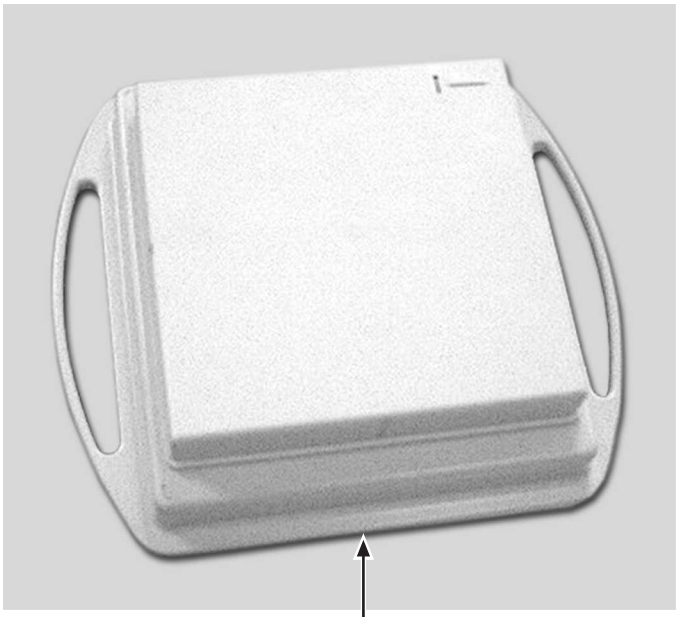
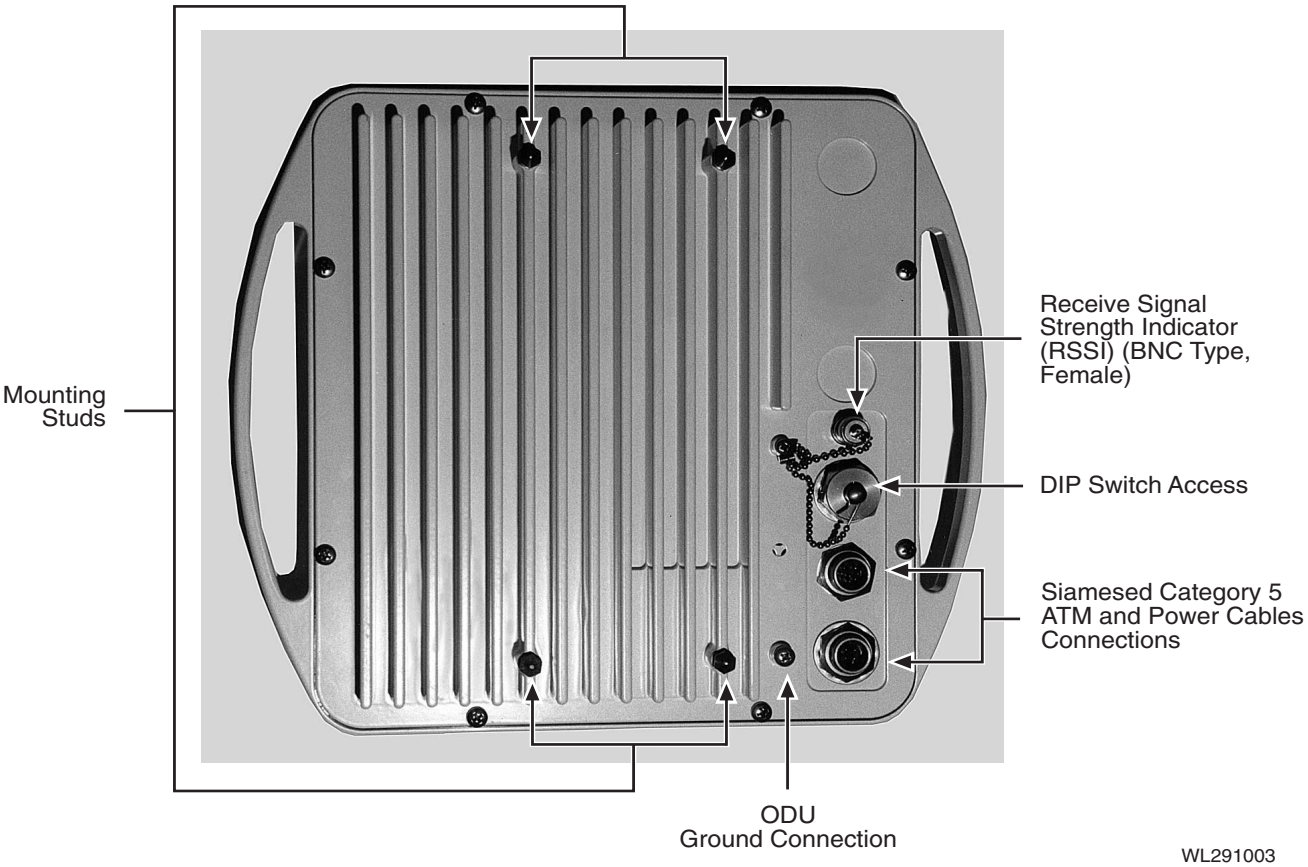


Figure 2.2d - Outdoor Unit, Back View, Integral Antenna



2.5.2 Link AX Receiver

The receiver in theLink AX is a conventional dual conversion design with IF frequencies of 474.88 MHz and 70 MHz.

From the receive port of the duplexer, the low level input signal is passed through a low noise preamplifier that provides 25 dB of gain. Following the preamplifier the signal is passed through a 200 MHz wide bandpass filter to provide image rejection for the first mixer.

The signal is then mixed with the first LO to convert the signal to 474.88 MHz. Following further amplification the signal is passed through a five pole, 20 MHz wide bandpass filter. This filter provides image filtering for the second mixer, and also helps attenuate signals on the adjacent receive channels. After filtering, the signal is further amplified and then passed through a variable attenuator stage before it is applied to the second mixer.

The output of the second mixer is at 70 MHz. The 70 MHz IF stages provide additional gain along with two sections of variable attenuation for the AGC function. The primary adjacent channel filtering is also at 70 MHz where the signal is passed through a 12 MHz wide SAW filter. The combination of filters provide a minimum of 47 dB of attenuation at the adjacent receive channels (±10.24 MHz).

At the end of the 70 MHz IF chain the signal is fed into a quadrature demodulator. The carrier recovery loop consists of a four quadrant multiplier that multiplies I and Q baseband signals to create an error voltage. This error voltage is then amplified and fed back to the 70 MHz VCO. This forms a phase locked loop that is locked to the received carrier frequency.

The 70 MHz output is also fed into a wide band logarithmic amplifier that provides a DC voltage output proportional to the 70 MHz signal strength. The DC voltage is then integrated and fed back to the variable attenuator stages to form an AGC control loop. This control loop keeps the signal level at the input to the demodulator chip constant over the entire operating range of the receiver.

Data recovery from the I baseband signal begins by passing the I signal through a slicer. The output of the slicer is a digital signal that contains both data and clocking information. A clock recovery circuit recovers receive timing information that is needed to clock the data through the descrambler, and differential decoder.

This 8.448 Mb bit stream is then converted into ATM cells. The SYNC bytes and the inserted zeros are stripped form the cells prior to their delivery to the ATM25 PHY. This method provides worst case cell rate of 15645 cells per second (cps) and typical cell rates of approximately 19200 cps.

2.5.3 Synthesizer

The FPGA provides four 22-bit streams in a serial format loaded to the synthesizer. This data provides all of the possible frequencies at which the system can operate. Depending upon the dip switch settings selected, the actual frequency being used is selected. When the reset button is pressed, the FPGA will reload this data to the synthesizer.

Frequency Synthesis

The local oscillator frequencies used in the Link AX are all synthesized from a 19.2 MHz, ± 2.5 PPM reference oscillator. The overall frequency stability of the radio is ± 2.5 PPM, directly reflecting the reference oscillator stability.

A dual frequency synthesizer chip is used to control both the first and second local oscillator loops. This chip supports one high frequency oscillator, up to 1.5 GHz, and one lower frequency oscillator to be used as a second LO.

The first local oscillator VCO operates at one half the transmitter output frequency, and changes with the transmit channel selected. The first LO consists of a bipolar VCO operating at 2.887 GHz ±25 MHz. The output of this VCO is buffered and then passed through a X2 prescaler chip before being fed back to the synthesizer chip. The phase comparison frequency for the first LO is 320 kHz.

After amplification the 2.887 GHz signal is passed through a frequency doubler to create the 5.775 GHz signal that is applied to the mixer stages.

The second local oscillator consists of a VCO that is phase locked to 404.88 MHz. This auxiliary synthesizer is operating with a phase comparison frequency of 240 kHz.

2.6 Indoor Unit

An optional Indoor Unit (IDU) can be used with the Link AX to provide diagnostics and troubleshooting aid to maintenance personnel. The IDU contains a single LED that illuminates with the presence of ATM25 data and power. Additionally a BNC connector is provided so that maintenance personnel can view RSSI voltage inside the building. The IDU is NOT required for operation of the Link AX radio system. Figure 2.3 shows the Link AX IDU.

Figure 2-3 Link AX Indoor Unit (IDU)