Annex A: Operational Description of Circuitry

RULE PART NUMBER: 2.1033 (c)(10)

1. PURPOSE

This report has been prepared to support the application for FCC Certification Per Code Of Federal Regulations, Title 47, Parts 2 And 90 for the MCUC5R radio-modem comprised of the JDT Model 242-3492-xxx Transceiver and Dataradio 210-3315-xxx Modem. The report presents necessary information concerning electrical circuit description, measured performance and physical construction and configuration. Also parts 4 and 5 present active circuit devices functions for Transceiver and, accordingly, for Modem.

2. DL-3492 TRANSCEIVER (JDT 242-3492-530)

The main components of the RF board include:

1. the RF exciter/power amplifier (transceiver section),
2. the Frequency Synthesizer/VCO, dual conversion superhetrodyne receiver, and a temperature compensated crystal oscillator as a frequency reference (Synthesizer/VCO section).
3. PSU

A block diagram of the transceiver is located at the end of this section.

2.1 Transceiver Circuit Description

The transmitter produces a nominal RF output power output of 5W at 13.3V DC. Frequency modulation of the transmit signal occurs in the synthesizer. Transmit audio processing circuitry is contained in the modem board.

Driver (Q500)

The VCO RF output signal is applied to R846, R847 and R848 that form a resistive splitter for the receive first local oscillator and the transmitter. The VCO signal is then applied to a 50 ohm pad formed by R500, R501, and R502. The RF signal is applied to Q500 which provides amplification and additional isolation between the VCO and transmitter. Biasing for this stage is provided by R503 and L500, C505 provides RF decoupling. The RF signal is then applied to the power amplifier module Q500.

Final (U510)

The RF signal from Q500 is applied to the input port of the RF power amplifier module, U510, which provides 5 watts (nominal) at the antenna connector J501. U510 operates on an input voltage from 10-16Vdc.

Power Control (U130C)

Power control is provided by U520, U130, Q520 and a stripline directional coupler. The power is adjust by Power Set Control R525 which provides a reference voltage to U130C. U130C drives Q520 and PA module U510. The stripline directional coupler is connected to a forward RF peak detector formed by R535, CR520, C531 and U520A. The other end of the stripline directional coupler is connected to a reverse RF peak detector formed by R593, CR592, C593 and U520B.

If the power output of U510 decreases due to temperature variations, etc., the forward peak detector voltage decreases. The detector voltage drop is buffered by U520A and applied to inverting amplifier U130C which increases the forward bias on Q520. The increased bias voltage on Q520 increases the

power output level of U510. If the power output of U510 increases, the forward peak detector voltage increases and U130C decreases the forward bias on Q520. The decreased bias voltage on Q520 decreases the output power of U510. The output of CR520 and CR592 are applied to U520. If the output of either buffer increases, the increase is applied to the inverting input of U130C. The output of U130C then decreases and Q520 decreases the input voltage to U510 to lower the power. The control voltage is isolated from RF by ferrite bead EP513 and C513 decouples RF. The forward/reverse power voltages from U520A/B are also applied to U913/U912 for outputs on J201.

LOW PASS Filter

The low-pass filter consists of L540, C541, L541, C542, L542, C543, and C544. The filter attenuates spurious frequencies occurring above the transmit frequency band. The transmit signal is then fed through the antenna switch to antenna jack J501.

Antenna Switch (CR540, CR541)

The antenna switching circuit switches the antenna to the receiver in the receive mode and the transmitter in the transmit mode. In the transmit mode, +9V is applied to L543 and current flows through diode CR540, L544, diode CR541 and R540. When a diode is forward biased, it presents a low impedance to the RF signal; conversely, when it is reverse biased (or not conducting), it presents a high impedance. Therefore, when CR540 is forward biased, the transmit signal has a low-impedance path to the antenna through coupling capacitor C546. L544, and C552 form a discrete quarter- wave line. When CR540 is forward biased, this quarter-wave line is effectively AC grounded on one end by C552. When a quarter-wave line is grounded on one end, the other end presents a high impedance to the quarter-wave frequency. This blocks the transmit signal from the receiver. C545 and C551 matches the antenna to 50 ohms in transmit and receive.

Transmitter Key-Up Control

Q130, Q131, and Q132 act as switches which turn on with the RX_EN line. When the line goes low the Q130 is turned of which turns Q131 on turning Q132 on. This applies 13.3V to U130 before the TX_EN line goes high. U130A/B provides the key-up and key-down conditioning circuit. C116 and R117 provide a ramp up and ramp down of the 9.0TX during key-up and key-down which reduces load pull of the VCO during key-up. The conditioning provides a stable 5.5V output by balancing the 5.5V reference with the 5.5V regulated supply. The output on U130B, pin 7 is applied to comparator U130D, pin 12, the non-inverting input. The output of U130D, pin 14 is applied to the base of current source Q135. The output of Q135 is on the emitter and is applied back to the inverting input of comparator U130D, pin 13. A decrease or increase at U130D, pin 13 causes a correction by U130D to stabilize the 9V transmit output. R140/141 establish the reference voltage on U130D, pin 13. C143 and C144 provide RF decoupling and C145 stabilizes the output. The 9V transmit voltage is then distributed to the circuits.

2.2 Synthesizer

The synthesizer output signal is produced by the VCO (voltage controlled oscillator). A DC voltage produced by the phase detector in U800 controls the VCO frequency. The phase detector senses the phase and frequency of the two input signals and causes the VCO control voltage to increase or decrease if they are not the same. The VCO is then "locked" on frequency.

Programming of the synthesizer provides the data necessary for the internal prescaler and counters. One input signal is the reference frequency. This frequency is produced by the 17.5 MHz reference oscillator (TCXO). The other input signal is the VCO frequency. a block diagram of synthesizer IC is shown at the end of this section.

Voltage-Controlled Oscillator

Oscillator (Q820)

The VCO is formed by Q820, several capacitors and varactor diodes, and ceramic resonator L826. It oscillates at the transmit frequency in transmit mode and first injection frequency in the receive mode Biasing of Q820 is provided by R823, R824 and R825. An AC voltage divider formed by C844, C845 initiates and maintains oscillation and also matches Q820 to the tank circuit ceramic resonator. L826 is grounded at one end to provide shunt inductance to the tank circuit.

Frequency control

The VCO frequency is controlled in part by DC voltage across varactor diode CR824. As voltage across a reverse-biased varactor diode increases, its capacitance decreases, Therefore, the vco frequency increases as the control voltage increases. The control line is isolated from tank circuit RF by choke L825. The amount of frequency change produced by CR824 is controlled by series capacitor C836. The VCO frequency is modulated using a similar method. The transmit audio/data signal from J201, pin 6 is applied across varactor diode CR823 which varies the VCO frequency at an audio rate. Series capacitors C824/C825 set the amount of deviation produced. R821 provides a DC ground on the anodes of CR8222/CR823, and isolation is provided by R820 and C826.The DC voltage across CR823 provides compensation to keep modulation relatively flat over the entire bandwidth of the VCO. This compensation is required because modulation increases as the VCO frequency increases. CR823 also balances the modulation signals applied to the VCO and TCXO.

Frequency Modulation

Both the VCO and reference oscillator (TCXO) are modulated in order to achieve the required frequency response. If only the VCO was modulated, the phase detector in U800 would sense the frequency change and increase or decrease the VCO control voltage to counteract the change (especially at the lower audio frequencies). If only the reference oscillator frequency is modulated, the VCO frequency would not change fast enough (especially at the higher audio frequencies). Modulating both VCO and reference oscillators produces a flat audio response. Potentiometer R827 sets the VCO modulation sensitivity so that it is equal to the reference oscillator modulation sensitivity.

Cascade Amplifiers (Q821/Q822)

The output signal on the collector of Q820 is coupled by L861/C864 to buffer amplifier Q821/Q822. This is a shared-bias amplifier which provides amplification and also isolation between the VCO and the stages which follow. The signal is direct coupled from the collector of Q822 to the base of Q821. The resistors in this circuit provide biasing and stabilization.

Amplifier (Q823)

Amplifier Q823 provides amplification and isolation between the VCO and receiver, and transmitter. C851/C861/L832 provides matching between the amplifiers. Bias for Q823 is provided by R840/R842/R843. Inductor L833 and capacitor C863 provide impedance matching on the output.

Supply Filter (Q845)

Q845 on the RF board is a capacitance multiplier to provide filtering of the 9.6V supply to the VCO. R945 provides transistor bias and C842 provides the capacitance that is multiplied. If a noise pulse or other voltage change appears on the collector, the base voltage does not change significantly because of C845.

VCO Band Select And T/R Frequency Shift (U840)

The VCO must be capable of producing frequencies from 840 to 960 MHz to produce the required receive injection and transmit frequencies. If this large of a shift was achieved by varying the VCO control voltage, the VCO gain would be undesirably high. Therefore, capacitance is switched in and out of the tank circuit to provide a coarse shift in frequency.

The 928 to 960 MHz band is divided into two segments , 928 to 944 MHz and 944 to 960 MHz. The band selection controlled by the shift register U840 and digital transistors Q843, and Q844 and pin diode CR820 on the vco board.

A frequency shift of 87.85 MHz is required to go from transmit to receive mode and visa versa. Transmit-to-Receive frequency shift is accomplished by programming the shift register U840 which drives the digital transistors Q841 and Q842. In transmit mode, Q841and Q842 forward bias pin diode CR821 which switches in an inductive transmission line in parallel with the vco resonator causing the vco frequency to increase. In receive mode, Q841, Q842 reverse bias CR821 which switches out the inductive transmission line and lowers the vco frequency for the mixer injection.

Synthesizer Integrated Circuit (U800)

Synthesizer chip U800 is shown in Figure 4-2. This device contains the following circuits: R (reference), Fractional-N, NM1 and NM2; phase and lock detectors, prescaler and counter programming circuitry.
Frequencies are selected by programming the R, Fractional-N, NM1 and NM2 in U800 to divide by a certain number. These counters are programmed by Modem board or a user supplied programming circuit. The counter divide numbers are chosen so that when the VCO is oscillating on the correct frequency, the VCO-derived input to the phase detector is the same frequency as the reference oscillator-derived frequency. The VCO frequency is divided by the internal prescaler and the main divider to produce the input to the phase detector.

Lock Detect

When the synthesizer is locked on frequency, the SYNTH LOCK output of U800, pin 18 (J201, pin 7) is a high voltage. Then when the synthesizer is unlocked, the output is a low voltage. Lock is defined as a phase difference of less than 1 cycle of the TCXO.

2.3 PSU

Regulated +9.6V
The RF enable signal applied on J201, pin 5 and to the base of Q110 turning the transistor on. This causes the collector to go low and applies a low to the control line of U111, pin 1 and R110 is a pull up resistor. The 13.3V from J201, pin 2 is on U111, pin 6 to produce a +9.6V reference output on U111, pin 4. C120 stabilizes the voltage and C122 provides RF decoupling.

Regulated +5.5V
The RF enable signal applied on J201, pin 5 and to the base of Q110 turning the transistor on . This causes the collector to go low and applies a low to the control line of U110, pin 1. C904 decouples RF and R131 is a pull up resistor. The 13.3V from J201, pin 2 is on U110, pin 6 to produce a +5.5V regulated output on U110, pin 4. C119 stabilizes the voltage and C115 provides is a bypass capacitor for U110.

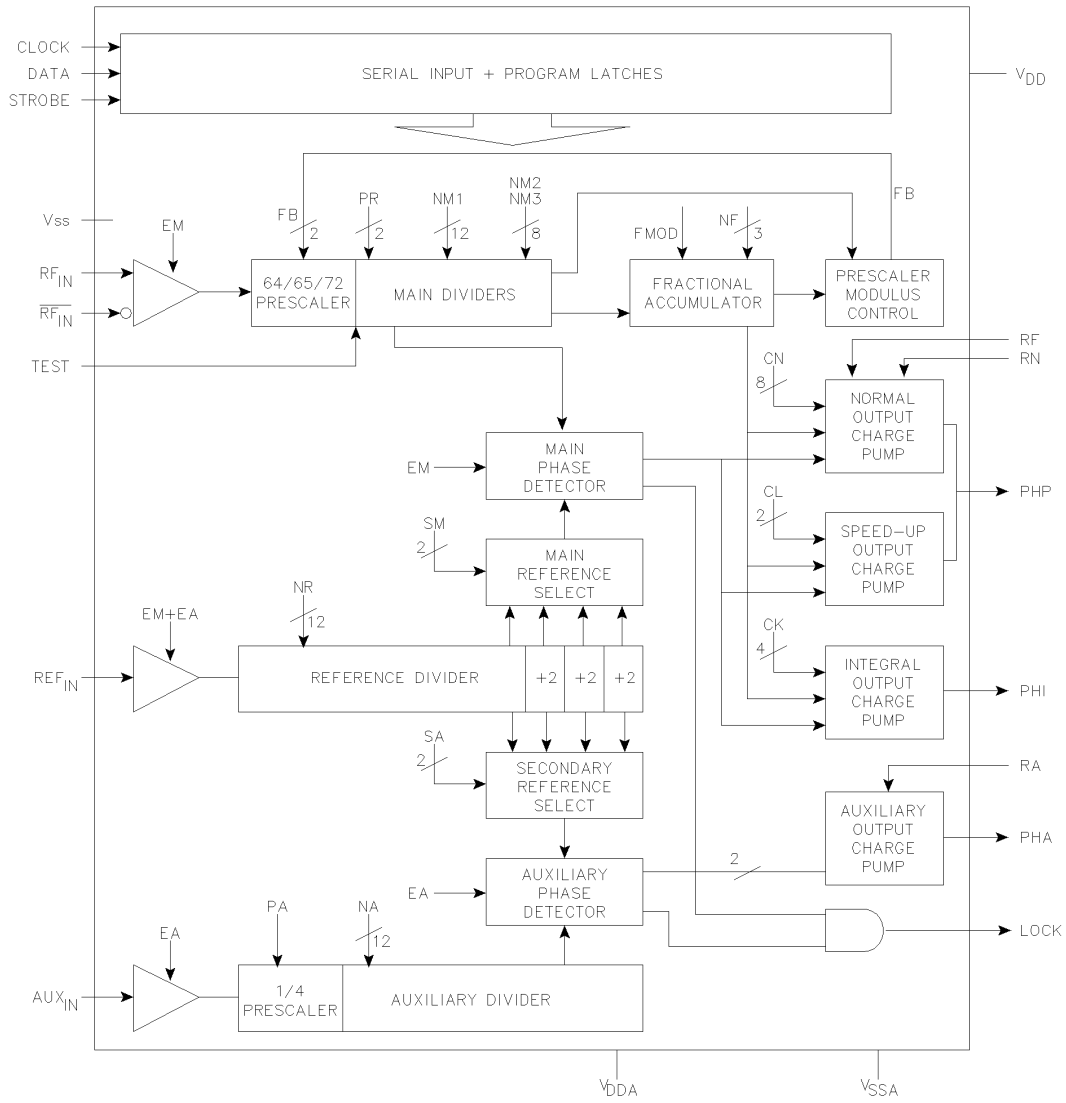


Figure 1

DI-3492 Synthesizer Integrated Circuit (U800)

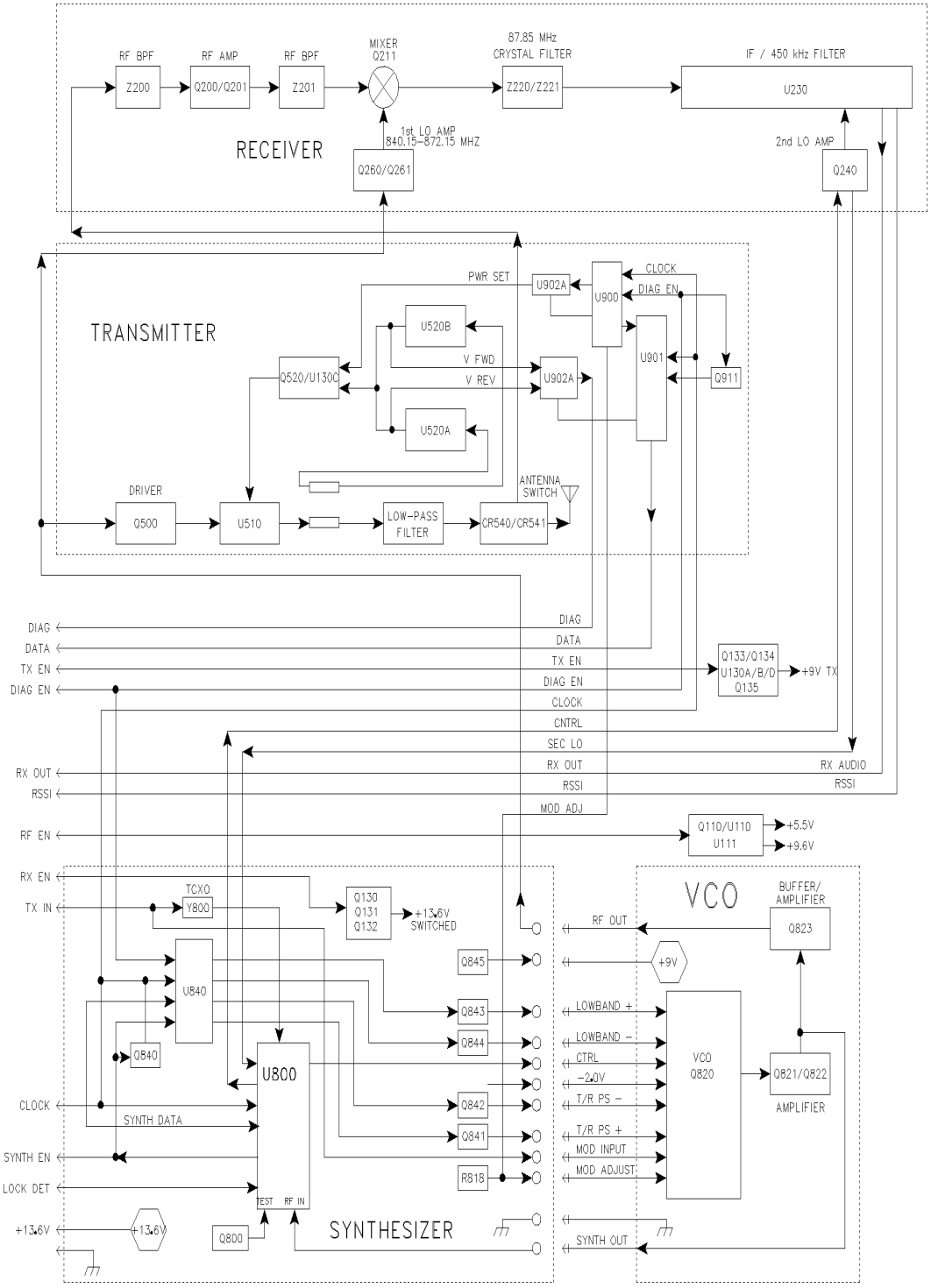


Figure .2

DI-3492 Transceiver Block Diagram

3. INTEGRA R- 3315 LOADER/MODEM

The Logic Board is divided into 5 sub-sections on the Block Diagram

1 CPU
2 RS232
3 Modem
4 Integra-T A/D and Digipot
5 Wake-Up Circuit
6 PSU

A block diagram of the MCU-R is located at the end of this section.

3.1 MICROPROCESSOR CIRCUIT

For the microprocessor section, two Z84015 CMOS low power Intelligent Peripheral Controllers are used. Each IPC is an 8-bit microprocessor integrated with CTC, SIO, PIO Clock Generator Controller and Watch Dog Timer.
One of the Z84015s (U17) is used in the normal mode. The other Z84015 (U21) is used in the evaluation mode and as such only the CTC, SIO and PIO section are used. The CPU section is disabled.
The first Z84015 Clock Generator uses a 19.6608 MHz crystal which provides a CPU clock rate of 9.8304 MHz for both Z84015s. The 9.8304 MHz clock is further divided by 2 to feed all 8 CTC (4 in each Z84015).

The 64K memory space of the Z84015 is divided into two blocks of 32k each. The lower 32K is used for the firmware program and the upper 32K by the CMOS RAM (U18).). The memory IC used for the program is a CMOS FLASH (U22) with 1024 sectors of 128 bytes each.

The dual Z84015 circuit provides up to 8 CTC, 4 SIO (Serial I/O) and 32 PIO (Parallel Input/Output) lines.
The CPU also provides the clock for the CPLD modem.

3.2 RS232

The RS232 IC (U15) is used to interface the application DE-9 connector to the SIO_B section of U17, and the set-up DE-9 connector to the SIO_A section of U21. When in sleep mode, two receivers remain enabled, this is needed for fast wakeup.

3.3 MODEM

The modem section is used to interface the serial digital data to the transceiver.
The CPLD modem IC (U16) with a programmable Raise-Cosine filter (U10), operates in DRCMSK mode at 4800, 9600 and 19200 bits/sec. It incorporates a 7-bit hardware scrambler and uses Differential (NRZI) encoding in DRCMSK mode to minimize data pattern-sensitivity. Electronic potentiometer U5B (E-Pot), controlled by CPU U17, is used to set the transmitter deviation by amplitude adjustment of the baseband signal. Electronic potentiometer U5C is also provided to adjust the frequency of the RF carrier.

TRANSMIT & RECEIVE DATA

Transmit Data from the RS-232 port is level-shifted to TTL by U15, then passed through the CPU for further processing and conversion from asynchronous to synchronous format. The CPLD modem, U16 takes the digital data stream from SIO-A of the CPU and synthesizes to the constant-amplitude analog baseband signal, which is filtered by U10, buffered by U9B then applied to radio module TXA at P1-6.

Received signals are applied to the RXA pin on P1-13 amplified by U3A, whose gain is set by the electronic potentiometer U5D, and then filtered by U10. The same filter circuit is used for transmission and reception: two analog multiplexer/demultiplexer gates (U8A and B) controlled by TX_EN line are used for sharing. The filter U10 cut-off frequency is programmable by the CPLD, based on the data rate. The analog signal is then buffered by U1D and fed to Peak Detectors U3C, U3D and U3B, and to the slicer

circuit U1C via U1B. The raw data is then passed to the CPLD modem U16 for descrambling and receive clock recovery. The resulting synchronous bit stream is then fed to CPU, SIO-A for further processing and convertion to asynchronous format before delivery to the RS-232 driver and to the user port.

3.4 INTEGRA-TR A/D AND DIGIPOT

An 8 channel, 8-bit successive approximation A/D converter, type ADC0838 (U4), is interfaced to CPU (U17) and Peripheral (U21).
CH0 and CH1 are connected to the positive and negative peak detector of the modem section. The software can thus read the positive or negative value of an RX signal, or using the differential mode, the actual peak-to-peak RX signal value.
CH3 is used to measure the radio RSSI signal which was amplified by U7A.
CH4 is connected to the radio diagnostic signal (P3-14). This pin is used to output an analog signal corresponding to the power output and the reflected signal.
CH5 is connected to U6 (LM50), a temperature sensor with a -40 to +125°C range.
CH6 is used to read the SWB+ voltage after proper scaling into the 0-5 V range.
CH7 and CH8 are connected to EXT SIGNAL 1 and 2. A 2:1 divider and protection circuit is inserted between both external signals and the A/D.
The EXTERNAL SIGNAL 1 and 2 pins are also connected to U21 at PB6 and PB7 through transistors Q3 and Q4, and thus can be used for ANALOG INPUT or DIGITAL OUTPUT (available on some Integra versions).
EXT_SIGNAL2 is also connected to the rx test point RX-TP through U8A (74HC4066). Under software control the RX-TP (scaled down by 2) is thus available on the power connector for trouble-shooting purposes.
A 4 channel digital potentiometer type (U5) is used to adjust the RX SIGNAL, TX MODULATION, CARRIER FREQUENCY and CARRIER DETECT THRESHOLD.
An 8 channel, 8-bit successive approximation A/D converter, type AD0838 (U9), is interfaced to CPU (U18) and Peripheral (U20).
U19 generates a power-on reset for the CPU and U6 is a temperature sensor used by the firmware to compensate for variations in RSSI.

The RSSI signal from the transceiver is amplified and filtered by U7A, it is then compared to a threshold value set by a digital potentiometer (U5A). The output of the comparator (U7B) is used to change the hold time of both peak detectors at the beginning of the receive packet.

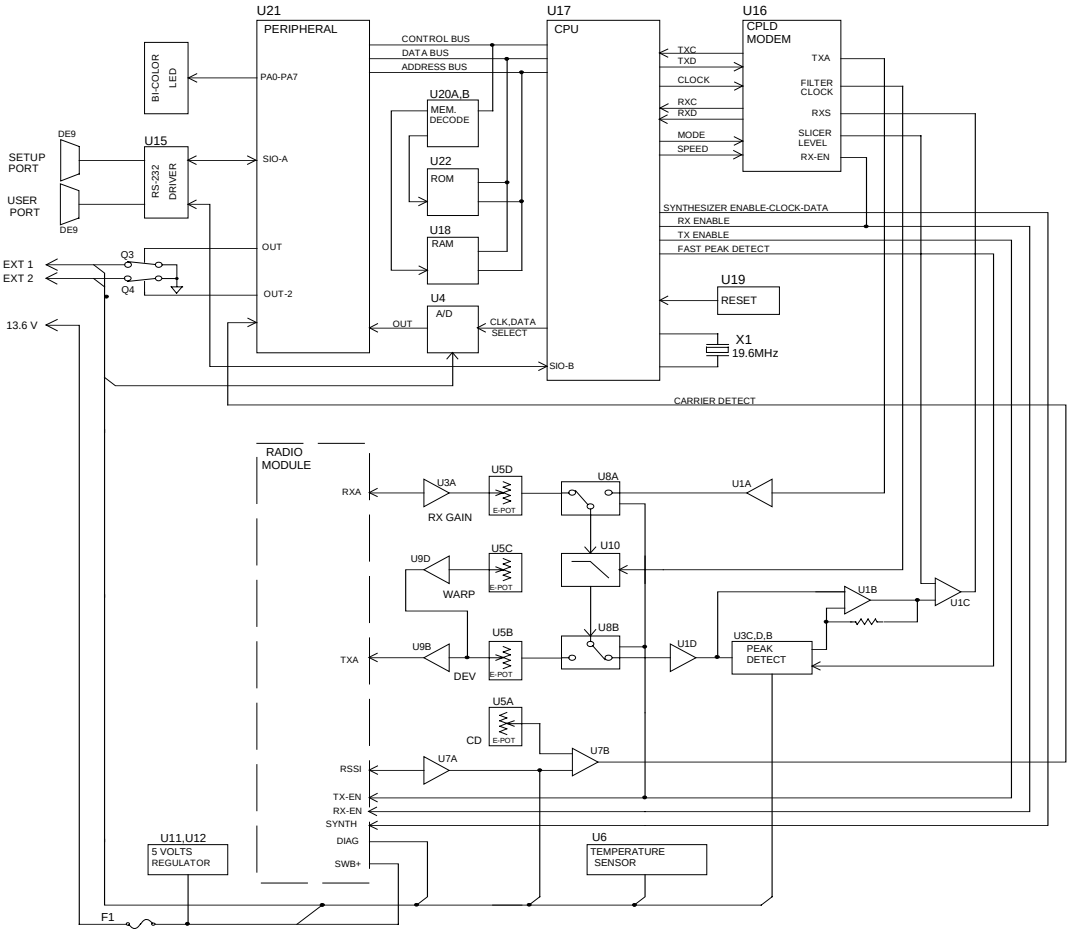
3.5 WAKE-UP CIRCUIT

The wake-up circuit for Integra-TR consists of a 50 ms monostable circuit that is triggered by the rising edge of a SLEEP signal from the CPU (U18). The falling edge of this 50 ms pulse (end of pulse) is connected to the \NMI of the CPU and thus will wake up the CPU from SLEEP mode after 50 ms.
When exiting SLEEP mode on a \NMI, the CPU firmware will increment a counter, then return to SLEEP until it reaches a limit set by a software parameter. When the programmed count is reached the CPU will wake up the radio and the RS232 driver, program the synthesizer, and watch for channel activity.
While in sleep mode (during the 50 ms pulse) an active RTS from either communication port will reset (terminate) the 50 ms pulse so that its falling edge will restart the CPU immediately.
The CPU will check to see if either RTS signal is valid each time it is restarted by the \NMI. The firmware will only start the sleep timer after checking that all "wakeup" inputs are inactive.

3.6 POWER SUPPLY

The 13.3 volt DC power input is protected by a 3 amp fuse and reverse protected by a diode.
A 5 volt, low voltage regulator (U12) is used to power all digital functions and another 5 volt, low voltage regulator is used to control the analog +5V_SW voltage in the sleep mode.

Integra TR Block diagram



4. DL-3492 transcevier active devices functions

Reference Designator	Function	Type
CR101A	TCXO Varactor	BB639
CR200	Protection Diode	MMBD6050LT1
CR240	2nd LO Varactor	BB535
CR520	Power Control	MMBD701LT1
CR540	Antenna Switch	MMBV3401
CR541	Antenna Switch	MMBV3401
CR592	Power Control	MMBD701LT1
CR840	VCO Varactor	BB535
Q100	Receive Enable Switch	MUN5213T1
Q101A	TCXO Oscillator	MMBT3904
Q101	Receive Enable Switch	MUN5114T1
Q102A	TCXO Buffer	MMBT3904
Q110	RF Enable Switch	MUN5213T1
Q130	TX Enable Switch	MUN5213T1
Q131	TX Enable Switch	MUN5213T1
Q132	TX Enable Switch	MUN5114T1
Q133	TX Enable Switch	MUN5213T1
Q134	TX Enable Switch	MUN5114T1
Q135	TX Enable Switch	PZT2222AT1
Q200	RF Amplifier Bias	MSB1218-RT1
Q201	Low Noise RF Amplifier	NE85633
Q211	1st LO Mixer	NE25118
Q240	2nd LO Buffer	MMBT918
Q260	2nd LO Amplifier	NE85633
Q261	2nd LO Amplifier Bias	MSB1218-RT1
Q500	PA Driver	MSA2111
Q520	RF Power Amplifier	PZT2222AT1
Q800	TCXO Level Amplifier	MSD1819A-RT1
Q840	Synthesizer Enable	MUN5213T1
Q841	Tx Pin shift Positive	MUN5213T1
Q842	TxPin shift Negative	MUN5213T1
Q843	Lowband pin shift Positive	MUN5213T1
Q844	Lowband pin shift Negative	MUN5213T1
Q845	VCO	MSD1819A-RT1
Q911	Diagnostics Enable	MMBT3904
U110	5.5 Volts Regulated	TK11900M
U111	9.6 Volts Regulated	TK11900M
U130	Power Control	MC33174D
U230	2nd If/Demodulator/Limiter	SA676DK
U510	6W Pwr module, 900 MHz	BGY114E
U520	Power Control	MC33172D
U800	FRACTIONAL-N Synthesizer	SA7025
U840	Shist register 8-STG SOI	MC14094
U900	TLC5620ID quad 8 bit dac	TLC5620ID
U901	Shift register 8-STG SOI	MC14094
U902	3 2CH analog mux/de-mux	MC14053

5. INTEGRA R 210-3315-XXX ACTIVE CIRCUITS DESCRIPTION

Designator	function	Type
D1	DIODE, HOT CARRIER, SOT-23	MMBD301LT1
D2	DIODE, HOT CARRIER, SOT-23	MMBD301LT1
D3	DIODE, SOT-23	BAV99LT1
D4	DIODE, SOT-23	BAV99LT1
D5	DIODE, SOT-23	BAV99LT1
D6	DIODE,RECTF,1A/100V	1N4001
DS1	LED,3MM,BICOLOR,RED/GREEN SMT	591-3001-102
DS2	LED,3MM,BICOLOR,RED/GREEN SMT	591-3001-102
DS3	LED,3MM,BICOLOR,RED/GREEN SMT	591-3001-102
DS4	LED,3MM,BICOLOR,RED/GREEN SMT	591-3001-102
Q1	TRANSISTOR, GENERAL PURPOSE,SOT-23	MMBT3904LT1
Q2	TRANSISTOR, GENERAL PURPOSE,SOT-23	MMBT3904LT1
Q3	TRANSISTOR, GENERAL PURPOSE,SOT-23	MMBT3904LT1
Q4	TRANSISTOR, GENERAL PURPOSE,SOT-23	MMBT3904LT1
U1	QUAD, OP-AMP , -40/+85 SO-14	TLC2274ID
U2	HEX INVERTER CMOS	74HC04AD
U3	QUAD OP-AMP	LMC6484AIM
U4	8 BIT A/D,-40/+85C SO-20W	ADC0838CIWM
U5	POTENTIOMETER 4 DIGITAL	AD8403AR50
U6	TEMPERATURE SENSOR,SOT-23	LM50CIM3
U7	DUAL OP-AMP,-40/+85 S0-8	TLC2272ID
U8	ANALOG MULTIPLEXERS/DEMULTIPLEXERS SOIC 16	MC74HC4053D
U9	QUAD, OP-AMP , -40/+85 SO-14	TLC2274ID
U10	FILTER, LINEAR PHASE LOW PASS S0-8	LTC1069-7
U11	REGULATOR,MICROPOWER VOLTAGE ,S0-8	LP2951CD
U12	REGULATOR,LOW DROPOUT,Q PACKAGE	LT1129IQ-5
U13	DUAL MONOSTABLE, SOIC	74HC4538AD
U14	QUAD NAND GATE	74HC00AD
U15	CONVERTER RS-232	ADM223AR
U16 (TO BE PROGRAMMED)	CPLD 64 MACROCELL	PZ5064-I12A44
U17	MICROPROCESSOR ,10MHz	Z8401510FEC
U18	RAM,CMOS,32K x 8, -40/=85, SOP-28	TC55257DFI-85L or TC55257DFL-85L (SCREENED -40 +85)
U19	RESET CIRCUIT, -40+85 ,S0-8	MC33064D-5
U20	HEX OR GATE,CMOS	74VHC32AD
U21	MICROPROCESSOR ,10MHz	Z84C1510FEC /Z8401510FEC
U22 (TO BE PROGRAMMED)	EPROM, FLASH 1 MEGABIT, -40/+85 PLCC	AT29C010A-90J1
X1	XTAL, FPX SERIES 19.6608 MHz	FPX196-20PF