2 CIRCUIT DESCRIPTION

2.1 Modulation Circuits

The modulation circuits are contained on the upper board. DI is the digital input and AI is the analog input to the modulator. DI is DC coupled and has a higher gain than AI. IC2a is the modulation input amplifier and also functions as the limiter to restrict the maximum permissible deviation. RV1 sets the analog gain. It also affects the gain on the digital input, but this is not usually relevant as digital signals always cause IC2a to limit.

IC26 and associated passive components form the inverting modulation filter. This is designed for a cut off frequency of about 3 kHz. For use with GMSK modems the filter is widened by removing C2,4,5 and 26. IC1 is an analog gate which removes the modulating signal while the transceiver is in receive mode. RV4 sets the maximum level of the deviation.

The modulation path is split into the high and low frequency paths after RV4. The low frequency path goes to the TCXO and modulates at frequencies outside the PLL bandwidth. The high frequency path goes to the VCO via RV2, and modulates at frequencies inside the PLL bandwidth. RV2 adjusts the level of high frequency modulation, which when correctly balanced with the low frequency modulation, results in flat modulation from DC to the upper bandwidth limit.

2.2 Transmitter Power Amplifier

Refer to the lower board circuit diagram. In transmit mode 2 mW of drive is available at the FOUT pin of the VCO module, which is switched via D9 and C39 to TR2 which is the driver stage of the transmitter. R15 and C35 apply negative feedback to the driver stage for stability and the driver's base bias is supplied from +5VTX via L15 and R19. The Power amplifier is of very unconventional design in that the driver and PA stages share the same DC current path of L10, L12, TR2, L13, TR3, R20, while the RF path is C39,TR2, C34, D8, TR3, C28. IC4a achieves power control by comparing the voltage drop across R20 to the power control reference voltage on pin 3 and altering the DC biassing of TR2 and 3 via R16 and D8. The power output from TR3 is strongly related to the average DC current.

C13, L5, C17, L6, C22, L8, C24 form 7 poles of low pass filtering for harmonic suppression. In transmit the RF switching diode D4 is forward biassed via the R6, D4, L3, D1 path. C1, L2, C3 add another 3 poles of low pass filtering. D1 prevents RF power being fed into the RF receive path.

2.3 Receiver

Refer to the lower board circuit diagram.

The input signal passes through several low pass filter stages and the first helical filters F1 and F2. These are tuned to the frequency of the wanted RF signal. They reduce blocking and inter-modulation problems in the first RF amplifier TR1. They also suppress spurious receiver responses, particularly the 1st image which is 90MHz below the wanted frequency.

The current passing through TR1 feeds the +3VRX line which supplies the VCO buffer, helping to reduce supply current in receive mode.

Signals are then passed to the 1st RF mixer TR4 where they are down converted to 45 MHz, the 1st IF frequency. The low side injection 1st local oscillator is provided by the VCO module at a level of about 0.5 mW via the switching diode D9. The mixer output is then filtered by 4 poles of crystal filtering F3, F4 to select the wanted product. The filters are tuned to the first IF of 45MHz. They select the wanted mixer output and control the inter-modulation problems in the first IF amplifiers TR5 and TR6 before being applied to the 2nd mixer which is inside IC8. They also suppress spurious receiver responses, particularly the 2nd image at the wanted frequency - 910kHz. They may contribute to the adjacent channel selectivity.

Crystal X2, associated components and the active device inside IC8 form the low side injection 2nd local oscillator which converts the wanted signal down to 455 kHz. The output from the 2nd mixer is filtered by F5 to select the wanted product before being passed back to the limiting amplifier inside IC8. F5 is the main selective element in the receiver responsible for the adjacent channel rejection. The discriminator is also inside IC8 although it requires an external quadrature coil L17 and damping resistors R37, R41. The audio signal is produced at pin 9, where it is passed to the audio and squelch circuits.

2.4 Receiver Audio and Squelch Circuits

Refer to the upper board circuit diagram. R15 and C8 remove most of the 455 kHz component from the audio signal. IC3a is a unity gain buffer which passes the audio signal to the outside via PL3. IC3b acts as a data slicer, which drives an open collector transistor TR7 as an interface for slow FSK data applications.

RV3 is used to set the noise level at which the squelch operates. The high frequency noise is passed back to the lower PCB via the SQ AUD pin. It is bandpass filtered by IC8, C56, 73, R36, 38, 44. The noise detection and squelch gates is internal to IC8 with C72 setting the detection time constant and the squelch flag provided by pin 13. TR7 ensures the squelch is always

ON while the transceiver is in TX mode. The squelch signal is passed up to the upper PCB where TR2 and C12 provide audio signal muting, and TR3 is an open collector squelch output. Because the data slicer has no hysteresis, the data slicer is muted by D4 which adds a small DC offset to IC3 pin 1 when the receiver is squelched.

2.5 Frequency Synthesizer

The frequency synthesizer provides the drive for the transmit strip and the 1st local oscillator for the receiver. The VCOs are built on a small module. This allows for good screening and grounding. The transmit VCO is built around TR1 and the RX VCO around TR2. Both are a variation on the Colpitts oscillator, with the TX VCO being modulated by D3. C8 and C4 allow the centre frequency of the VCO to be tuned. The power is supplied to the VCOs by TR6 with provides low frequency smoothing. TR3 and TR4 switch between the two VCOs. IC1 amplifies and buffers the VCO output to minimise load pulling effects. C10, L5 and C14 do some low pass filtering to reduce harmonic levels. In RX IC1 is fed from RXV via D4 for reduced power consumption. In TX IC1 is fed directly from +5V via TR5 to give a higher output power level. The RF is fed onto the lower PCB where it drives the programmable divider inside the synthesizer chip IC7. The frequency reference for the synthesizer is the TCXO, X1. The output of the phase detector is pin 5 of IC7, which is used to correct the VCO frequency after being filtered by C20, R5, C9, R4, C6, which makes the loop filter. The synthesizer IC has an alternative power supply path in RX mode, via D3 for current saving. The synthesizer is programmed from the PIC micro-controller by a 3-wire bus on pins 9, 10 and 11.

2.6 PIC Micro-controller and Power Supply Regulation

IC9 is a linear regulator which produces a +5V rail from the 6.0 to 15.0 V input. If the supply voltage drops too low it resets the PIC micro-controller via R38. The PIC stores the frequency and channel information, reads the input lines, programmes the synthesizer, and sequences the RX and TX power supplies and the power amplifier and out of lock signals. Timing is provide by the clock built around resonator X1. The RX power supply is switched with TR5 and the TX power supply by TR4. The power amplifier reference voltage is set by RV5. PL4 is for on board reprogramming of the software for the PIC. Frequency and channel information can be reprogrammed via the RS232 port and TR6.

2.7 EMC Filtering

The I/O pins are protected for EMC and static with a series R and a capacitor to 0V. The ST500 has been fully tested & meets ETS 300 683.