SECTION 4 CIRCUIT DESCRIPTION

4-1 RECEIVER CIRCUITS

4-1-1 ANTENNA SWITCHING CIRCUIT (MAIN unit)

The antenna switching circuit functions as a low-pass filter while receiving and as resonator circuit while transmitting. The circuit does not allow transmit signals to enter receiver circuits.

Received signals enter the antenna connector and pass through the low-pass filter (L1–L3, C1, C2, C6–8). The filtered signals are then applied to the RF circuit passed through the λ/4 type antenna switching circuit (D5, D6, L6).

4-1-2 RF CIRCUIT (MAIN unit)

The RF circuit amplifies signals within the range of frequency coverage and filters out-of-band signals.

The signals from the antenna switching circuit pass through the two-stage tunable bandpass filters (D8, D4). The filtered signals are amplified at the RF amplifier (Q2) and then enter other two-stage bandpass filters (D9, D10) to suppress unwanted signals. The filtered signals are applied to the 1st mixer circuit (Q3).

The tunable bandpass filters (D4, D8–D10) employ varactor diodes to tune the center frequency of the RF passband for wide bandwidth receiving and good image response rejection. These diodes are controlled by the CPU (IC20) via the D/A converter (IC7).

The gate control circuit reduces RF amplifier gain and attenuates RF signal to keep the audio output at a constant level.

The receiver gain is determined by the voltage on the "RSSI" line from the FM IF IC (IC1, pin 12). The gate control circuit supplies control voltage to the RF amplifier (Q2) and sets the receiver gain.

When receiving strong signals, the "RSSI" voltage increases and the gate control voltage decreases. As the gate control voltage is used for the bias voltage of the RF amplifier (Q2), then the RF amplifier gain is decreased.

4-1-3 1ST MIXER AND 1ST IF CIRCUITS (MAIN unit)

The 1st mixer circuit converts the received signals to a fixed frequency of the 1st IF signal with the PLL output frequency. By changing the PLL frequency, only the desired frequency will pass through a MCF (Monolithic Crystal Filter; FI1) at the next stage of the 1st mixer.

The RF signals from the bandpass filter are applied to the 1st mixer circuit (Q3). The applied signals are mixed with the 1st LO signal coming from the RX VCO circuit (Q13) to produce a 46.35 MHz 1st IF signal. The 1st IF signal passes through a MCF (Monolithic Crystal Filter; FI1) to suppress out-of-band signals. The filtered signal is amplified at the 1st IF amplifier (Q4) and applied to the 2nd IF circuit.

4-1-4 2ND IF AND DEMODULATOR CIRCUITS (MAIN unit)

The 2nd mixer circuit converts the 1st IF signal to a 2nd IF signal. A double-conversion superheterodyne system improves the image rejection ratio and obtains stable receiver gain.

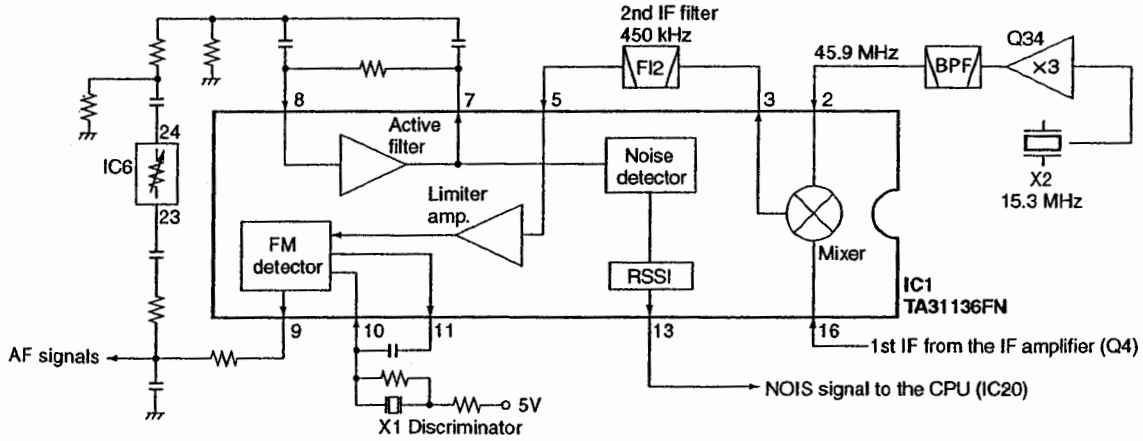
The 1st IF signal from the 1st IF amplifier (Q4) is applied to the 2nd mixer section of the FM IF IC (IC1, pin 16) and is then mixed with the 2nd LO signal for conversion to a 450 kHz 2nd IF signal.

IC1 contains the 2nd mixer, limiter amplifier, quadrature detector, active filter and noise amplifier circuits, etc. A tripled frequency from the PLL reference oscillator is used for the 2nd LO signal (45.9 MHz).

The 2nd IF signal from the 2nd mixer (IC1, pin 3) passes through a ceramic filter (FI2) to remove unwanted heterodyned frequencies. It is then amplified at the limiter amplifier section (IC1, pin 5) and applied to the quadrature detector section (IC1, pins 10, 11 and X1) to demodulate the 2nd IF signal into AF signals.

The AF signals are output from pin 9 (IC1) and are then applied to the AF amplifier circuit.

• 2nd IF and demodulator circuits



4-1-5 AF AMPLIFIER CIRCUIT (MAIN unit)

The AF amplifier circuit amplifies the demodulated AF signals to drive a speaker.

The AF signals from the FM IF IC (IC1, pin 9) are amplified at the AF amplifier section of the compander IC (IC14, pins 5, 4) and are then applied to the high-pass filter circuit (IC21b).

The high-pass filter characteristics are controlled by the FSW signal from the LCD driver IC (FRONT unit; IC1, pin 6). When FSW signal is high, the cut-off frequency is shifted higher to remove CTCSS or DTCS signals.

The filtered AF signals from the high-pass filter (IC21b, pin 7) are applied to the de-emphasis section of compander IC (IC14, pin 3) with frequency characteristics of –6 dB/octave, and are then passed through the low-pass filter, high-pass filter, expander sections of compander IC (IC14). The output signal from IC14 (pin 38) is applied to the electronic volume controller (IC6, pin 1).

The output AF signals from the electronic volume controller (IC6, pin 2) are applied to the AF amplifier (IC18) and AF power amplifier (IC8) to drive the speaker.

4-1-6 RECEIVER MUTE CIRCUITS (MAIN unit)

• NOISE SQUELCH

The noise squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals, the squelch circuit switches the AF mute switch.

Some noise components in the AF signals from the FM IF IC (IC1, pin 9) are passed through the level controller (IC6, pins 24, 23). The level controlled signals are applied to the active filter section in the FM IF IC (IC1, pin 8). Noise components about 10 kHz are amplified and output from pin 7.

The filtered signals are converted into the pulse-type signals at the noise detector section and output from pin 13 (NOIS).

The NOIS signal from the FM IF IC is applied to the CPU (IC20, pin 37). The CPU then analyzes the noise condition and controls the AF mute signal via "AFON" line (IC20, pin 18) to the AF regulator (Q39, Q40, D31).

• CTCSS AND DTCS

The tone squelch circuit detects AF signals and opens the squelch only when receiving a signal containing a matching subaudible tone (CTCSS or DTCS). When tone squelch is in use, and a signal with a mismatched or no subaudible tone is received, the tone squelch circuit mutes the AF signals even when noise squelch is open.

A portion of the AF signals from the FM IF IC (IC1, pin 9) passes through the low-pass filter (IC5) to remove AF (voice) signals and is applied to the CTCSS or DTCS decoder inside the CPU (IC20, pin 46) via the "CDEC" line to control the AF mute switch.

4-2 TRANSMITTER CIRCUIT

4-2-1 MICROPHONE AMPLIFIER CIRCUIT (MAIN unit)

The microphone amplifier circuit amplifies audio signals within +6 dB/octave pre-emphasis characteristics from the microphone to a level needed for the modulation circuit.

The AF signals (MIC) from the FRONT unit via J2 (pin 1) are passed through the level controller (IC6, pins 9, 10) to the microphone amplifier circuit.

The AF signals from the level controller (IC6) are applied to the microphone amplifier section of compander IC (IC14, pin 12). The amplified signals are passed through the compressor, low-pass filter and high-pass filter sections of IC14.

The filtered AF signals are amplified at the buffer amplifier (Q21) and pre-emphasized with +6dB/octave at the pre-emphasis circuit (R122, C187), and are then applied to the IDC amplifier section of IC14 (pin 8).

The amplified AF signals are passed through the limitter amplifier, low-pass filter and smoothing filter sections of IC14 after being passed through the AF mute switch inside of IC14.

The output signals from pin 6 are passed through the analog switch (IC15), splatter filter (IC21d) and applied to the level controller (IC6, pins 21, 22). The deviation level controlled signals are then applied to modulation circuit as the "MOD" signal.

The narrow/wide switch (Q22) is connected to the input of the splatter filter (IC21d) and switched by the "NWC" signal coming from the CPU (IC20, pin 19). When "NWC" is at a high level, the narrow/wide switch (Q22) shifts the filter cut-off frequency for narrow deviation selection.

4-2-2 MODULATION CIRCUIT

The modulation circuit modulates the VCO oscillating signal (RF signal) using the microphone audio signals.

The AF signals from the level controller (IC6, pin 22) change the reactance of varactor diode (D18) to modulate the oscillated signal at the TX VCO circuit (Q14, D17, D53–D55). The modulated VCO signal is amplified at the buffer amplifiers (Q11, Q10) and is then applied to the drive amplifier circuit via the T/R switch (D14).

The CTCSS/DTCS signals from the CPU (IC20, pins 89–91) are passed through the low-pass filter (Q37), level controller (IC6, pins 12, 11) and mixer (IC21a), and are then applied to the VCO circuit via the splatter filter (IC21d).

4-2-3 DRIVE AMPLIFIER CIRCUIT (MAIN unit)

The drive amplifier circuit amplifies the VCO oscillating signal to the level needed at the power amplifier.

The RF signal from the buffer amplifier (Q10) passes through the T/R switch (D14) and is amplified at the YGR (Q9) and pre-drive (Q8) amplifiers. The amplified signal is applied to the power amplifier circuit.

4-2-4 POWER AMPLIFIER CIRCUIT (MAIN unit)

The power amplifier circuit amplifies the driver signal to an output power level.

The RF signal from the pre-drive amplifier (Q8) is applied to the power module (IC3) to obtain 25 W for IC-F510/F520, or 50 W for IC-F521 of RF power.

The amplified signal is passed through the antenna switching circuit (D2), low-pass filter and APC detector, and is then applied to the antenna connector.

Control voltage for the power amplifier (IC3, pin 3) comes from the APC amplifier (IC2) to stabilize the output power. The transmit mute switch (D32) controls the APC amplifier when transmit mute is necessary.

4-2-5 APC CIRCUIT (MAIN unit)

The APC circuit protects the power amplifier from a mismatched output load and stabilizes the output power.

The APC detector circuit detects forward signals and reflection signals at D11 and D1 respectively. The combined voltage is at minimum level when the antenna impedance is matched at 50 Ω, and is increased when it is mismatched.

The detected voltage is applied to the APC amplifier (IC2, pin 3), and the power setting "T4" signal from the D/A converter (IC7, pin 4), controlled by the CPU (IC20), is applied to the other input for reference. When antenna impedance is mismatched, the detected voltage exceeds the power setting voltage. Then the output voltage of the APC amplifier (IC2, pin 4) controls the input current of the power module (IC3) to reduce the output power.

4-3 PLL CIRCUITS

4-3-1 PLL CIRCUIT

A PLL circuit provides stable oscillation of the transmit frequency and receive 1st LO frequency. The PLL output compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of a programable divider.

The PLL circuit contains the TX/RX VCO circuit (Q14, Q13). The oscillated signal is amplified at the buffer amplifiers (Q11, Q12) and then applied to the PLL IC (IC4, pin 17) via the low-pass filter (L32, C298, C299, C509).

The PLL IC contains a prescaler, programable counter, programable divider and phase detector, etc. The entered signal is divided at the prescaler and programable counter section by the N-data ratio from the CPU. The reference signal is generated at the reference oscillator (X2) and is also applied to the PLL IC. The PLL IC detects the out-of-step phase using the reference frequency, and outputs it from pin 13. The output signal is passed through the charge pump (Q50, Q51, Q54, Q55) and active loop filter (Q52, Q53), and is then applied to the VCO circuit as the lock voltage.

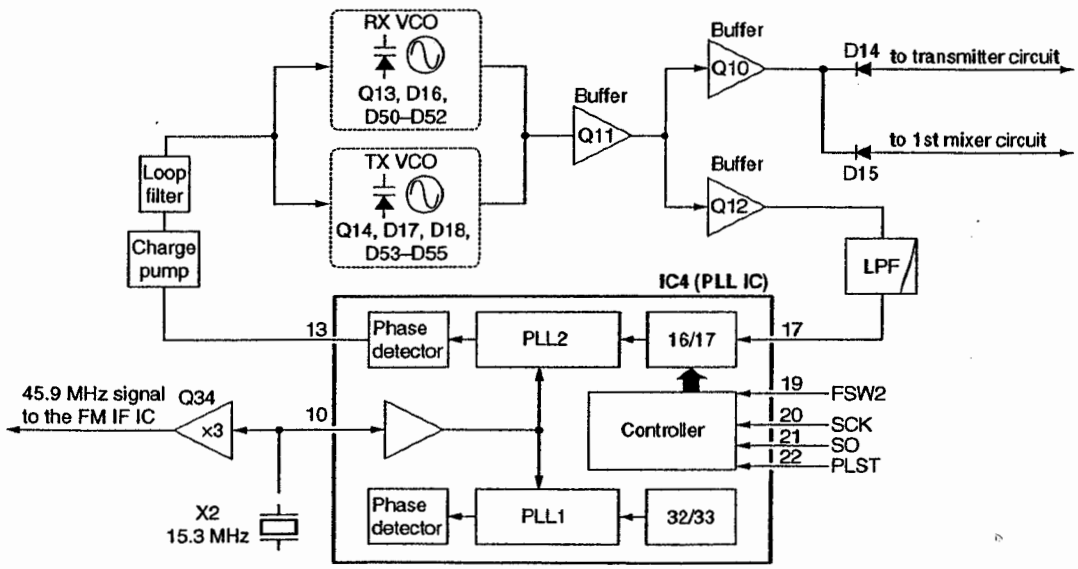
If the oscillated signal drifts, its phase changes from that of the reference frequency, causing a lock voltage change to compensate for the drift in the oscillated frequency.

4-3-2 VCO CIRCUIT

The VCO circuit contains a separate RX VCO (Q13, D16, D50–D52) and TX VCO (Q14, D17, D18, D53–D55). The oscillated signal is amplified at the buffer amplifiers (Q11, Q10) and is then applied to the T/R switch circuit (D14, D15). Then the receive 1st LO (Rx) signal is applied to the 1st mixer (Q3) and the transmit (Tx) signal to the YGR amplifier circuit (Q9).

A portion of the signal from the buffer amplifier (Q11) is fed back to the PLL IC (IC4, pin 17) via the buffer amplifier (Q12) and low-pass filter (L32, C298, C299, C509) as the comparison signal.

• PLL circuit



4-4 POWER SUPPLY CIRCUITS

4-4-1 VOLTAGE LINES (MAIN unit)

Line	Description
HV	The voltage from a DC power supply.
VCC	The same voltage as the HV line which is controlled by the power switching circuit (Q23, Q24). When the [POWER] switch is pushed, the CPU outputs the "PWON" control signal to the power switching circuit to turn the circuit ON.
CPU5V	Common 5 V for the CPU converted from the HV line by the CPU5V regulator circuit (IC10). The circuit outputs the voltage regardless of the power ON/OFF condition.
8V	Common 8 V converted from the VCC line by the 8V regulator circuit (IC9).
5V	Common 5 V converted from the VCC line by the 5V regulator circuit (Q27, Q28).
R8V	Receive 8 V controlled by the R8 regulator circuit (Q26, Q30, D24) using the "TXC" signal from the CPU (IC20, pin 16).
T8V	Transmit 8 V controlled by the T8 regulator circuit (Q25, Q29, D23) using the "TMUT" signal from the CPU (IC20, pin 17).

4-5 PORT ALLOCATIONS

4-5-1 OUTPUT EXPANDER (FRONT unit; IC1)

Pin number	Port name	Description
1–3	KS0–KS2	Output ports for key matrix.
4	DIM1	Outputs LCD backlight control signal. Low : While LCD backlight is dim.
5	DIM2	Outputs LCD backlight control signal. Low : While LCD backlight is OFF.
6	FSW	Outputs high-pass filter's characteristics select signal.
7	HORN	Outputs external device control signal. High : When matched 2/5-tone signals are received.
12–55	SEG1–SEG40, COM1–COM4	Output ports for LCD control signal.

4-5-2 OUTPUT EXPANDER (MAIN unit; IC7)

Pin number	Port name	Description
1–3	T1–T3	Output tunable band pass filter control signals.
4	T4	Output port for tunable band pass filter control signal while receiving. output power control signal while transmitting.

4-5-3 CPU (MAIN unit; IC20)

Pin number	Port name	Description
1	DSDA	I/O port for data signals from/to the D/A converter (IC7).
2	DAST	Outputs strobe signals for the level controller (or D/A converter) (IC6).
8, 9	LINH, LCS	Output ports for LCD control signals to the LCD driver (FRONT unit; IC1)
10	LCK	Outputs clock signal for the LCD driver (FRONT unit; IC1)
11	LSO	Outputs data signals for the LCD driver (FRONT unit; IC1)
13	PLST	Outputs strobe signals for the PLL IC (IC4).
15	FSW2	Outputs control signal for the PLL IC (IC4).
16	TXC	Outputs R8 regulator circuit (Q26, Q30, D24) control signal.
17	TMUT	Outputs T8 regulator circuit (Q25, Q29, D23) control signal.
18	AFON	Outputs control signal for the AF regulator circuit (Q39, Q40, D31). High : While AF amplifier (IC8) is activated.
19	NWC	Outputs IF bandwidth control signal. High : While IF bandwidth is narrow.
20	DDSD	Input port for the data signals from the DTMF decoder (IC19).
21	DDAC	Outputs clock signal to the DTMF decoder (IC19).
22	SO	Outputs data signals to the PLL IC (IC4), level controller (or D/A converter) (IC6), compander IC (IC14) and optional board (connect to J1).
23	SI	Input port for the clock signal from the optional board via J1.
24	SCK	Outputs clock signal to the PLL IC (IC4), level controller (or D/A converter) (IC6), D/A converter (IC7), compander IC (IC14) and optional board (connect to J1).
25	CCS	Outputs chip select signal for the optional board via J1.
26–28	KR2–KR0	Input ports for the key matrix.
29	PTTO	Input port for the PTT switch from the optional board via J1. Low : External PTT switch is ON.
30	HANG	Input port for the microphone hanger detection signal. Low : Microphone on hook
31	BUSY	Outputs BUSY detection signal for the optional board via J1.

CPU (IC20)—continued

Pin number	Port name	Description
32	RMUT	Input port for AF mute signal from the optional board via J1.
33	MMUT	Input port for MIC mute signal from the optional board via J1.
34–36	OPT1–OPT3	I/O ports for the optional board control signals.
37	NOIS	NOIS signal input port from the FM IF IC (MAIN unit; IC1) for noise squelch operation.
38	POSW	Input for the POWER switch. Low : While POWER switch is pushed.
39	DDST	Input port for DTMF detection signal from the DTMF decoder (IC19).
40	IGSW	Remote power control signal input port from the external connector (J8).
41	PWON	Outputs control signal for the power switching circuit (Q24, Q23) via D28.
43	SENC	Outputs single tone signal.
44	BEEP	Outputs beep audio signals.
45	SDEC	Single tone signal input port for decoding from the LPF (IC21c).
46	CDEC	CTCSS/DTCS signals input port for decoding from the LPF (IC5).
47	ULCK	Input port for the PLL unlock signal from the PLL IC (IC4).
48	BATV	Input port for the overvoltage detection from the connected power supply.
49	LVIN	Input port for the PLL lock voltage.
50	RSSI	Input port for receiving signal strength level detection.
51	TEMP	Input port for the transceiver's internal temperature.
52	AFVI	Input port for the AF volume control (FRONT unit; R12). High : [VOL] is maximum clockwise.
55	EPTT	Input port for the PTT switch from the external connector (J6). Low : External PTT switch is ON.
59	RES	Input port for the reset signal.
68	CLO	Output port for the cloning signal.
69	CLI	Input port for the cloning signal.
70	CSFT	Outputs CPU clock shift signal.
71	DUSE	Outputs cut-off frequency control signal to the low-pass filter (IC5) for CTCSS/DTCS switching.
74	XCTS	Input port for the connected modem unit via external connector (J9).

CPU (IC20)—continued

Pin number	Port name	Description
75	XRTS	Output port for the connected modem unit via external connector (J9).
76	XTXD	Input port for serial data signals from the connected MAP27 unit via external connector (J9).
77	XRXD	Outputs serial data signals for the connected MAP27 unit via external connector (J9).
79	NTXD	Output serial data signals (data format is in accordance with NMEA0183) for the connected unit via external connector (J8).
80	NRXD	Input port for serial data signals (data format is in accordance with NMEA0183) from the connected unit via external connector (J8).
81	CIRQ	Input port for interruption signal from the optional board via J1
88	DIM	Input port for the LCD backlight control signal from the external connector (J6).
89–91	CENC2–CENC0	Output ports for the CTCSS/ DTCS signals.
92	AFCL	Outputs reset signal for the compander IC (IC14).
94, 95	AMSK, ADIN	Output control signals for the compander IC (IC14).
96	APST	Outputs strobe signals to the compander IC (IC14).
97	PMFM	Outputs control signal for the MSK PM/FM switching circuit (IC15).
98	ESDA	I/O port for the data signals from the EEPROM (IC23).
99	ESCL	Outputs clock signal for the EEPROM (IC23).
100	PA	Outputs MIC audio select signal for the analog switch (IC25). Low : While "Public-address" function is ON.