SECTION 4 CIRCUIT DESCRIPTION

4-1 RECEIVER CIRCUITS

4-1-1 ANTENNA SWITCHING CIRCUIT

The antenna switching circuit functions as a low-pass filter while receiving and a resonator circuit while transmitting. The circuit does not allow transmit signals to enter receiver circuits.

Received signals enter the antenna connector (J1) and pass through the low-pass filters (L1–L3, C2, C3, C8–C10). The filtered signals are passed through the ¼ type antenna switching circuit (D5, D6, L5) and then applied to the RF circuit.

4-1-2 RF CIRCUIT

The RF circuit amplifies signals within the range of frequency coverage and filters out-of-band signals.

The signals from the antenna switching circuit pass through the two-stage bandpass filters (D7, D8, L8, L9). The filtered signals are amplified at the RF amplifier (Q1) and then enter the three-stage bandpass filters (D9–D11, L12, L13) to suppress unwanted signals.

D7–D11 employ varactor diodes, that are controlled by the PLL lock voltage, to track the bandpass filter. These varactor diodes tune the center frequency of an RF passband for wide bandwidth receiving and good image response rejection.

4-1-3 1ST MIXER AND 1ST IF CIRCUITS

The 1st mixer circuit converts the received signal to a fixed frequency of the 1st IF signal with the PLL output frequency. By changing the PLL frequency, only the desired frequency will be passed through a pair of crystal filters at the next stage of the 1st mixer.

The RF signals from the bandpass filter are mixed with the 1st LO signals coming from the VCO circuit via the buffer amplifier (Q3) at the 1st mixer circuit (Q2) to produce a 30.875 MHz 1st IF signal. The 1st IF signal is passed through a pair of crystal filters (FI1) in order to obtain wide selection capability and to pass only the desired signals. The filtered signal is applied to the 2nd IF circuit after being amplified at the 1st IF amplifier (Q4).

4-1-4 2ND IF AND DEMODULATOR CIRCUITS

The 2nd mixer circuit converts the 1st IF signal to a 2nd signal. The double superheterodyne system (which conver receive signals twice) improves the image rejection ratio ar obtains stable receiver gain.

The 1st IF signal from the IF amplifier (Q4) is applied to th 2nd mixer section of the FM IF IC (IC1, pin 16) and is th mixed with the 2nd LO signal for conversion to a 455 kHz 2 IF signal.

IC1 contains the 2nd mixer, local oscillator, limiter amplifi quadrature detector, active filter and audio amplifier circu The local oscillator section and X1 generate 30.420 MHz the 2nd LO signal.

• Wide and narrow types (MAIN unit)

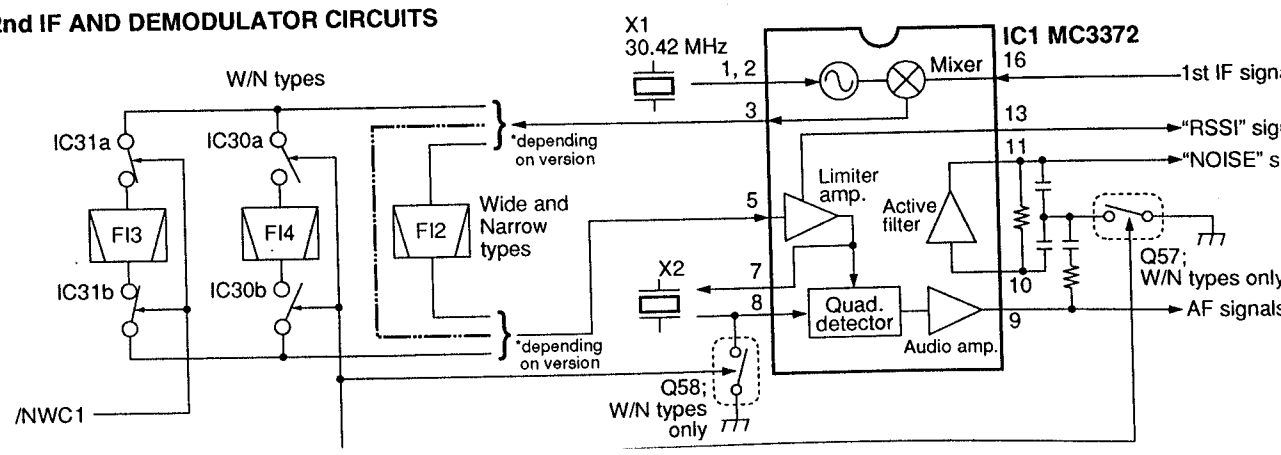
The 2nd IF signal from the 2nd mixer (IC1, pin 3) pass through the ceramic filter (FI2) to suppress unwanted h erodyne frequencies. The filtered signal is amplified at limiter amplifier section (pin 5) and applied to the quadrat detector section in the FM IF IC to demodulate the 2nd IF s nal into AF signals using the ceramic discriminator (X2). T demodulated AF signals are output from pin 9 of the IC a applied to the AF circuit via the receiver mute circuit.

• Wide/Narrow types (MAIN-A unit)

The 2nd IF signal from the 2nd mixer (IC1, pin 3) pas through either one of 2 ceramic filters (FI3: Narrow, Wide) to suppress unwanted heterodyne frequencies either one of 2 N/W switches (IC30:Wide, IC31: Narrow). filtered signal is applied to the quadrature detector sectio the FM IF IC to demodulate the 2nd IF signal into AF sig using the ceramic discriminator (X2) after being amplifie the limiter amplifier section (pin 5). The demodulated AF nals are output from pin 9 of the IC and applied to the AF cuit via the receiver mute circuit.

The N/W switches (IC30, IC31) select a ceramic filter (F FI4), and the other N/W switches (Q57, Q58) adjusts input level to the FM IF IC (IC1, pins 9, 10) to switch bandwidth depending whether the /NWC and NWC sig from the CPU (IC23, pins 24, 25) have wide or narrow tings.

• 2nd IF AND DEMODULATOR CIRCUITS



4-1-5 AF CIRCUIT

The AF signals from the FM IF IC (IC1, pin 9) are amplified at the AF amplifier (IC2) and are then applied to the high-pass filter circuit (IC3a/b). The high-pass filter characteristics are controlled by the HFSW signal from the CPU (IC20, pin 58). When the HFSW signal level is high, the cut-off frequency is shifted higher to remove CTCSS or DTCS signals.

The filtered AF signals from the high-pass filter (IC3, pin 1) are passed through the de-emphasis circuit (R68, C74) with frequency characteristics of –6 dB/octave, and are then applied to the electronic volume controller (IC7) via the AF mute switch (Q6).

The output AF signals from the electronic volume controller (IC7, pin 9) are applied to the AF power amplifier (IC8) to drive the speaker.

4-1-6 RECEIVE MUTE CIRCUITS

• NOISE SQUELCH

A squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals, the squelch circuit switches the AF mute switch.

Some noise components in the AF signals from the FM IF IC (IC1, pin 9) are passed through the active filter section in the IC (pins 10, 11). The N/W switch (Q57) adjusts the input noise level to the IC between wide and narrow bandwidths. (Wide/Narrow types only)

The noise signals from the FM IF IC (IC1, pin 11) are passed through the level controller (IC5, pins 21, 22), and are then converted into pulse-type signals (NOIS) at the noise detector circuit (Q9, Q10).

The NOIS signal from the noise detector (Q10) is applied to the CPU (IC20, pin 19). The CPU then analyses the noise condition and controls the AMUT and SP ports to toggle the AF mute switches (Q6, Q7).

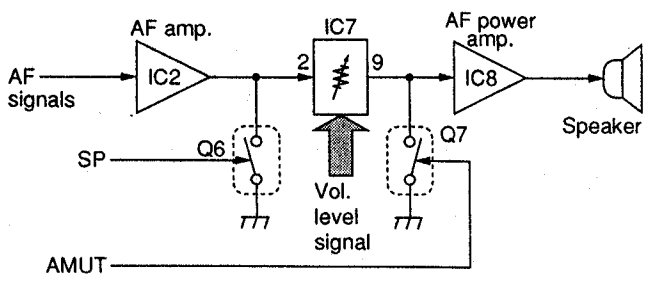
• CTCSS AND DTCS

A portion of the AF signals from the AF amplifier (IC2) pass through the low-pass filters (IC4a/b) and are then amplified at the tone amplifier (IC28a). The signals are applied to the CTCSS decoder in the CPU (IC20, pin 98) to control the AMUT and SP ports.

When the DTCS system is in use, the amplified signals are converted into digital signals at IC28b, then applied to the DTCS decoder in the CPU (IC20, pin 23).

The LFSW port (IC20, pin 62) controls the low-pass filter (IC4a) characteristics to shift the cut-off frequency for CTCSS and DTCS separately.

• AF AND RECEIVE MUTE CIRCUITS



4-2 TRANSMITTER CIRCUITS

4-2-1 MICROPHONE AMPLIFIER CIRCUIT

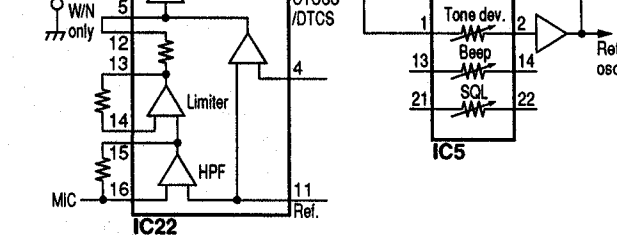
The microphone amplifier circuit amplifies audio signals fron the microphone, within +6 dB/octave pre-emphasis charac teristics, to a level needed for the modulation circuit.

The AF signals (MIC) from the FRONT unit via J5 (pin 10) ar passed through the audio switch (IC10, pins 5, 6). Whil transmitting, the MCON signal from the CPU (IC20, pin 79 becomes high, and the AF signals pass to the microphon amplifier circuit. The applied signals are amplified at th microphone amplifier (IC22) via the preamplifier (IC21b). Th amplified signals are applied to the limiter amplifier in IC22.

The entered signals are pre-emphasized with +6 dB/octav at a limiter amplifier, then passed through a splatter filter sec tion in IC22. The output signals from pin 8 pass through th level controller (IC5, pins 4, 3) and are then applied to th modulation circuit (D23).

In addition to the Wide/Narrow types, the N/W switch is cor nected to the input (N/W switch; Q65) and output (N/W switch; Q63) lines of the splatter filter circuit for each. Q63 controlled by the "NWC1" and Q65 is controlled by th "/NWC1" signal coming from the CPU (IC23, pins 24, 25) t adjust filter cut-off frequency (by Q65) and maximum fre quency deviation (by Q63).

• MICROPHONE AMPLIFIER CIRCUIT



4-2-2 MODULATION CIRCUIT

The modulation circuit modulates the VCO oscillating sign (RF signal) using the microphone audio.

The AF signals from the level controller (IC5) change th reactance of a varactor diode (D23) to modulate the oscilla ed signal at the Tx VCO circuit (Q23). The modulated VC signal, RF signal, is amplified at the buffer amplifiers (Q1 Q20) and is then applied to the drive amplifier circuit via th T/R switch (D17).

CTCSS/DTCS signals from the level controller (IC5, pin are amplified at IC21a, and are applied to the reference osc lator circuit (X3) to modulate the oscillated signal.

4-2-3 DRIVE/POWER AMPLIFIER CIRCUITS

The drive amplifier circuit amplifies the VCO oscillating sign to the level needed at the power amplifier.

The signal from the buffer amplifier (Q20) passes through the T/R switch (D17), and is amplified by the drivers (Q15–Q17) and the power module (IC11) to obtain 25 W (IC-F2010) or 35 W (IC-F2020) of RF power.

The amplified signal is passed through the antenna switching circuit (D4), low-pass filter and APC detector, and is then applied to the antenna connector.

The collector voltages for the driver (Q16) come from the MT8V regulator (Q38, D28). The transmit mute switch (Q39) controls the regulator when transmit mute is necessary.

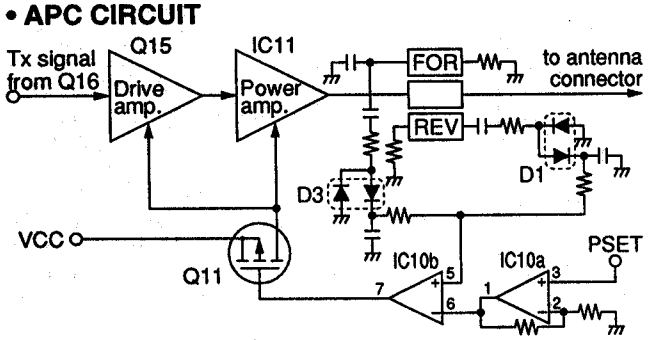
4-2-4 APC CIRCUIT

The APC circuit protects the power module (IC11) from a mismatched output load and stabilizes the output power.

The APC detector circuit detects forward signals and reflected signals at D3 and D1 respectively. The combined voltage is at a minimum level when the antenna impedance is matched to 50 Ω and is increased when it is mismatched.

The detected voltage is applied to the inverse amplifier (IC10b, pin 5), and the power setting voltage (PSET) is applied to the other input (IC10b, pin 6) via the amplifier (IC10a). When antenna impedance is mismatched, the detected voltage exceeds the power setting voltage. Then the output voltage of the inverse amplifier (IC10b, pin 7) controls the input current of the driver (Q15) and the power module (IC11) to reduce the output power via the APC driver (Q11).

• APC CIRCUIT



4-3 PLL CIRCUITS

4-3-1 PLL CIRCUIT

A PLL circuit provides stable oscillation of the transmit frequency and the receive 1st LO frequency. The PLL circuit consists of the PLL IC, charge pump and loop filter and employs a pulse swallow counter.

Oscillated signals from the VCO pass through buffer amplifiers (Q19, Q18) are prescaled in the PLL IC (IC12, pin 11) based on the divided ratio (N-data). The PLL IC (IC12) detects the out-of-step phase using the reference frequency and outputs it from pin 6. The output signal is passed through the charge pump (Q30–Q33) and loop filter (R154/C181, R153/C179), and is then applied to the VCO circuit as the lock voltage.

The accelerator switch (IC13a/b) selects the effective loop filter to accelerate the PLL lock up speed.

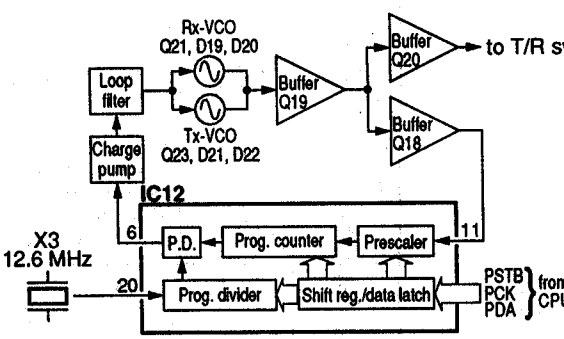
The lock voltage is also used for the receiver tuneable ba pass filters to match the filter's center frequency to desired receive frequency. The lock voltage is amplifie the buffer amplifier (Q29) and is then applied to the bandp filters (D8–D11).

4-3-2 VCO CIRCUIT

The VCO circuit contains separate Rx (Q21, D19, D20) Tx (Q23, D21, D22) VCOs. The oscillated signal is amp at the buffer amplifier (Q19, Q20) and is then applied to T/R switch (D17, D18). Then the receive 1st LO sign applied to the 1st mixer circuit (Q2) via the buffer amp (Q3) and the transmit signal to the driver (Q17).

A portion of the signal from the buffer amplifier (Q19) is back to the PLL IC (IC12, pin 11) via the buffer amp (Q18) as the comparison signal.

• PLL CIRCUIT



4-4 POWER SUPPLY CIRCUITS

VOLTAGE LINES

LINE	DESCRIPTION
HV	The voltage from the external power conne
VCC	Same voltage as the HV line passed throug power control circuit (Q12) controlled by P signal from the CPU (IC20, pin 67).
CPU5V	Common 5 V converted from the HV line 5V regulator circuit (IC25). This voltage is plied to the CPU regardless of the power s
+5V	Common 5 V converted from the VCC line +5V regulator circuit (Q42, Q43, D30) usin CPU5V line voltage as the reference.
+8V	Common 8 V converted from the VCC line +8V regulator circuit (IC16).
R8V	Receive 8 V converted from the VCC line R8V regulator circuit (Q36, D27) using the line voltage as the reference and controll VRX signal from the CPU (IC20, pin 66).
T8V	Transmit 8 V converted from the VCC line T8V regulator circuit (Q40, D29) using th line voltage as the reference and controll VTX signal from the the CPU (IC20, pin 65
MT8V	Transmit 8 V converted from the VCC line MT8V regulator circuit (Q38, D28) using th line voltage as the reference and controll TMUT signal from the the CPU (IC20, pin

4-5 PORT ALLOCATIONS

CPU (IC20)

Pin number	Port name	Description
1	AFV	Input port for the volume control.
11	SIFT	Outputs CPU clock shift signal.
19	NOIS	Input port for noise signals (pulse-type) for noise squelch operation.
21	POSW	Input port for the power switch. Low : While power switch is pushed
23	DDEC	Input port for DTCS decoding.
24	/NWC	Outputs N/W switch control signals. Low : While narrow is selected (Wide/Narrow types only)
25	NWC	Outputs N/W switch control signals. High : While narrow is selected (Wide/Narrow types only)
32–35	CTN3–CTN0	Output ports for CTCSS/DTCS signals.
36	PTTO	Outputs the PTT control signal. Low : While transmitting
39	PTTI	Input port for the PTT control signal from PTTO port.
42	ECK	Outputs clock signal for EEPROMs.
43	ESI	Input port for serial signal from EEPROMs.
44	ESO	Outputs serial signal for EEPROMs.
45, 46	ECS1, ECS2	Output ports for EEPROM select signals. ECS1: For internal EEPROM (IC27) ECS2: For optional EEPROM
47	PDA	Outputs data signal for the PLL IC (IC12).
48	PCK	Outputs clock signal for the PLL IC (IC12).
49	UNLK	Input port for the PLL unlock signal. High : During unlock
50	PSTB	Outputs strobe signals for the PLL IC (IC12).
51	PLLT	Outputs PLL accelerator control signal. High : While scanning, etc.
52	PLLR	Outputs PLL accelerator control signal. High : While transmitting
53	DDA	Outputs data signal for the level controller (IC5).
54	DCK	Outputs clock signal for the level controller (IC5).
55	DSTB	Outputs strobe signals for the level controller. (IC5)
56	PASP	Outputs "Public-address" mute signal. High : While PA and Ext. SP functions are not used
57	SP	Outputs the mute switch (Q7) control signal (incl. beep). High : While squelched, etc.
59	HFSW	Outputs high-pass filter's characteristics select signal. High : During CTCSS operation
59	PA	Outputs mic. audio select signal to the audio switch (IC25). High : While "Public-address" function is ON
60	TMUT	Outputs MT8V regulator circuit (Q38, D27) control signal. High : While transmit is muted
61	HORN	Outputs high level control signal for the pre-set time to the connected external unit when matched 2- or 5-tone code is received.
64	DIM	Input port for an external LCD backlight brightness control signal. Low : LCD backlight is dimmed
65	VTX	Outputs the T8V regulator circuit (Q38, D28) control signal. Low : While transmitting
66	VRX	Outputs the R8V regulator circuit (Q36, D27) control signal. Low : While receiving
67	PWON	Outputs the power control circuit (Q12) control signal. High : During power ON
79	MCON	Outputs mic. audio mute control signal to the audio switch (IC25). High : While DTMF signals are being transmitted, etc.
80	AMUT	Outputs the AF mute switch (Q5) control signal. High : While squelched, etc.
81	MMUT	Input port for microphone audio mute control signal from an optional unit.
82	RMUT	Input port for receive audio mute control signal from an optional unit.
84	BUSY	Outputs busy signal for an optional unit.
85	AFON	Input port for the AF amplifier ON signal from an optional unit.
90	BEEP	Outputs beep audio signals.
91	DTMF	Outputs DTMF audio signals.
98	CDEC	Input port for CTCSS decoding.
99	RSSI	Input port for receiving signal strength level detection.