RPT503 Circuit Description
DRAFT

To be read with reference to drawing 2961-7866.

Multiple ICs (quad op amps, multiple logic gates etc.) are denoted in this description by their output pin. E.g. IC32 (pin 8) is the operational amplifier comprising pins 9 and 10 inputs and pin 8 output.

Sheet 1

XL7 is the main reference oscillator for the transmitter. It operates at 13.000MHz. Stability is 2ppm from –25 to +55 deg C and output is 0.8V p-p clipped sine. The low frequency component of the data modulation is applied to the control input on pin 1. This gives FSK modulation. Three eepots are used to set various frequencies:

1. IC53A sets FSK frequency for data level high
2. IC53B sets FSK frequency for data level low
3. IC52A sets centre frequency for analogue modulation.

IC64 routes the data (DATA-A) to the appropriate eepot depending on the level of the mode line (A/D.)

The three potentiometers apply dc levels to buffer amplifier IC61. The output from this stage feeds the control input of the reference oscillator XL7 via low pass filter IC62.

The position of the eepot slider is governed by the microcontroller IC60 on sheet 3

Sheet 2

The circuits of sheet 2 control the high frequency component of the modulation.

IC46B sets the level for the high frequency component of the data modulation. This will also effect the analogue modulation, so data modulation must be adjusted before the analogue modulation is set up.

IC32 (pin 8) is a buffer amplifier.

IC32 (pin 7) is a combiner which combines the data modulation from IC31 (pin7) and the analogue modulation from IC46A.

Audio (analogue) from sheet 3 passes through low pass filter circuit IC32 (pin1) and then eepot IC46A which sets the analogue modulation limiting level.

Data (DATA-B) from sheet 3 is split into the high and low frequency paths.

High frequency path passes through IC18 (pin3) and IC31 (pin1) which convert the signal from logic to analogue levels.

IC31 (pin7) is a low pass filter which sets the modulated data rise time.

Low frequency path passes through IC33 (pin 3), which is set by R181 as a buffer. If R158 is fitted instead of R181, then this stage would invert.

IC66 together with IC67 delay the data in the low frequency path so that it reaches the modulator at the same time as the high frequency component.

Sheet 3

The circuits of sheet 3 are the interface and controller circuits.

IC60 is the microcontroller which carries out the "housekeeping" for the transmitter. It sets up synthesizer and eepot values as well as monitoring levels and error conditions. It communicates with the outside world via RS232 interface IC58 which connects to a PC for setup purposes.

SK8 is the line interface connector for modulation/control and for line synchronisation. 600 ohm line input from the encoder passes through isolating transformer T3 to level adjuster circuit IC8 (pin 14.) Line input level is set by eepot IC45a. IC31 (pin 8) with diodes D43 and capacitor C310 form a rectifier which monitors the line input level. IC31 (pin14) forms a buffer which feeds the line level signal to a D/A converter in IC60. The line level can thus be monitored on a connected PC in order to adjust eepot IC45a to the correct value.

IC8 (pin 1), D42, TR21 and TR22 form the vox circuit. The vox key signal is connected to Micro IC60.

Eepot IC45b is used to set the speech (analogue) modulation level.

IC8 (pin 7) is the pre-emphasis circuit.

IC8 (pin 8) is a unity gain buffer.

IC3 is a switched capacitor low pass filter which limits the bandwidth of the speech modulation. The cut off point is determined by the clock frequency which is set by capacitors C144 and C145. C145 lowers the cut off point and is fitted for 12.5kHz bandwidth. Cut off frequencies are set at 3kHz for 25kHz bandwidth and 2.5kHz for 12.5kHz bandwidth. Audio output from IC3 goes to sheet 2.

IC19 is a 1200bd modem to demodulate data from the line input.

IC18 (pin 8) ensures that only valid data is presented to IC33 (pin 6.)

IC33 (pin 6) selects data polarity. When pin 5 is high the data is inverted in IC33 (pin 6.) When pin 5 is low data is fed through unchanged. The output from the polarity selector goes to sheet 2 (DATA-B.)

IC23 is the DTMF detector which decodes the DTMF transmitter control codes from the line input. These are interpreted by microcontroller IC60.

TR24 and TR25 interface and protect the external key and mode lines.
TR23 feeds the external error line.

Connector PL1 is the interface to the internal encoder (RPE500) if fitted.

Connector SK1 is the auxiliary connector. This is used for:

1. Flash programming the microcontroller
2. Programming and adjusting the transmitter over the RS232 interface from a PC.
3. External direct data, mode and key lines.
4. Error output (single open collector.)

Sheet 4

The circuits on sheet 4 are the main synthesizer.

Reference signal, 13MHz, is from sheet 1.

IC4 is the synthesizer system and comprises dividers and a phase detector. Values for a particular channel are loaded from the microcontroller IC60 on start up. C104, C311, C110, C111, R68 and R70 comprise the loop filter. R67 aids fast lock up.

IC68 is a buffer amplifier which feeds the loop control voltage to microcontroller IC60 so that it can be monitored during set up.

TR28 is the low noise VCO. Frequency is set by tuned line L1, CV1 and variable capacitance diodes D18 for loop feedback and D47 for modulation.

TR26 and TR27 are a cascade buffer amplifier. The output from the buffer is split in R133, R134 and R135. Part is fed back to the synthesizer IC4 to close the loop. The other part is fed to pre-driver IC28. IC28 has a gain of about 15dB and produces the RF DRIVE signal to sheet 5.

IC35 and IC37 are switched regulators, each providing switched 5V supplies to their respective circuits.

R106 and C108 filter the out of lock signal to TR12 and TR13 which drives the out of lock LED and signal back to IC60.

Sheet 5

The circuits of sheet 5 are the amplifiers which raise the signal level up to the 5 watts output required from the transmitter.

IC44 is the driver, fed by the RF DRIVE signal from sheet 4. Gain is approx 20 dB. To save power in standby and to reduce RF bleed through, the supply to IC44 is switched by TR29 and TR30 from the KEYLINE signal.

L23, L24 and associated capacitors form a low pass filter which passes about 15dBm to the power amplifier PM1.

PM1 amplifies the signal up to about 7W maximum. The output level is set by eepot IC52B which sets the control voltage to PM1 via buffer IC43.

L20, L21 and L22 with associated capacitors form a low pass filter to suppress harmonics generated in PM1.

D31 and D32 with their directional coupler formed from pcb tracks, monitor the forward and reverse power from SK9, the output connector. The two signals are amplified by IC41 and IC42 then fed to the microcontroller IC60 for monitoring.

C249 blocks dc to or from the output socket SK9.

R244 is to prevent the build up of any high static potential from SK9.

Sheet 6

Sheet 6 shows the main power connector SK10 or PL2 and the 5V regulator IC27. Also various power connections to ICs within the transmitter.

Sheet 7

Sheet 7 shows the line synchronisation circuit. When programming the RPT503 from the field programmer it is possible to set up as Master, Slave or No Line Synchronisation.

When set up as Master:

Analogue switch IC50 is on and Analogue switch IC51 is off.

The synthesiser chip, IC48, is used only as a programmable divider. A 13.000MHz signal from the reference oscillator XL7 (on sheet 1) is fed into fIN (IC48 pin 6.) IC48 is programmed by the microcontroller IC60 (on sheet 3) during initialisation to continuously divide the 13.000MHz signal down to 40kHz at Fo/LD output, pin 14. The 40kHz signal is a series of narrow pulses which is fed to D-type flip flop IC65 pin12. This flip flop divides the signal by 2 to produce a square waveform at 20kHz. Potential divider formed by R252, R256 and R257 reduces the signal level and feeds it into the 20kHz bandpass filter comprising IC49 (pin 7) and IC 49 (pin 14.) Output from the filter is a sine wave which is amplified by IC49 (pin 8) and fed out to the Line-Synchronisation Line via switch IC50, capacitor C267 and isolating transformer T8. The output level of the Line Synchronisation signal is adjusted via EPOT IC70A.

Synthesiser chip IC48 has its charge pump output set to open circuit by microcontroller IC60 during initialisation. This is so that there is no signal fed to the reference oscillator control to degrade its stability.

When set up as Slave:

Analogue switch IC50 is off and Analogue switch IC51 is on.

The synthesiser chip, IC48, is used as a phase locked loop. A 13.000MHz signal from the reference oscillator XL7 (on sheet 1) is fed into fIN (IC48 pin 6.) IC48 is programmed by the microcontroller IC60 (on sheet 3) during initialisation to divide this down to 5kHz.

The synchronising signal (20kHz sine wave) is isolated by transformer T8 and passes through C267, R384 and switch IC51 to the 20kHz bandpass filter comprising IC49 (pin 7) and IC 49 (pin 14.) This removes line noise from the signal. Output from the filter is then squared by IC49 (pin 1) and further squared by IC65 (pin 5.) This 20kHz square wave is then fed into the OSCIN input (pin 8) of the synthesiser chip IC48. IC48 divides the 20kHz down to 5kHz and compares it with the 5kHz from the divided 13.000MHz oscillator in a phase detector. An error signal is produced which is passed through the loop filter comprising C275, C274, R267, R360 and C351. This signal is fed back to the control voltage input of the 13.000 MHz oscillator to correct any error.

Transistors TR19 and TR20 monitor the lock detect output of IC48 via low pass filter R276 and C276. The microcontroller monitors the LineSyncFail signal.

IC71 is a voltage follower to monitor the control loop signal, but is not used (R381 not fitted.)

IC72 and D50 form a rectifier. This rectifies the 20 kHz output signal in Master mode or the input signal in Slave mode. The output of the rectifier is smoothed by R379 and C361 to produce a DC level representative of the amplitude of the 20kHz signal. This is buffered by voltage follower IC73 to produce signal LineSyncSetup. LineSyncSetup is monitored by an analogue to digital converter in IC60.

When set up as No Line Synchronisation:

Synthesiser chip IC48 has its charge pump output set to open circuit by microcontroller IC60 during initialisation. This is so that there is no signal fed to the reference oscillator control to degrade its stability.