REVISION					
DASH NO.	ECN	REV	DESCRIPTION	DATE	APPROVED

BASE-2A

Rev C

Schematic

SHEET Description

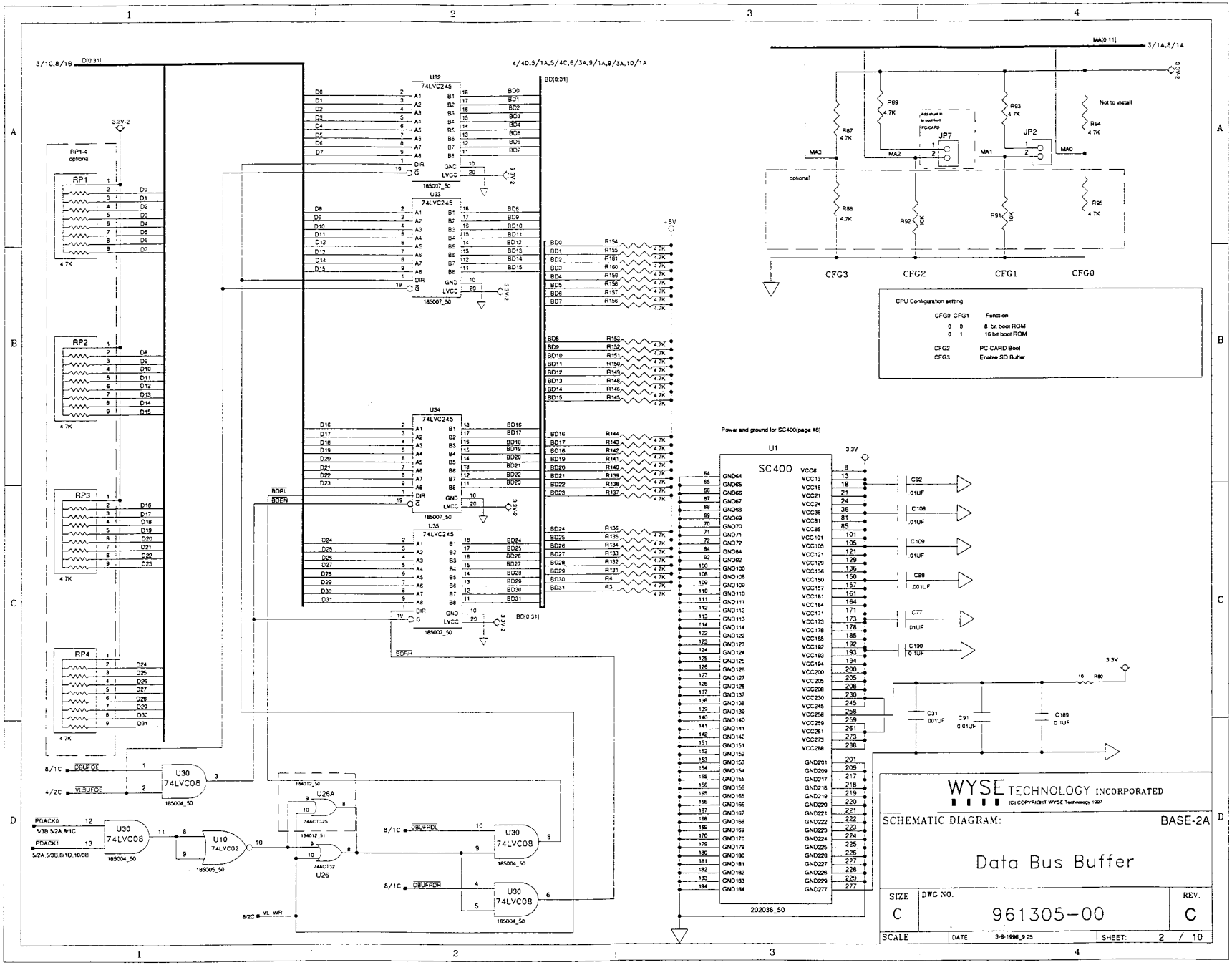
2	Data Bus Buffer
3	DRAM Bank 0,2 and Bank 1,3
4	FLASH Memory
5	Audio and Network
6	Graphics Controller
7	Video, Power Connectors and Bypass Cap.
8	System Controller
9	Serial and Parallel Ports
10	PC-Card Socket, ISA Connector and Keyboard Controller

Mars

PCB Layout Copy

3-11-1998_10:22

CONTRACT NO		WYSE TECHNOLOGY INCORPORATED (C) COPYRIGHT WYSE Technology 1997
APPROVAL	DATE	SCHEMATIC DIAGRAM: BASE-2A
DRAWN J.QIU;M.VU		Winterm BASE-2A Logic PCBA
CHK ROHIT LELE		
ENG T.WEY		
ISSUED		
THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO WYSE TECHNOLOGY USE OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN OFFICER OF WYSE TECHNOLOGY IS EXPRESSLY FORBIDDEN. COPYRIGHT (C) WYSE TECHNOLOGY 1997		SIZE C / DWG NO. 961305-00 / REV. C
		SCALE / DATE 3-11-1998_10:22 / SHEET 1 / 10


WYSE TECHNOLOGY INCORPORATED
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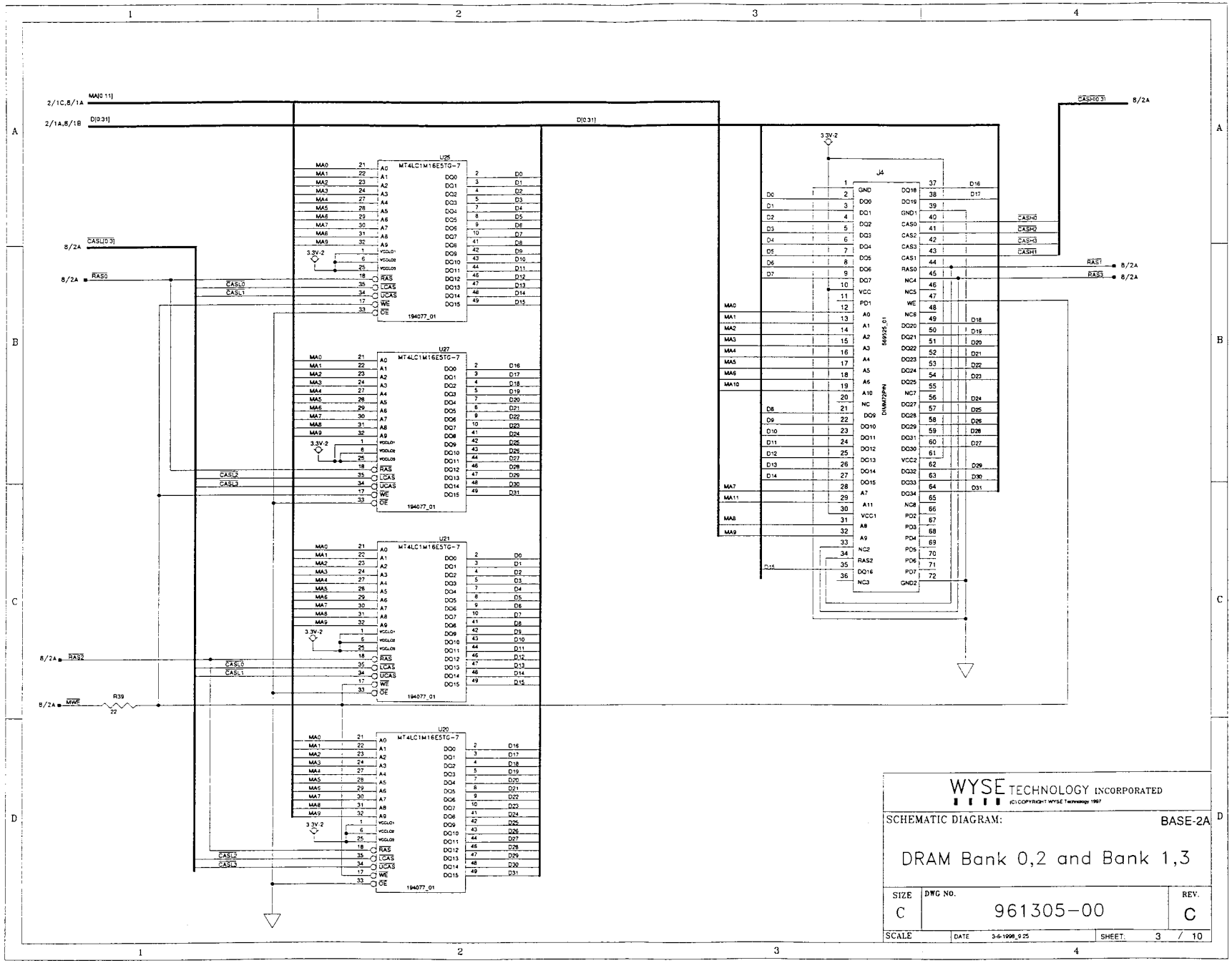
SCHEMATIC DIAGRAM:
BASE-2A
Data Bus Buffer
SIZE
C
DWG NO.
961305-00
REV.
C
SCALE
DATE
3-6-1998 9:25
SHEET:
2 / 10
U1
SC400
202036_50
U30
74LVC08
185004_50
U10
74LVC02
185005_50
U26A
74ACT32S
U26
74ACT32
U32
U33
U34
U35
74LVC245
185007_50
RP1
RP2
RP3
RP4
4.7K
RP1-4 optional
3.3V-2
+5V
3.3V
D[0:31]
BD[0:31]
3/1C,8/1B
4/4D,5/1A,5/4C,6/3A,9/1A,9/3A,10/1A
MA[0:11]
3/1A,8/1A
R87 4.7K
R88 4.7K
R89 4.7K
R92 10K
R93 4.7K
R91 10K
R94 4.7K
R95 4.7K
Not to install
optional
JP7
JP2
CFG3
CFG2
CFG1
CFG0
CPU Configuration setting
CFG0 CFG1 Function
0 0 8 bit boot ROM
0 1 16 bit boot ROM
CFG2 PC-CARD Boot
CFG3 Enable SD Buffer
Power and ground for SC400(page #8)
C92 .01UF
C108 .01UF
C109 .01UF
C89 .001UF
C77 .01UF
C190 0.1UF
C31 .001UF
C91 0.01UF
C189 0.1UF
R90 10
DBUFOE
VL_BUFOE
PDACK0
PDACK1
DBUFRDL
DBUFRDH
VL_WR
BDRL
BDEN
BDRH


2/1C,8/1A MA[0.11]
2/1A,8/1B D[0.31]
D[0.31]
8/2A CASU[0.3]
8/2A RAS0
8/2A RAS2
8/2A MWE
R39
22
U25
U27
U21
U20
MT4LC1M16E5TG-7
194077_01
3.3V-2
CASL0
CASL1
CASL2
CASL3
J4
DIMM72PIN
569525_01
CASH0.3 8/2A
CASH0
CASH2
CASH3
CASH1
RAS1 8/2A
RAS3 8/2A
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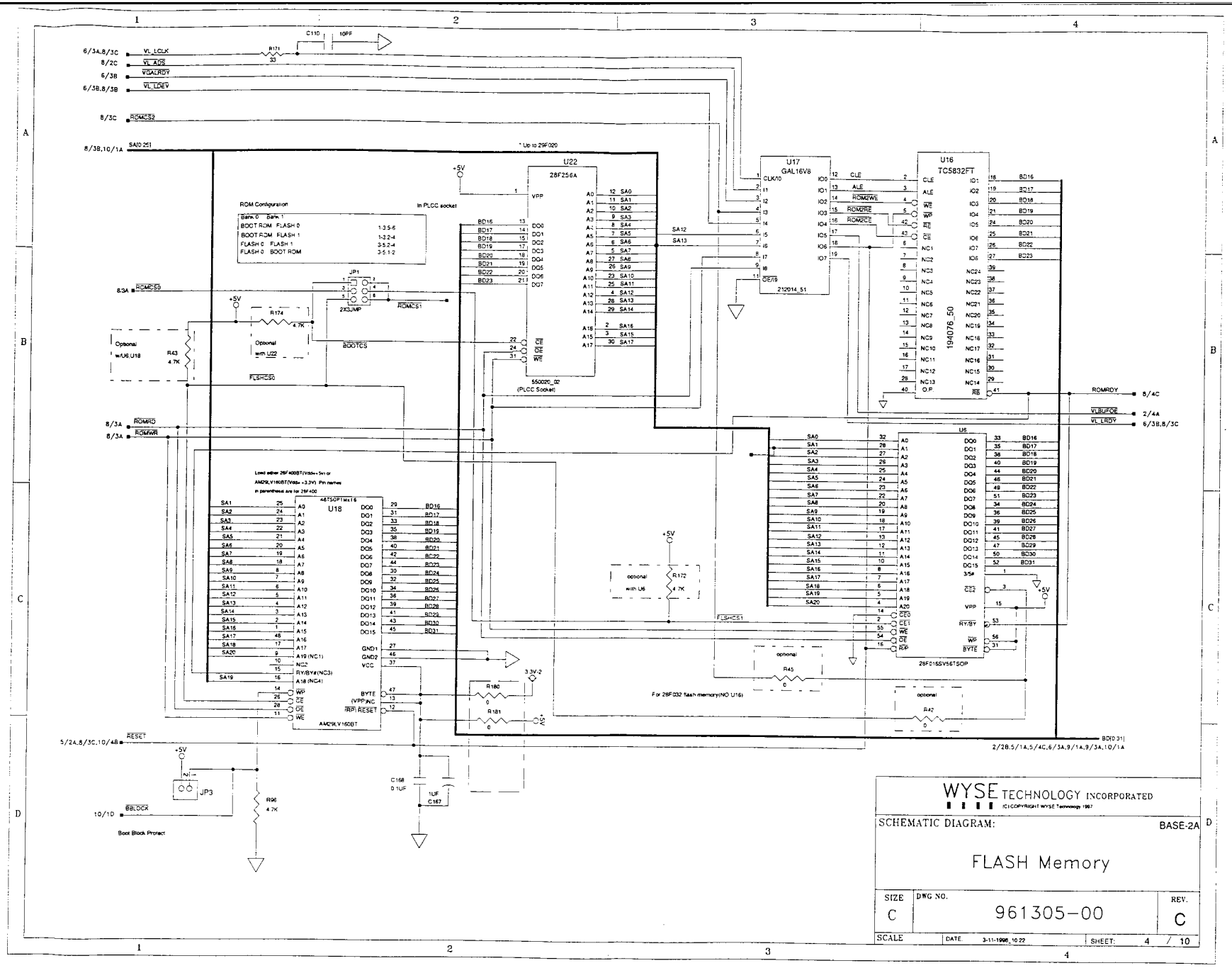
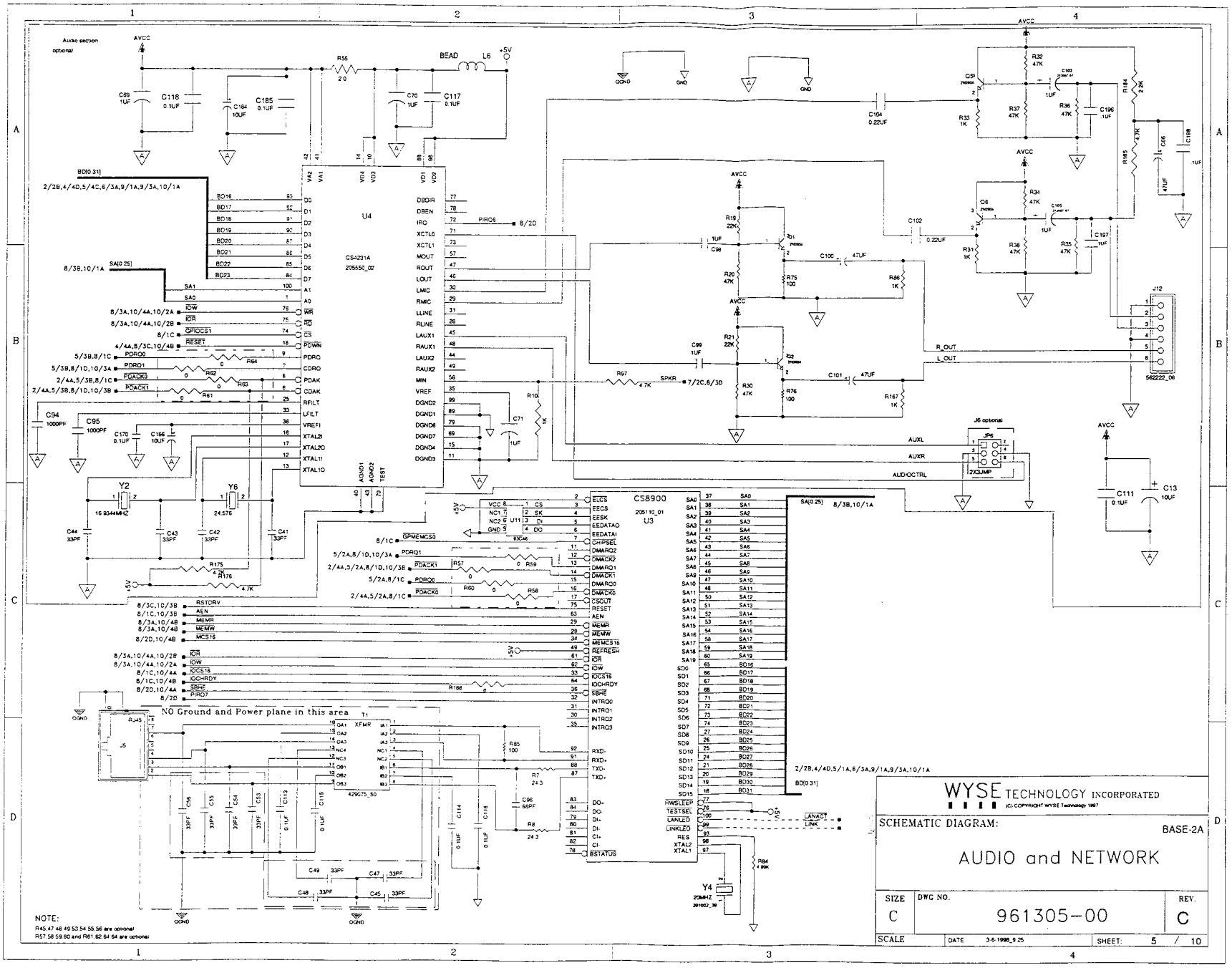
SCHEMATIC DIAGRAM:
BASE-2A
DRAM Bank 0,2 and Bank 1,3
SIZE
C
DWG NO.
961305-00
REV.
C
SCALE
DATE 3-6-1998_9:25
SHEET 3 / 10


WYSE TECHNOLOGY INCORPORATED
(C) COPYRIGHT WYSE Technology 1997
SCHEMATIC DIAGRAM:
BASE-2A
FLASH Memory
SIZE
C
DWG NO.
961305-00
REV.
C
SCALE
DATE 3-11-1998 10:22
SHEET: 4 / 10
U22
28F256A
U17
GAL16V8
U16
TC5832FT
194076_50
U18
AM29LV160BT
U6
28F015SV56TSOP
JP1
2X3JMP
JP3
ROM Configuration
Bank 0 Bank 1
BOOT ROM FLASH 0 1-3,5-6
BOOT ROM FLASH 1 1-3,2-4
FLASH 0 FLASH 1 3-5,2-4
FLASH 0 BOOT ROM 3-5,1-2
In PLCC socket
* Up to 29F020
550020_02
(PLCC Socket)
212014_51
Load either 28F400BT(Vcc=+5v) or
AM29LV160BT(Vcc= +3.3V) Pin names
in parenthesis are for 28F400
48TSOP14x18
For 28F032 flash memory(NO U16)
Boot Block Protect
VL_LCLK
VL_A0S
VGALRDY
VL_LDEV
ROMCS2
SA0:25
ROMCS0
ROMCS1
BOOTCS
FLSHCS0
FLSHCS1
ROMRD
ROMWR
RESET
BBLOCK
ROMRDY
VLBUFOE
VL_LRDY
BD[0:31]
2/28,5/1A,5/4C,6/3A,9/1A,9/3A,10/1A
8/4C
2/4A
6/3B,8/3C
Optional w/U6,U18
Optional with U22
optional with U6
optional
R43 4.7K
R174 4.7K
R172 4.7K
R96 4.7K
R180 0
R181 0
R45 0
R47 0
R171 33
C110 10PF
C168 0.1UF
C167 1UF
3.3V-2
+5V


Audio section optional
AVCC
BEAD
L6
+5V
R55
2.0
C69 1UF
C118 0.1UF
C184 10UF
C185 0.1UF
C70 1UF
C117 0.1UF
OGND
GND
C104 0.22UF
C102 0.22UF
C100 47UF
C101 47UF
C99 1UF
C98 1UF
R67 4.7K
SPKR
7/2C,8/3D
R10 1K
C71 1UF
R86 1K
R167 1K
R_OUT
L_OUT
J12
562222_06
J6 optional
JP6
2X3JMP
AUXL
AUXR
AUDIOCTRL
C111 0.1UF
C13 10UF
BD[0.31]
2/2B,4/4D,5/4C,6/3A,9/1A,9/3A,10/1A
8/3B,10/1A
SA[0.25]
U4
CS4231A
205550_02
PIRQ6
8/2D
8/3A,10/4A,10/2A
8/3A,10/4A,10/2B
8/1C
4/4A,8/3C,10/4B
5/3B,8/1C
5/3B,8/1D,10/3A
2/4A,5/3B,8/1C
2/4A,5/3B,8/1D,10/3B
C94 1000PF
C95 1000PF
C170 0.1UF
C166 10UF
Y2 16.9344MHZ
Y6 24.576
C44 33PF
C43 33PF
C42 33PF
C41 33PF
R175 4.7K
R176 4.7K
U11 93C46
CS8900
205110_01
U3
GPMEMCS0
PDRQ1
PDACK1
PDRQ0
PDACK0
RSTDRV
AEN
MEMR
MEMW
MEMCS16
REFRESH
IOR
IOW
IOCS16
IOCHRDY
SBHE
PIRQ7
R188 0
NO Ground and Power plane in this area
T1
XFMR
429075_50
J5
RJ45
R65 100
R7 24.3
R8 24.3
C96 68PF
C49 33PF
C47 33PF
C48 33PF
C45 33PF
Y4 20MHZ
391062_30
R64 4.99K
LANACT
LINK
NOTE:
R45,47,48,49,53,54,55,56 are optional
R57,58,59,60 and R61,62,64,64 are optional
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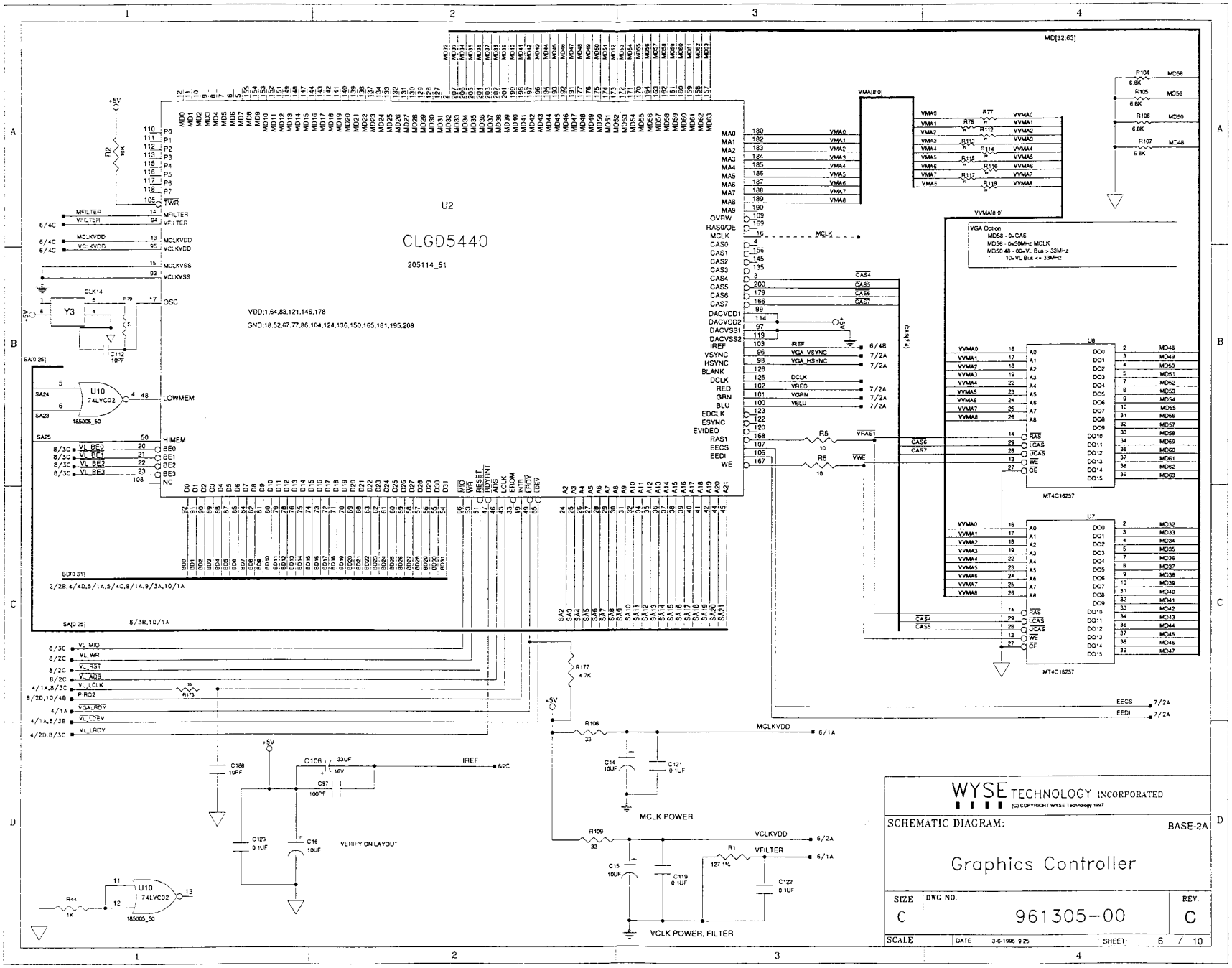
SCHEMATIC DIAGRAM:
BASE-2A
AUDIO and NETWORK
SIZE C
DWG NO. 961305-00
REV. C
SCALE
DATE 3-6-1998_9:25
SHEET: 5 / 10


U2
CLGD5440
205114_51
VDD:1,64,83,121,146,178
GND:18,52,67,77,86,104,124,136,150,165,181,195,208
U10
74LVC02
185005_50
Y3
U8
U7
MT4C16257
VGA Option.
MD58 - 0=CAS
MD56 - 0=50MHz MCLK
MD50 48 - 00=VL Bus > 33MHz
10=VL Bus <= 33MHz
MCLK POWER
VCLK POWER, FILTER
VERIFY ON LAYOUT
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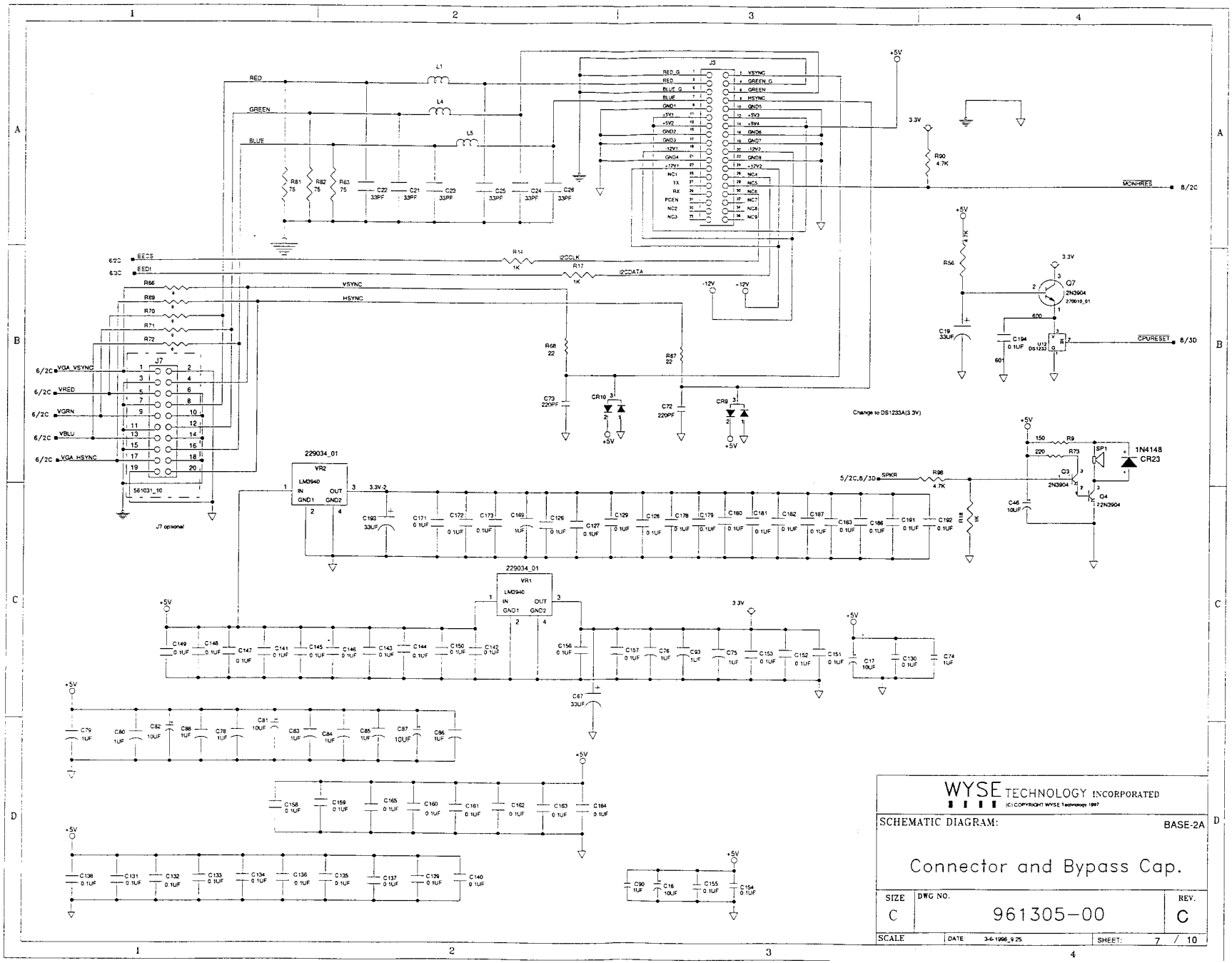
SCHEMATIC DIAGRAM:
BASE-2A
Graphics Controller
SIZE
C
DWG NO.
961305-00
REV.
C
SCALE
DATE
3-6-1998 9:25
SHEET:
6 / 10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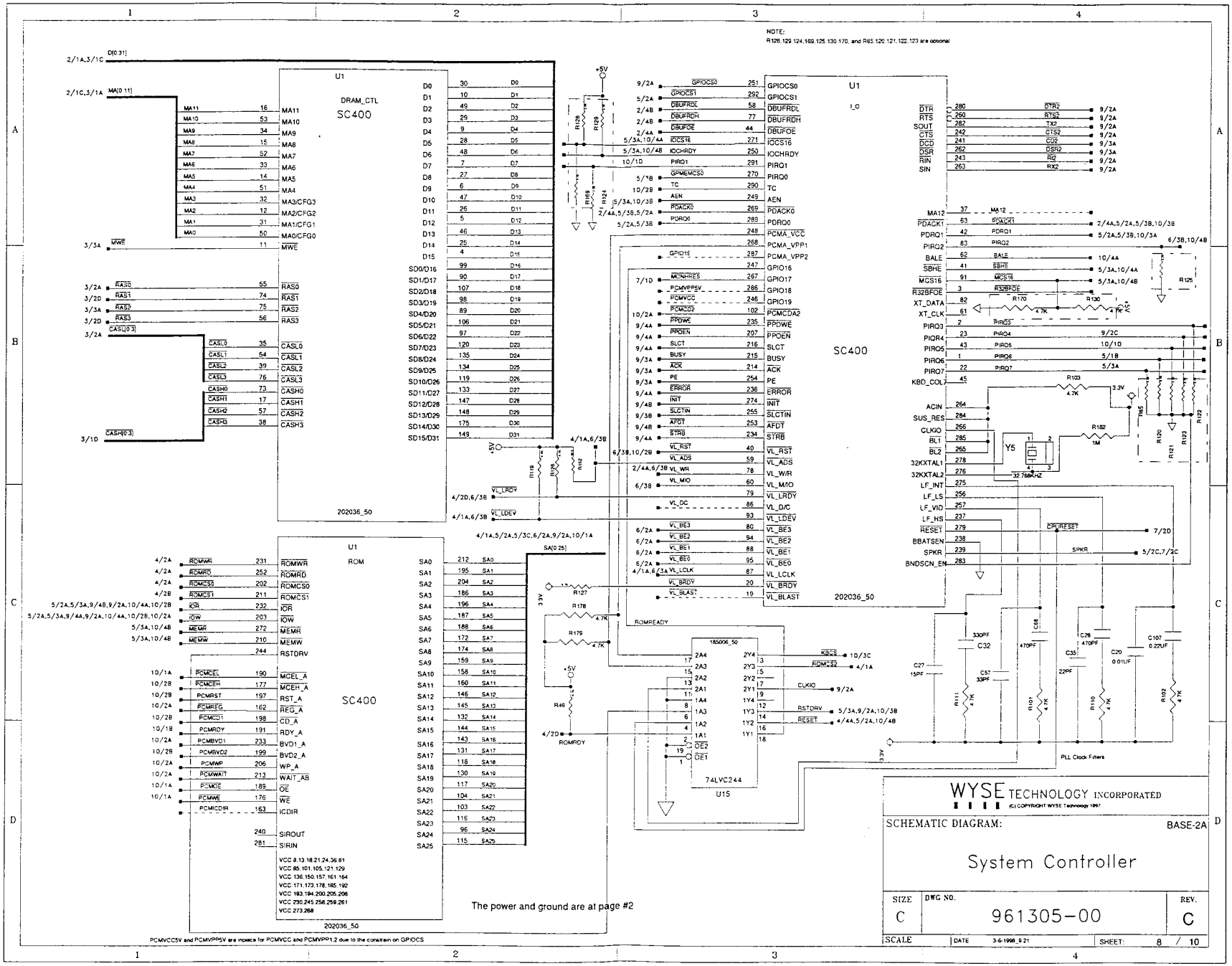
SCHEMATIC DIAGRAM:
BASE-2A
Connector and Bypass Cap.
SIZE
C
DWG NO.
961305-00
REV.
C
SCALE
DATE
3-6-1998_9:25
SHEET:
7 / 10
J7 optional
Change to DS1233A(3.3V)


NOTE:
R126,129,124,169,125,130,170, and R65,120,121,122,123 are optional
U1
DRAM_CTL
SC400
202036_50
U1
I_O
SC400
202036_50
U1
ROM
SC400
202036_50
74LVC244
U15
185006_50
Y5
32.768KHZ
PLL Clock Filters
The power and ground are at page #2
PCMVCC5V and PCMVPP5V are inpace for PCMVCC and PCMVPP1,2 due to the constrain on GPIOCS
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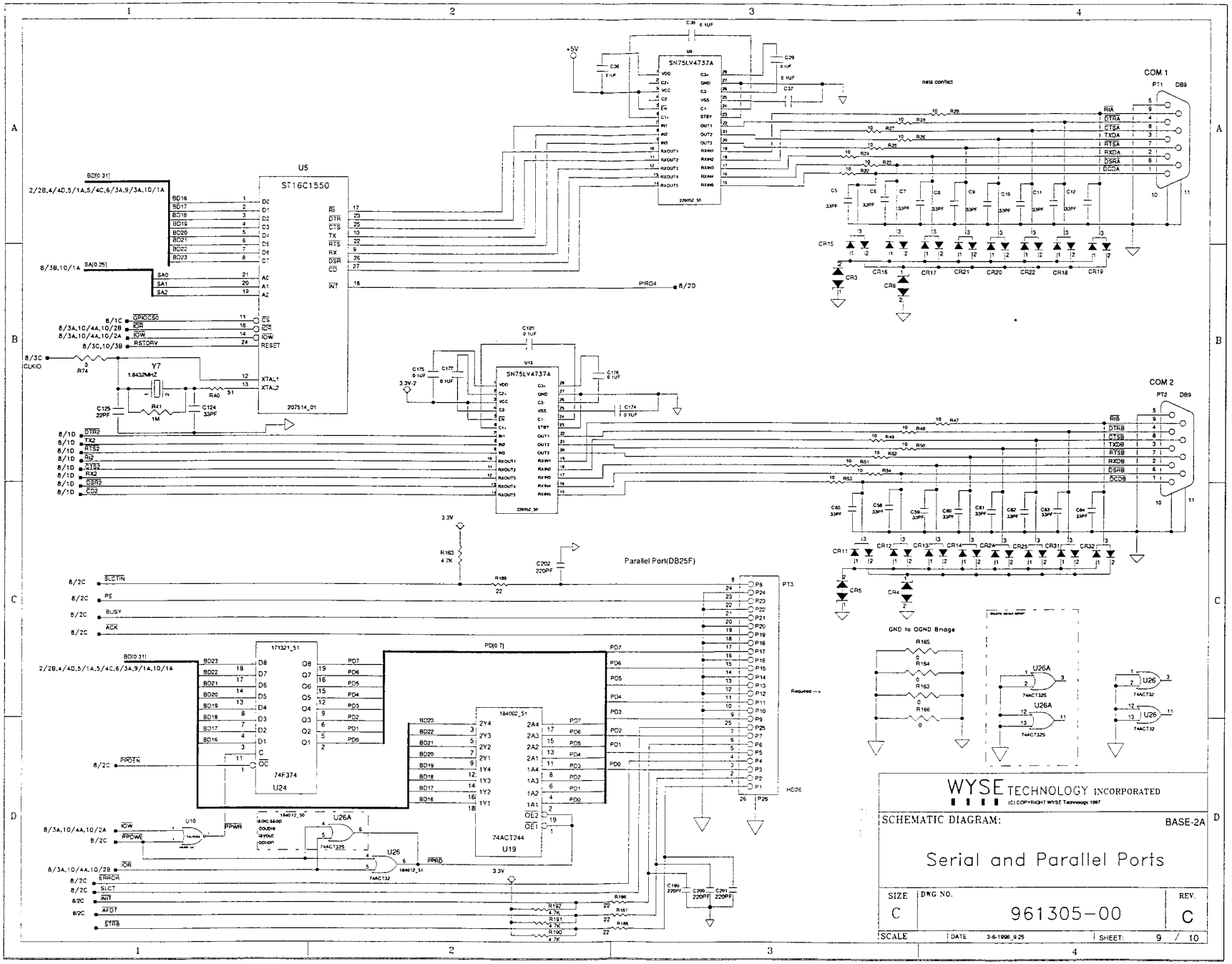
SCHEMATIC DIAGRAM:
BASE-2A
System Controller
SIZE
C
DWG NO.
961305-00
REV.
C
SCALE
DATE
3-6-1998, 9:21
SHEET:
8 / 10


U5
ST16C1550
U9
SN75LV4737A
U13
SN75LV4737A
COM 1
PT1
DB9
COM 2
PT2
DB9
Parallel Port(DB25F)
PT3
HD26
74F374
U24
74ACT244
U19
74ACT32
74ACT325
GND to QGND Bridge
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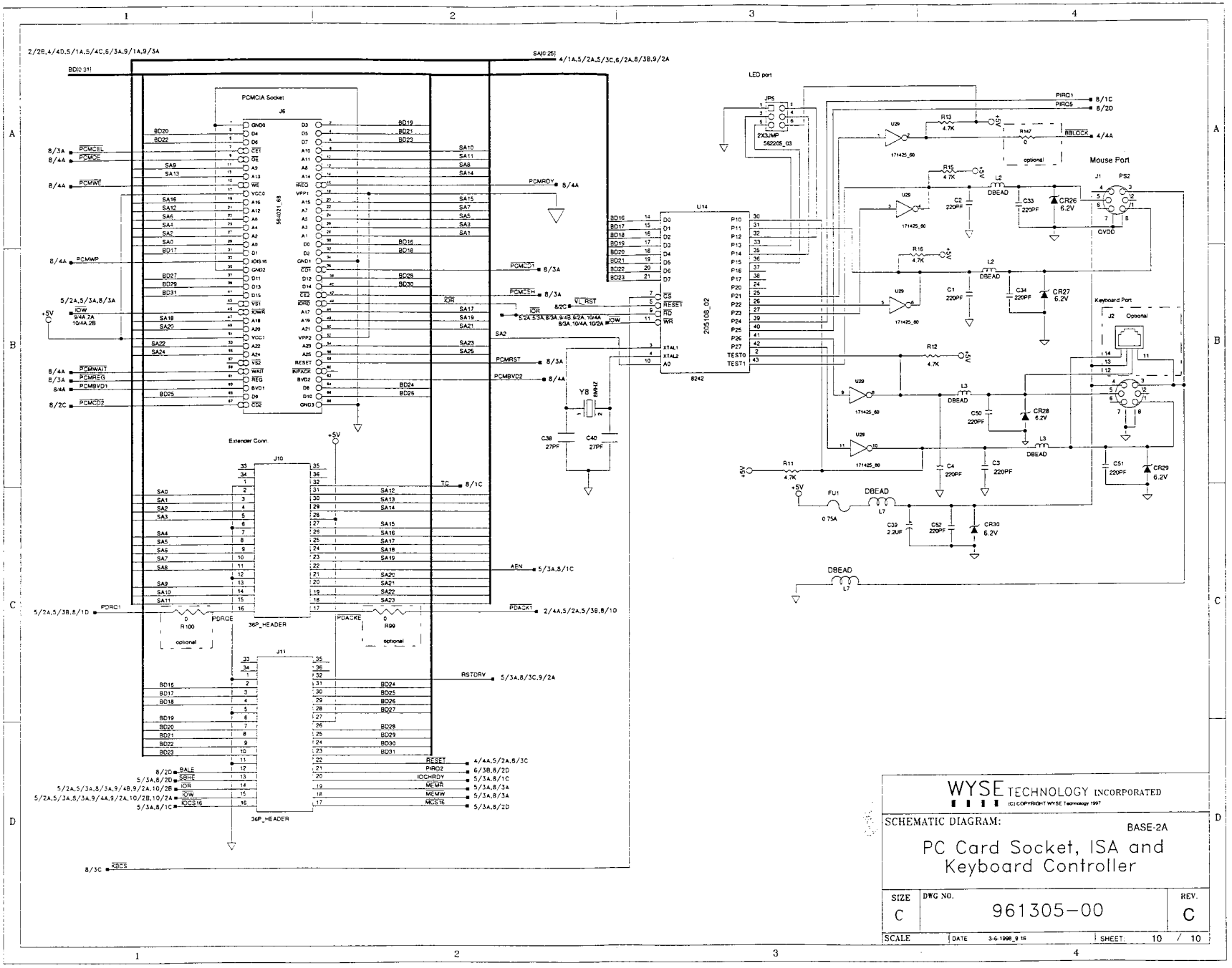
SCHEMATIC DIAGRAM:
BASE-2A
Serial and Parallel Ports
SIZE
C
DWG NO.
961305-00
REV.
C
SCALE
DATE
3-6-1998 9:25
SHEET:
9 / 10


PCMCIA Socket
J6
56/021_68
Extender Conn.
J10
36P_HEADER
J11
36P_HEADER
LED port
JP5
2XJUMP
562205_03
U14
205108_02
8242
Y8
8MHZ
Mouse Port
J1
PS2
Keyboard Port
J2
Optional
optional
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SCHEMATIC DIAGRAM:
BASE-2A
PC Card Socket, ISA and Keyboard Controller
SIZE
C
DWG NO.
961305-00
REV.
C
SCALE
DATE
3-6-1998 9:16
SHEET
10 / 10