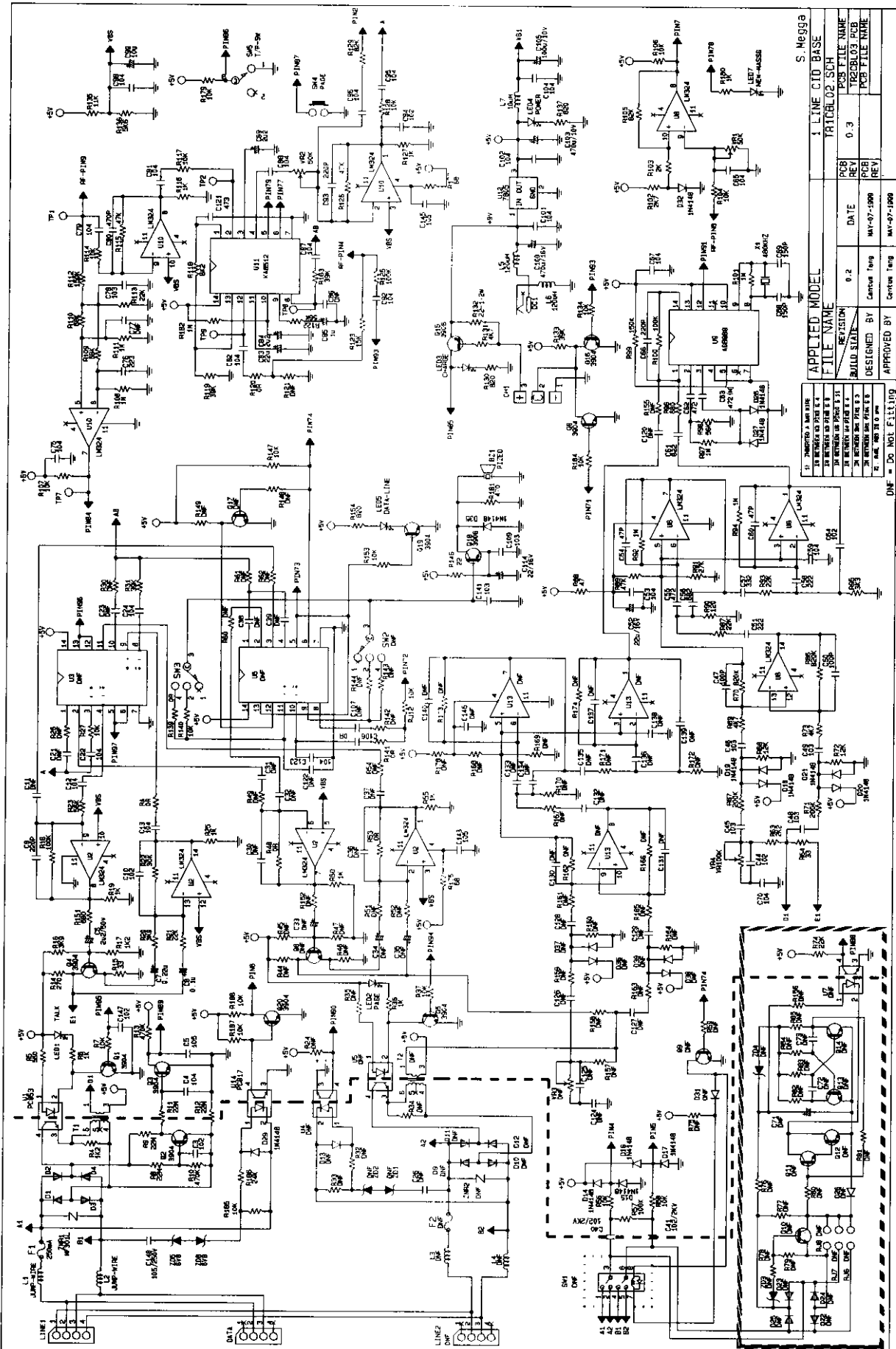


EXHIBIT D

Circuit Diagram

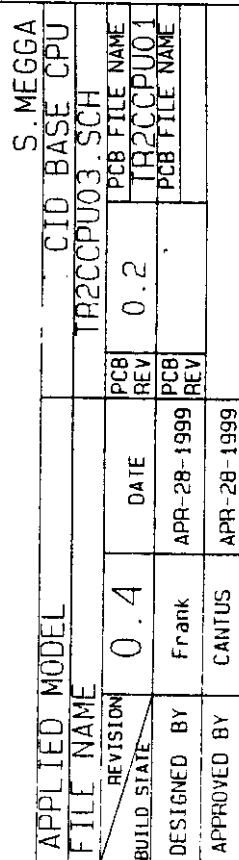


APPLIED MODEL
FILE NAME
1 LINE CTD BASE
TRICBL02.SCH

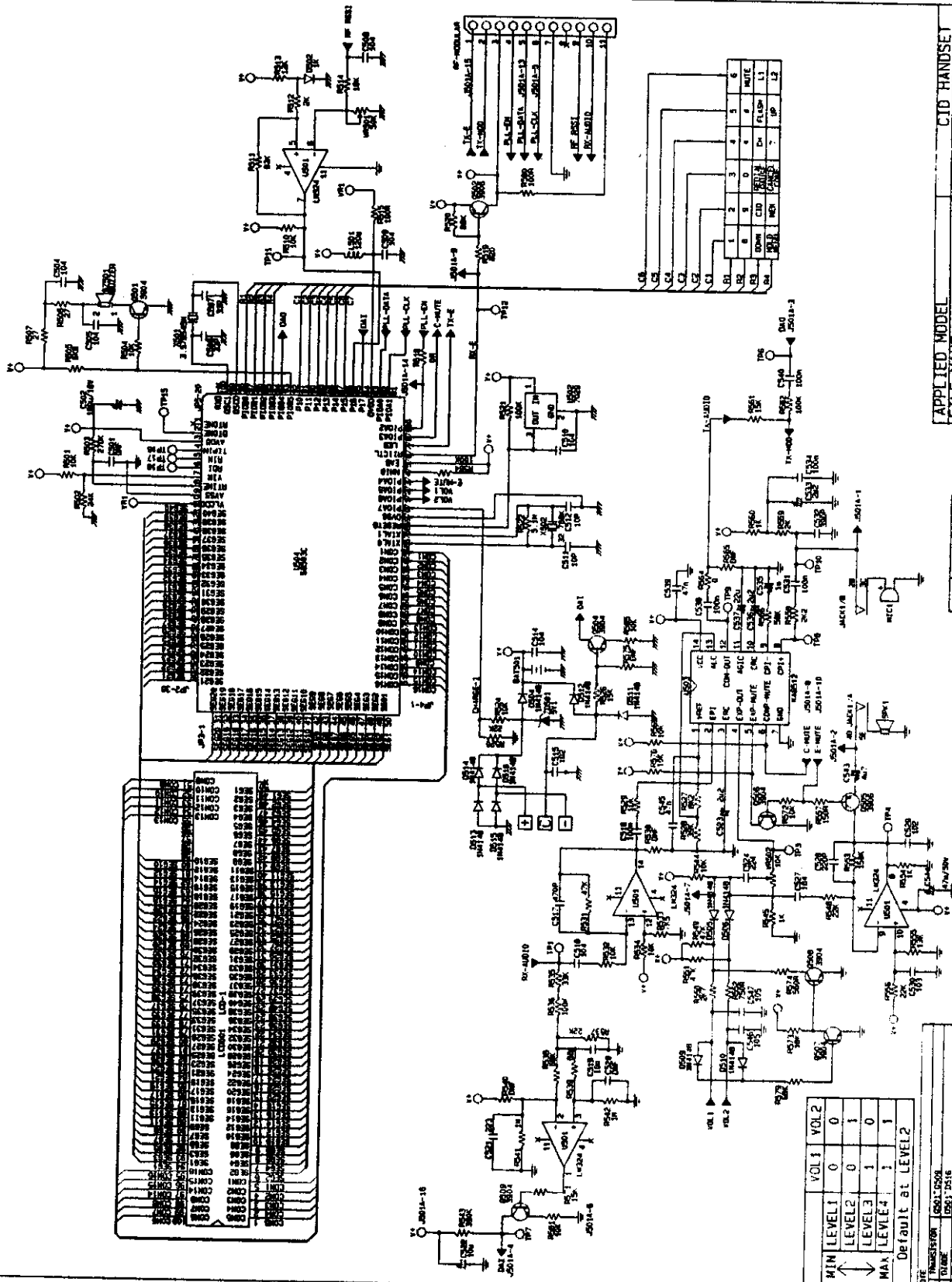
DESIGNED BY	DATE	REV	PCB
MAINTENANCE	0.2	0.3	PCB
DESIGNED BY	DATE	REV	PCB
MAINTENANCE	0.2	0.3	PCB

DESIGNED BY: S. Megga
DATE: 01-07-1999
REV: 0.3
PCB: TRICBL03 PCB
PCB FILE NAME: TRICBL03 PCB

DO NOT FILL IN



NOTE	
1	TRANSISTOR
2	DIODE
3	ZENER DIODE
4	RESISTOR
5	CAPACITOR
6	IC
7	JFT
8	INDUCTORS



APPLIED MODEL				C10 HANDSET			
FILE NAME				1H2CHL06 SCH			
REVISION				0.4			
BUILD STATE				PCB REV			
DESIGNED BY				MICHAEL			
APPROVED BY				CANTUS			
DATE				APR-28-1999			
PCB FILE NAME				1H2CHL06 PCB			
REV				REV			

10305	10315
6K8	DNF

MIN	LEVEL1	0	0
LEVEL2	0	1	1
LEVEL3	1	0	0
MAX	LEVEL4	1	1
Default at LEVEL2			

1	DESCRIPTION	0001-0001
2	DATE	0001-0001
3	REVISION	0001-0001
4	REVISION	0001-0001
5	REVISION	0001-0001
6	REVISION	0001-0001
7	REVISION	0001-0001
8	REVISION	0001-0001

