APPENDIX 2
BASE STATION PA TEST & TUNE-UP PROCEDURE

1. Introduction

This document forms the production test schedule for the Base Station PA. The running order of the document must be followed to reduce the number of equipment set-up changes and reduce the number of soldered contacts that have to be made. A full General Assembly drawing detailing all boards, connectors and cables can be found in section 4.2 of this Appendix. At this point we must make the distinction between the PA board, which is the forward gain stage module, and the PA which describes the completed Base Station unit containing all the sub-modules including the PA board.

2. Abbreviations and Definitions

VNA	Vector Network Analyzer
DVM	Digital Voltmeter
PSU	Power Supply Unit
RX	Receive
TX	Transmit
FET	Field Effect Transistor
RBW	Resolution Bandwidth
UC	Up-converter
DC	Down-converter

2.1 Harmonic Filter Tuning

VNA Setting	Value
Source Power	0dBm
Center Frequency	224MHz
Span	300MHz
Marker 1	214MHz
Marker 2	234MHz
dB/Div	5dB

Table 1. Control board VNA set-up.

Configure VNA settings as shown in table 1, with port 1 of the VNA connected to the TX output of the PA and port 2 to the RX output. **NB. DC blocks must be used on each port of the VNA**.

Power up the control board and obtain a display of **gain** and **return loss** on the VNA. Compare display with Figure 1a). Ensure the insertion loss is less than 1 dB and return loss is no greater than 12 dB across the 214-234 MHz band. Adjustments to insertion loss and return loss can be made by either altering the position and space between the coils of inductors L4 and L5, or moving capacitors C29 and C32 along the 50R line within the filter screening can. Obtain a plot when satisfactory display is achieved.

Now connect port 1 of the VNA to SK1 of the control board and obtain a display of the TX path Compare with Figure 1b. No re-tuning of the filter should be required to achieve an acceptable response in the TX path; any extra loss can be attributed to TX/RX PIN diode switches or in-line connectors.

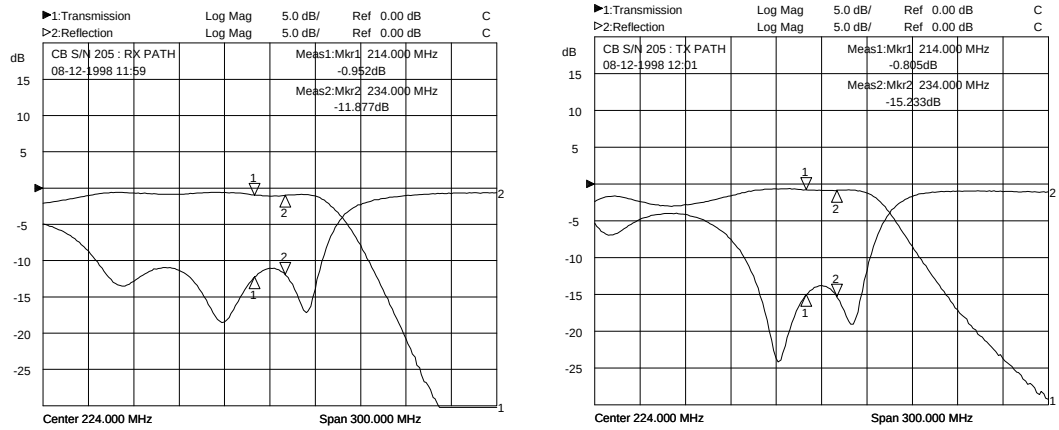


Figure 1. Harmonic filter responses

a) RX path b) TX path

3. PA Board

Figure 2 shows a block diagram of the PA board together with details of the stage bias currents and nominal gain responses across the band. A full PCB and component layout can be found in section 0 of this Appendix. **NB. Ensure all soldering irons are properly grounded and forced air cooling of the module is maintained during all stages of testing**.

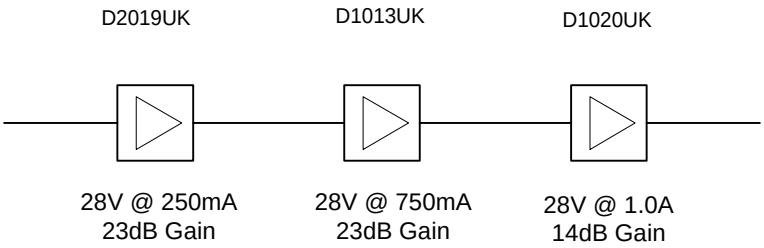


Figure 2. PA board device line-up.

Configure the test equipment in the manner shown in Figure 3. Table 2 shows the VNA settings. Please note, the RF source power of the VNA has been reduced to **–25dBm**.

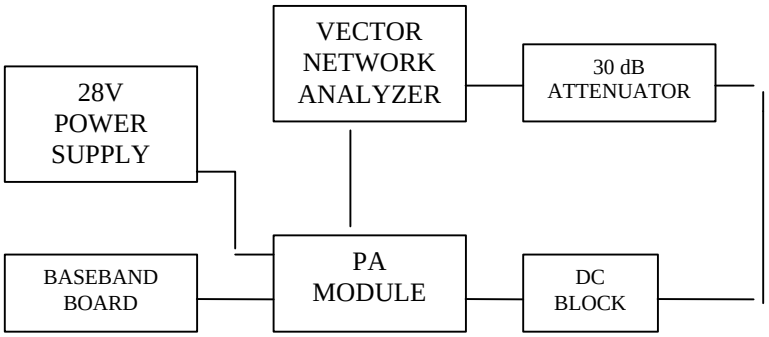


Figure 3. PA board equipment set-up.

VNA Setting	Value
Source Power	-25dBm
Center Frequency	224MHz
Span	300MHz
Marker 1	214MHz
Marker 2	234MHz
DB/Div	5dB

Table 2. PA board VNA settings.

3.1 D2019 Stage

With reference to Table 3 and Section 0, we must first isolate the D2019 from the rest of the circuit to allow us to power-up the FET devices individually. This process requires the removal of key components on the power supply rails within the PA board. A break in the RF path must also be made to allow the inclusion of test coaxial. **NB. The listed components refer to a fully populated board**.

Component Type	Layout No
Inductors	L11, L12
0R Links	R71
RF Alloy Links	TP1

Table 3. D2019 power isolation components.

To ensure the D2019 is biased off before power-up, ensure multi-turn resistor R7 is turned fully counter-clockwise until the end-stop is reached. Connect VNA port 1 to SK1 of the PA board, remove alloy link at TP1 and solder test output coaxial center conductor to the RF path after trimmer C13 and shielding conductor to ground plane, keeping the exposed conductors as short as possible. Connect output coaxial to port 2 of VNA.

Power-up stage with +28V PSU supply with the current limit set to 50 mA. Now increase PSU current limit to 300mA. Adjust R7 clockwise until a current of around 250mA is drawn. Measure & record gate voltage. Obtain a display of the **gain** and **return** loss on the VNA.

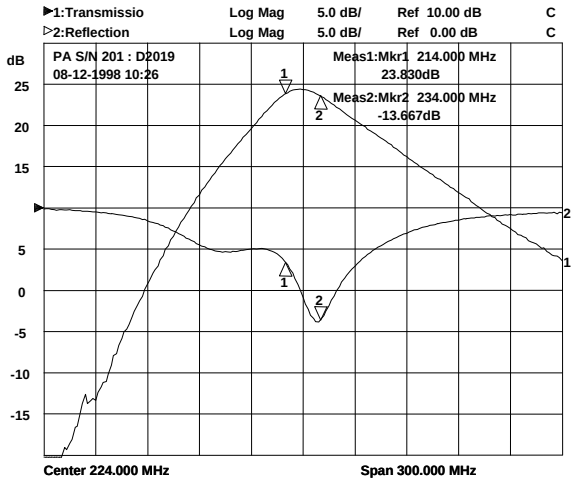


Figure 4. D2019 gain and return loss response.

With reference to Figure 4, adjust trimmer capacitors C5, C13 and C50 to obtain a similar response. A gain of 22 dB should be possible across the 214-234 MHz band. A return loss of 7-10 dB should also be possible. Each trimmer has a different effect on the response: initial experimentation with each one will enable the operator to gain experience on the best combination of settings. Capture a plot of the final response.

3.2 D1013 Stage

With reference to Table 4 and Section 0, isolate the D1013 from the rest of the circuit. Remove components listed in Table 4. Break RF path in two points, TP1 and TP2. Use C24 to couple the output, to allow the inclusion of test input and output coaxial. **NB. The listed components refer to a fully populated board**.

Component Type	Layout No
Inductors	L11, L12
0R Links	R70
VRES	R14
Capacitors	C24
RF Alloy Links	TP1

Table 4. D1013 power isolation components.

Bias off the D1013 before power-up by adjusting multi-turn resistor R11 fully counterclockwise until the end-stop is reached. Connect VNA port 1 via an input coaxial test lead to RF path at TP1 before C60 and ground. Connect output coaxial to TP2 after L7 and C22. Connect output coaxial to port 2 of VNA.

Power-up stage with +28V PSU supply with the current limit set to 50mA. Now increase PSU current limit to 800mA. Adjust R11 clockwise until a current of around 750mA is drawn. Obtain a display of the **gain** and **return** loss on the VNA.

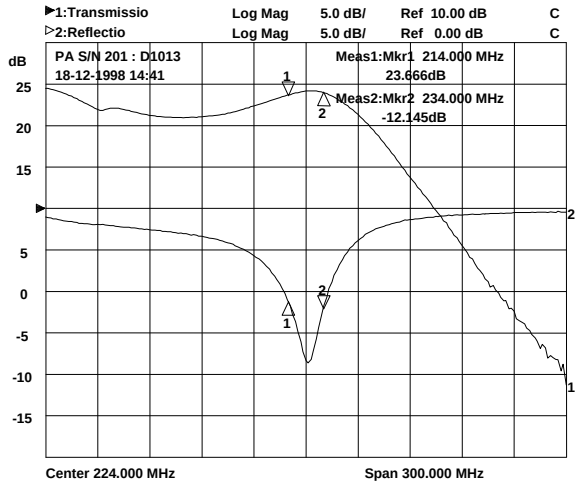


Figure 5. D1013 gain and return loss response.

With reference to Figure 5 adjust trimmer capacitors C15 and C22 to obtain a similar response. A gain of at 22dB should be possible across the 214-234MHz band. A return loss of 7-10dB should also be possible. Capture a plot of the final response.

3.3 D1020 Stage

With reference to Table 5 and Section 0, isolate the D1020 from the rest of the circuit. Remove components listed in table. Break RF path to allow the inclusion of test input coaxial at TP2, using C24 to couple the output. **NB. The listed components refer to a fully populated board**.

Component Type	Layout No
Inductors	L8
Resistor	R12
0R Links	R70

Table 5. D1020 power isolation components.

Bias off the D1020 before power-up by adjusting multi-turn resistor R14 fully anticlockwise until the end-stop is reached. Connect VNA port 1 to the input coaxial test lead. Connect port 2 of VNA to SK2.

Power-up stage with +28V PSU supply with the current limit set to 50mA. Now increase PSU current limit to 1100mA. Adjust R14 clockwise until a current of around 1000mA is drawn. Obtain a display of the **gain** and **return** loss on the VNA.

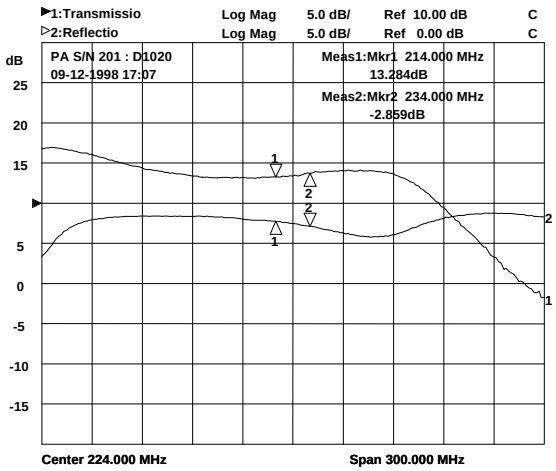


Figure 6. D1020 gain and return loss response

With reference to Figure 6, adjust trimmer capacitor C27 to obtain a similar response. A gain of at least 12 dB should be possible across the 214-234 MHz band. A return loss of 2.5-5 dB should be possible. Capture a plot of the final response.

3.4 Full Line-up tuning

Replace all removed components in power supply lines and RF path. Connect port 1 of VNA to SK1 and port 2 to SK2. Set PSU current limit to 2100mA. Power-up stage – current drawn should be around 2000mA obtain a response on the VNA.

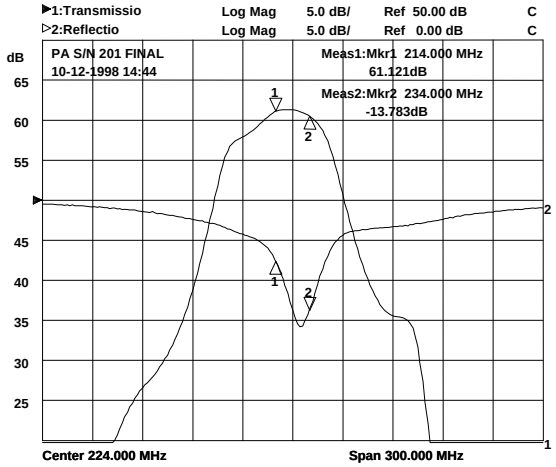


Figure 7. Full line-up gain and return loss response.

If the PA begins to current limit, try adjusting C27, C22 or C16 until limiting stops. Compare response with Figure 7. A gain of around 60 dB and a return loss of 7-10 dB should be possible with minor adjustments to all trimmer capacitors. Adjusting trimmers associated with the D2019 should have the greatest effect on return loss.

Connect control board into RF path with PSU current limit set to 2500mA. Connect Aluminium semi-rigid cable 5 from SK2 of PA board to SK1 of control board. Connect TX output connector of test combo connector to DC block/attenuator path. Re-tune PA line-up to compensate for the effect. Capture a plot of the final response.

4. Module Integration

NB. A fully integrated PA requires forced air cooling when running at power. With reference to General Assembly drawing in section 4.2, connect all inter-module cables and configure test equipment as shown in
Figure *8*.

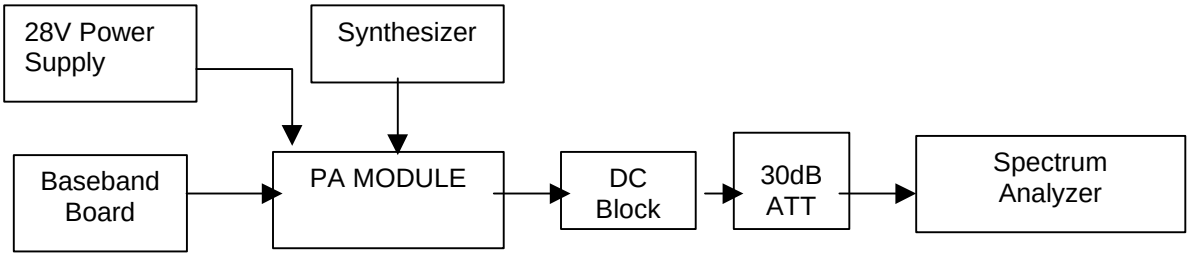


Figure 8. Integrated module test set-up.

Source Setting	Value
LO Power	0dBm
LO Frequency	224MHz
I & Q Signal	Single tone

Table 6. Module integration source settings.

4.1 Phase Control Balance and Mid-Band Setting

With reference to General Assembly drawing in section 4.2, connect all modules together. Configure source and PSU settings as shown in Table 6. Measure the phase control voltage present at the lineariser board PH_CTL feed-through, from BRSI adjust the phase control voltage until 2V is present.

Configure spectrum analyzer with center frequency at 224 MHz and span 2 MHz. Fully power-up PA by switching on +28 V power supply. Adjust Phase control voltage. The response will display side-lobes as shown in Figure 9a, these will appear either above or below the main tones. The magnitude of the lobes will vary relative to the phase control voltage. Phase balance is achieved when the side-lobes disappear into the noise floor, exhibiting equal magnitude above and below the main tone - as can be seen in Figure 9b.

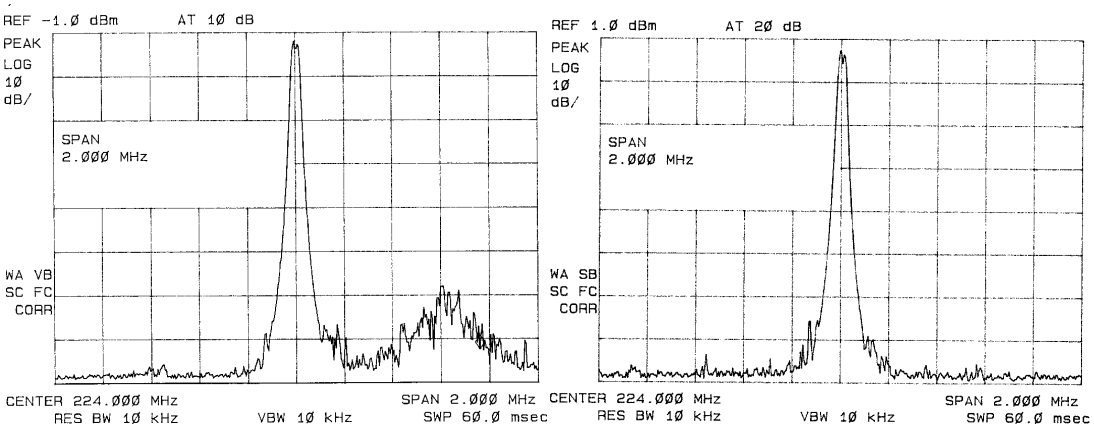
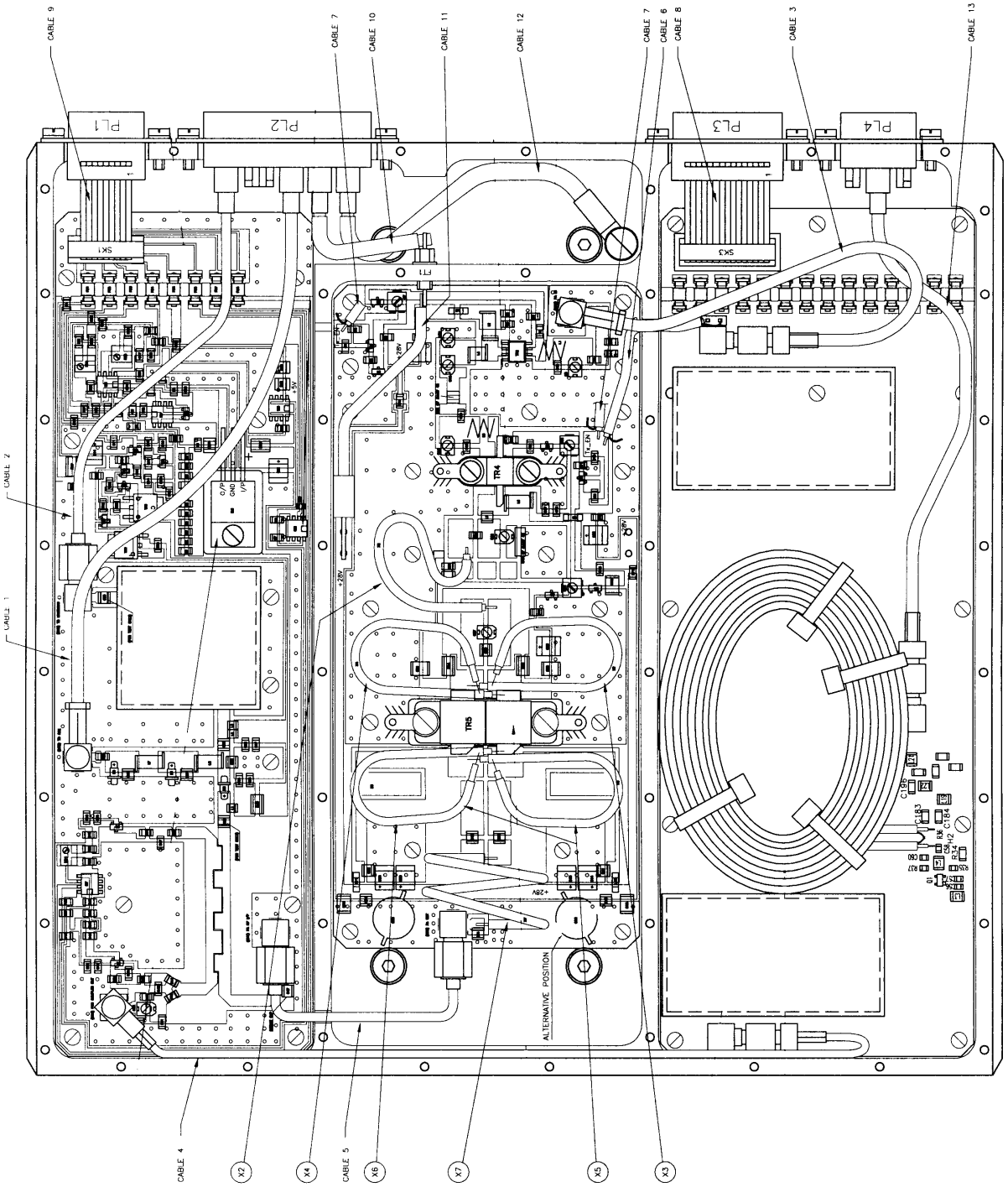


Figure 9. Phase balance responses.

a) Unbalanced phase control voltage b) Balanced phase control voltage.

4.2 General Assembly Drawing (l to r: PA Control, PA (transmitter), Linearizer)



4.3 Connectors and Pin Allocation

4.3.1 External Interfaces

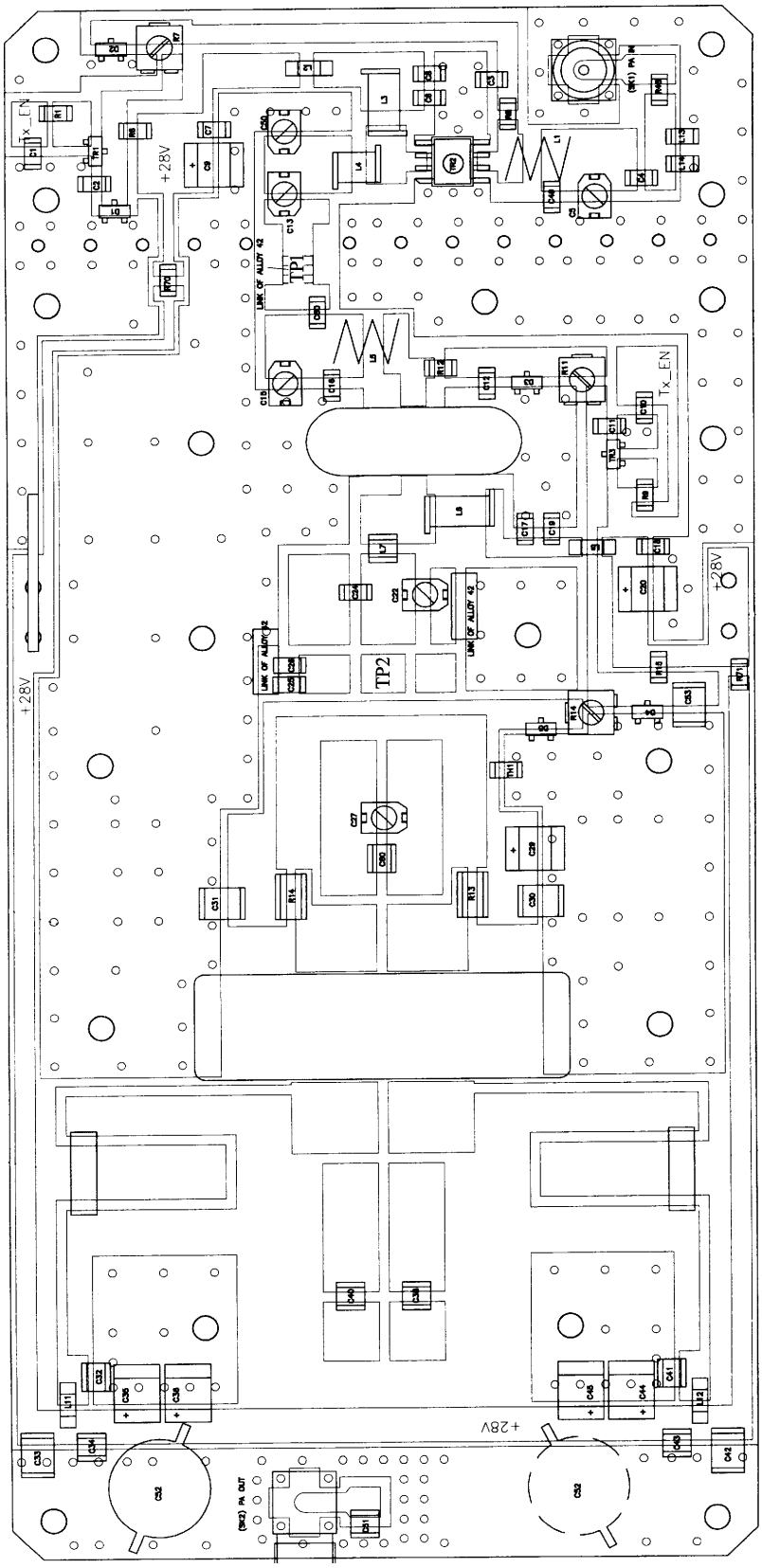
4.3.2

Table *7* shows the signal interfaces between the transmitter module and the rest of the base-station unit.

Signal Name	Direction	Type	Connector	Description
-15V	In	Power	PL1, pin 5	-15V Power supply
+28V	In	Power	PL1, pin 6	+28V Power supply to Control Board
+28V	In	Power	PL2, pin A2	+28V Power supply to PA, 5 A max.
AGND	In	Power	PL2, pin A1	Analogue ground
TX_RF	In/Out	RF	PL2, pin A4	Transmitter RF output / Receiver RF input via Masthead
I_IN_AC	In	Analogue	PL3, pin 1	Baseband I channel input, AC coupled
AGND	In	Power	PL3, pin 3	Analogue ground for the lineariser board
Q_IN_AC	In	Analogue	PL3, pin 9	Baseband Q channel input, AC coupled
SHDN	In	Digital	PL3, pin 11	Enables PA
5dB_UP	In	Digital	PL3, pin 4	HCMOS power control, 5dB step
5dB_DOWN	In	Digital	PL3, pin 12	HCMOS power control, 5dB step
10dB_ATT	In	Digital	PL3, pin 13	HCMOS power control: 10dB step
15dB_ATT	In	Digital	PL3, pin 15	HCMOS power control: 15dB step
PH_CTL	In	Analogue	PL3, pin 6	Cartesian loop phase control Output voltage range 0 to 5 V
DC_NULL	In	Digital	PL3, pin 14	Cartesian loop dc null control
INSTB	Out	Digital	PL3, pin 12	Transmitter instability detector (to DSP)
VSWR	Out	Digital	PL1, pin 3	VSWR alarm indicator (Not used)
+15V	In	Power	PL3, pin 8	+15V power for Cartesian loop
TX_RX	In	Digital	PL1, pin 9	Switches between TX & RX mode
TX_EN	In	Digital	PL3, pin 15	Disables the PA during a DC Null operation.
SCL	In	Digital	PL1, pin 2	Dallas chip clocking signal
SDA	In/out	Digital	PL1, pin 1	Dallas chip data line
RX_I_HI	Out	Digital	PL1, pin 8	Indication of masthead unit condition HCMOS high: Current drawn > 120 mA HCMOS low: Current drawn <= 120 mA
RX_I_LOW	Out	Digital	PL1, pin 7	Indication of masthead unit condition HCMOS high: Current drawn < 480 mA HCMOS low: Current drawn >= 480 mA
RX_RF	Out	RF	PL2, pin A3	Received RF from TX/RX switch
LO_TX	In	RF	PL1, pin A1	Local oscillator input 0dBm

Table 7. External interface signals.

4.3.3 PA Board



4.3.4 Control Board