

# CGI Reader Overview



# Revision History

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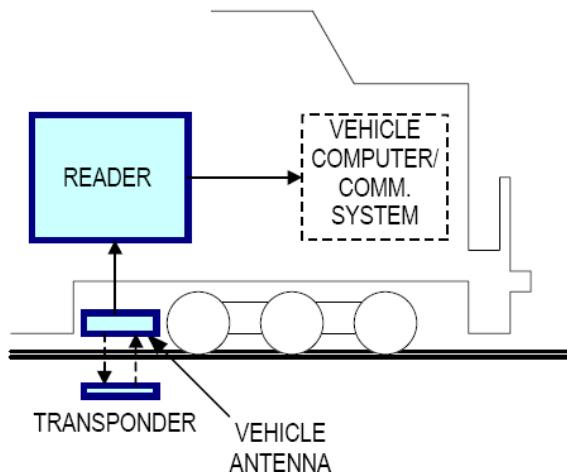




# CGI Reader Main Processor Board - Hardware Design

## 1 Introduction

The Transponder system provides a mean to transfer data between a moving vehicle (typically a locomotive) relative to a fixed wayside point, it provides indications to a reader as the vehicle passes successive points of known separation. Data transfer between the vehicle and the wayside occurs at fixed-point locations defined by the position of the Tags. The unit describe here shall be the part of object location/ identification system that consist of the transponder (Passive RFID), vehicle antenna, reader and communication system.



**Figure 1-1 CGI Location/Identification System**

### 1.1 Purpose of this document

The purpose of this document is to list major aspects of the electronic design

#### Scope

This document contains major electronic design aspects.

The Reader consists of two modules

1. Main Processor Module
2. RF Module

### 1.2 References

Sr.	Reference	Detail
1		
2		
3		
4		
5		

**Table 1-1 References**



### 1.3 Abbreviation, Definitions and Acronyms

Items	Detail
AM	Amplitude Modulation
CGI	Cattron Group International
CPLD	Complex Programmable Logic Device
DC	Direct Current
DPLL	Digital Phase Lock Loop
DPSK	Differential Phase Shift Keying
DXF	Design Exchange Format
JTAG	Joint Test Action Group
RF	Radio Frequency
RFID	Radio Frequency Identification

**Table 1-2 Abbreviation, Definitions and Acronyms**



## 2 Mechanical Design

### 2.1 Design Overview

#### 2.1.1 Board Size

Board Size is 9.31" x 7.45".

#### 2.1.2 Mounting Holes

Board has Ten Plated, mounting hole and tooling holes as per following drawing.

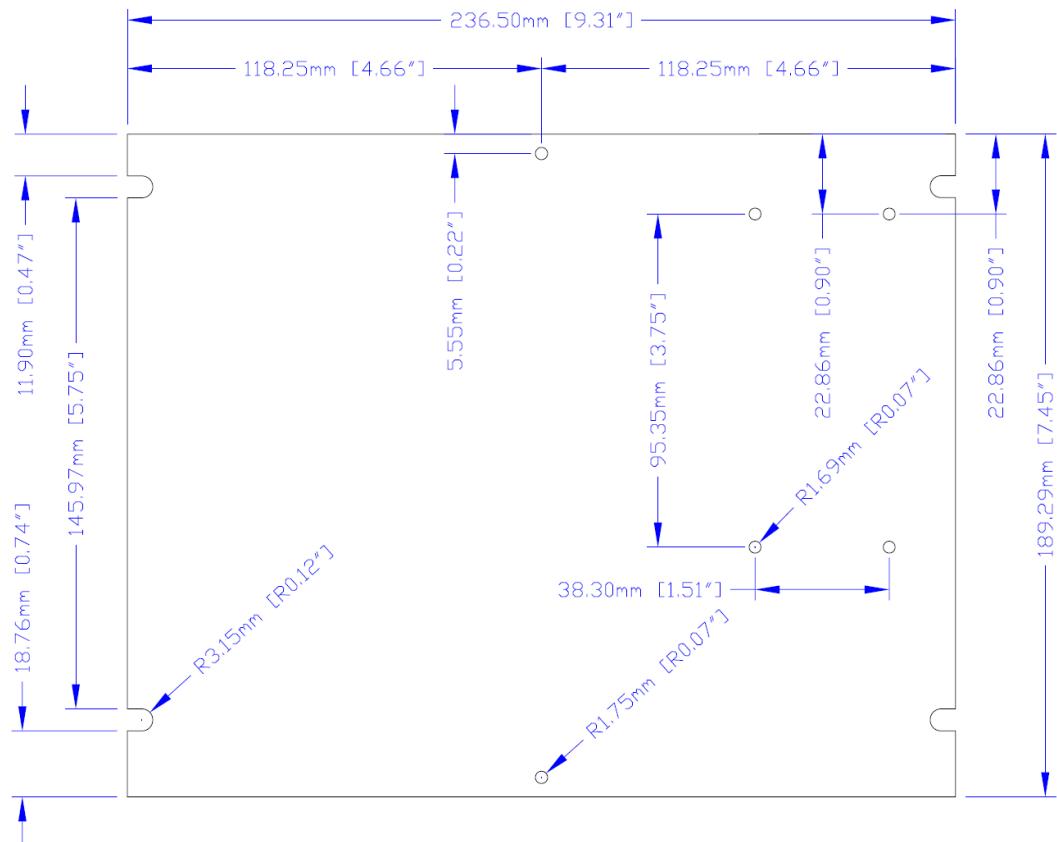
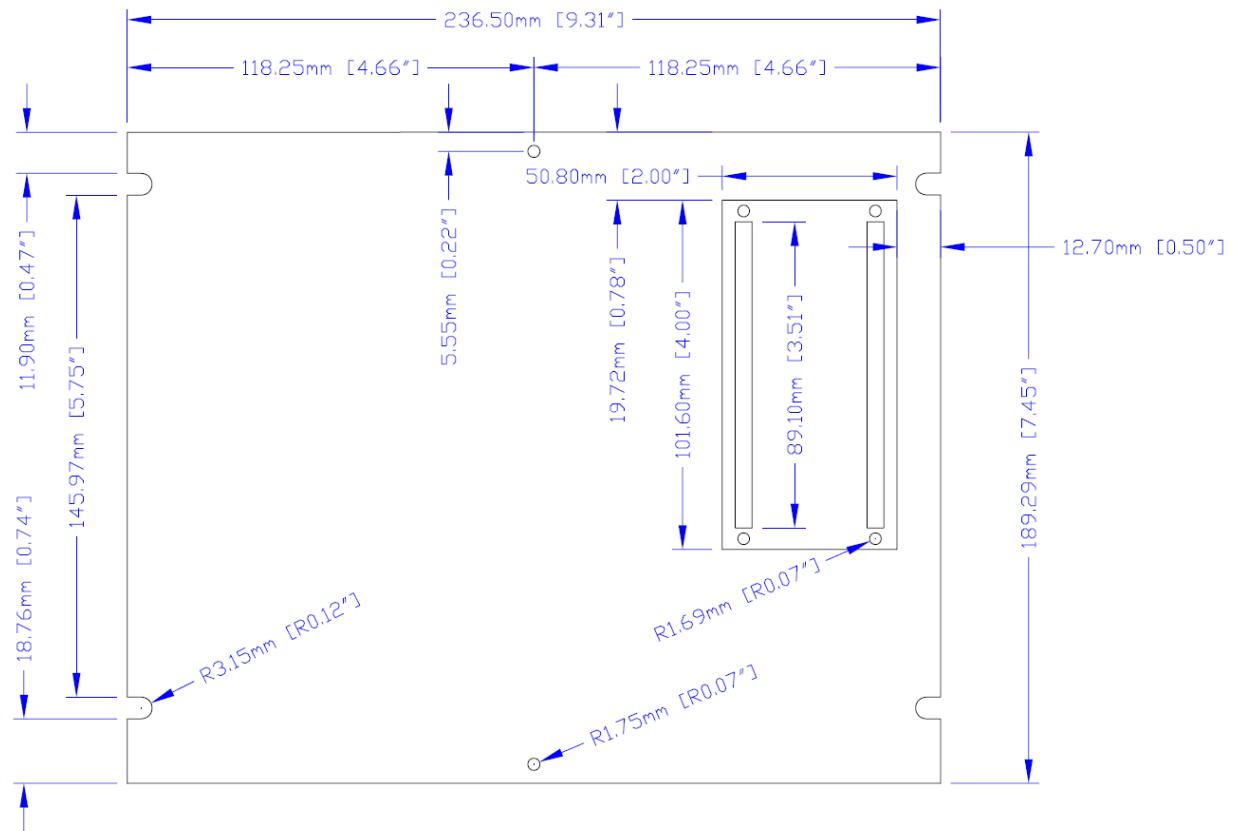


Figure 2-1 Board Outline with Mounting Holes



### 2.1.3 Floor Plan

The board features a critical RF board along with RF interface connector as per following drawing.



**Figure 2-2 Floor Plan**

### 2.1.4 Component Height Restriction

There are no components which have height higher than 1400 mils.



### 3 Electrical Design

The Electrical Design deals with major circuit details, calculation and theory of operation.

#### 3.1 Design Overview

The Reader is a microcontroller and CPLD based data acquisition unit

It is directly connected to an external 72V DC power supply.

The Antenna energizes the track-mounted transponder through an electromagnetic interface.

The Transponder has no self contained power supply, it utilizes the signal received from the Antenna as a power source as well as a clock signal. This clock signal has frequency equal to the signal generated by the Antenna oscillator frequency of 200 kHz.

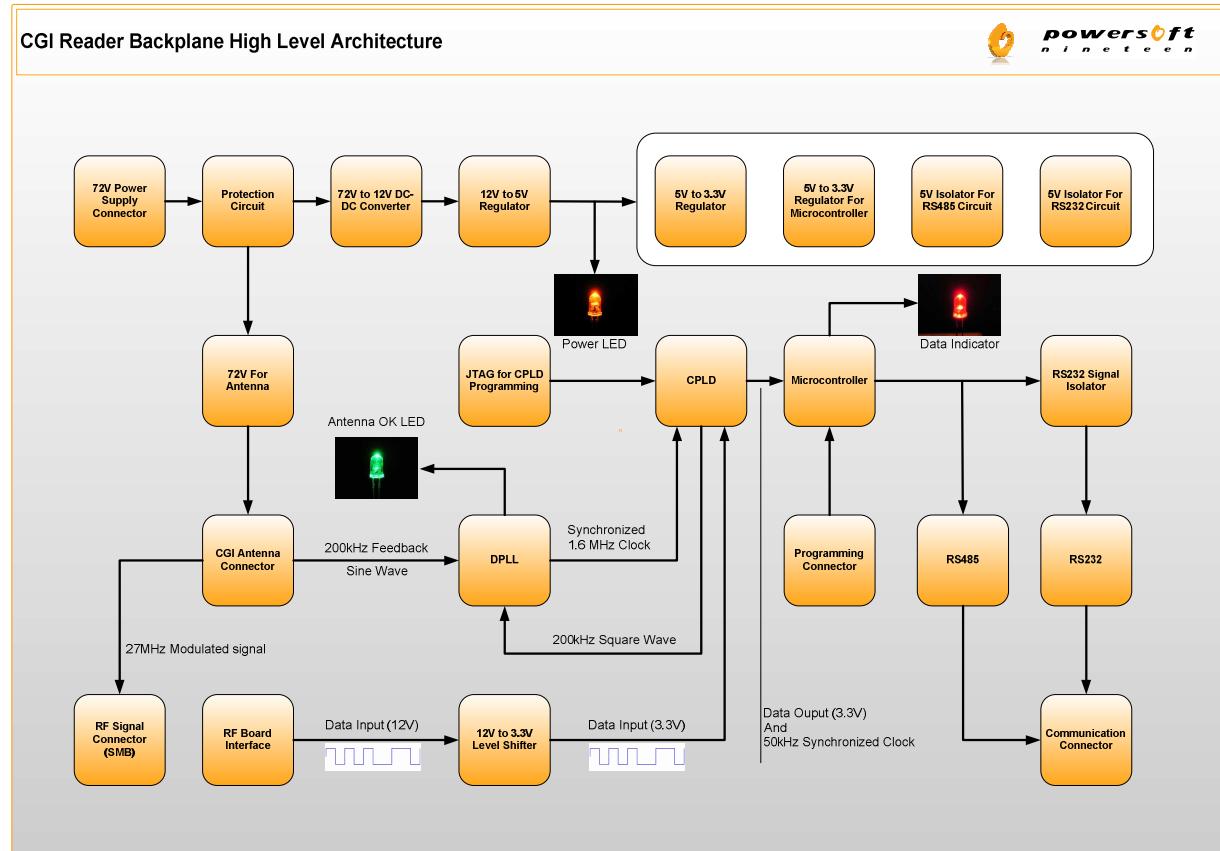


Figure 3-1 CGI Reader Back Plane High-level Architecture

Figure 3-1 Show high level architecture of Back Plane module of the Reader. All digital data processing systems, synchronization systems, power supplies and communication systems available on this module.

When the Transponder is inductively energized by the Antenna, it continuously transmits DPSK and AM modulated binary data frame messages towards the Antenna at approximately 27MHz.

The Antenna incorporates two separate circuits. The first one receives the high frequency (27 MHz nominal) transmission from the Transponder and the second one interfaces circuitry to the Reader for DC power, 200 KHz frequency reference and RF data. The receiving antenna portion picks up the signal and passes it to the Reader.

This signal contains a BCH encoded message that consists of 64 data bits. The Reader demodulates the received signal and verifies its integrity. After data verification, the Reader transmits the validated transponder number via the Reader's communication connector as an asynchronous serial ASCII message.



## Interfaces

The transponder design has four interfaces to interact with the external environment.

### 3.1.1 JTAG Interface

The JTAG interface is used to program and debug the CPLD through a JTAG cable.

### 3.1.2 Microcontroller Programming interface

This interface is used to program and debug the C8051F340 Microcontroller.

### 3.1.3 RF Interface

This interface is used to get the modulated signal from the Transponder.

### 3.1.4 Communication Interface

With this the Reader can communicate with other RS232 or RS485 compatible devices.

## 3.2 Theory of Circuit Operation

The operation of the circuit is described in following sections.

### 3.2.1 72V Power Supply Connector

Connector J8 is used to connect reader with external 72V DC power source. An EMI filter will not allow external EMI to enter the reader nor internal EMI to exit from the system and protect from overloads.

72V is provided to the Antenna

### 3.2.2 72V to 12V DC-DC Converter

The reader has a 72V to 12V DC-DC convertor

### 3.2.3 12V to 5V Regulator

The reader regulates 12V to 5V.

### 3.2.4 5V to 3.3V Regulator

The 5V is further down stepped to 3.3V

### 3.2.5 5V Isolated Supplies for RS232 and RS485

An isolated 5V supply is generated for the RS232 and RS 485 ICs

### 3.2.6 Antenna Connector

Antenna Connector J3 connects the antenna unit with the reader. The reader can supply 72V to antenna through this connector. Also it can receive 200 kHz feedback frequency for synchronization.

### 3.2.7 RF Interface Connector

The Reader consists of two modules, Backplane and RF module. Both modules are connected with each other by using two 35x2 connectors.

### 3.2.8 Digital Phase Look Loop

DPLL digital phase look loop removes any phase difference to achieve synchronization. The output frequency at VCO out varies accordingly with voltage level present at VCO in . The output frequency which is approximately equal to 1.6MHz will be used in the CPLD. The CPLD produces 200 kHz approx. square wave and the output frequency will be within a controlled range.

### 3.2.9 CPLD

The transponder system has a Xilinx XCR3064XL CPLD which operates on 3.3V DC. The 200 kHz square wave will output from CPLD which is used in DPLL for phase comparison. The VCOout signal is used in CPLD for data extraction as well to produce 200 kHz square wave.

### 3.2.10 Microcontroller

The microcontroller gets 64 bits data from CPLD The microcontroller extracts the BCH encoded sequence converting the 64 bits into 16 hex digits. and is converted in to ASCII and serially passed to the communicating device attached to the reader through RS232 or RS485 link.



### ***3.2.11 Communication Connector***

Connects the reader to an on-board computer or data acquisition device incorporating a serial port.

