MRM 7700 Circuit Description

1. General

This is a software configurable transceiver module based on the Analog Devices ADF7021 synthesized transceiver chip. It may be factory pre configured to suit several pre tested and certified configurations.
Module capabilities are

1.1 Transmitter
Power programmable from 0dBm to 23dBm (*Factory Pre Set to required level and not user adjustable*)
Frequency (7700H) 450-470MHz
Modulation programmable, deviation, mode, filtering, and rate.
Channel bandwidth 12k5Hz

1.2 Receiver
Direct conversion Receiver
Sensitivity -117dBm
Channel spacing 12k5Hz
Adjacent channel rejection >40dB
Image rejection >40dB

2. Power Supplies

Three power sources are required,

2.1 3V3 on J1 27 used to supply the Synthesizer chip U1.

2.2 3V3 or 5V for the EEPROM U11

2.3 VBAT on J1 1,2 used to supply the onboard regulators for everything else.

2.3.1 U2 Regulator is a low noise LT1965 1.1A LDO linear device that provides the TX/RX Switch with 4VSW and also the main power amplifier U9 via Q4 with 4VRFSW.
4VSW is enabled by the ENA line asserting high.
4VRFSW is enabled with the PA-ON line asserting high
U7 Regulator provides 3V3SW for the TCXO, the receiver pre-amplifier Q1, and the Data IO guiding analog switch and control, U12 and Q2.
U7 is also enabled by ENA asserting high.

2.3.2 Final Amp Power Switch
Q4 is a P channel trench FET with very low RDS on of 0.052 Ohms, this switches the 4V onto the power amplifier and is isolated by inductor L16, C24 and C45.

3. Synthesizer

3.1 U1 is the main synthesizer transceiver chip, this is software programmable for many different modulation modes, nominally 2GFSK
DATCLK output clocks in the data to be transmitted.

3.2 U1 is enabled by a High on its CE input pin 24, supplied from ENA J1 21, if ENA is low the device is in very low power mode.
The TCXO for U1 is U6, a 3V3 version with a 1PPM stability -40+85C clipped sine o/p, 14.31818MHz, this requires the output to feed U1 pin 39 (OSC1) (option R10), The TCXO frequency can be pulled with R13.

3.3 VCO
The VCO can be selected according to several requirements, dependant on several factors, (see datasheet), if an external VCO inductor is required this is L3, value sets frequency and is only likely to be needed for lower frequencies 406MHz and below, otherwise (nominally for 7700H), an internal VCO is used running at twice the operating frequency.
VCO loop, (third order), filter set by C12, R8, C11, C10, R7.

3.4 Register programming and Data I/O.
Register control via lines PLE, PDI, PDO, PCLK.
MUX out for multi use, regulator ready, VCO lock, etc.
Data in/out is digital only from pin 34, is routed to Data IO J1/25, on systems with a bidirectional processor port, alternately for systems with separate TX O/P port and RX I/P port the routing is directed by Q2 and U11 with R35 fitted, so that TX input is from J1 26 and RX output goes to J1 25 and 33.

3.5 RF Out
In TX mode RF output from pin 4 is filtered by a Butterworth 3rd order filter, L14, L15 and C21 before being presented to the input of the switched gain power amplifier U9.
Synthesizer RF power is fully programmable from -16dBm to +13dBm.

3.6 Transient Suppression due to switching
Automatic power ramping at a programmed rate/data bit minimizes spurious radiation due to RF switching.

3.6 RF in
In RX mode, RF is presented to pin 6 and 7, the chip has three programmable gain modes and three IF Bandwidths, 12.5kHz, 19kHz and 25kHz, the IF frequency is 100kHz. There is no available analog output Quality of the recovered data is measured as a bit error rate, BER.

4. RF Amplifier
U9 is an integrated switched gain amplifier, the minimum gain of this device is 4dB nominally, equivalent to + 0dB at the output after losses.
U9 has two control lines G8 and G16, these add in this amount of gain when asserted high, i.e. if G8 is high the gain is +8dB, if G16 then +16dB if both then +24dB, limited by the device saturation point approaching 500mW.
Appropriate gain setting coupled with maximum possible RF output from the ADF7021 to achieve the required output power, provides best suppression of spurious at the antenna port due to RF switching by allowing the ramping facility of the synthesizer to exert maximum benefit.

Second Harmonic suppression is provided by L9 & C52.

5 Antenna Switch Circuit.
U10 provides two output control lines; O2 is high when PA-ON is asserted high, O1 is high when PA-ON is low (RX). These two outputs provide bias for the Pin diodes D7 and D8. The forward biased diode will have about 6mA of forward bias and a Cathode voltage of about 2V, this provides the reverse bias for the other diode, the cathode of which is 2V and the Anode of which is at 0V. D8 is the TX path and D7 is the RX path.

6 RF Output Filtering
Is provided by C49 and L12,13 as a T filter matched to the operating frequency band.

7 Receiver Pre amplifier
Q1 has a gain of about 23dB, this will enable U1 to run at lower gains and improve its IP3 performance. The pre-amplifier is followed by FL2 a triple tuned Helical filter before being matched to U1's RF inputs. FL1 and FL2 have a -1dB bandwidth of about 28MHz.

8 Onboard Memory
Some applications may want to store module configuration data within the memory, U11 is a serial 8KB device.

9 Zener diode supply protection.
Diodes D3-D6 are provided to protect against the failure of any internal supply, these would normally only be fitted to intrinsically same units.