

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description

The 5721 ITFS/MDS/MMDS Digital Transmitter can be subdivided further as follows:

Modulator Tray	<ul style="list-style-type: none">- Digital Data Input Card- IF Output QAM Modulator Card- Front Panel Display and Control- Power Supply
Upconverter/Amplifier Tray	<ul style="list-style-type: none">- Modulator Module- IF Processing Module- Power Amplifier Module- Power Supply Module- Control Monitoring Module- L.O./Upconverter Module- Backplane Board- Front Panel LCD Display/Keypad Entry

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Modulator Tray

Due to proprietary concerns on the part of Comstream Corporation, The circuit description of the CM720M modulator will be presented on a system level.

The CM720M modulator tray generates a 64 QAM digital IF output which is used to drive the upconverter/amplifier tray. External, multiplexed 28 MBPS data is applied to the rear of the modulator tray using a shielded RJ-45 jack (J5). The digital data is received using an IC chip set known as TAXI[®] (Transparent Asynchronous Transmitter/Receiver Interface) on the Digital Data Input Card. TAXI is a registered trademark of Advanced Micro Devices (AMD).

The TAXI receiver operates in 10 bits-per-byte mode (8 data bits, 1 even parity bit, 1 active low-frame sync bit). The TAXI receiver reference clock (5 MHz) is fed to the modulator.

The digital bit stream of data from the Digital Data Card is fed to the Quadrature Amplitude Modulator (QAM) digital modulator on the Modulator Card. The data/clock signal is continuously monitored for the following:

1. Clock out of spec (more/less than 100 ppm of spec)
2. Loss of clock
3. Parity errors
4. Frame sync errors
5. Sync acquisition errors
6. TAXI decoding violations

The system is normally frequency locked to the input clock. If the input clock is not present, the system switches over to internal timing to preserve the output spectrum. When the system clock returns, the system will detect the presence of the clock and return to normal operation.

The output power of the modulator, which is monitored continuously, is adjustable from -27 dBm to -5 dBm.

The front panel of the CM720M modulator contains a seven-segment LED display, a LCD display, two LED fault indicators, control keys, and a numerical keypad to monitor and control the operating status of the tray. Also included on the front panel are IF and RF output test ports (refer to *Chapter 3: Front Panel Operation* of the Installation and Operation Manual, included in Exhibit II of this report, for a complete description of front panel operation).

The CM720M power supply is autoranging for AC inputs from 90 to 264 VAC and 47 to 63 Hz.

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IF Processing Module

The IF output signal from the CM720M modulator is applied to the IF input jack (J14) on the rear of the tray. This IF input signal is then fed to the IF Processing Card (1585-3108).

The IF signal enters the card at J1 and is transformer coupled for impedance matching of the IF signal (75Ω to 50Ω). The signal is then applied to an adjustable resistor pad network which allows for three IF input level ranges of 10 dB each. The signal is amplified and applied to a 6 dB transformer directional coupler which provides a sample to a peak detector in the ALC portion of the circuit. The main output of the coupler is fed to frequency response correction circuitry which consist of four adjustable notch filters. The frequency response correction circuit may be removed using on board jumpers. The output of the frequency response corrector is amplified and applied to a PIN diode attenuator. The ALC circuitry takes a peak detected sample of the IF signal and generates an ALC voltage which biases the PIN diode attenuator. The ALC circuit senses any change in the IF level and automatically adjust the loss through the PIN attenuator to compensate, thereby maintaining a constant IF output regardless of minor changes in the input signal. The ALC circuit uses a DC level generated externally to control the output power level. There are two possible bias voltage inputs. The first, Inner Loop, is generated from a peak detected sample of the output amplifier. The second, Outer Loop, is used only if an external final amplifier tray is connected to the system. If both Inner Loop and Outer Loop inputs are used, the signal that is the largest in level controls the ALC circuit.

The ALC circuit may be bypassed by placing switch SW2 in the manual position. When the ALC circuit is disabled, the loss through the PIN attenuator is adjusted by a manual gain potentiometer which then directly controls the output in a manual fashion.

The ALC circuit also contains a average detector which detects the average level of the IF signal. This average level is compared to the output of the peak detector and if the average level approaches the peak level, indicating a loss of modulation on the IF signal, a mute signal will be generated muting the IF. This prevents against overpower conditions in situations where the modulating signal is interrupted. The ALC circuit provides several front panel LED indicators including: Peak Vs. Average Fault, I/P Fault, Mute, and ALC Fault.

The output of the PIN diode attenuator is amplified and applied to three sections of group delay equalization which compensate for group delay created by external filters. Each section of group delay may be removed from the circuit using on board jumpers. For non-adjacent analog applications, Delay Equalizer 1 is removed from the circuit. For adjacent analog applications, all three sections are used. For adjacent and non-adjacent digital applications, Delay Equalizer 3 is removed from the circuit. The output of the delay equalizer circuit is fed to a 6 MHz lumped element bandpass filter. The bandpass filter may be removed from the circuit using on board jumpers. The bandpass filter may also be bypassed through a SAW filter when tight filtering of the IF is required.

The output of the bandpass filter is applied to a linearity correction circuit which compensates for compression in later stages of the system. The output of the linearity correction circuit is fed to a 6 dB transformer directional coupler which provides a front panel sample of the IF signal. The main output of the coupler is connected to the output of the IF Processing Card (J1B).

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Frequency Generator/Upconversion/PLL Module

The Frequency Generator/Upconversion/PLL Module consist of a L.O./Upconverter Board (1585-3117), Interdigital Filter (2140-1006), and a Single stage Amplifier Board (1585-3101).

The L.O./Upconverter Board generates a UHF L.O. frequency using a voltage controlled oscillator (VCO) IC (V804ME01). The VCO is locked to an external precise 10 MHz reference using a frequency synthesizer PLL IC (LMX2325TM) in a phase lock loop configuration. The LMX2325TM is a high performance frequency synthesizer with integrated prescalers and uses a proprietary digital phase lock loop technique to produce a very stable low noise signal that is used to control the VCO frequency. The desired L.O. frequency is selected using the front panel LCD display/keypad. The Control Monitoring Assembly detects the keyboard input and routes the serial data to the serial data input of the PLL IC.

Under normal operating conditions, the external 10 MHz precise reference input will be routed to the oscillator input of the PLL IC through a magnetic latching relay (K1). IF the external precise reference is removed the relay will open and an internal 10 MHz reference oscillator IC will be routed to the oscillator input of the PLL IC.

The L.O. signal from the VCO is buffered to an internal microstrip coupler which provides an L.O. sample that is routed to a rear panel jack. The L.O. signal is then amplified by an IC amplifier (U8) to a sufficient level to drive the L.O. input of an IC mixer(U10). An IF input to the mixer is provided via the IF Processing Assembly. The output of the mixer is amplified by an IC amplifier (U12) and fed to the RF output jack of the board (J8).

The RF signal is then fed to a 6 MHz bandpass interdigital filter (2140-1006) which selects the desired conversion frequency (L.O. - IF) and attenuates any undesired signals generated during the mixing process.

The RF output of the filter is then fed to the Single Stage Amplifier Board (1585-3101) which consist of a single IC amplifier (VNA-25) with a gain of 14 dB. An RF sample is obtained using a microstrip coupler (J2). The main RF output is connected to the output jack of the module (J8).

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2.4 Circuit Description - continued

Power Amplifier Module

The Power Amplifier Module consist of an 20W PEP Amplifier Module (1585-3194), 1 Section Bias Board (1585-3270), and Dual Power Detector Board (1585-3125).

The 20W pep Amplifier provides amplification of the RF signal. The RF input signal from the Frequency Generator/Upconversion/PLL Module enters the module at J1.

The power amplifier consist of four GaAs FET amplifiers designated Q1 through Q4 (FLL101ME driving a second FLL101ME driving a FLL351ME driving a MGFS45V2527-51) with an overall gain of approximately 47 dB. A 20 dB microstrip coupler provides a sample of the RF signal at J3. A reflective power sample is provided by a circulator (Z1).

The DC biasing of the FET amplifiers in each section of the module is controlled and filtered by corresponding daughter boards (daughter board D1 controls the biasing for Q1, Q2 and Q3 and daughter board D3 controls the biasing for Q4). which are soldered directly to the main board. The DC bias drain to source currents are set by adjusting the negative gate to source voltages which are adjusted by potentiometers on the daughter boards.

The 1 Section Bias Protection Board distributes the -5V bias voltage and the +10V drain voltage to the Amplifier Module as well as providing protection from an overcurrent condition with board mounted fuses.

The -5V bias voltage is generated on board using a TL104 Op Amp circuit. This bias voltage is also used as an interlock which is fed to the Transmitter Control and Monitoring Module. If the bias voltage is lost, the control circuitry will immediately shut down the switching supply, thereby removing the drain voltages from the amplifier module and protecting the GaAs FET devices.

A Differential amplifier Op Amp circuit is used to monitor the drain current of the FET devices. The Op Amp output drives an LED indicator as well as an opto-isolated O/P amplifier status line.

The Dual Power Detector Board inputs forward and reflective power samples from the Amplifier Module and detects the levels using peak detector circuits. These circuits provide voltage levels proportional to the power level of the samples signals which are used for metering and ALC purposes. Metering adjustments are provided with on board potentiometers.

The Dual Power Detector board also contains a gating pulse tining circuit that serves to maintain the proper power level when sync suppression scrambling systems are used.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

The 5 Section Bias Protection Board distributes the -5V bias voltages and +10V drain voltages to the Amplifier Module as well as providing protection from an over current condition with board mounted fuses.

The -5V bias voltage is generated on board using a voltage regulator (LM377T). This bias voltage is also used as an interlock which is fed to the Transmitter Control and Monitoring Module. IF the bias voltage is lost, the control circuitry will immediately shut down the switching supply, thereby removing the drain voltages from the amplifier modules and protecting the GaAS FET devices.

Differential amplifier OP Amp circuits are used to monitor the drain currents of the FET devices. The OP Amp outputs drive LED indicators as well as an opto-isolated O/P amplifier status line.

The Dual Power Detector Board inputs forward and reflective power signals from the Amplifier Module and detects the levels using peak detector circuits. These circuits provide voltage levels proportional to the power level of the sampled signal which are used for metering and ALC purposes. Metering adjustment is provided with on board potentiometers.

The Dual Power Detector Board also contains a gating pulse timing circuit that serves to maintain the proper power level when sync suppression scrambling systems are used.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Transmitter Control Monitoring and Module

The Transmitter Control and Monitoring Module (1585-1129) consist of an 8-bit microcontroller (MC68HC705B⁶) and associated control circuitry and provides the capability to control and monitor the operating status of the transmitter. The interconnection between the Transmitter Control and Monitoring Module, IF Processing Module, and Local Oscillator/Upconverter Module is accomplished through the Backplane Board. The interconnection between the Transmitter Control and Monitoring Module, Power Supply Module, and Power Amplifier Module is accomplished through interconnect cables. A detailed listing of all the interfaces between the Transmitter Control and Monitoring Module and the various modules which make up the ITS-5724 transmitter is given below.

Power Amplifier Module

<u>Signal Name</u>	<u>Signal Type/Description</u>
Amplifier Interlock	Discrete contact closure input - indicates Power Amplifier Module is installed.
Reflective Pwr Metering	Analog input (0 - 1.25V) - indicates reflective power from Power Amplifier Module.
Overtemp Fault	Discrete contact closure input - indicates overtemp condition exist in Power Amplifier Module.
O/P Amplifier Status	Discrete open collector input - indicates operating status of output amplifier.
-5V Bias Sense	Analog input (0 - 6V) - indicates the voltage level of the - 5V bias supply.

Local Oscillator/Upconverter Module

<u>Signal Name</u>	<u>Signal Type/Description</u>
External Reference Indicator	Discrete open collector input - indicates the presence of external 10 MHz reference.
Logic Enable	Discrete CMOS output - provides a load enable signal to the frequency synthesizer chip.
Data	Discrete CMOS output - provides serial data to the frequency synthesizer chip.
Clock	Discrete CMOS output - provides the serial clock to the frequency synthesizer chip.
AFC	Analog input (1 - 10V) - indicates the level of the AFC voltage.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Transmitter Control Monitoring and Module - continued

<u>Signal Name</u>	<u>Signal Type/Description</u>
L.O./Upconverter Interlock	Discrete contact closure input - indicates L.O./Upconverter Module is installed.
Unlock Indicator	Discrete open collector input - indicates the L.O./Upconverter Module is locked to the external or internal 10 MHz reference.

IF Processing Module

<u>Signal Name</u>	<u>Signal Type/Description</u>
Open Loop Monitor	Analog input (1 - 1.25V) - indicates output power of an external amplifier.
Forward Power Metering	Analog input (0 - 1.25 V) - indicates output power tray's power amplifier.
IF Processor Interlock	Discrete Contact Closure Input - indicates that IF Processing module is installed.
ALC Voltage	Analog input (0 - 10V) - indicates voltage applied to pin attenuator in ALC circuit.
Mute to IF Processor	Discrete open collector output - controls mute feature in the IF processor.
Mute from IF Processor	Discrete open collector input - indicates IF processor is in mute.
Input Fault	Discrete open collector input - indicates that IF is not present.
ALC Conditioning	Analog Input (-1 - +1V) - Provides adjustment voltage to the ALC circuitry to correct for frequency dependence of peak detector.

Power Supply Module

<u>Signal Name</u>	<u>Signal Type/Description</u>
P.S Good	Discrete open collector input - indicates switching power supply is operating properly.
P.S Enable	Discrete open collector output - enable signal to switching power supply.

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2.4 Circuit Description - continued

Transmitter Control and Monitoring Module - continued

Front Panel Assembly

<u>Signal Name</u>	<u>Signal Type/Description</u>
Fault Anode	Fault LED drive voltage (+5V) - supply to anode of Fault LED.
Fault Cathode	Discrete open collector output - provides pull down to turn on Fault LED.
Operate Anode	Fault LED drive voltage (+5V) - supply to anode of Operate LED.
Operate Cathode	Discrete open collector output - provides pull down to turn on Operate LED.
S1-S5	Discrete contact closure inputs - input lines from front panel keyboard switches.
VSS (GND)	Ground - Provides return to front panel board.
VCC	+5VDC - provides +5V to front panel display logic.
VEE	Control voltage output (0 - 5V) - controls contrast of LCD display.
RS	Discrete TTL/HCMOS output - indicates to display whether instruction or data command is being sent.
E	Discrete TTL/HCMOS output - initiates the transfer of data to the display.
DB0-DB7	Discrete TTL/HCMOS bidirectional data lines - data lines which pass data between the display and transmitter control and monitoring module.
Anode Backlight	Control voltage output (3.8 - 4.6 V) - provides drive voltage to LCD backlight of display.
Cathode Backlight	Control voltage return - return for control voltage of LCD display.

SCADA Communications Interface

<u>Signal Name</u>	<u>Signal Type/Description</u>
+ Serial Line	+RS-485 communications line - provides the +differential line for the +bidirectional line of the bidirectional RS-485 communications..
- Serial Line	-RS-485 communications line - provides the -differential line for the +bidirectional line of the bidirectional RS-485 communications..

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Transmitter Control and Monitoring Module - continued

Control and Remote Interface

<u>Signal Name</u>	<u>Signal Type/Description</u>
Standby Command (FA)	Discrete open collector input - indicates frequency agile is requesting transmitter be placed into standby mode.
Operate Command (FA)	Discrete open collector input - indicates frequency agile is requesting transmitter be placed into operate mode.
Aural/Visual Mute (FA)	discrete open collector input - indicates that frequency agile is presently in aural/visual mute.
ABS Standby CMD	Discrete open collector input - indicates that Automatic Back-up System is requesting transmitter be placed into standby.
EXT Operate CMD	Discrete open collector output - enables external amplifier when transmitter enters operate mode.
XMTR Interlock Iso Return	Ground - configurable ground return which can be either jumpered directly to ground or be the "source" pin of an FET so that transmitter interlock can be daisy chained with other transmitters.
XMTR Interlock	Discrete open collector output - enables transmitter interlock or complete interlock daisy chain.
EXT O/P Amp Mod Status	Discrete open collector input - indicates external amplifier has a fault.
EXT P.S. Status (amp)	Discrete open collector input - indicates power supply in external amplifier is functional.
Operate Indication	Discrete open collector output - indicates transmitter is in operate mode.
EXT Overtemp (amp)	Discrete open collector input - indicates external amplifier has overtemp condition.
EXT Refl Pwr (amp)	Analog input (0 - 1.25V) - indicates reflected power of external amplifier.
Standby CMD (RCVR)	Discrete open collector input - indicates external receiver is requesting transmitter be placed into standby.
Operate Command	Discrete open collector input - indicates external receiver is requesting transmitter be placed into operate.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Transmitter Control and Monitoring Module - continued

Control and Remote Interface	
<u>Signal Name</u>	<u>Signal Type/Description</u>
RMT Operate Indicator	Discrete open collector output - indicates transmitter is in operate mode.
O/P Amp Module Status	Discrete open collector output - indicates no faults present in amplifier modules of transmitter.
RMT FWD Power O/P	Analog output (0 - 1.25V) - power amplifier module forward power loop through.
RMT REFL Power	Analog output (0 - 1.25V) - power amplifier module reflective power loop through.
RMT XMTR Fault Ind	Discrete open collector output - indicates fault exist in transmitter.
IF Present Status O/P	Discrete open collector output - indicates IF is not present.
RMT PLL Locked Ind	Discrete open collector output - indicates frequency generator/upconverter is unlocked.
RMT XMTR Overtemp Ind	Discrete open collector output - indicates transmitter amplifier module is in overtemp.
P.S. Fault Ind	Discrete open collector output - indicates that power supply of transmitter has failed.
EXT PLL Ref Present	Discrete open collector output - indicates external 10 MHz reference is not present.
RMT XMTR Stby Command	Discrete open collector input - indicates remote interface is requesting transmitter be placed in standby.
RMT XMTR Oper Command	Discrete open collector input - indicates remote interface is requesting transmitter be placed in operate.

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2.4 Circuit Description - continued

Power Supply Module

The transmitter may be powered by either a 115 VAC/60 Hz or 230 VAC/50 Hz source. The AC source enters the tray at jack J1 and passes through the Power Entry Module. The Power Entry Module contains a switch, for selecting 115V or 230 V input, a line filter and fuse protection. The output of the Power Entry Module is distributed to a terminal block (TB1). Varistors VR1, VR2, VR3 and VR4 provide transient and over voltage protection to the transmitter. The rear panel circuit breaker applies AC voltage to the input of the 530 W Switching Power Supply (MP6-2K-4II-00-415-CE) located on the Power Supply Module.

The Switching Supply provides three outputs. The first output is a +11 VDC/31A line used to power the GaAs FET amplifiers with power. The remaining outputs are +12 VDC lines used to supply the modules within the transmitter. The +12 VDC line is also used to power the 12 VDC cooling fan via the Backplane Board.