EXHIBIT I

FCC TYPE ACCEPTANCE REPORT

ADC TELECOMMUNICATIONS

MODEL 5721

FCC ID-CJJ79XITS-7040

DIGITAL ITFS/MDS/MMDS TRANSMITTER

Date Filed _____

This application is filed in compliance with
Part 2, Part 21 and Part 74
of the FCC Rules and Regulations.

ADC Telecommunications
102 Rahway Road
McMurray, PA 15317

Rev. 1.0

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1.0 IDENTIFICATION OF APPLICANT AND EQUIPMENT

1.1 Applicant:

ADC Telecommunications
102 Rahway Road
McMurray, PA 15317-3345

The above name and address is printed on a label attached to the rear panel of the equipment.

1.2 Equipment and Model Number: 5721

This information is provided on the front panel of the equipment.

1.3 ADC Telecommunications shall manufacture this product in quantities necessary to satisfy market demand.

2.0 TECHNICAL DESCRIPTION - MODEL 5721

2.1 Introduction

The 5721 is a complete MDS/MMDS/ITFS transmitter capable of operating as digital television transmitter at a nominal power of 2.5 Watts (average). The 5721 is comprised of a modulator (Comstream CM720M) and Upconverter Amplifier.The modultor receives a 28 Mbit/sec serial bit stream, consisting of multiplexed MPEG-2 transport streams, translates the signal to a Quadrature Amplitude Modulated (QAM) format, converts the digital information to analog, and modulates the signal to IF. The modulator trtay's IF output signal is routed to upconverter/amplifier tray for IF signal processing and upconversion to the MDS/MMDS/ITFS frequency. The RF signal is then fed to an amplifier module for final amplification. The 5721 utilizes ALC circuitry for automatic level control of the output signal to maintain a constant power level. The 5721 transmitter is a 19-inch rack mount assembly and can be supplied with or without a cabinet. The unit is supplied complete with cables and cabinet slides.

Parameters and specifications for operation of this unit as a digital transmitter are provided on the following pages, and a complete circuit description and alignment procedure are also included in this report. Refer to the overall system block diagram and the particular referenced schematics in the attached circuit description section of this report.

2.0 TECHNICAL DESCRIPTION

2.2 Technical Specifications

Type of Emissions: 6M00D7W
Frequency Range ..... 2150 to 2162 and 2500 to 2686 MHz (any 6 MHz channel)
Output Power Rating: ..... 2.5 watts average
DC voltage and total current of final amplifier stage ..... 10 volts DC at 6.86 amps
(Class A - Not RF power dependent)

2.3 Performance Specifications

Operating Frequency Range ..... 2150 to 2162 and 2500 to 2686 MHz
RF output - Nominal:
Power ..... 2.5 watts average
Impedance ..... 50 ohms
Connector ..... Type N

Input (Modulator): ..... QAM, MPEG-2 Transport Stream
Impedance ..... 75 Ω (BNC)

Out-of-Band Power ..... Per FCC Rules
-25 dB max (at band edges)
-40 dB max (250.00 KHz above and 250.00 KHz below band edges)
-60 dB max (3.00 MHz above and 3.00 MHz below band edges)

Electrical Requirements

Power Line Voltage:
Modulator ..... 90 to 264 VAC, 47 to 63 Hz
Upconverter/Amplifier ..... 117 VAC ±10%, 60 Hz or
220 VAC ±10%, 50 Hz
Power Consumptin:
Modulator ..... 50 watts
Upconverter/Amplifier ..... 250 watts

Environmental

Maximum Altitude:
Modulator ..... 10,000 feet (3,048m)
Upconverter/Amplifier ..... 12,000 feet (3,660m)

Ambient Temperature:
Modulator ..... 0° to 50°C
Upconverter/Amplifier ..... 0° to 50°C

2.0 TECHNICAL DESCRIPTION

2.2 Technical Specifications - continued

Mechanical

Dimensions (WxDxH):

Modulator	19" x 21" x 8.75" (48.3cm x 53.3cm x 22.24cm)
Upconverter/Amplifier	19" x 18" x 1.75" (48.3cm x 45.7cm x 4.45cm)

Weight::

Modulator	12 lbs. (5.45 kgs)
Upconverter/Amplifier	45 lbs. (22.0 kgs)

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description

The 5721 ITFS/MDS/MMDS DigitalTransmitter can be subdivided further as follows:

Modulator Tray	- Digital Data Input Card - IF Output QAM Modulator Card - Front Panel Display and Control - Power Supply
Upconverter/Amplifier Tray	- Modulator Module - IF Processing Module - Power Amplifier Module - Power Supply Module - Control Monitoring Module - L.O./Upconverter Module - Backplane Board - Front Panel LCD Display/Keypad Entry

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description

Modulator Tray

Due to proprietary concerns on the part of Comstream Corporation, The circuit description of the CM720M modulator will be presented on a system level.

The CM720M modulator tray generates a 64 QAM digital IF output which is used to drive the upconverter/amplifier tray. External, multiplexed 28 MBPS data is applied to the rear of the modulator tray using a shielded RJ-45 jack (J5). The digital data is received using an IC chip set known as TAXI® (Transparent Asynchronous Transmitter/Receiver Interface) on the Digital Data Input Card. TAXI is a registered trademark of Advanced Micro Devices (AMD).

The TAXI receiver operates in 10 bits-per-byte mode (8 data bits, 1 even parity bit, 1 active low-frame sync bit). The TAXI receiver reference clock (5 MHz) is fed to the modulator.

The digital bit stream of data from the Digital Data Card is fed to the Quadrature Amplitude Modulator (QAM) digital modulator on the Modulator Card. The data/clock signal is continuously monitored for the following:

1. Clock out of spec (more/less than 100 ppm of spec)
2. Loss of clock
3. Parity errors
4. Frame sync errors
5. Sync acquisition errors
6. TAXI decoding violations

The system is normally frequency locked to the input clock. If the input clock is not present, the system switches over to internal timing to preserve the output spectrum. When the system clock returns, the system will detect the presence of the clock and return to normal operation.

The outptut power of the modulator, which is monitored continuously , is adjustable form -27 dBm to -5 dBm.

The front panel of the CM720M modulator contains a seven-segment LED display, a LCD display, two LED fault indicators, control keys, and a numerical keypad to monitor and control the operating status of the tray. Also included on the front panel are IF and RF output test ports (refer to *Chapter 3: Front Panel Operation* of the Installation and Operation Manual, included in Exhibit II of this report, for a complete description of front panel operation).

The CM720M power supply is autoranging for AC inputs from 90 to 264 VAC and 47 to 63 Hz.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

IF Processing Module

The IF output signal from the CM720M modulator is applied to the IF input jack (J14) on the rear of the tray. This IF input signal is then fed to the IF Processing Card (1585-3108).

The IF signal enters the card at J1 and is transformer coupled for impeadance matching of the IF signal (75Ω to 50Ω). The signal is then applied to an adjustable resistor pad network which allows for three IF input level ranges of 10 dB each. The signal is amplified and applied to a 6 dB transformer directional coupler which provides a sample to a peak detector in the ALC portion of the circuit. The main output of the coupler is fed to frequency response correction circuitry which consist of four adjustable notch filters. The frequency response correction circuit may be removed using on board jumpers. The output of the frequency response corrector is amplified and applied to a PIN diode attenuator. The ALC circuitry takes a peak detected sample of the IF signal and generates an ALC voltage which biases the PIN diode attenuator. The ALC circuit senses any change in the IF level and automatically adjust the loss through the PIN attenuator to compensate, thereby maintaining a constant IF output regardless of minor changes in the input signal. The ALC circuit uses a DC level generated externally to control the output power level. There are two possible bias voltage inputs. The first, Inner Loop, is generated form a peak detected sample of the output amplifier. The second, Outer Loop, is used only if an external final amplifier tray is connected to the system. If both Inner Loop and Outer Loop inputs are used, the signal that is the largest in level controls the ALC circuit.

The ALC circuit may be bypassed by placing switch SW2 in the manual position. When the ALC circuit is disabled, the loss through the PIN attenuator is adjusted by a manual gain potentiometer which then directly controls the output in a manual fashion.

The ALC circuit also contains a average detector which detects the average level of the IF signal. This average level is compared to the output of the peak detector and if the average level approaches the peak level, indicating a loss of modulation on the IF signal, a mute signal will be generated muting the IF. This prevents against overpower conditions in situations where the modulating signal is interrupted. The ALC circuit provides several front panel LED indicators including: Peak Vs. Average Fault, I/P Fault, Mute, and ALC Fault.

The output of the PIN diode attenuator is amplified an applied to three sections of group delay equalization which compensate for group delay created by external filters. Each section of group delay may be removed from the circuit using on board jumpers. For non-adjacent analog applications, Delay Equalizer 1 is removed from the circuit. For adjacent analog applications, all three sections are used. For adjacent and non-adjacent digital applications, Delay Equalizer 3 is removed from the circuit. The output of the delay equalizer circuit is fed to a 6 MHz lumped element bandpass filter. The bandpass filter may be removed from the circuit using on board jumpers. The bandpass filter may also be bypassed through a SAW filter when tight filtering of the IF is required.

The output of the bandpass filter is applied to a linearity correction circuit which compensates for compression in later stages of the system. The output of the linearity correction circuit is fed to a 6 dB transformer directional coupler which provides a front panel sample of the IF signal. The main output of the coupler is connected to the output of the IF Processing Card (J1B).

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Frequency Generator/Upconversion/PLL Module

The Frequency Generator/Upconversion/PLL Module consist of a L.O./Upconverter Board (1585-3117), Interdigital Filter (2140-1006), and a Single stage Amplifier Board (1585-3101).

The L.O./Upconverter Board generates a UHF L.O. frequency using a voltage controlled oscillator (VCO) IC (V804ME01). The VCO is locked to an external precise 10 MHz reference using a frequency synthesizer PLL IC (LMX2325TM) in a phase lock loop configuration. The LMX2325TM is a high performance frequency synthesizer with integrated prescalers and uses a proprietary digital phase lock loop technique to produce a very stable low noise signal that is used to control the VCO frequency. The desired L.O. frequency is selected using the front panel LCD display/keypad. The Control Monitoring Assembly detects the keyboard input and routs the serial data to the serrial data input of the PLL IC.

Under normal operating conditions, the external 10 MHz precise reference input will be routed to the oscillator input of the PLL IC through a magnetic latching relay (K1). IF the external precise reference is removed the relay will open and an internal 10 MHz reference oscillator IC will be routed to the oscillator input of the PLL IC.

The L.O. signal from the VCO is buffered to an internal microstrip coupler which provides an L.O. sample that is routed to a rear panel jack. The L.O. signal is then amplified by an IC amplifier (U8) to a sufficient level to drive the L.O. input of an IC mixer(U10). An IF input to the mixer is provided via the IF Processing Assembly. The output of the mixer is amplified by an IC amplifier (U12) and fed to the RF output jack of the board (J8).

The RF signal is then fed to a 6 MHz bandpass interdigital filter (2140-1006) which selects the desired conversion frequency (L.O. - IF) and attenuates any undesired signals generated during the mixing process.

The RF output of the filter is then fed to the Single Stage Amplifier Board (1585-3101) which consist of a single IC amplifier (VNA-25) with a gain of 14 dB. An RF sample is obtained using a microstrip coupler (J2). The main RF output is connected to the output jack of the module (J8).

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Power Amplifier Module

The Power Amplifier Module consist of an 20W PEP Amplifier Module (1585-3194), 1 Section Bias Board (1585-3270), and Dual Power Detector Board (1585-3125).

The 20W pep Amplifier provides amplification of the RF signal. The RF input signal from the Frequency Generator/Upconversion/PLL Module enters the module at J1.

The power amplifier consist of four GaAS FET amplifiers designated Q1 through Q4 (FLL101ME driving a second FLL101ME driving a FLL351ME driving a MGFS45V2527-51) with an overall gain of approximately 47 dB. A 20 dB microstrip coupler provides a sample of the RF signal at J3. A reflective power sample is provided by a circulator (Z1).

The DC biasing of the FET amplifiers in each section of the module is controlled and filtered by corresponding daughter boards (daughter board D1 controls the biasing for Q1, Q2 and Q3 and daughter board D3 controls the biasing for Q4). which are soldered directly to the main board. The DC bias drain to source currents are set by adjusting the negative gate to source voltages which are adjusted by potentiometers on the daughter boards.

The 1 Section Bias Protection Board distributes the –5V bias voltage and the +10V drain voltage to the Amplifier Module as well as providing protection from an overcurrent condition with board mounted fuses.

The –5V bias voltage is generated on board using a TL104 Op Amp circuit. This bias voltage is also used as an interlock which is fed to the Transmitter Control and Monitoring Module. If the bias voltage is lost, the control circuitry will immediately shut down the switching supply, thereby removing the drain voltages from the amplifier module and protecting the GaAs FET devices.

A Differential amplifier Op Amp circuit is used to monitor the drain current of the FET devices. The Op Amp output drives an LED indicator as well as an opto-isolated O/P amplifier status line.

The Dual Power Detector Board inputs forward and reflective power samples from the Amplifier Module and detects the levels using peak detector circuits. These circuits provide voltage levels proportional to the power level of the samples signals which are used for metering and ALC purposes. Metering adjustments are provided with on board potentiometers.

The Dual Power Detector board also contains a gating pulse tining circuit that serves to maintain the proper power level when sync suppression scrambling systems are used.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

The 5 Section Bias Protection Board distributes the -5V bias voltages and +10V drain voltages to the Amplifier Module as well as providing protection from an over current condition with board mounted fuses.

The -5V bias voltage is generated on board using a voltage regulator (LM377T). This bias voltage is also used as an interlock which is fed to the Transmitter Control and Monitoring Module. IF the bias voltage is lost, the control circuitry will immediately shut down the switching supply, thereby removing the drain voltages from the amplifier modules and protecting the GaAS FET devices.

Differential amplifier OP Amp circuits are used to monitor the drain currents of the FET devices. The OP Amp outputs drive LED indicators as well as an opto-isolated O/P amplifier status line.

The Dual Power Detector Board inputs forward and reflective power signals from the Amplifier Module and detects the levels using peak detector circuits. These circuits provide voltage levels proportional to the power level of the sampled signal which are used for metering and ALC purposes. Metering adjustment is provided with on board potentiometers.

The Dual Power Detector Board also contains a gating pulse timing circuit that serves to maintain the proper power level when sync suppression scrambling systems are used.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Transmitter Control Monitoring and Module

The Transmitter Control and Monitoring Module (1585-1129) consist of an 8-bit microcontroller (MC68HC705B`6) and associated control circuitry and provides the capability to control and monitor the operating status o the transmitter. The interconnection between the Transmitter Control and Monitoring Module, IF Processing Module, and Local Oscillator/Upconverter Module is accomplished through the Backplane Board. The interconnection between the Transmitter Control and Monitoring Module, Power Supply Module, and Power Amplifier Module is accomplished through interconnect cables. A detailed listing of all the interfaces between the Transmitter Control and Monitoring Module and the various modules which make up the ITS-5724 transmitter is given below.

Power Amplifier Module

Signal Name	Signal Type/Description
Amplifier Interlock	Discrete contact closure input - indicates Power Amplifier Module is installed.
Reflective Pwr Metering	Analog input (0 - 1.25V) - indicates reflective power from Power Amplifier Module.
Overtemp Fault	Discrete contact closure input - indicates overtemp condition exist in Power Amplifier Module.
O/P Amplifier Status	Discrete open collector input - indicates operating status of output amplifier.
-5V Bias Sense	Analog input (0 - 6V) - indicates the voltage level of the - 5V bias supply.

Local Oscillator/Upconverter Module

Signal Name	Signal Type/Description
External Reference Indicator	Discrete open collector input - indicates the presence of external 10 MHz reference.
Logic Enable	Discrete CMOS output - provides a load enable signal the the frequency synthesizer chip.
Data	Discrete CMOS output - provides serial data to the frequency synthesizer chip.
Clock	Discrete CMOS output - provides the serial clock the frequency synthesizer chip.
AFC	Analog input (1 - 10V) - indicates the level of the AFC voltage.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Transmitter Control Monitoring and Module - continued

Signal Name	Signal Type/Description
L.O./Upconverter Interlock	Discrete contact closure input - indicates L.O./Upconverter Module is installed.
Unlock Indicator	Discrete open collector input - indicates the L.O./Upconverter Module is locked to the external or internal 10 MHz reference.

IF Processing Module

Signal Name	Signal Type/Description
Open Loop Monitor	Analog input (1 - 1.25V) - indicates output power of an external amplifier.
Forward Power Metering	Analog input (0 - 1.25 V) - indicates output power tray's power amplifier.
IF Processor Interlock	Discrete Contact Closure Input - indicates that IF Processing module is installed.
ALC Voltage	Analog input (0 - 10V) - indicates voltage applied to pin attenuator in ALC circuit.
Mute to IF Processor	Discrete open collector output - controls mute feature in the IF processor.
Mute from IF Processor	Discrete open collector input - indicates IF processor is in mute.
Input Fault	Discrete open collector input - indicates that IF is not present.
ALC Conditioning	Analog Input (-1 - +1V) - Provides adjustment voltage to the ALC circuitry to correct for frequency dependence of peak detector.

Power Supply Module

Signal Name	Signal Type/Description
P.S Good	Discrete open collector input - indicates switching power supply is operating properly.
P.S Enable	Discrete open collector output - enable signal to switching power supply.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Transmitter Control and Monitoring Module - continued

Front Panel Assembly

Signal Name	Signal Type/Description
Fault Anode	Fault LED drive voltage (+5V) - supply to anode of Fault LED.
Fault Cathode	Discrete open collector output - provides pull down to turn on Fault LED.
Operate Anode	Fault LED drive voltage (+5V) - supply to anode of Operate LED.
Operate Cathode	Discrete open collector output - provides pull down to turn on Operate LED.
S1-S5	Discrete contact closure inputs - input lines from front panel keyboard switches.
VSS (GND)	Ground - Provides return to front panel board.
VCC	+5VDC - provides +5V to front panel display logic.
VEE	Control voltage output (0 - 5V) - controls contrast of LCD display.
RS	Discrete TTL/HCMOS output - indicates to display whether instruction or data command is being sent.
E	Discrete TTL/HCMOS output - initiates the transfer of data to the display.
DB0-DB7	Discrete TTL/HCMOS bidirectional data lines - data lines which pass data between the display and transmitter control and monitoring module.
Anode Backlight	Control voltage output (3.8 - 4.6 V) - provides drive voltage to LCD backlight of display.
Cathode Backlight	Control voltage return - return for control voltage of LCD display.

SCADA Communications Interface

Signal Name	Signal Type/Description
+ Serial Line	+RS-485 communications line - provides the +differential line for the +bidirectional line of the bidirectional RS-485 communications..
- Serial Line	-RS-485 communications line - provides the -differential line for the +bidirectional line of the bidirectional RS-485 communications..

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Transmitter Control and Monitoring Module - continued

Control and Remote Interface

Signal Name	Signal Type/Description
Standby Command (FA)	Discrete open collector input - indicates frequency agile is requesting transmitter be placed into standby mode.
Operate Command (FA)	Discrete open collector input - indicates frequency agile is requesting transmitter be placed into operate mode.
Aural/Visual Mute (FA)	discrete open collector input - indicates that frequency agile is presently in aural/visual mute.
ABS Standby CMD	Discrete open collector input - indicates that Automatic Back-up System is requesting transmitter be placed into standby.
EXT Operate CMD	Discrete open collector output - enables external amplifier when transmitter enters operate mode.
XMTR Interlock Iso Return	Ground - configurable ground return which can be either jumpered directly to ground or be the “source” pin of an FET so that transmitter interlock can be daisy chained with other transmitters.
XMTR Interlock	Discrete open collector output - enables transmitter interlock or complete interlock daisy chain.
EXT O/P Amp Mod Status	Discrete open collector input - indicates external amplifier has a fault.
EXT P.S. Status (amp)	Discrete open collector input - indicates power supply in external amplifier is functional.
Operate Indication	Discrete open collector output - indicates transmitter is in operate mode.
EXT Overtemp (amp)	Discrete open collector input - indicates external amplifier has overtemp condition.
EXT Refl Pwr (amp)	Analog input (0 - 1.25V) - indicates reflected power of external amplifier.
Standby CMD (RCVR)	Discrete open collector input - indicates external receiver is requesting transmitter be placed into standby.
Operate Commend	Discrete open collector input - indicates external receiver is requesting transmitter be placed into operate.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Transmitter Control and Monitoring Module - continued

Control and Remote Interface

Signal Name	Signal Type/Description
RMT Operate Indicator	Discrete open collector output - indicates transmitter is in operate mode.
O/P Amp Module Status	Discrete open collector output - indicates no faults present in amplifier modules of transmitter.
RMT FWD Power O/P	Analog output (0 - 1.25V) - power amplifier module forward power loop through.
RMT REFL Power	Analog output (0 - 1.25V) - power amplifier module reflective power loop through.
RMT XMTR Fault Ind	Discrete open collector output - indicates fault exist in transmitter.
IF Present Status O/P	Discrete open collector output - indicates IF is not present.
RMT PLL Locked Ind	Discrete open collector output - indicates frequency generator/upconverter is unlocked.
RMT XMTR Overtemp Ind	Discrete open collector output - indicates transmitter amplifier module is in overtemp.
P.S. Fault Ind	Discrete open collector output - indicates that power supply of transmitter has failed.
EXT PLL Ref Present	Discrete open collector output - indicates external 10 MHz reference is not present.
RMT XMTR Stby Command	Discrete open collector input - indicates remote interface is requesting transmitter be placed in standby.
RMT XMTR Oper Command	Discrete open collector input - indicates remote interface is requesting transmitter be placed in operate.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Power Supply Module

The transmitter may be powered by either a 115 VAC/60 Hz or 230 VAC/50 Hz source. The AC source enters the tray at jack J1and passes through the Power Entry Module. The Power Entry Module contains a switch, for selecting 115V or 230 V input, a line filter and fuse protection. The output of the Power Entry Module is distributed to a terminal block (TB1). Varistors VR1, VR2, VR3 and VR4 provide transient and over voltage protection to the transmitter. The rear panel circuit breaker applies AC voltage to the input of the 530 W Switching Power Supply (MP6-2K-4ll-00-415-CE) located on the Power Supply Module.

The Switching Supply provides three outputs. The first output is a +11 VDC/31A line used to power the GaAs FET amplifiers with power The remaining outputs are +12 VDC lines used to supply the modules within the transmitter. The +12 VDC line is also used to power the 12 VDC cooling fan via the Backplane Board.

2.0 TECHNICAL DESCRIPTION

2.5 Alignment Procedure

In the following procedure, the complete transmitter is adjusted for optimum performance, beginning with the start up procedure of the CM720M modulator, followed by the upconverter/amplifier, starting at the baseband input and adjusting each circuit for its specified performance while observing the appropriate output parameters of the board or subassembly being adjusted.

Because of the broadband nature of most of the amplifier stages, this is a straightforward procedure, easily accomplished if baseband, IF, and RF test equipment is available. In this procedure, the input signals are first connected and each circuit is adjusted in sequence by connecting the test equipment to the specified point.

Equipment Needed

Spectrum Analyzer	10 MHz Reference Generator
Oscilloscope	Video Signal Generator
RF Power Meter	Voltmeter
30 dB Directional Coupler	50Ω Load
10 dB Directional Coupler	

Adjust the spectrum analyzer for the following settings:

1. Resolution BW = 30 KHz
2. Video Averaging (ON) = 10
3. Span = 20 MHz
4. Video Bandwidth = 30 KHzx
5. Center Frequency = 44 MHz

The average power of a modulated QAM digital signal, with the specified analyzer settings, is +23dB higher than the displayed signal. The measurements in this alignment procedure will be given in average levels.

Example: Analyzer reading of –30 dBm
Average power = -30 dBm + 23 dBm = - 7 dBm.

2.0 TECHNICAL DESCRIPTION

2.5 Alignment Procedure - continued

MODULATOR TRAY

Follow the step listed below to bring the CM720M modulator online.

1. Turn on the tray by connecting the AC power cable the unit and observing the front panel LEDs. The front panel lights flash through a consistent sequence when the unit is first powered on. when power-up is complete, the four seven-segment LEDs will illuminate, and the Fault LEDs will not illuminate.

2. Verify that the power-up message is displayed on the front panel LCD. If necessary, adjust the LCD contrast by pressing the increase/decrease buttons on the front panel.

3. Set the time/date.

4. Set the transmit power to -40 dBm to -50 dBm.

5. Confirm that transmit power is enabled.

6. Use the front panel to verify that the AQM mode is at the desired setting.

7. Use the front panel to verify that the scrambler, Reed-Solomon encoder, interleaver, and differential encoder are all enabled.

At this point the CM720M modulator has been powered up and the output spectrum may be observed.

Using a spectrum analyzer verify the proper shape and center frequency (44 MHz) of the spectrum at the IF output port (J5). Verify that the power level corresponds to that set in step 4 above.

The modulator circuitry requires no user adjustments.

2.0 TECHNICAL DESCRIPTION

2.5 Alignment Procedure - continued

UPCONVERTER/AMPLIFIER TRAY

Control Monitoring Module (A4) 1585-1129

Set front panel configuration DIP switches as follows:

SW1	Open (no external amplifier)	SW5	Open (not used)
SW1	Open (external ITS-5010 modulator)	SW6	Open (not used)
SW3	Open (not used)	SW7	Open (not used)
SW4	Open (not used)	SW8	Open (English language LCD)

IF Processing Module (A3) 1585-1207

1. Select 75Ω input impeadance using jumpers J28 and J29.

2. Select Low Input Impeadance using jumpers J8, J9, J10 and J11.

3. Enable Peak Vs. Average detection by placing J30 into the In position.

4. Enable Frequency Response Correction by placing J2 and J3 into the In position.

5. Set Delay Equilizers and Attenuation Equilizers as follows:

Delay Equlizer1 (J35, J36)	Out
Attenuation Equlizer1 (J37, J38)	Out
Delay Equlizer2 (J43, J44)	Out
Delay Equlizer3 (J31, J32)	Out
Attenuation Equlizer3 (J33, J34)	Out

6. Set filter circuit to Band Pass Filter by placing jumpers J19, J20, J22 and J23 into the BPF position.

7. Select High Output Gain by placing jumpers J26 and J27 into the High position.

8. Remove linear equalization by placing front panel Linear Equalization toggle switch into the out position.

9. Select Manual Gain by placing Gain Selection toggle switch into the Manual position.

LO/Upconverter Module (A5) 1585-1143

1. Place Reference jumper J1 into the External position..

2.5 Alignment Procedure - continued

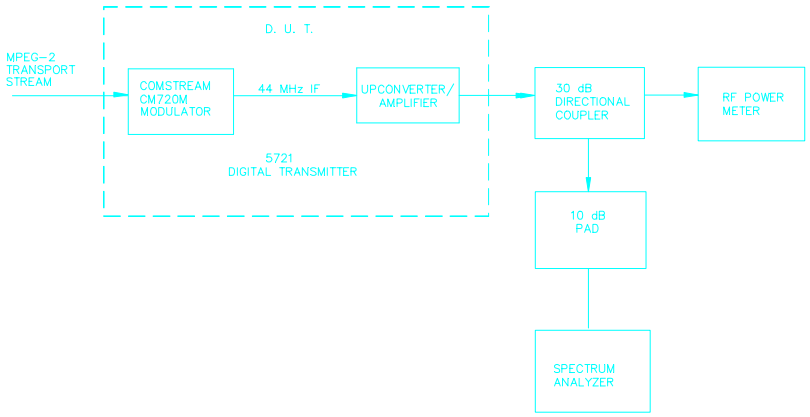
Power Amplifier Module (A6) 1585-1136

1. Select Average Detection by placing J2 into the Average position on the Dual Power Detector Module.

2.0 TECHNICAL DESCRIPTION

2.5 Alignment Procedure - continued

Connect the 5721 as shown below:



Power Setup/Meter Calibration

1. Apply power to the tray by placing the rear panel power switch (CB1) into the on position.
2. Measure voltage on Forward Detector Level test point on the Power Amplifier module front panel and adjust for 0 volts using the Forward Zero potentiometer.
3. Measure voltage on Reflective Detected Level test point on the Power Amplifier module front panel and adjust for 0 volts using the Reflected Zero potentiometer.
4. Verify that no faults are displayed on the LCD display on the front panel of the tray.
5. Place transmitter into operate by pressing the Operate button below the LCD display.
6. Adjust Manual Gain potentiometer on front panel of IF Processing module for 2.5 watts (average) as observed on RF power meter.
7. Measure voltage on Forward Detected test point on front panel of Power Amplifier module and adjust for 1 volt using the Forward Level potentiometer.
8. Place transmitter into standby by pressing the Standby button below the font panel LCD display.
9. Remove cable connection from RF output jack (J8) of tray.
10. Place transmitter into operate mode by pressing the Operate button below the front panel LCD display.
11. Measure Reflective Detected Level test point and adjust for 1V using Reflected Level potentiometer.
12. Place transmitter into standby by pressing the Standby button below the front panel LCD display.

2.0 TECHNICAL DESCRIPTION

2.5 Alignment Procedure - continued

13. Reconnect cable to RF output jack (J8) of the tray.

14. Place transmitter into the operate mode by pressing the Operate button below the front panel LCD display.

15. Adjust ALC potentiometer on front panel of IF Processing module for 1 volt on the Forward Detected Level test point on power Amplifier Module.

RF Response

1. Adjust video generator for cable sweep input signal.

2. Adjdust Spectrum Analyzer for the following settings:

Span	10MHz
Resolution BW	100KHz
Video BW	100 KHz
Center Frequency	Channel Frequency

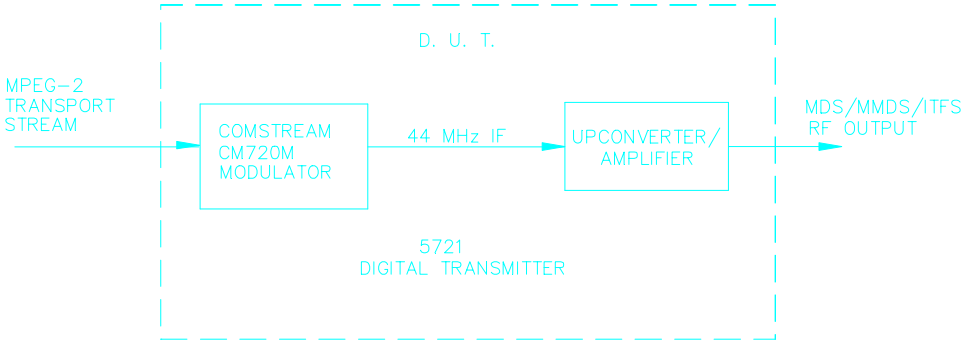
3. Adjust the four Frequency Response potentiometers on the front panel of the IF Processing module for flat response on spectrum analyzer.

2.0 TECHNICAL DESCRIPTION

2.6 Block Diagrams

System Block Diagram:

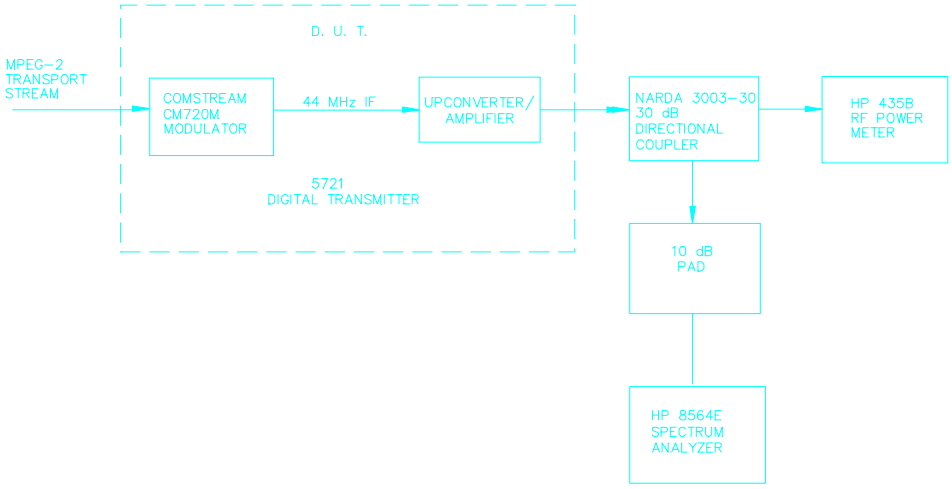
The following is a system block diagram for the 5721 digital transmitter. Detailed Block Diagrams and Schematics are included in Exhibit II.



3.0 ENGINEERING DATA

3.1 RF Power Measurements

The following block diagram describes the test equipment set-up for the following measurement:



Using the test set-up above, the output power of the 5721 was adjusted to obtain 2.5 watts average output power as observed on the power meter.

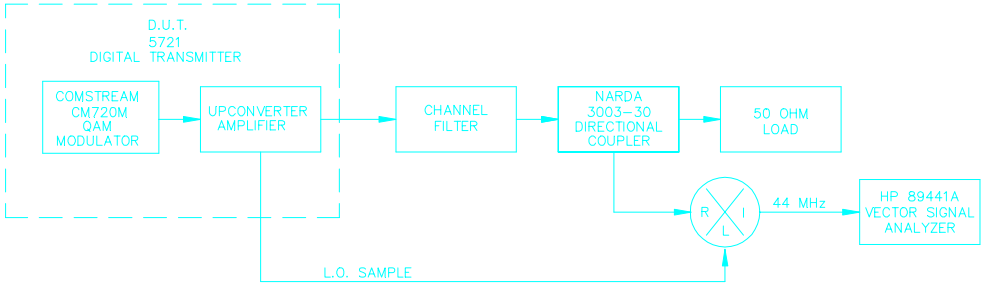
With the power level properly set to 2.5 watts (average), all required test were performed and recorded in the following sections.

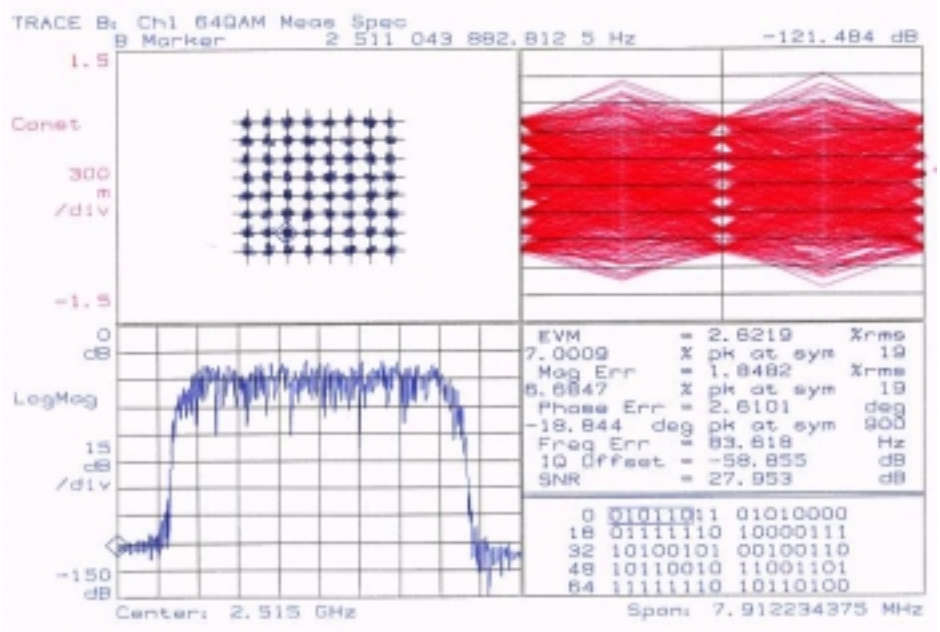
3.0 ENGINEERING DATA

3.2 Modulation Characteristics

The modulator tray incorporates a modulation technique known as QAM, Quadrature Amplitude Modulation, which uses two carriers, each of the same frequency, but 90° apart in phase. This means that one carrier trails the other by one fourth of a cycle. Each is then phase and amplitude modulated by a portion of the digital input signal. The two modulated signals are then combined and transmitted as a single waveform. The spectrum of a QAM signal is noise-like in appearance and has a relatively stable average power and a widely varying peak-envelope-power (PEP). The power is normally referred to in average power. QAM, used in conjunction with digital compression, provides a high bandwidth efficiency allowing a data rate of 30 MBPS in a 6 MHz channel bandwidth.

The following information and diagram is for descriptive purposes only, since there are currently no FCC MMDS/ITFS regulations for digital modulation characteristics.





Typical Demodulated Vector Signal Analyzer Display

3.0 ENGINEERING DATA

3.2 Modulation Characteristics - continued

Constellation Diagram	(Upper left box) This diagram displays the in-phase signal (I) on the x-axis versus the quadrature phase signal (Q) on the y-axis. The points shown on the constellation vector diagram correspond only to the symbol clock time. These points are commonly referred to as detection decision points and are called symbols. Constellation diagrams help identify such things as amplitude imbalance, quadrature error or phase noise.
Eye Diagram	(Upper right box) Eye diagrams are commonly used in digital communication systems and help identify problems such as ISI (inter- symbol interference) and jitter. The eye diagram is the display of I (real) or Q (imaginary) signal versus the time that is triggered by the symbol clock.
Spectrum Display	(Lower left box) This display shows the spectrum of the QAM modulated signal and is useful for determining and adjusting the frequency response of the signal.
Error Vector Magnitude	(Lower right box) This parameter indicates the magnitude of the vector which connects the I Q reference signal phasor to the I Q measured signal phasor. The error vector magnitude (EVM) is computed by the square root of the sum of the squares for each complex pair of points, in the time record, normalized to a reference point.
Magnitude Error	(Lower right box) This parameter indicates the difference in amplitude between the I Q reference signal and the I Q measured signal. Magnitude error is an indication of the quality of the amplitude component of the modulated signal. Magnitude error might indicate a high incidental AM modulation on the signal.
Phase Error	(Lower right box) This parameter indicates the difference in phase between the I Q reference signal and the I Q measured signal. The magnitude of the parameter is an indication of the quality of the phase component of the modulated signal. Phase error might be attributed by high incidental FM modulation on the signal.
Frequency Error	(Lower right box) This parameter indicates the carrier frequency error in relation to the analyzer's center frequency and is measured in Hz. Typical examples of frequency error are errors in RF frequency, LO frequency or digitizer clock rate.

3.0 ENGINEERING DATA

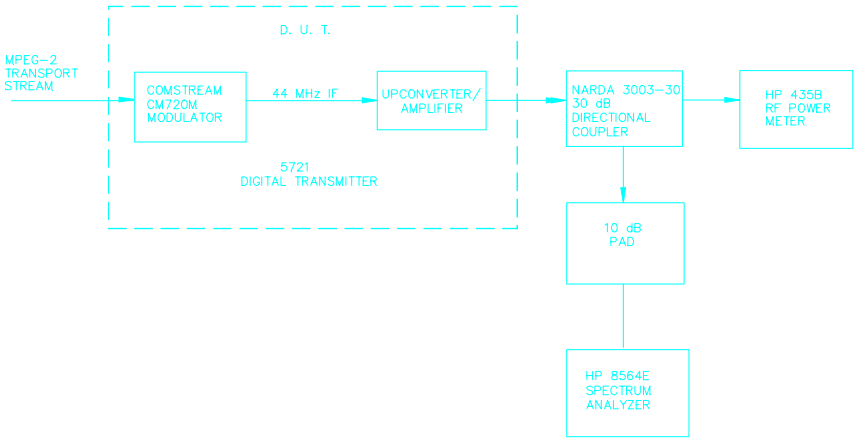
3.2 Modulation Characteristics - continued

I Q Offset (Origin Offset)	(Lower right box) This parameter indicates the magnitude of the carrier feedthrough (if the carrier is 100% suppressed, the I Q offset is zero). Carrier feedthrough is an indication of the balance of the I Q modulator used to generate the modulated signal. If the modulator is balanced, the carrier is nulled by the RF spectrum. Imbalance in the I Q modulator results in carrier feedthrough and appears as an origin offset in the constellation diagram.
Signal to Noise Ratio	(Lower right box) The signal to noise ratio (SNR) is the average symbol power of the transmitted waveform relative to the noise power. The noise power includes any term that causes the symbol to deviate from the ideal state position, such as additive noise, distortion and ISI (inter-symbol interference).
Detected Data	(Lower right box) The binary data in the box represents the detected or recovered data from the digitally modulated signal.

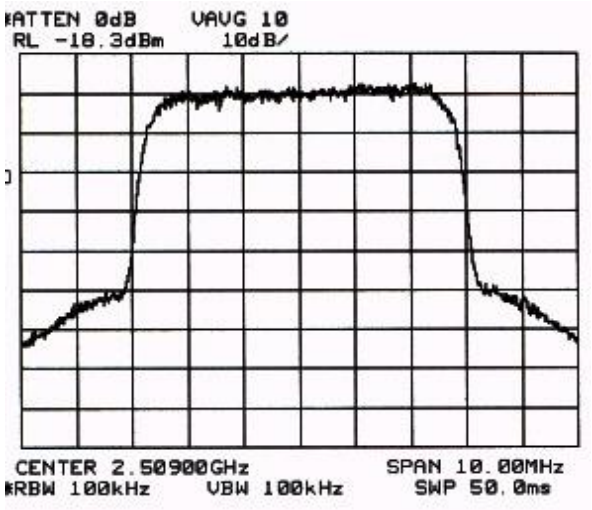
3.0 ENGINEERING DATA

3.3 Occupied Bandwidth

Using the following test set-up, the transmitter was operated at maximum power and a plot of the transmitter occupied bandwidth spectrum was taken and is shown below.



Spectrum Analyzer Plot (Occupied Bandwidth):

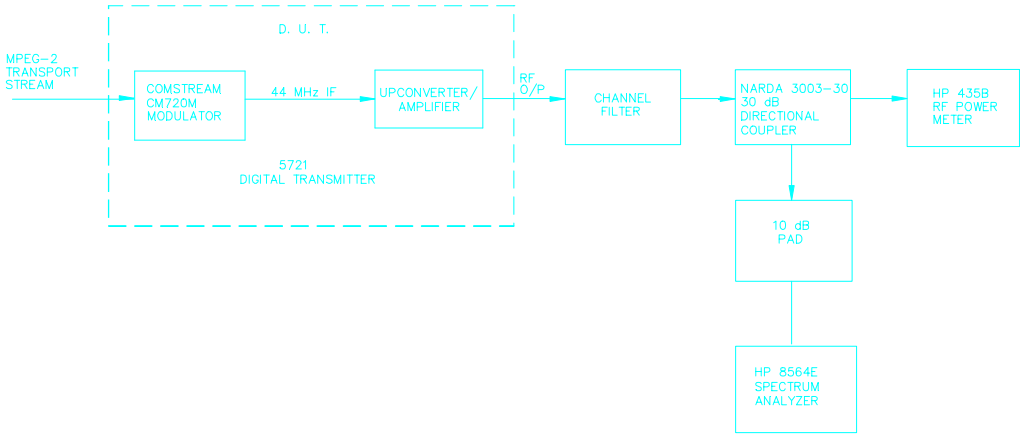


3.0 ENGINEERING DATA

3.4 Out-of-Band Power

Using the test set-up shown below, the spectrum outside of the specified channel was observed and the data was taken on all products above the -70 dB noise floor of the spectrum analyzer. The measured data is shown in the table on the following page for 2.5 watts average output power.

Spurious Emissions were observed on the analyzer at both 20 MHz and 40 MHz span (see spectrum plots on the following page). With the average inband signal set as the reference, the spurious emissions were observed and recorded.

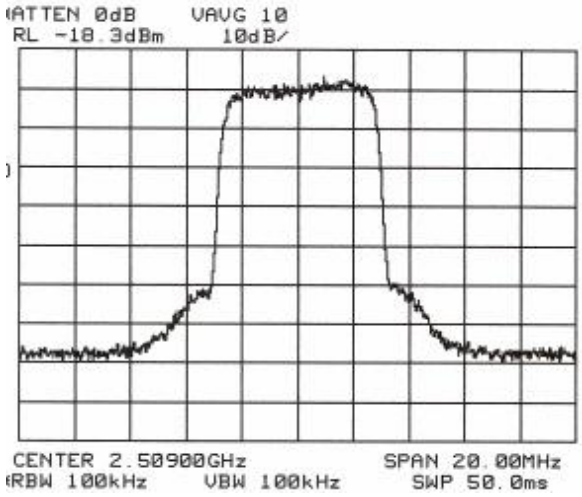


Frequency	Source	Level Observed
2509.00 MHz	Center of Channel	0 dB (Reference)
44.00 MHz	IF	None Observed
2507.00 MHz	Lower Channel Edge	-38 dB
2512.00 MHz	Upper Channel Edge	-27 dB
2506.75 MHz	250 KHz Below Channel	-47 dB
2512.25 MHz	250 KHz Above Channel	-48 dB
2504.00 MHz	3 MHz Below Channel	-69 dB
2515.00 MHz	3 MHz Above Channel	-65 dB
5018.00 MHz	2nd Harmonic	None Observed
7527.00 MHz	3rd Harmonic	None Observed
10036.00 MHz	4th Harmonic	None Observed
12545.00 MHz	5th Harmonic	None Observed
15054.00 MHz	6th Harmonic	None Observed
17563.00 MHz	7th Harmonic	None Observed
20072.00 MHz	8th Harmonic	None Observed
22581.00 MHz	9th Harmonic	None Observed
25090.00 MHz	10th Harmonic	None Observed

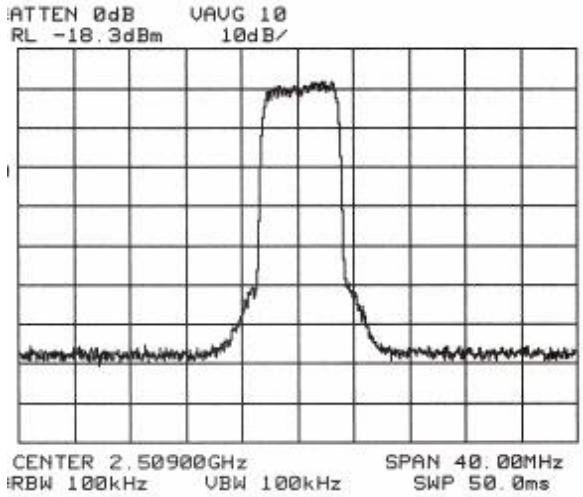
3.0 ENGINEERING DATA

3.4 Out-of-Band Power - continued

Spectrum Analyzer Plot (Out-of-Band Power)/20MHz Span:



Spectrum Analyzer Plot (Out-of-Band Power)/40MHz Span:



3.0 ENGINEERING DATA

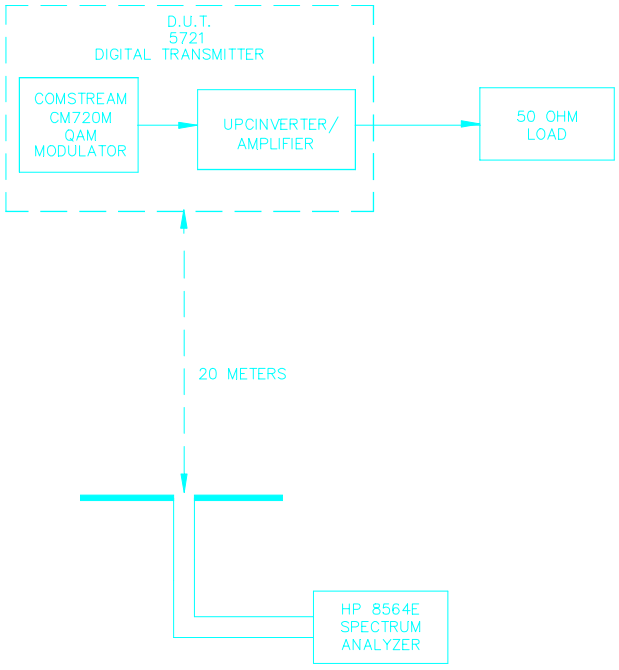
3.5 Radiated Emissions

Using the test set-up below, with the transmitter operating at 2.5 watts (average) output power, the spectrum analyzer was moved 20 meters from the transmitter and connected to a dipole antenna cut to the carrier frequency (2509 MHz). This antenna was oriented to maximize the received level, and the data was recorded. The antenna was then cut to the IF frequency, local oscillator frequency, and the second through the tenth harmonic frequencies and all signals received were maximized by antenna orientation, and their absolute levels were recorded.

With these various antennas the data was taken and recorded in the table on the following page.

Note: The spectrum analyzer had a maximum sensitivity of -100 dBm during these test.

Test Set-up:



3.0 ENGINEERING DATA

3.5 Radiated Emissions - continued

MEASURED LEVELS

Frequency	Source	Level Observed
44.00 MHz	IF	None Observed
2553.00 MHz	Local Oscillator	None Observed
2509.00 MHz	Center Channel	-80.0 dBm
5018.00 MHz	2nd Harmonic	None Observed
7527.00 MHz	3rd Harmonic	None Observed
10036.00 MHz	4th Harmonic	None Observed
12545.00 MHz	5th Harmonic	None Observed
15054.00 MHz	6th Harmonic	None Observed
17563.00 MHz	7th Harmonic	None Observed
20072.00 MHz	8th Harmonic	None Observed
22581.00 MHz	9th Harmonic	None Observed
25090.00 MHz	10th Harmonic	None Observed

3.0 ENGINEERING DATA

3.5 Radiated Emissions - continued

The measured levels were then compared to the following reference level:

If all of the transmitter's power (20 Watts) was radiated by an isotropic radiator, the power density at 20 meters would be:

$$Pd = Pt/4\pi R^2 = 2.5/4\pi (20)^2 \cong 0.4974 \times 10^{-3} \text{ w/m}^2$$

Using a dipole transmitting antenna increases this by 1.64 to:

$$1.64 * 0.4974 \times 10^{-3} = 0.8157 \times 10^{-3} \text{ w/m}^2$$

If a dipole receive antenna of area $1.64 * \lambda^2/4\pi$ is used to receive the signal, the received level would be:

$$0.8157 \times 10^{-3} * 1.64 * \lambda^2/4\pi = 1.512 \times 10^{-6} \text{w} = -58.2 \text{ dBw} = -28.2 \text{ dBm}$$

The receive levels were therefore at the following relative levels:

Frequency	Relative Measured Level (Ref = -28.2 dBm)
2509.00 MHz	**-51.8 Bc**

3.0 ENGINEERING DATA

3.6 Frequency Stability

The5721 is designed to operate using an external 10 MHz precise reference oscillator. The frequency stability of this external reference determines the frequency stability of the transmitter.

The frequency determining variables of the transmitter may be defined as follows:

F_{LO} = Desired local oscillator frequency
F_{IF} = Desired IF oscillator frequency
F_R = Desired external reference oscillator frequency
F_{RF} = Desired RF output frequency
E_{LO} = Local oscillator frequency offset error
E_{IF} = IF oscillator frequency offset error
E_R = External reference oscillator frequency offset error
E_{RF} = RF output frequency error

The PLL circuitry maintains a constant ratio between the external reference frequency and the output frequency of the oscillator. This ratio is defined below for both the LO and IF oscillators.

$G_{LO} = F_{LO}/F_R$
$G_{IF} = F_{IF}/F_R$

Any change in the external 10 MHz reference will effect a corresponding change in the output frequency such that the above ratios are maintained.

$$G_{LO} = (F_{LO} + E_{LO})/(F_R + E_R) = F_{LO}/F_R$$

$$G_{IF} = (F_{IF} + F_{IF})/(F_R + E_R) = F_{IF}/F_R$$

Solving for the change in output frequency yields:

$$E_{LO} = E_R * (F_{LO}/F_R) = E_R * G_{LO}$$

$$E_{IF} = E_R * (F_{IF}/F_R) = E_R * G_{IF}$$

The desired RF carrier frequency is equal to the LO frequency minus the IF frequency:

$$F_{RF} = F_{LO} - F_{IF}$$

The actual RF frequency, including any error introduced by the external reference, may be defined as follows:

$F_{RF} + E_{RF} = (F_{LO} + E_{LO}) - (F_{IF} + E_{IF})$
$F_{RF} + E_{RF} = (F_{LO} + F_{IF}) - (E_{LO} - E_{IF})$
$F_{RF} + E_{RF} = F_{RF} + (E_{LO} - E_{IF})$

3.0 ENGINEERING DATA

3.6 Frequency Stability - continued

Calculating for the error of the RF carrier yields:

$E_{RF} = (E_{LO} - E_{IF})$
$E_{RF} = E_R * G_{LO} - E_R * G_{IF}$
$E_{RF} = E_R (G_{LO} - G_{IF})$
$E_{RF} = E_R/F_R * (F_{LO} - F_{IF})$
$E_{RF} = E_R/F_R * F_{RF}$

Therefore, the error of the RF carrier is a function of the external 10 MHz reference error.

The maximum RF frequency error for this service is ±1.0 KHz. The highest channel frequency for this service (G4 = 2681.25 MHz) represents the worst case condition. With these values the maximum allowable reference error ($E_{R(max)}$) can be calculated.

$E_{R(max)} = 3.73$ Hz

The required reference oscillator stability may be calculated as follows:

Stability = $E_{R(max)}/F_R$
Stability = 3.73 Hz/10 x 10^6 Hz = 0.373 x 10^{-6}

Therefore, the RF frequency error of the ITS-5721 will not exceed ±1.0 KHz when operated with a precise reference oscillator with a stability equal to or better than 0.373 x 10^{-6}.

Commercially available GPS precise reference oscillators, such as the TRAK Systems 8821 which has a frequency stability of 1 x 10^{-11} over a temperature range of -10 to 50 °C, and a line voltage/frequency range from 85 to 265 VRMS/48 to 440 Hz (see TRAK Systems 8821 specifications on the following pages), insure a frequency stability within the tolerance specified in the Rules and Regulations for this service.

TRAK SYSTEMS DIVISION OF **TRAK MICROWAVE**

GPS Clock

Model 8821A (1-3/4") and B (3-1/2")

- **Accurate Time and Frequency with Just One Satellite**
- **Parallel Tracking of Six Satellites**
- **Oscillator Disciplined to GPS**
- **Choice of Oscillator Options**
- **5 MHz, 10 MHz, 1.544 MHz, or 2.048 MHz Outputs**
- **PC Software Disk for Setup and Output**
- **1 PPS Output Sync Within 1 Microsecond of GPS**
- **IRIG B Modulated and DC Output Options**
- **Form - C Relay and TTL Status Outputs**
- **Dual RS-232 Ports**
- **85 - 265 Vac or 100 - 370 Vdc Operation (24 or 48 Vdc Optional)**

The Model 8821 GPS Clock is a reduced-cost version of TRAK Systems' extremely successful Model 8812 and 8820 GPS Station Clocks. This versatile unit incorporates a six-channel parallel GPS receiver, a disciplined crystal oscillator, and a precise time and frequency generator in a single assembly. Phase offset of the 1 PPS output, referenced to UTC, is typically less than one microsecond when one or more satellites are being tracked.

The unit operates from 85 - 265 Vrms, 48-440 Hz or 100-370 Vdc, voltage ranging is automatic. No strapping or switchover is required. Optional power inputs include 24 Vdc and 48 Vdc.

The Model 8821 incorporates automatic oscillator calibration by GPS, automatic leap second correction and built-in calendar for automatic leap year updates. By using the remote setup feature, the operator may set up for automatic daylight savings time corrections. These features, a very high MTBF, and an RS-232 remote status monitoring feature virtually eliminate the need for site visits for setup, calibration, and maintenance.

The unit is supplied with a monitor and control application program for DOS-based computers. Program is normally supplied on a 3-½ inch floppy disk.

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MODEL 8821 SPECIFICATIONS

Internal Oscillator Options

E4A (Standard Model 8821A OCXO)

Accuracy while Tracking: (one-hour averaging)	<1 X 10^{-11}
Aging rate when coasting*:	<5 X 10^{-9}/day
1 PPS coasting drift*: (first 8 hours)	<6 µs/hour
Phase noise @ 10 Hz offset	<-100 dBc
Phase noise @ 100 Hz offset	<-130 dBc
Phase noise @ 1 KHz offset	<-135 dBc
Phase noise @ 10 KHz offset	<-140 dBc
Harmonic distortion	<-40 dBc
Non-Hormonic distortion	<-100 dBc

B7A (Standard Model 8821B OCXO)

Accuracy while Tracking: (one-hour averaging)	<1 X 10^{-11}
Aging rate when coasting*:	<5 X 10^{-10}/day
1 PPS coasting drift*: (first 8 hours)	<500 ns/hour
Phase noise @ 10 Hz offset	<-105 dBc
Phase noise @ 100 Hz offset	<-125 dBc
Phase noise @ 1 KHz offset	<-140 dBc
Phase noise @ 10 KHz offset	<-145 dBc
Harmonic distortion	<-30 dBc
Non-Hormonic distortion	<-100 dBc

Other Frequencies

Option B7 also available for output of 1.544 MHz, 2.048 MHz, or 5 MHz from the Model8821B.

Synchronization

The position of the antenna is determined by measuring the pseudo-range to four satellites and computing the position of these satellites using ephemeris data.

*Coasting factors apply only if there has been an antenna or receiver failure or if antenna is blocked from view of all satellites.

The receiver basic specifications are as follows:

Receiver Description:	L1 C/A code pseudo-ranging
Channels:	Six independent, continuous tracking channels
Frequency:	1575.42 MHz
Acquisition Time:	Typically less than two minutes

Navigation Outputs

Latitude, longitude, and height with a position accuracy of ± 30 meters, 2 drms (without SA) are available on the RS-232 ports.

Tracking Modes

In its default tracking mode, the Model 8821 automatically tracks one to six satellites, as available, on a stationary platform.

Two other modes, one for use on a moving platform and the other for use with an operator-entered fixed position, can be selected.

Timekeeping

The Model 8821 normally accumulates Universal Time (UTC). By command, this may be changed to local time. When local time is used, automatic daylight savings time adjustments are made at preprogrammed dates. Leap second and leap year adjustments are made automatically. Time is available on the RS-232 ports with a resolution of one millisecond.

Optional IRIG B Output**

Format:	Modulated IRIG B 122
Level:	3 Vpp nominal
Drive:	Will drive 50 ohms
Mod. Ratio:	Adjustable 2:1 to 6:1
Phase:	Modulated code on-time mark adjustable to within ± 10 microseconds of on-time reference.

** Rate and IRIG B outputs are a single option. Not available separately

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Optional Rate/DC Code Output**

Frequency:	One of the following may be selected: 1 PPH, 6 PPH, 12 PPH, 1 PPM, or 1 PPS - 1 MPPS in decade steps. IRIG B DC may be output in place of a selected rate.
Levels:	TTL
Drive:	50 ohms
Coherence:	Within one microsecond of UTC
Connector:	BNC

1 PPS Output

Levels:	TTL
Pulsewidth:	100 microseconds
Drive:	50 ohms
Coherence:	Within one microsecond of UTC
Connector:	BNC

High Rate Output (Sinewave)

Frequency:	Same as internal oscillator (10 MHz standard, others optional)
Level:	1 Vrms ± 10%
Drive:	50 ohms
Coherence:	Phase coherent to 1 PPS
Connector:	BNC

Optional Output Frequencies
Other available frequency outputs (Model 8821B only) include 5 MHz, 1.544 MHz, and 2.048 MHz.

Optional TTL Rate Output
TTL levels on High Rate Output in place of sinewave. Drive is 50 ohms.

Status Output
Three contacts of a Form-C relay provide tracking status output on a 9-pin connector. Contact rating is 1/2 amp. Also on this connector is status at TTL logic levels.

Remote Setup and Status
The following is a partial list of setup and status commands via the RS-232 Port.

Set/Request UTC/LOCAL
Set/Request local time offset
Set/Request daylight savings dates
Set/Request output rate
Set/Request local position
Set/Request minimum tracking elevation
Request time output
Request navigation data
Request tracking/locked status
Request time offset data
Request leap second status
Request satellites being tracked
Request firmware version

Time/Status Display (option)
The unit can be ordered with an LED display of time and status.

Power Supply
The unit operates on 85-265 Vrms, 48-440 Hz, or 100-370 Vdc. Power required is 25 watts nominal. Options available for 24 or 48 Vdc in place of ac.

Internal Battery
An internal lithium battery maintains GPS module stored data and coarse timekeeping during time that no external power is applied.

Physical
Model 8821A chassis is 19" wide X 1.72" high X 9" deep. Model 8821B chassis is 3.47 inches high. Weight is 9 pounds.

Antenna unit is 4.25 inches in diameter X 6.5 inches high. Weight is 7 ounces. It is connected to the main chassis via a coaxial cable. A 50 foot cable with TNC connectors is supplied. Optional lead-in systems with coaxial cables and in-line amplifiers are available to 2500 feet. Refer to application note AN-3A for complete details.

Temperature

Main unit:	-10 to + 50° C
Antenna:	-40 to + 70° C

See Page 2 for notes.

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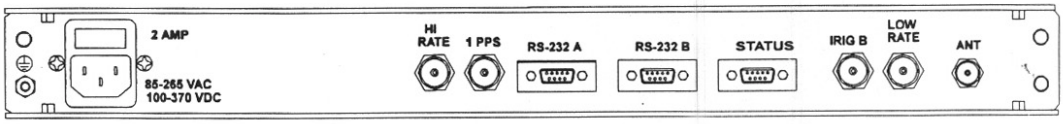
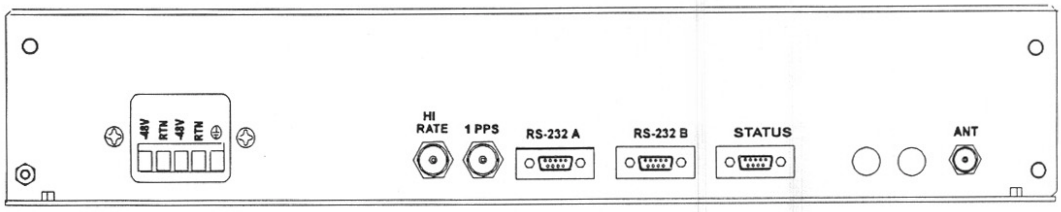
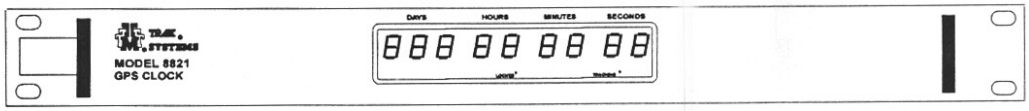
Typical Views



Model 8821A Rear Panel (with Code/Low Rate Option)



Model 8821B Rear Panel (with 48 Vdc Power Option)



Model 8821A with Display Option

Specification subject to change without notice.

Printed in U.S.A., January, 1996

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3.0 ENGINEERING DATA

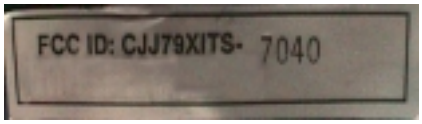
3.7 Test Equipment

MODEL	MANUFACTURER	DESCRIPTION		SERIAL #
8564E	Hewlett Packard	Spect. Analyzer 9 KHz-40 GHz		Rental
8595E	Hewlett Packard	Spect. Analyzer 9 kHz- 6.5GHz		3543A01613
3003-30	Narda	Directional Coupler	41991	
435B	Hewlett Packard	RF Power Meter	2732009080	
2349A	Hewlett Packard	30 Watt Power Head		3318A05525
2230	Tektronix	Oscilloscope		2230B025251
1992	Racal-Dana	Frequency Counter		950304
8135	Bird	50 Ohm Termination		8520
79	Fluke	Digital Multimeter		56660032
F-11-CHM-2-2	Thermotron	Temperature Test Chamber		5737
TEK-95	Tektronix	Video Generator		B0109999
VM700A	Tektronix	Video Measurement Set		B020724
1450-1	Tektronix	Television Demodulator		B020540
2022D	Marcone Instruments	Signal Generator	119168/061	
31732	California Amplifier	31 Channel Downconverter		6280121184

4.0 IDENTIFICATION LABELS/LABEL PLACEMENT AND PHOTOGRAPHS

4.1 Rear Panel FCC Identification Label:

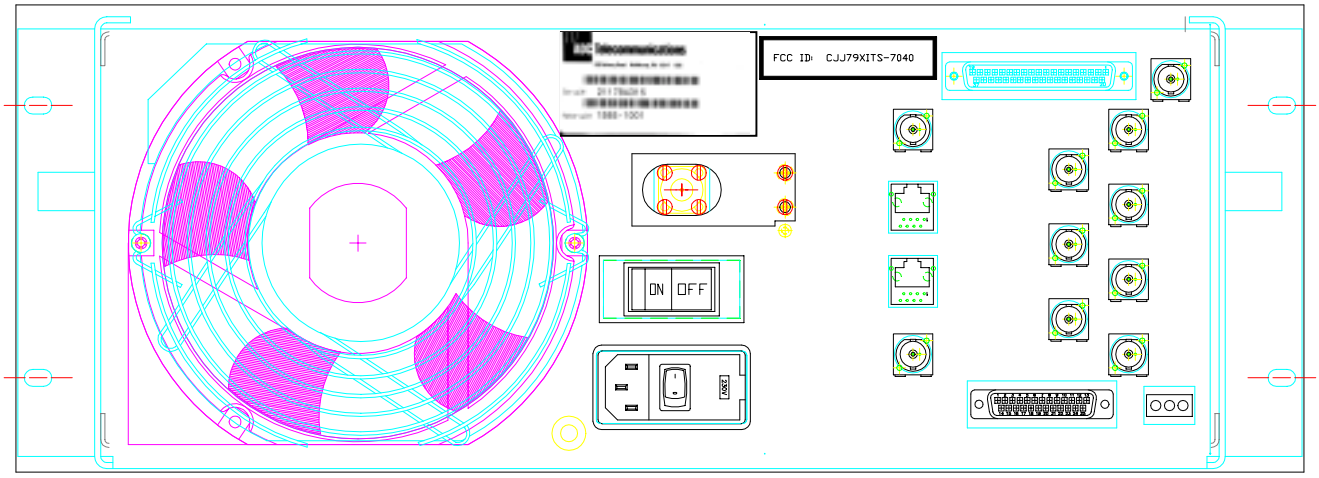
Note: The following Identification Labels and Label Placement Drawing can also be found in the Labels attachment.



4.2 Rear Panel ADC Telecommunications Manufacturer's Label:

4.0 IDENTIFICATION LABELS/LABEL PLACEMENT AND PHOTOGRAPHS

4.3 Rear Panel Drawing (Label Placement):



4.0 IDENTIFICATION LABELS/LABEL PLACEMENT AND PHOTOGRAPHS

4.4 Photograph List

Note: The following photos can also be found in the external photos attachment:

4.4.1 Front view, Complete 5721 Transmitter (Closed Front Panel).

4.4.2 Front view, Upconverter/Amplifier Tray (Open Front Panel).

4.4.3 Rear view, Complete 5721 Transmitter.

Note: The following photos can also be found in the internal photos attachment:

4.4.4 Top view, IF Processing Module.

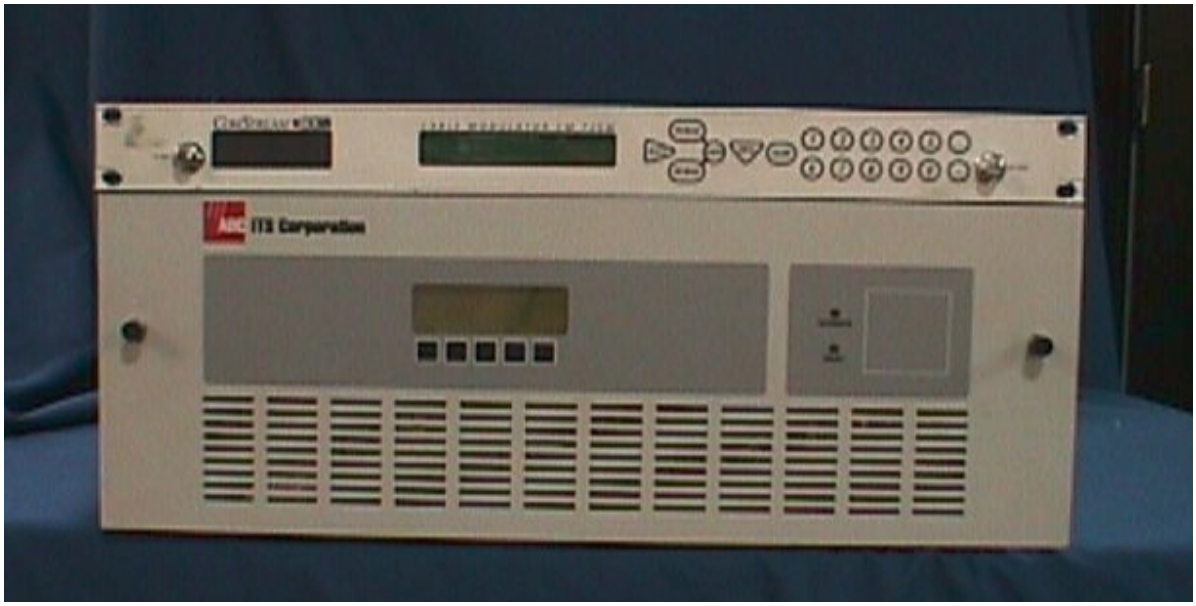
4.4.5 Top view, Local Oscillator/Upconverter Module.

4.4.6 Top view, Power Supply Module.

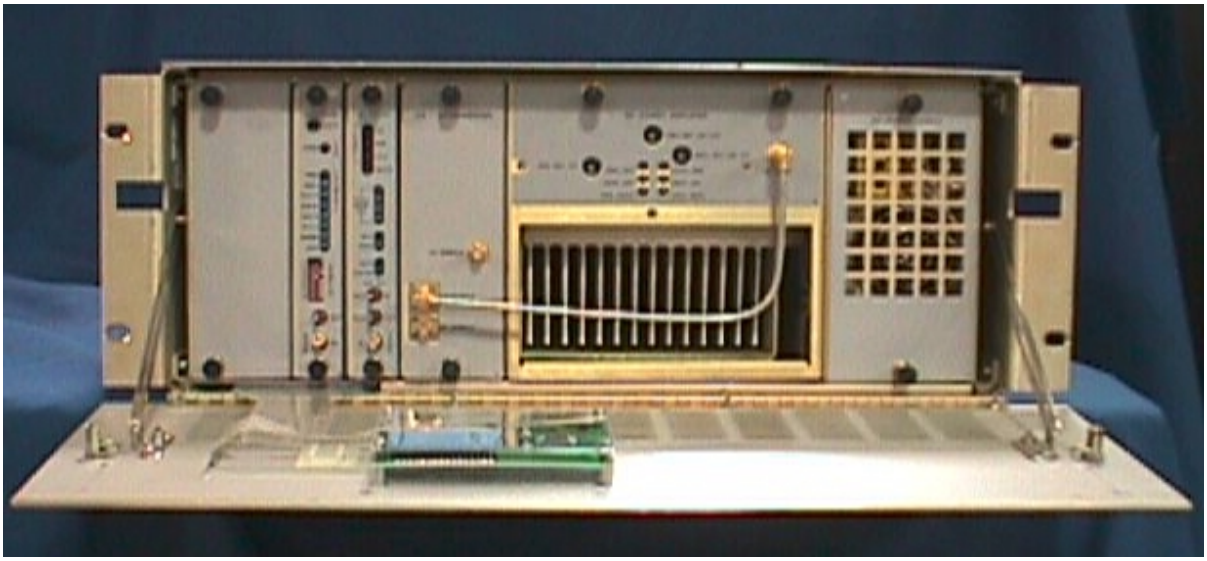
4.4.7 Top view, Transmitter Control and Monitoring Module.

4.4.8 Top view, Power Amplifier Module.

4.4.1 Front view, Complete 5721 Transmitter (Closed Front Panel)

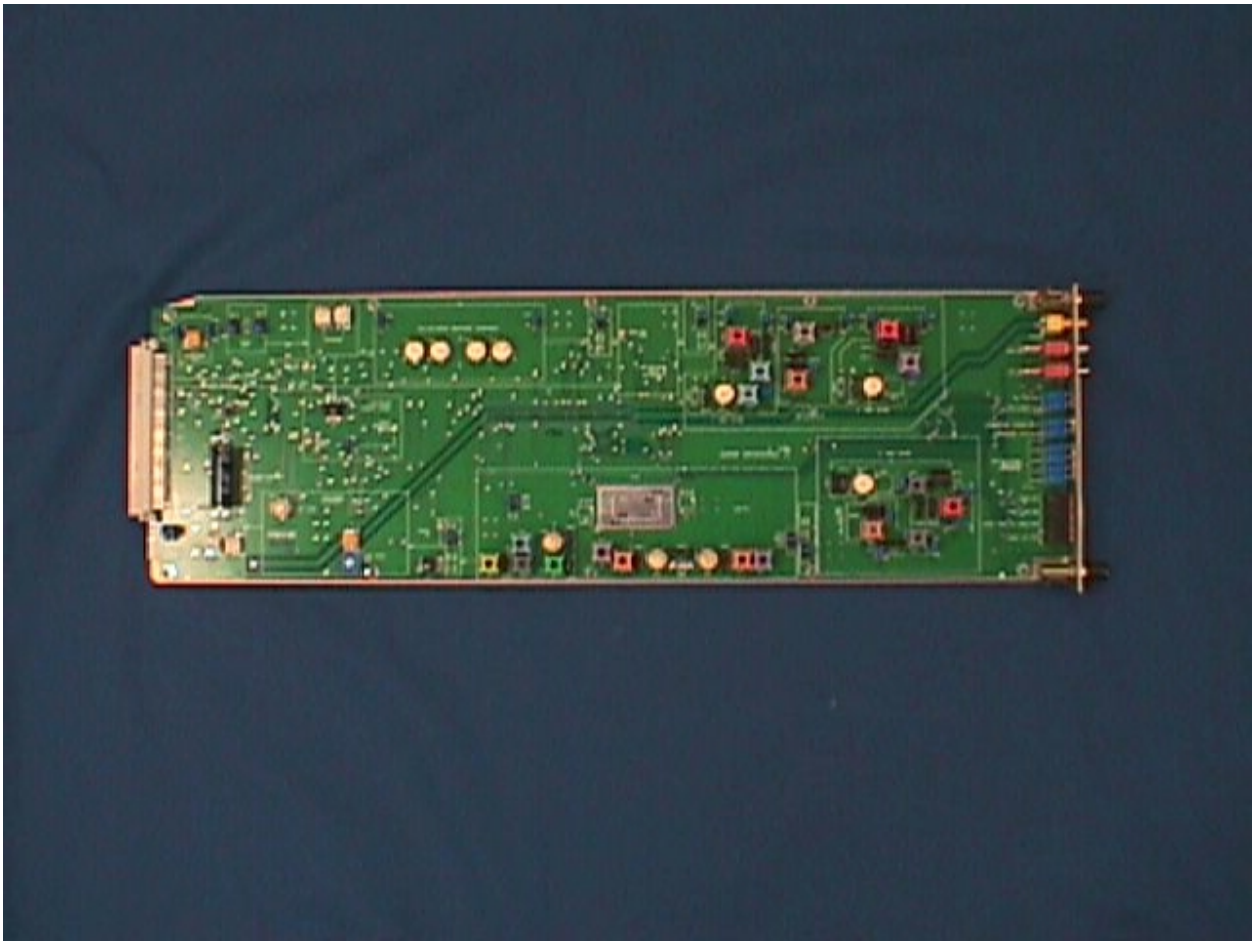


4.4.2 Front view, Upconverter Amplifier Tray (Open Front Panel)

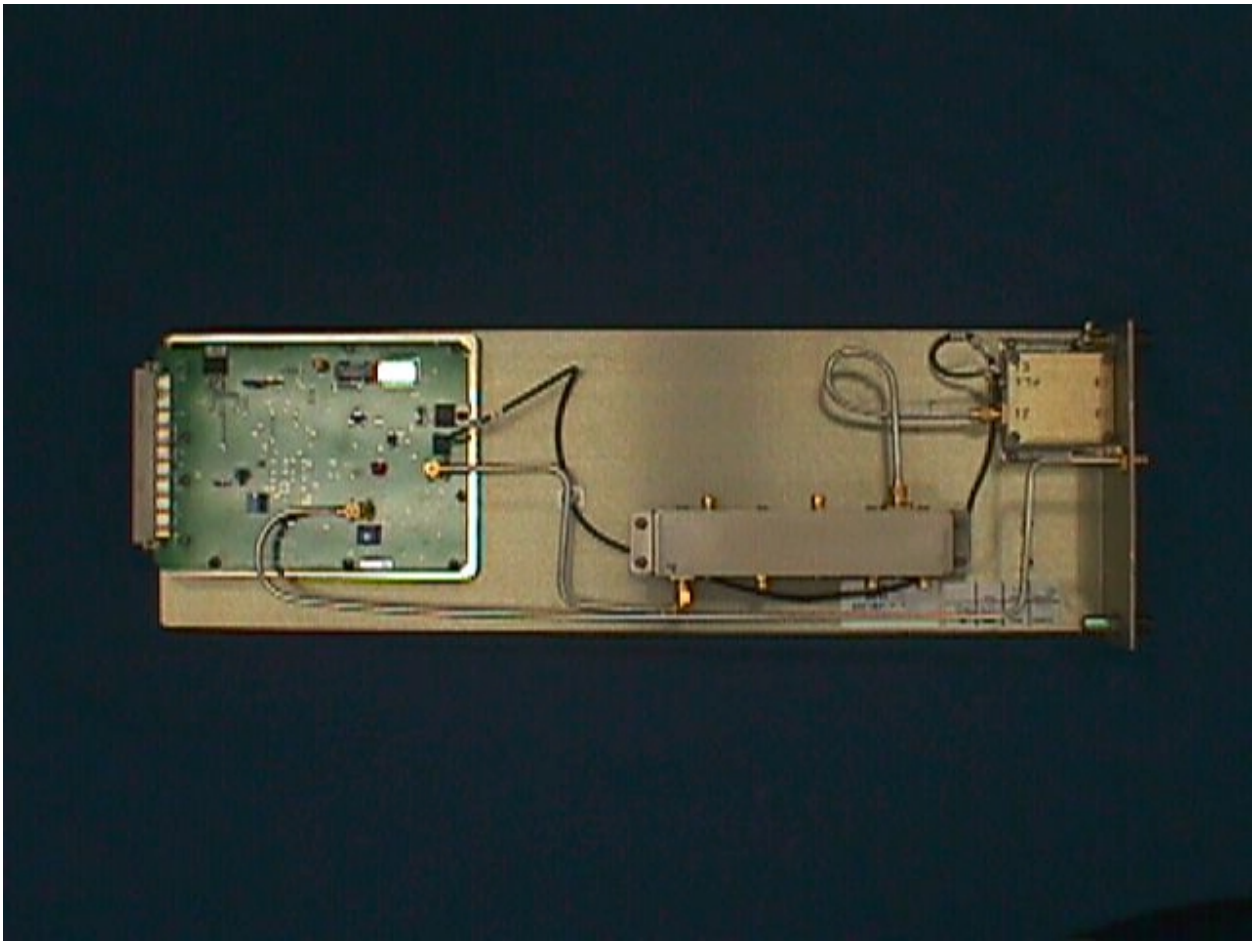


4.4.3 Rear view, Complete 5721 Transmitter

4.4.4 Top view, 5721, IF Processing Module

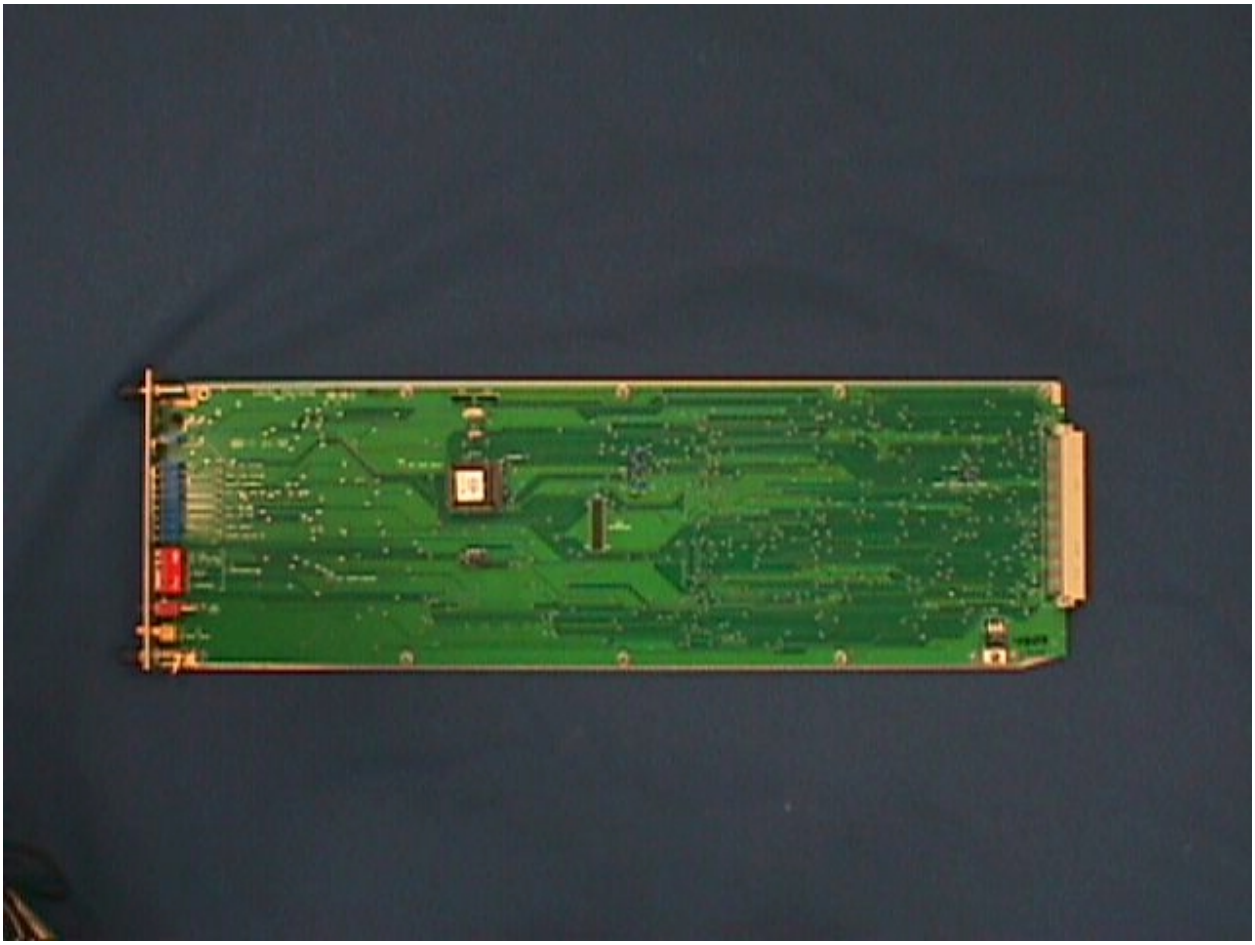


4.4.5 Top view, 5721, Local Oscillator/Upconverter Module

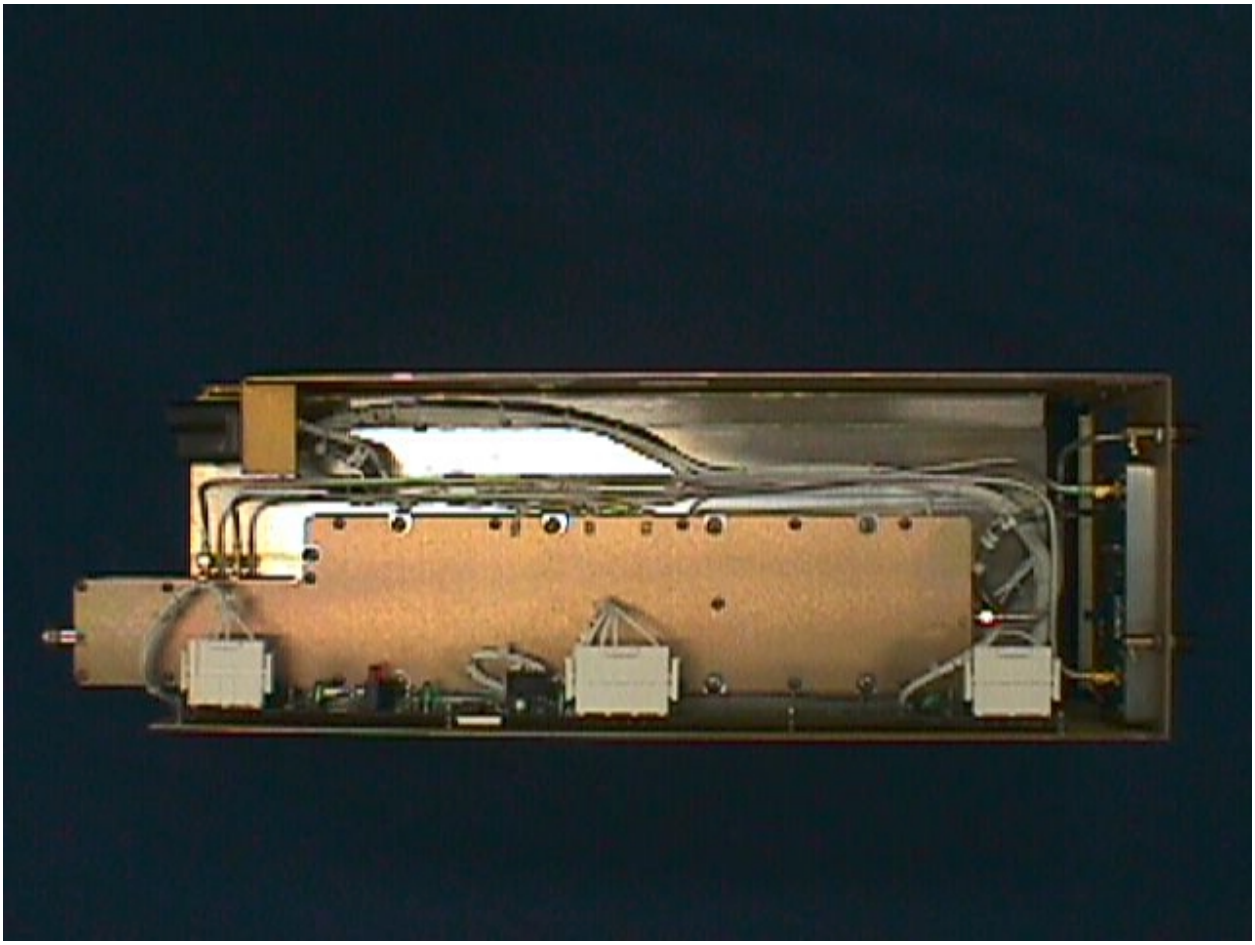


4.4.6 Top view, 5721, Power Supply Module

4.4.7 Top view, 5721, Transmitter Control and Monitoring Module



4.4.8 Top view, 5721, Power Amplifier Module



5.0 CERTIFICATION OF TEST DATA

This equipment has been tested in accordance with the requirements contained in the appropriate Commission regulation. To the best of my knowledge, these tests were performed using measurement procedures consistent with industry or Commission standards and demonstrate that the equipment complies with the appropriate standards. Each unit manufactured, imported or marketed, as defined in the Commission's regulations, will conform to the sample(s) tested within the variations that can be expected due to quantity production and testing on a statistical basis. I further certify that the necessary measurements were made by ADC Telecommunications, 102 Road, McMurray, Pennsylvania 15317.

Dave Urban, Chief Engineer

Todd Anderson, Engineer