

1.0 IDENTIFICATION OF APPLICANT AND EQUIPMENT

1.1 Applicant:

Information Transmission Systems Corp.
375 Valley Brook Road
McMurray, PA 15317

The above name and address is printed on a label attached to the rear panel of the equipment.

1.2 Equipment and Model Number: ITS-5726

This information is provided on the front panel of the equipment.

1.3 ITS Corporation shall manufacture this product in quantities necessary to satisfy market demand.

2.0 TECHNICAL DESCRIPTION - MODEL ITS-5726

2.1 Introduction

The ITS-5726 is a complete digital transmitter capable of operating as television transmitter at an output power of 50 watts (average). Functionally, the ITS-5726 is comprised of a QAM modulator tray, upconverter/amplifier tray, amplifier tray and external 10 pole channel filter.

The modulator receives a 28 Mbit/sec serial bit stream, consisting of multiplexed MPEG-2 transport streams, translates the signal to a Quadrature Amplitude Modulated (QAM) format, converts the digital information to analog, and modulates the signal to IF (44 MHz). The 64 QAM IF signal from the modulator is applied to a SAW filter at the input of the upconverter/amplifier which provides spectral shaping of the 64 QAM IF signal thus providing performance repeatability between various 64 QAM modulators. The upconverter/amplifier tray then performs IF signal processing, upconversion to the one of four 6 MHz channels in the Wireless Communication Service (WCS) frequency band (2305 - 2320 MHz and 2345 - 2360 MHz), and amplification. The upconverter/amplifier tray utilizes ALC circuitry for automatic level control of the output signal to maintain a constant power level. The output signal from the upconverter tray then drives the external amplifier tray which amplifies the signal to the rated output power of the unit. The output of the amplifier is filtered using a Coleman Microwave 407625 10 pole WCS bandpass channel filter in accordance with the emission limits specified in Part 27 of the Rules and Regulations.

All three trays are 19-inch rack mount assemblies and can be supplied with or without a cabinet. The trays are supplied complete with cables and cabinet slides.

Parameters and specifications for operation of this unit as a digital transmitter are provided on the following pages, and a complete circuit description and alignment procedure are also included in this report. Refer to the overall system block diagram and the particular referenced schematics in the attached circuit description section of this report.

2.0 TECHNICAL DESCRIPTION

2.2 Technical Specifications

Type of Emissions	6M00D7W
Frequency Range	2305 to 2320 and 2345 to 2360 MHz (four 6 MHz channels)
Output Power Rating	50 watts average
DC voltage and total current of final amplifier stage.....	10 volts DC at 65 amps (Class A - Not RF power dependent)

2.3 Performance Specifications

Operating Frequency Range 2305 to 2320 and 2345 to 2360 MHz

RF output - Nominal:

Power.....	25 -50 watts average (adjustable in driver)
Impedance	50 ohms
Connector.....	Type N

Input (Modulator) QAM, MPEG-2 Transport Stream

Impedance: 75Ω (BNC)

Out-of-Band Power:

2320-2345 MHz 80 + 10 Log(50W) = 97dB max

below 2300 and above 2370 MHz 70 + 10 Log(50W) = 87dB max

2300-2320 MHz and 2345-2370 MHz 43 + 10 Log(50W) = 60dB max

Electrical Requirements

Power Line Voltage:

Modulator.....	90 to 132 VAC, 47 to 63 Hz
Upconverter	117/220 VAC ±10%, 50 or 60 Hz
Amplifier	208/240 VAC ±10%, 50 or 60 Hz

Power Consumption:

Modulator.....	55 watts
Upconverter	380 watts
Amplifier	1243 watts

Environmental

Maximum Altitude:

Modulator.....	10,000 feet (3,050m)
Upconverter	12,000 feet (3,660m)
Amplifier	12,000 feet (3,660m)

Ambient Temperature

Modulator.....	+5° to +45°C
Upconverter	0° to +50°C
Amplifier	0° to +50°C

2.0 TECHNICAL DESCRIPTION

2.3 Performance Specifications - continued

Mechanical

Dimensions: (WxDxH)

Modulator.....	16.9" x 17.7" x 1.73" (43.0cm x 45.0cm x 4.4cm)
Upconverter	19" x 21" x 8.75" (48.3cm x 53.3cm x 22.24cm)
Amplifier	19" x 30" x 10.25" (48.3cm x 76.2cm x 26.0cm)

Weight:

Modulator.....	11 lbs. (5.0 kgs)
Upconverter	47 lbs. (21.3 kgs)
Amplifier	125 lbs. (56.7 kgs)

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description

The ITS-5726 WCS Transmitter can be subdivided further as follows:

Modulator	- Reception Digital Interface Card - QAM Modulator Card - Supervision and Management Card - Power supply Unit
Upconverter/Amplifier	- IF Processing Module - Power Amplifier Module - Power Supply Module - Control Monitoring Module - L.O./Upconverter Module - Backplane Board - Front Panel LCD Display - Keyboard Entry Board - LCD Display
Amplifier	- RF Input - RF Output - Amplifier Modules - Bias Circuits - Feed Forward Correction - Control Logic - Switching Power Supplies - DC to DC Converter - Peak Detector - Splitters - Combiner - Couplers

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description

Modulator Tray

The modulator tray generates a 64 QAM digital IF output which is used to drive the upconverter/amplifier tray. It also provides processing of the MPEG2 bit stream received from program encoding and multiplexing equipment.

The consist of a Reception Digital Interface Card, DVB-QAM Encoder Card, QAM Modulator Card, Supervision and Management Card, and Power Supply Unit.

The Reception Digital Interface Card provides connection provides connection of the unit to encoding equipment through a proprietary RS422 (M2P) parallel interface or to multiplexing equipment through a DIVICOM Rx Int interface.

The DVB Encoder Card provides channel encoding of the bit streams and associated clock signals transmitted by the Reception Digital Interface Card. Bit streams are encoded in compliance with DVB recommendations for transmission to the QAM modulator function. The DVB QAM Encoder functions include: energy dispersal (scrambling), Reed/Solomon forward error detection, interleaving, differential inner encoding, QAM symbol mapping.

The QAM Modulator Card provides square-root Nyquist filtering in compliance with DVB recommendations, and amplitude modulation of two carriers in phase quadrature (QAM).

The Supervision and Management Card supervises the unit through processing of fault indications supplied by the various cards of the unit. The corresponding major and minor alarms are transmitted through relay contacts.

Local configuration access to the modulator cards is available via the front panel keypad/display or using a PC connected to the RS-232 interface. Remote configuration access is provided through a Ethernet (LAN) interface. Test functions activated via the operating software options allow Unit and link supervision.

The front panel contains a Keypad/LCD display, two LED fault indicators, and two LED status indicators (Test and On). Also included on the front panel are IF, clock (Clk), baseband I signal, and baseband Q signal output test ports (refer to *Chapter 4: Operation* of the Installation and Operation Manual, included in Exhibit III of this report, for a complete description of front panel operation).

The modulator power supply produces tertiary voltages used to operate the various cards of the unit from a standard 115VAC and 47 to 63 Hz supply.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Upconverter/Amplifier Tray

IF Processing Module

The input to the Upconverter/Amplifier tray is the IF output from the modulator tray. The 64 QAM IF output signal from the modulator is applied to the IF input jack (J1) on the rear of the tray. This IF input signal is then fed to the IF Processing Card (1585-3108).

The IF signal enters the card at J1 and is transformer coupled for impedance matching of the IF signal (75Ω to 50Ω). The signal is then applied to an adjustable resistor pad network which allows for three IF input level ranges of 10 dB each. The signal is amplified and applied to a 6 dB transformer directional coupler which provides a sample to a peak detector in the ALC portion of the circuit. The main output of the coupler is fed to frequency response correction circuitry which consist of four adjustable notch filters. The frequency response correction circuit may be removed using on board jumpers. The output of the frequency response corrector is amplified and applied to a PIN diode attenuator. The ALC circuitry takes a peak detected sample of the IF signal and generates an ALC voltage which biases the PIN diode attenuator. The ALC circuit senses any change in the IF level and automatically adjust the loss through the PIN attenuator to compensate, thereby maintaining a constant IF output regardless of minor changes in the input signal. The ALC circuit uses a DC level generated externally to control the output power level. There are two possible bias voltage inputs. The first, Inner Loop, is generated form a peak detected sample of the output amplifier. The second, Outer Loop, is used only if an external final amplifier tray is connected to the system. If both Inner Loop and Outer Loop inputs are used, the signal that is the largest in level controls the ALC circuit.

The ALC circuit may be bypassed by placing switch SW2 in the manual position. When the ALC circuit is disabled, the loss through the PIN attenuator is adjusted by a manual gain potentiometer which then directly controls the output in a manual fashion.

The ALC circuit also contains a average detector which detects the average level of the IF signal. This average level is compared to the output of the peak detector and if the average level approaches the peak level, indicating a loss of modulation on the IF signal, a mute signal will be generated muting the IF. This prevents against overpower conditions in situations where the modulating signal is interrupted. The ALC circuit provides several front panel LED indicators including: Peak Vs. Average Fault, I/P Fault, Mute, and ALC Fault.

The output of the PIN diode attenuator is amplified and applied to three sections of group delay equalization which compensate for group delay created by external filters. Each section of group delay may be removed from the circuit using on board jumpers. For non-adjacent analog applications, Delay Equalizer 1 is removed from the circuit. For adjacent analog applications, all three sections are used. For adjacent and non-adjacent digital applications, Delay Equalizer 3 is removed from the circuit. The output of the delay equalizer circuit is fed to a 6 MHz lumped element bandpass filter. The bandpass filter may be removed from the circuit using on board jumpers. The bandpass filter may also be bypassed through a SAW filter when tight filtering of the IF is required.

The output of the bandpass filter is applied to a linearity correction circuit which compensates for compression in later stages of the system. The output of the linearity correction circuit is fed to a 6 dB transformer directional coupler which provides a front panel sample of the IF signal. The main output of the coupler is connected to the output of the IF Processing Card (J1B).

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Frequency Generator/Upconversion/PLL Module

The Frequency Generator/Upconversion/PLL Module consist of a L.O./Upconverter Board (1585-3117), Interdigital Filter (2140-1006), and a Single stage Amplifier Board (1585-3101).

The L.O./Upconverter Board generates a UHF L.O. frequency using a voltage controlled oscillator (VCO) IC (V804ME01). The VCO is locked to an external precise 10 MHz reference using a frequency synthesizer PLL IC (LMX2325TM) in a phase lock loop configuration. The LMX2325TM is a high performance frequency synthesizer with integrated prescalers and uses a proprietary digital phase lock loop technique to produce a very stable low noise signal that is used to control the VCO frequency. The desired L.O. frequency is selected using the front panel LCD display/keypad. The Control Monitoring Assembly detects the keyboard input and rounts the serial data to the serial data input of the PLL IC.

Under normal operating conditions, the external 10 MHz precise reference input will be routed to the oscillator input of the PLL IC through a magnetic latching relay (K1). If the external precise reference is removed the relay will open and an internal 10 MHz reference oscillator IC will be routed to the oscillator input of the PLL IC.

The L.O. signal from the VCO is buffered to an internal microstrip coupler which provides an L.O. sample that is routed to a rear panel jack. The L.O. signal is then amplified by an IC amplifier (U8) to a sufficient level to drive the L.O. input of an IC mixer(U10). An IF input to the mixer is provided via the IF Processing Assembly. The output of the mixer is amplified by an IC amplifier (U12) and fed to the RF output jack of the board (J8).

The RF signal is then fed to a 6 MHz bandpass interdigital filter (2140-1006) which selects the desired conversion frequency (L.O. - IF) and attenuates any undesired signals generated during the mixing process.

The RF output of the filter is then fed to the Single Stage Amplifier Board (1585-3101) which consist of a single IC amplifier (VNA-25) with a gain of 14 dB. An RF sample is obtained using a microstrip coupler (J2). The main RF output is connected to the output jack of the module (J8).

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Power Amplifier Module

The Power Amplifier Module consist of an 40W PEP Amplifier Module (1585-3196), 3 Section Bias Board (1585-3250), and Dual Power Detector Board (1585-3125).

The 40 W PEP Amplifier module is subdivided into two functional sections: preamplifier section, and power amplifier section.

The RF input signal from the Frequency Generator/Upconversion/PLL Module enters the module at J1 and is fed to the preamplifier section. The preamplifier consist of four cascaded GaAs FET amplifiers (FLL 101ME driving a FLL 351ME driving a FLL351ME driving a FLL 120MK) with an overall gain of approximately 45 dB. The output of the final FET is applied to a 3.0 dB microstrip hybrid coupler which splits the signal into two equal signals. The split signal is then fed to the power amplifier section of the module.

The power amplifier consist of two parallel GaAS FET amplifiers (both S45V2527-51's) with an overall gain of approximately 12 dB. The output signals of the parallel amplifiers are applied to a microstrip hybrid coupler which combines the two signals. The output of the coupler is applied to a circulator, which provides an RF sample, then to the output of the module (J8). A 20 dB forward power sample is obtained using an internal microstrip coupler.

The DC biasing of the FET amplifiers in each section of the module is controlled and filtered by corresponding daughter boards (daughter boards D1, D2 and D3 for the preamplifier, daughter boards D4, D5, and D6 for the power amplifier) which are soldered directly to the main board. The DC bias drain to source currents are set by adjusting the negative gate to source voltages which are adjusted by potentiometers on the daughter boards.

The 3 Section Bias Protection Board distributes the -5V bias voltages and +10V drain voltages to the Amplifier Module as well as providing protection from an over current condition with board mounted fuses.

The -5V bias voltage is generated on board using a voltage regulator (LM377T). This bias voltage is also used as an interlock which is fed to the Transmitter Control and Monitoring Module. If the bias voltage is lost, the control circuitry will immediately shut down the switching supply, thereby removing the drain voltages from the amplifier modules and protecting the GaAS FET devices.

Differential amplifier OP Amp circuits are used to monitor the drain currents of the FET devices. The OP Amp outputs drive LED indicators as well as an opto-isolated O/P amplifier status line.

The Dual Power Detector Board inputs forward and reflective power signals from the Amplifier Module and detects the levels using peak detector circuits. These circuits provide voltage levels proportional to the power level of the sampled signal which are used for metering and ALC purposes. Metering adjustment is provided with on board potentiometers.

The Dual Power Detector Board also contains a gating pulse timing circuit that serves to maintain the proper power level when sync suppression scrambling systems are used.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Transmitter Control Monitoring and Module

The Transmitter Control and Monitoring Module (1585-1129) consist of an 8-bit microcontroller (MC68HC705B`6) and associated control circuitry and provides the capability to control and monitor the operating status of the transmitter. The interconnection between the Transmitter Control and Monitoring Module, IF Processing Module, and Local Oscillator/Upconverter Module is accomplished through the Backplane Board. The interconnection between the Transmitter Control and Monitoring Module, Power Supply Module, and Power Amplifier Module is accomplished through interconnect cables. A detailed listing of all the interfaces between the Transmitter Control and Monitoring Module and the various modules which make up the ITS-5722 transmitter is given below.

Power Amplifier Module

<u>Signal Name</u>	<u>Signal Type/Description</u>
Amplifier Interlock	Discrete contact closure input - indicates Power Amplifier Module is installed.
Reflective Pwr Metering	Analog input (0 - 1.25V) - indicates reflective power from Power Amplifier Module.
Overtemp Fault	Discrete contact closure input - indicates overtemp condition exist in Power Amplifier Module.
O/P Amplifier Status	Discrete open collector input - indicates operating status of output amplifier.
-5V Bias Sense	Analog input (0 - 6V) - indicates the voltage level of the - 5V bias supply.

Local Oscillator/Upconverter Module

<u>Signal Name</u>	<u>Signal Type/Description</u>
External Reference Indicator	Discrete open collector input - indicates the presence of external 10 MHz reference.
Logic Enable	Discrete CMOS output - provides a load enable signal to the frequency synthesizer chip.
Data	Discrete CMOS output - provides serial data to the frequency synthesizer chip.
Clock	Discrete CMOS output - provides the serial clock to the frequency synthesizer chip.
AFC	Analog input (1 - 10V) - indicates the level of the AFC voltage.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

<u>Signal Name</u>	<u>Signal Type/Description</u>
L.O./Upconverter Interlock	Discrete contact closure input - indicates L.O./Upconverter Module is installed.
Unlock Indicator	Discrete open collector input - indicates the L.O./Upconverter Module is locked to the external or internal 10 MHz reference.

IF Processing Module

<u>Signal Name</u>	<u>Signal Type/Description</u>
Open Loop Monitor	Analog input (1 - 1.25V) - indicates output power of an external amplifier.
Forward Power Metering	Analog input (0 - 1.25 V) - indicates output power tray's power amplifier.
IF Processor Interlock	Discrete Contact Closure Input - indicates that IF Processing module is installed.
ALC Voltage	Analog input (0 - 10V) - indicates voltage applied to pin attenuator in ALC circuit.
Mute to IF Processor	Discrete open collector output - controls mute feature in the IF processor.
Mute from IF Processor	Discrete open collector input - indicates IF processor is in mute.
Input Fault	Discrete open collector input - indicates that IF is not present.
ALC Conditioning	Analog Input (-1 - +1V) - Provides adjustment voltage to the ALC circuitry to correct for frequency dependence of peak detector.

Power Supply Module

<u>Signal Name</u>	<u>Signal Type/Description</u>
P.S Good	Discrete open collector input - indicates switching power supply is operating properly.
P.S Enable	Discrete open collector output - enable signal to switching power supply.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Front Panel Assembly

<u>Signal Name</u>	<u>Signal Type/Description</u>
Fault Anode	Fault LED drive voltage (+ 5V) - supply to anode of Fault LED.
Fault Cathode	Discrete open collector output - provides pull down to turn on Fault LED.
Operate Anode	Fault LED drive voltage (+ 5V) - supply to anode of Operate LED.
Operate Cathode	Discrete open collector output - provides pull down to turn on Operate LED.
S1-S5	Discrete contact closure inputs - input lines from front panel keyboard switches.
VSS (GND)	Ground - Provides return to front panel board.
VCC	+ 5VDC - provides + 5V to front panel display logic.
VEE	Control voltage output (0 - 5V) - controls contrast of LCD display.
RS	Discrete TTL/HCMOS output - indicates to display whether instruction or data command is being sent.
E	Discrete TTL/HCMOS output - initiates the transfer of data to the display.
DB0-DB7	Discrete TTL/HCMOS bidirectional data lines - data lines which pass data between the display and transmitter control and monitoring module.
Anode Backlight	Control voltage output (3.8 - 4.6 V) - provides drive voltage to LCD backlight of display.
Cathode Backlight	Control voltage return - return for control voltage of LCD display.

SCADA Communications Interface

<u>Signal Name</u>	<u>Signal Type/Description</u>
+ Serial Line	+ RS-485 communications line - provides the +differential line for the +bidirectional line of the bidirectional RS-485 communications..
- Serial Line	-RS-485 communications line - provides the -differential line for the +bidirectional line of the bidirectional RS-485 communications..

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Control and Remote Interface

<u>Signal Name</u>	<u>Signal Type/Description</u>
Standby Command (FA)	Discrete open collector input - indicates frequency agile is requesting transmitter be placed into standby mode.
Operate Command (FA)	Discrete open collector input - indicates frequency agile is requesting transmitter be placed into operate mode.
Aural/Visual Mute (FA)	discrete open collector input - indicates that frequency agile is presently in aural/visual mute.
ABS Standby CMD	Discrete open collector input - indicates that Automatic Back-up System is requesting transmitter be placed into standby.
EXT Operate CMD	Discrete open collector output - enables external amplifier when transmitter enters operate mode.
XMTR Interlock Iso Return	Ground - configurable ground return which can be either jumpered directly to ground or be the "source" pin of an FET so that transmitter interlock can be daisy chained with other transmitters.
XMTR Interlock	Discrete open collector output - enables transmitter interlock or complete interlock daisy chain.
EXT O/P Amp Mod Status	Discrete open collector input - indicates external amplifier has a fault.
EXT P.S. Status (amp)	Discrete open collector input - indicates power supply in external amplifier is functional.
Operate Indication	Discrete open collector output - indicates transmitter is in operate mode.
EXT Overtemp (amp)	Discrete open collector input - indicates external amplifier has overtemp condition.
EXT Refl Pwr (amp)	Analog input (0 - 1.25V) - indicates reflected power of external amplifier.
Standby CMD (RCVR)	Discrete open collector input - indicates external receiver is requesting transmitter be placed into standby.
Operate Command	Discrete open collector input - indicates external receiver is requesting transmitter be placed into operate.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Control and Remote Interface	
<u>Signal Name</u>	<u>Signal Type/Description</u>
RMT Operate Indicator	Discrete open collector output - indicates transmitter is in operate mode.
O/P Amp Module Status	Discrete open collector output - indicates no faults present in amplifier modules of transmitter.
RMT FWD Power O/P	Analog output (0 - 1.25V) - power amplifier module forward power loop through.
RMT REFL Power	Analog output (0 - 1.25V) - power amplifier module reflective power loop through.
RMT XMTR Fault Ind	Discrete open collector output - indicates fault exist in transmitter.
IF Present Status O/P	Discrete open collector output - indicates IF is not present.
RMT PLL Locked Ind	Discrete open collector output - indicates frequency generator/upconverter is unlocked.
RMT XMTR Overtemp Ind	Discrete open collector output - indicates transmitter amplifier module is in overtemp.
P.S. Fault Ind	Discrete open collector output - indicates that power supply of transmitter has failed.
EXT PLL Ref Present	Discrete open collector output - indicates external 10 MHz reference is not present.
RMT XMTR Stby Command	Discrete open collector input - indicates remote interface is requesting transmitter be placed in standby.
RMT XMTR Oper Command	Discrete open collector input - indicates remote interface is requesting transmitter be placed in operate.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Power Supply Module

The transmitter may be powered by either a 115 VAC/60 Hz or 230 VAC/50 Hz source. The AC source enters the tray at jack J1 and passes through the Power Entry Module. The Power Entry Module contains a switch, for selecting 115V or 230 V input, a line filter and fuse protection. The output of the Power Entry Module is distributed to a terminal block (TB1). Varistors VR1, VR2, VR3 and VR4 provide transient and over voltage protection to the transmitter. The rear panel circuit breaker applies AC voltage to the input of the 530 W Switching Power Supply (MP6-2K-411-00-415-CE) located on the Power Supply Module.

The Switching Supply provides three outputs. The first output is a +11 VDC/31A line used to power the GaAs FET amplifiers with power. The remaining outputs are +12 VDC lines used to supply the modules within the transmitter. The +12 VDC line is also used to power the 12 VDC cooling fan via the Backplane Board.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Amplifier Tray

The RF input signal from the driver transmitter enters the external amplifier tray at J1 and is fed to the input of a Two Way Splitter (2111-1008) which splits the signal into four equal signals that are fed the inputs of two 25W Power Amplifier Assemblies (1586-3117). The amplifier modules are identical in design and function and therefore only one need be described..

The 25W Power Amplifier Assembly consist of an Amplifier Module (1586-3104), 8 Section Bias Board (1586-3109), and DC to DC Converter (ITS-DC380-11).

The amplifier assembly provides both amplification and Feed Forward distortion cancellation. This module is subdivided into 5 functional sections: power amplifier section, feed forward correction signal section, correction signal preamplifier section, correction signal main amplifier section, and feed forward cancellation/RF output section.

The RF input signal from the Two Way Splitter Module enters the power amplifier section of the amplifier assembly at J2 and is phase and amplitude adjusted using a microstrip delay line and resistor pad network. The signal is then applied to a 3 dB Branch Line Coupler which provides a sample of the input signal to the feed forward correction signal section later in the signal path. The main output signal from the coupler is fed to the power amplifier which consist of five GaAs FET amplifiers (MGFS45V2527-1 driving four parallel MGFS45V2527-1's) with an overall gain of approximately 24 dB. A 20 dB microstrip coupler provides and uncorrected (distorted) sample of the power amplifier output signal. This sample is used in the feed forward correction signal section of the module which generates the correction signal that will be amplified and coupled with the RF output signal to cancel the distortion created in the power amplifier.

The input signal (undistorted) sample is phase shifted 180° through a delay line and fed to the feed forward correction signal section of the assembly where it is phase and amplitude adjusted and coupled with the uncorrected signal from the output amplifier. Combining these two signals (the phase shifted (180°) input signal, and the distorted power amplifier output signal) cancels the information carrying component of the signal, leaving only the distortion of the output amplifier.

This correction signal is fed to the correction signal preamplifier section of the module which consist of two cascaded GaAs FET amplifiers (FL1100 driving a FLL200) with an overall gain of approximately 24 dB. The signal is then fed to the feed forward correction signal main amplifier where it is amplified to a sufficient level to cancel the distortion created by the power amplifier. The correction signal main amplifier consist of two parallel GaAs FET amplifiers (both MGFS45V2527-1) with an overall gain of approximately 12 dB.

The amplified correction signal and the phase shifted (180°) output of the power amplifier are applied to a hybrid microstrip coupler in the feed forward distortion cancellation/RF output section of the module where the signals are coupled together using a 6.5 dB Branchline Coupler, effectively canceling the distortion in the output signal. The main output signal connects to the output of the amplifier assembly at J8.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

The DC biasing of the FET amplifiers in each section of the module is controlled and filtered by corresponding daughter boards which are soldered directly to the main board. The DC bias drain to source currents are set by adjusting the negative gate to source voltages which are adjusted by potentiometers on the daughter boards.

The 8 Section Bias Board distributes the -5V bias voltages and +10.4V drain voltages to the Amplifier Module as well as providing protection from an over current condition with board mounted fuses.

The -5V bias voltage is generated on board using a voltage regulator (LM377T). This bias voltage is also used as an interlock which is fed to the Power Detector/Control Board (1586-1118). If the bias voltage is lost, the control circuitry on the Power Detector/Control Board will immediately shut down the switching supply, thereby removing the drain voltages from the amplifier modules and protecting the GaAs FET devices.

Differential amplifier OP Amp circuits are used to monitor the drain currents of the FET devices. The OP Amp outputs drive LED indicators as well as an opto-isolated O/P amplifier status line.

The DC to DC converter inputs +390VDC from the Power Factor Corrected Front End Module (1586-1111) and generates two 10.8 VDC outputs using three DC to DC converter IC's (VI-B61-EU). An Enable signal from the driver transmitter is used to activate the DC to DC converter.

The output signals from the two 25 W Power Amplifier assemblies are combined into a single output signal using a 2-Way Combiner (2111-1008) module. A Reject Load Module (1586-1106) is used to absorb any reflected power. The combined signal is applied to a directional coupler (A13) which provides forward and reflective power samples to the Power Detector/Control Board.

Control

The Power Detector/Control Board (1586-1118) provides the dual function of forward/reflective power detection and operating status control and monitoring capability. The board is designed to protect the amplifier in the event of one of the following faults: over temperature, loss or reduction in output power, and loss of the -5 VDC GaAs FET bias voltage. The Power Detector/Control Board also provides the capability to remotely control and monitor the amplifier status through external remote connections at J3 (25 pin D) on the rear of the tray.

Power Supplies

The amplifier is powered through a standard 220 VAC 60 Hz source. The AC source enters the tray at jack J1, passes through a fuse protected circuit breaker, and is distributed to the Power Factor Corrected (PFC) Front End Module.

The AC source is applied to a terminal block (TB2) within the PFC Front End Module and distributed to a 40 W switching power supply (LPS23), a 80 W switching power supply (LPS63) and a AC/DC Power Factor Corrected 2000W supply.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

The 40 W switching supply supplies +12 V to the other boards within the tray. The 80 W switching supply supplies -12 V to the other boards within the tray. The 200W AC/DC supply supplies +390 VDC to the DC to DC Converters within the 25W Amplifier Modules.

2.0 TECHNICAL DESCRIPTION

2.5 Alignment Procedure

In the following procedure, the complete transmitter is adjusted for optimum performance, beginning with the start up procedure of the PQM 2100 modulator, followed by the upconverter/amplifier and amplifier trays, starting at the IF input and adjusting each circuit for its specified performance while observing the appropriate output parameters of the board or subassembly being adjusted.

Because of the broadband nature of most of the amplifier stages, this is a straightforward procedure, easily accomplished if baseband, IF, and RF test equipment is available. In this procedure, the input signals are first connected and each circuit is adjusted in sequence by connecting the test equipment to the specified point.

Adjust the spectrum analyzer for the following settings:

1. Resolution Bandwidth = 30 KHz
2. Video Averaging (On) = 10
3. Span = 20 MHz
4. Video Bandwidth = 30 KHz
5. Center frequency = 44 MHz

The average power of a modulated QAM digital signal, with the specified analyzer settings, is +23 dB higher than the displayed signal. The measurements in this alignment procedure will be given in average levels.

Example: Analyzer reading of -30 dBm.
Average Power = -30 dBm + 23 dBm = - 7 dBm.

Modulator Tray

Follow the steps listed below to bring the PQM2100 modulator online (refer to Chapter 4: *Operation* of the PQM2100 Technical Manual included as Exhibit III of this report for a complete description of the Keypad /LCD user interface).

1. Turn on the tray by connecting the AC power cable the unit and placing the rocker switch on the back panel to the on position and observing the front panel LEDs. When power-up is complete, the LCD display will illuminate, the Fault LEDs will remain off, and the On LED will illuminate.
2. Press any key to enter the Passwor Entry screen.
3. If no password has been assigned, access the main menu by pressing Enter then enter the desired password using the Password Modification menu..
4. If Password exist, enter the current password and confirm by pressing Enter to bring up the Alarm Mode sub menu.
5. Press → to access the Alarm Mode selection screen.

2.0 TECHNICAL DESCRIPTION

2.5 Alignment Procedure - continued

6. Using the up and down arrows select the alarm mode (Normal: alarm relay contact opening in event of alarm, or Default: alarm relay contact closure in event of alarm).
7. Press Enter to proceed to the Active Alarms Display menu
8. Using the up and down arrow keys, check that no alarms are present.
9. Return to the Alarm Mode menu by pressing the \leftarrow key and select the Parameters sub menu using the up and down arrow keys..
11. Press \rightarrow to enter the Parameters submenu.
10. Press the \rightarrow key to access the Bit Rate screen.
11. Using the arrow keys enter a Bit Rate of 3038297 kbit/s then press enter to save. After the Bit Rate has been entered, the modulation level (64 QAM) and Symbol Rate (5063 Kbaud) are automatically set.

At this point the PQM2100 modulator has been powered up and the output spectrum may be observed.

2.0 TECHNICAL DESCRIPTION

2.5 Alignment Procedure - continued

Upconverter/Amplifier Tray

Using a spectrum analyzer verify the proper level (-11 to -6 dBm average) and frequency of the spectrum at the IF output port of the Modulator.

Verify proper configuration of ITS-5722 modules as follows:

Control Monitoring Module (A4) 1585-1129

Set front panel configuration DIP switches as follows:

SW1	Open (no external amplifier)	SW5	Open (not used)
SW1	Open (external PQM2100 modulator)	SW6	Open (not used)
SW3	Open (not used)	SW7	Open (not used)
SW4	Open (not used)	SW8	Open (English language LCD)

IF Processing Module (A3) 1585-1207

1. Select 75Ω input impedance using jumpers J28 and J29.
2. Select Low Input Impedance using jumpers J8, J9, J10 and J11.
3. Enable Peak Vs. Average detection by placing J30 into the In position.
4. Enable Frequency Response Correction by placing J2 and J3 into the In position.
5. Set Delay Equilizers and Attenuation Equilizers as follows:

Delay Equilizer1 (J35, J36)	Out
Attenuation Equilizer1 (J37, J38)	Out
Delay Equilizer2 (J43, J44)	Out
Delay Equilizer3 (J31, J32)	Out
Attenuation Equilizer3 (J33, J34)	Out

6. Set filter circuit to Band Pass Filter by placing jumpers J19, J20, J22 and J23 into the SAW position.
7. Select High Output Gain by placing jumpers J26 and J27 into the High position.
8. Remove linear equalization by placing front panel Linear Equalization toggle switch into the out position.
9. Select Manual Gain by placing Gain Selection toggle switch into the Manual position.

2.0 TECHNICAL DESCRIPTION

2.5 Alignment Procedure - continued

LO/Upconverter Module (A5) 1585-1143

1. Place Reference jumper J1 into the External position..

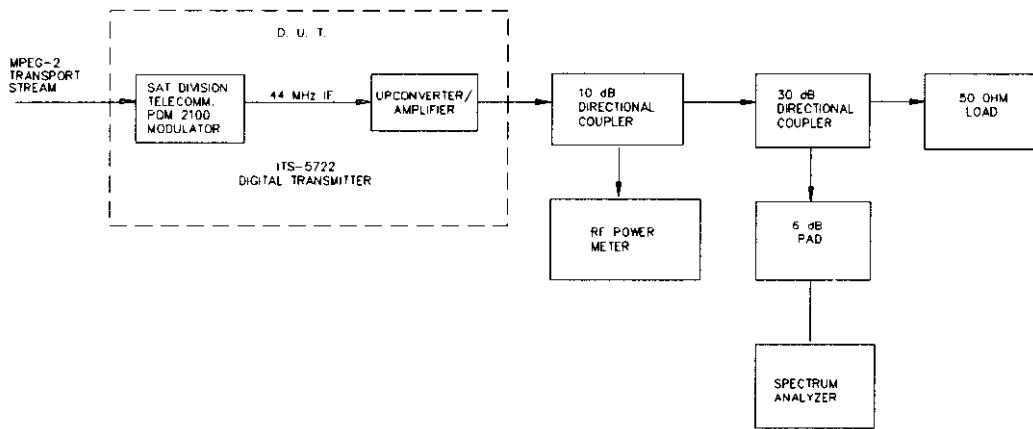
Power Amplifier Module (A6) 1585-1136

1. Select Average Detection by placing J2 into the Average position on the Dual Power Detector Module.

2.0 TECHNICAL DESCRIPTION

2.4 Alignment Procedure - continued

Connect the ITS-5722 as shown below:



Power Setup/Meter Calibration

1. Apply power to the tray by placing the rear panel power switch (CB1) into the on position.
2. Measure voltage on Forward Detector Level test point on the Power Amplifier module front panel and adjust for 0 volts using the Forward Zero potentiometer.
3. Measure voltage on Reflective Detected Level test point on the Power Amplifier module front panel and adjust for 0 volts using the Reflected Zero potentiometer.
4. Verify that no faults are displayed on the LCD display on the front panel of the tray.
5. Place transmitter into operate by pressing the Operate button below the LCD display.
6. Adjust Manual Gain potentiometer on front panel of IF Processing module for 5 watts (average) as observed on RF power meter.
7. Measure voltage on Forward Detected test point on front panel of Power Amplifier module and adjust for 1 volt using the Forward Level potentiometer.
8. Place transmitter into standby by pressing the Standby button below the font panel LCD display.
9. Remove cable connection from RF output jack (J8) of tray.
10. Place transmitter into operate mode by pressing the Operate button below the front panel LCD display.
11. Measure Reflective Detected Level test point and adjust for 1V using Reflected Level potentiometer.
12. Place transmitter into standby by pressing the Standby button below the front panel LCD display.

2.0 TECHNICAL DESCRIPTION

2.4 Alignment Procedure - continued

13. Reconnect cable to RF output jack (J8) of the tray.
14. Place transmitter into the operate mode by pressing the Operate button below the front panel LCD display.
15. Adjust ALC potentiometer on front panel of IF Processing module for 1 volt on the Forward Detected Level test point on power Amplifier Module.

RF Response

1. Adjust Spectrum Analyzer for the following settings:

Span	10MHz
Resolution BW	100KHz
Video BW	100 KHz
Center Frequency	Channel Frequency

2. Adjust the four Frequency Response potentiometers on the front panel of the IF Processing module for flat response on spectrum analyzer.

Upconverter/Amplifier Tray

Connect the RF output (J8) of the driver transmitter to the RF input (J2) of the amplifier tray. Connect the RF output (J4) of the amplifier tray to a RF power meter through a suitable directional coupler. Connect the main output of the coupler to a suitable load.

PFC Switching Power Supply (A3, A5) VS3-73-450-0001

The two 2000W Power Factor Corrected Switching Power Supplies operate from a standard 220 line voltage and output + 390VDC which is applied to a DC to DC converter in each of the 25W Power Amplifier Assemblies. The PFC Switching Power Supplies contain no user adjustments.

40W Switching Power Supply (A6) LPS-23

The 40W Switching Power Supply supplies +12 VDC to the various boards within the tray. No user adjustments are provided..

80W Switching Power Supply (A4) LPS-63

The 80W Switching Power Supply supplies -12 VDC to the various boards within the tray. No user adjustments are provided..

2.0 TECHNICAL DESCRIPTION

2.4 Alignment Procedure - continued

25 W Amplifier Assembly (A1, A2, A3, A4) 1586-1117

The 25 Watt Amplifier Assembly is a wideband GaAs FET array that is factory pre-tuned to cover the particular channel frequency.

This Amplifier module does not contain any RF tuning adjustments. The module contains GaAs FET amplifiers. The operating current for each device (Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11 and Q12), with no drive applied, is controlled by a pot mounted on a bias board within the module, next to each corresponding FET, and can be set by measuring the voltage drop across the the corresponding 0.05Ω resistors on the bias protection board. See chart below.

GaAs FET Transistor	Potentiometer Adjustment	Bias Protection Board Resistor	Voltage Across Bias Protection Resistor	Drain Current Calculated
Q4	R802	R58	.175V	7.0A
Q5	R802	R64	.175V	7.0A
Q6	R802	R121	.175V	7.0A
Q7	R802	R67	.175V	7.0A
Q8	R802	R122	.175V	7.0A
Q9 & Q10	R802	R63	.175V	2.38A
Q11	R802	R2	.175V	7.0A
Q12	R802	R1	.175V	7.0A

8 Section Bias Protection Board (A1) 1586-1109

There is one 8 Section Bias Protection Board located in each of the two 25 Watt Power Amplifier Assemblies.

These boards provide over current fuse protection and operating status LED indication of the amplifier modules. These boards also contain bias resistors used to set the operating current of the FET amplifiers within the amplifier modules (see 25 Watt Amplifier Assembly set up above). No user adjustments are provided on the board.

Power Detector/Control Board (A6) 1586-1118

Using a dummy load and a directional coupler with a calibrated power meter the Forward and Reflective power may be calibrated as follows:

1. To calibrate forward power on the front panel meter, first connect a suitable rated load and a calibrated power meter through a directional coupler to the RF output jack (J4) on the rear of the tray. Place the driver transmitter into manual mode operation.
2. Place the driver transmitter into the Operate mode.

2.0 TECHNICAL DESCRIPTION

2.4 Alignment Procedure - continued

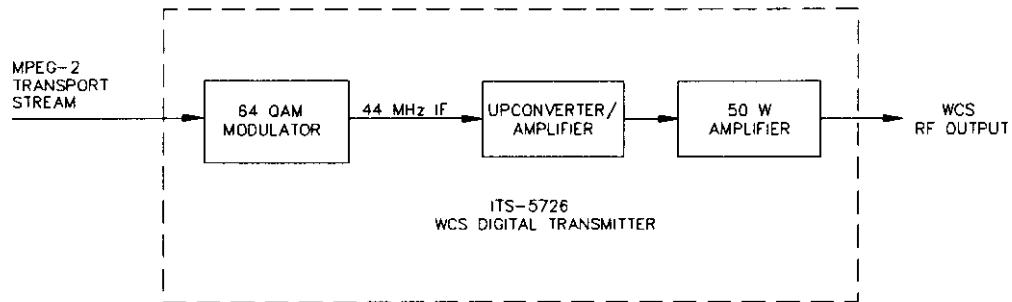
3. Apply a digital IF test signal to the input of the driver transmitter and adjust the manual gain potentiometer of the driver transmitter for the full rated average output power level of the amplifier.
4. Adjust potentiometer R17 on the Power Detector/Control Board for 1V at TP2.
5. Remove the load connected to the amplifier and quickly Reflective Metering potentiometer for 1V at TP3. Note: This step must be performed quickly as to not sustain damage to the FET devices.

2.0 TECHNICAL DESCRIPTION

2.6 Block Diagrams

System Block Diagram:

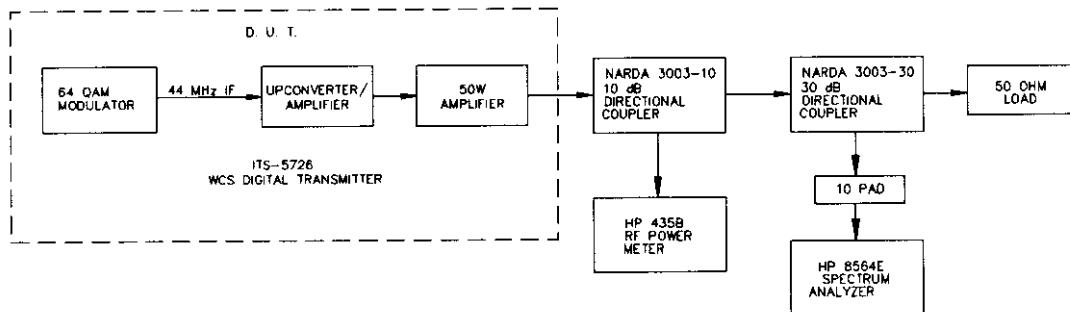
The following is a system block diagram for the ITS-5726 digital WCS transmitter. Detailed Block Diagrams and Schematics are included in Exhibit II.



3.0 ENGINEERING DATA

3.1 RF Power Measurements

The following block diagram describes the test equipment set-up for the following measurement:



The output power of the ITS-5726 was adjusted to obtain 50 watts average RF output as observed on the power meter.

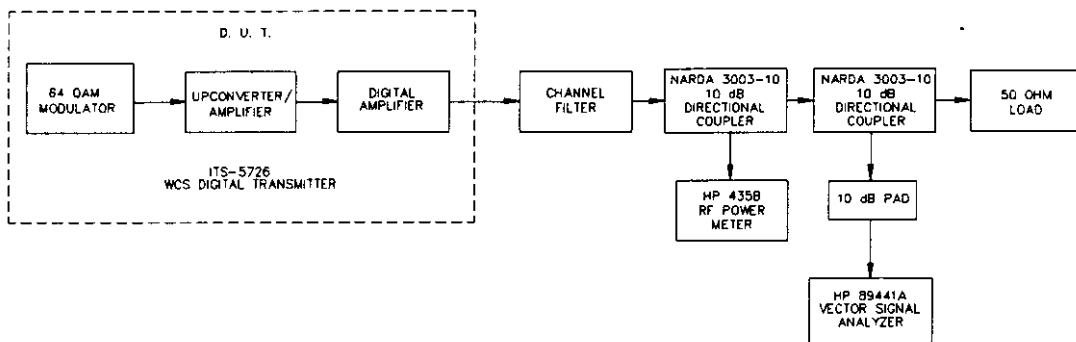
With the power level properly set to 50 watts average, all required test were performed and recorded in the following sections.

3.0 ENGINEERING DATA

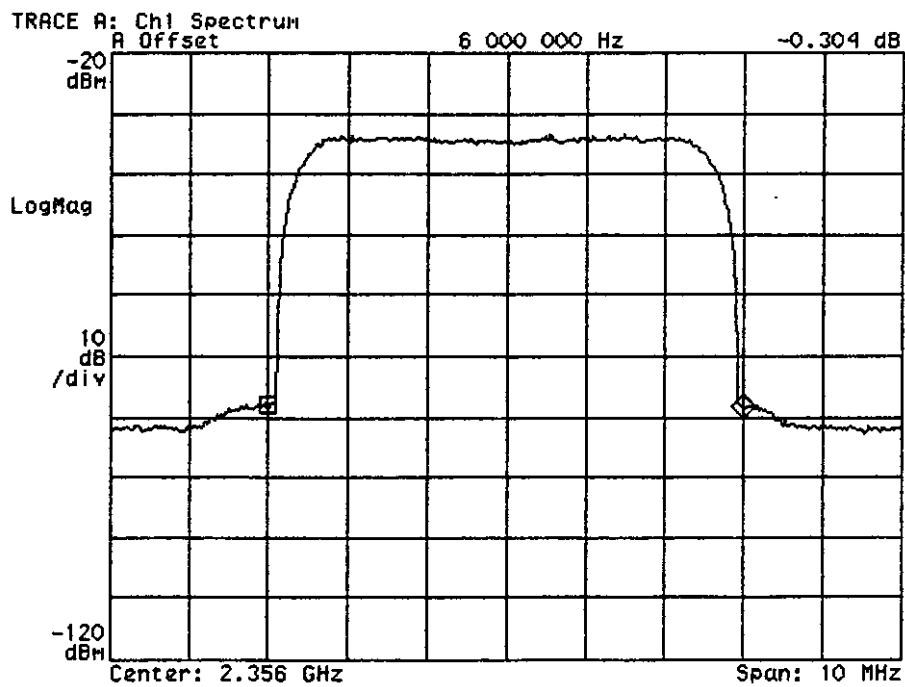
3.3 Occupied Bandwidth

Using the following test set-up, the transmitter was operated at maximum power and a plot of the transmitter occupied bandwidth spectrum was taken.

Note: The Resolution BW setting was adjusted to 100 KHz for this measurement.



Spectrum Analyzer Plot (Channel Occupied Bandwidth):

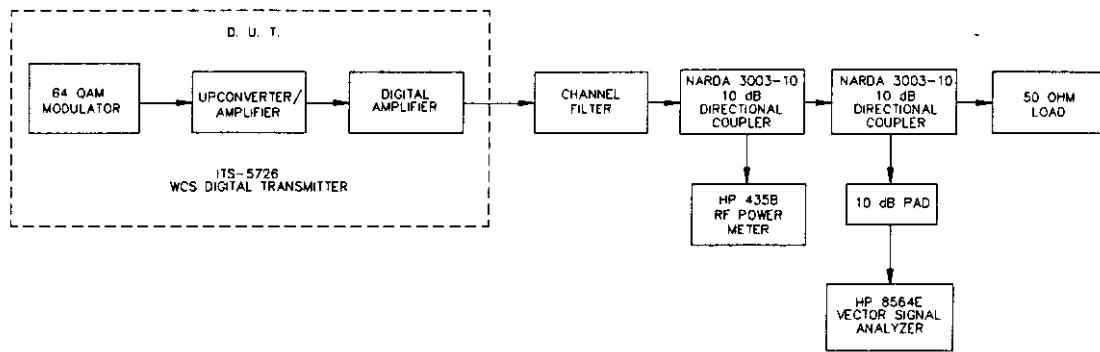


As indicated by the markers at the channel edges on the above plot, the occupied bandwidth of a quadrature amplitude modulated signal is approximately 6 MHz.

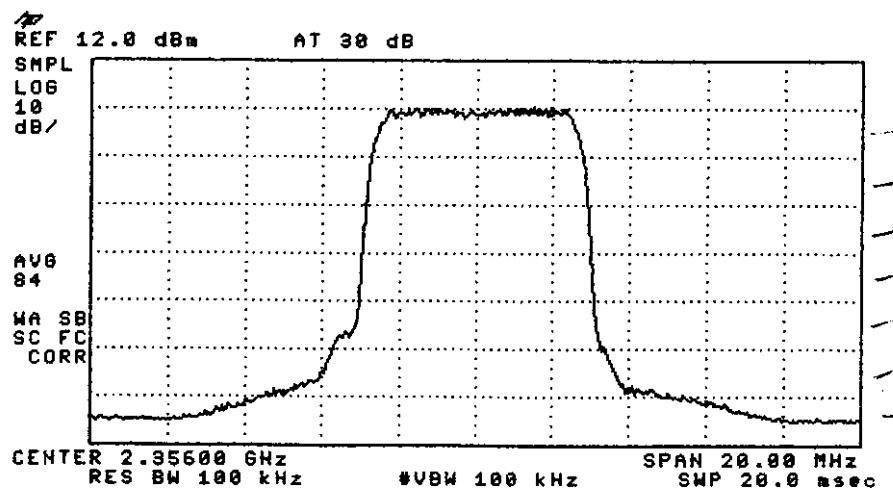
3.0 ENGINEERING DATA

3.4 Out-of-Band Power

Using the test set-up shown below, a reference was established on the spectrum analyzer for measuring out-of-band emissions (see the following test set-up/data in this section). Also, the spectrum was observed on the analyzer at both 20 MHz and 40 MHz span (see spectrum plots below).



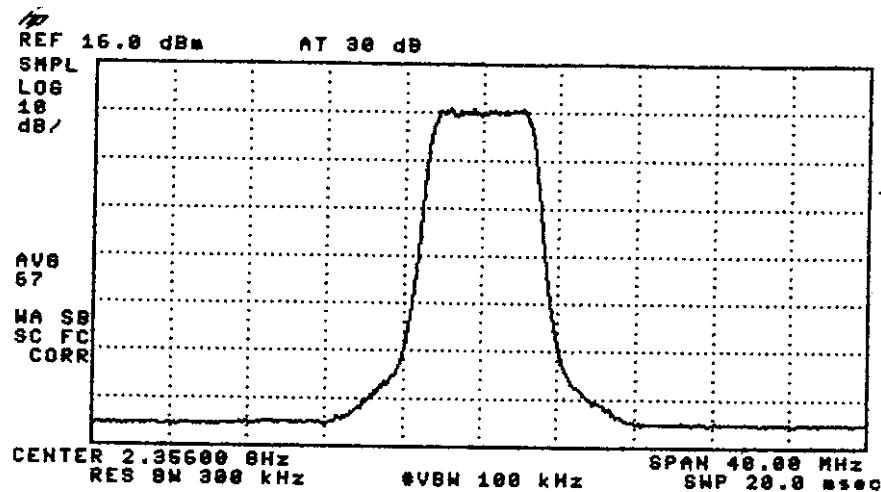
Spectrum Analyzer Plot (20 MHz Span):



3.0 ENGINEERING DATA

3.4 Out-of-Band Power - continued

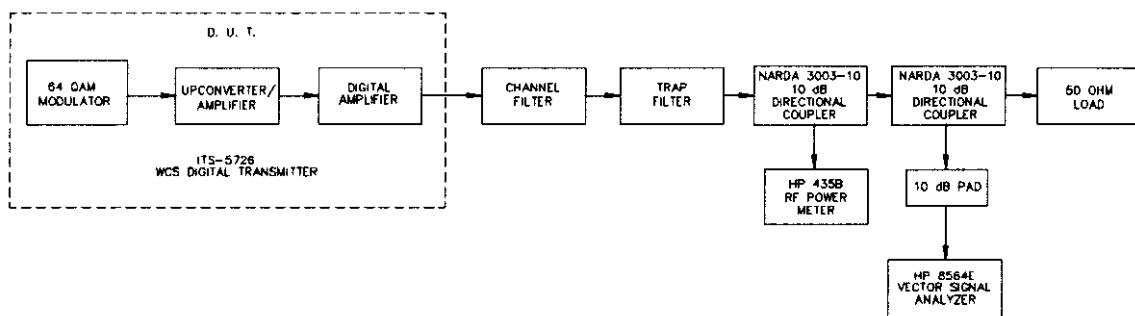
Spectrum Analyzer Plot (40 MHz Span):



3.0 ENGINEERING DATA

3.4 Out-of-Band Power - continued

Using the test setup below, a 6 MHz trap filter was utilized to trap the channel of operation and thereby increase the dynamic range capability of the analyzer. With the average in band signal measured with the above test set-up set as the reference, the spurious emissions were observed. The measured data is shown in the table below for 50 watts (average) output power.



Frequency	Source	Maximum Level Observed
2356.00 MHz	Center of Channel	0 dB (reference)
44 MHz	IF	-100 dB
2400.00 MHz	Local Oscillator	-100 dB
2353.00 MHz	Lower Channel Edge	-43.0 dB
2359.00 MHz	Upper Channel Edge	-43.0 dB
< 2300.00 MHz	-	-100 dB
2300.00 - 2320.00 MHz	-	-100 dB
2320.00 - 2345.00 MHz	-	-100 dB
2360.00 - 2370.00 MHz	-	-77 dB
> 2370.00 MHz	-	-100 dB
4712.00 MHz	2nd Harmonic	-100 dB
7068.00 MHz	3rd Harmonic	-100 dB
9424.00 MHz	4th Harmonic	-100 dB
11780.00 MHz	5th Harmonic	-100 dB
14136.00 MHz	6th Harmonic	-100 dB
16492.00 MHz	7th Harmonic	-100 dB
1848.00 MHz	8th Harmonic	-100 dB
21204.00 MHz	9th Harmonic	-100 dB
23560.00 MHz	10th Harmonic	-100 dB

3.0 ENGINEERING DATA

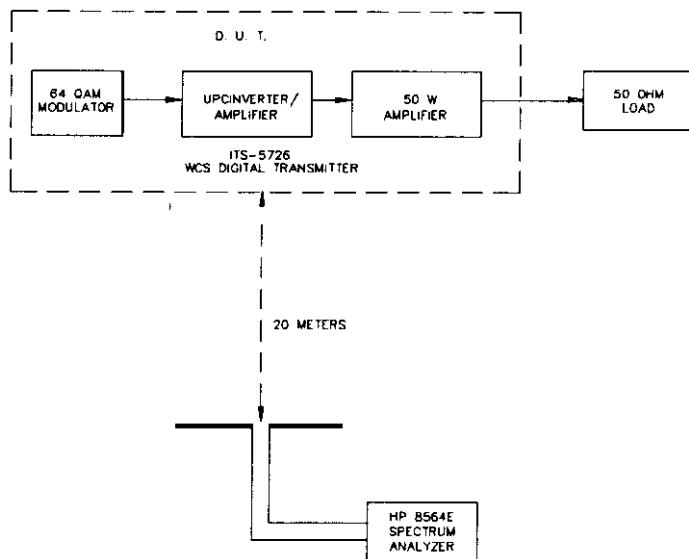
3.5 Radiated Emissions

Using the test set-up below, with the transmitter operating at 50 watts average output power and at a carrier frequency of 2356.00 MHz, the spectrum analyzer was moved 20 meters from the transmitter and connected to a dipole antenna cut to the IF frequency (44 MHz). This antenna was oriented to maximize the received level, and the data was recorded. The antenna was then cut to the carrier frequency, local oscillator frequency, and the second through the tenth harmonic frequencies of the transmitter and all signals received were maximized by antenna orientation, and their absolute levels were recorded.

With these various antennas the data was taken and recorded in the table on the following page.

Note: The spectrum analyzer had a maximum sensitivity of -110 dBm during these test.

Test Set-up:



3.0 ENGINEERING DATA

3.5 Radiated Emissions - continued

MEASURED LEVELS

Frequency	Source	Level Observed
2356.00 MHz	Center of Channel	-74 dB
44 MHz	IF	None Observed
2400.00 MHz	Local Oscillator	None Observed
4712.00 MHz	2nd Harmonic	None Observed
7068.00 MHz	3rd Harmonic	None Observed
9424.00 MHz	4th Harmonic	None Observed
11780.00 MHz	5th Harmonic	None Observed
14136.00 MHz	6th Harmonic	None Observed
16492.00 MHz	7th Harmonic	None Observed
1848.00 MHz	8th Harmonic	None Observed
21204.00 MHz	9th Harmonic	None Observed
23560.00 MHz	10th Harmonic	None Observed

The measured levels were then compared to the following reference level:

If all of the transmitter's power (50 Watts) was radiated by an isotropic radiator, the power density at 20 meters would be:

$$P_d = P_t / 4\pi R^2 = 50 / 4\pi (20)^2 \approx 9.947 \times 10^{-3} \text{ W/m}^2$$

Using a dipole transmitting antenna increases this by 1.64 to:

$$1.64 \times 9.947 \times 10^{-3} = 16.313 \times 10^{-3} \text{ W/m}^2$$

If a dipole receive antenna of area $1.64 \times \lambda^2 / 4\pi$ is used to receive the signal, the received level would be:

$$16.313 \times 10^{-3} \times 1.64 \times \lambda^2 / 4\pi = 34.52 \times 10^{-6} \text{ W} = -44.6 \text{ dBw} = -14.6 \text{ dBm}$$

The receive levels were therefore at the following relative levels:

<u>Frequency</u>	<u>Relative Measured Level</u>
	(Ref = -14.6 dBm)

2536 MHz	-59.4 dBc
----------	-----------

The cabinet radiation was also checked with the receive dipole antenna cut to 2356.00 MHz, within very close proximity to the transmitter's trays, and the received level recorded at no time exceeded a level in excess of -10 dBm. The power density at this level would then be:

$$P_r / A = 5.7 \times 10^{-3} \text{ mW/cm}^2$$

This level is far less than the current or proposed standard for safe radiation levels.

3.0 ENGINEERING DATA

3.6 Frequency Stability

The ITS-5726 is designed to operate using an external 10 MHz precise reference oscillator. The frequency stability of this external reference determines the frequency stability of the transmitter.

The frequency determining variables of the transmitter may be defined as follows:

F_{LO} = Desired local oscillator frequency
 F_{IF} = Desired IF oscillator frequency
 F_R = Desired external reference oscillator frequency
 F_{RF} = Desired RF output frequency
 E_{LO} = Local oscillator frequency offset error
 E_{IF} = IF oscillator frequency offset error
 E_R = External reference oscillator frequency offset error
 E_{RF} = RF output frequency error

The PLL circuitry maintains a constant ratio between the external reference frequency and the output frequency of the oscillator. This ratio is defined below for both the LO and IF oscillators.

$$G_{LO} = F_{LO}/F_R$$
$$G_{IF} = F_{IF}/F_R$$

Any change in the external 10 MHz reference will effect a corresponding change in the output frequency such that the above ratios are maintained.

$$G_{LO} = (F_{LO} + E_{LO})/(F_R + E_R) = F_{LO}/F_R$$

$$G_{IF} = (F_{IF} + E_{IF})/(F_R + E_R) = F_{IF}/F_R$$

Solving for the change in output frequency yields:

$$E_{LO} = E_R * (F_{LO}/F_R) = E_R * G_{LO}$$

$$E_{IF} = E_R * (F_{IF}/F_R) = E_R * G_{IF}$$

The desired RF carrier frequency is equal to the LO frequency minus the IF frequency:

$$F_{RF} = F_{LO} - F_{IF}$$

The actual RF frequency, including any error introduced by the external reference, may be defined as follows:

$$F_{RF} + E_{RF} = (F_{LO} + E_{LO}) - (F_{IF} + E_{IF})$$
$$F_{RF} + E_{RF} = (F_{LO} + F_{IF}) - (E_{LO} - E_{IF})$$
$$F_{RF} + E_{RF} = F_{RF} + (E_{LO} - E_{IF})$$

3.0 ENGINEERING DATA

3.6 Frequency Stability - continued

Calculating for the error of the RF carrier yields:

$$\begin{aligned}E_{RF} &= (E_{LO} - E_{IF}) \\E_{RF} &= E_R * G_{LO} - E_R * G_{IF} \\E_{RF} &= E_R (G_{LO} - G_{IF}) \\E_{RF} &= E_R / F_R * (F_{LO} - F_{IF}) \\E_{RF} &= E_R / F_R * F_{RF}\end{aligned}$$

Therefore, the error of the RF carrier is a function of the external 10 MHz reference error.

With a maximum RF frequency error of ± 1.0 KHz and the highest channel frequency for this service (WCS4 = 2356 MHz), the maximum allowable reference error ($E_{R(max)}$) can be calculated.

$$E_{R(max)} = 4.2 \text{ Hz}$$

The required reference oscillator stability may be calculated as follows:

$$\begin{aligned}\text{Stability} &= E_{R(max)} / F_R \\&= 4.2 \text{ Hz} / 10 \times 10^6 \text{ Hz} = 0.42 \times 10^{-6}\end{aligned}$$

Therefore, the RF frequency error of the ITS-5726 will not exceed ± 1.0 KHz when operated with a precise reference oscillator with a stability equal to or better than 0.42×10^{-6} .

Commercially available GPS precise reference oscillators, such as the TRAK Systems 8821 which has a frequency stability of 1×10^{-9} over a temperature range of 0 to 50 °C, and a line voltage/frequency range from 85 to 265 VRMS/48 to 440 Hz (see TRAK Systems 8821 specifications on the following pages), insure a frequency stability within ± 1.0 KHz.

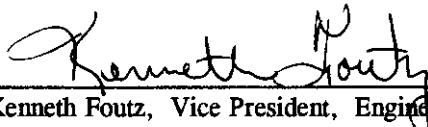
3.0 ENGINEERING DATA

3.7 Test Equipment

MODEL	MANUFACTURER	DESCRIPTION	SERIAL #
8564E	Hewlett Packard	Spect. Analyzer 9 KHz-40 GHz	3410A00137
3003-30	Narda	Directional Coupler	02162
3003-10	Narda	Directional Coupler	09034
435B	Hewlett Packard	RF Power Meter	2445A10481
2349A	Hewlett Packard	30 Watt Power Head	1801A03237
8401	Bird	50 Ohm Termination	6196
85	Fluke	Digital Multimeter	61750234
89441A	Hewlett Packard	Vector Sig. Analyzer (IF section)	3416A1547
89441A	Hewlett Packard	Vector Sig. Analyzer (RF Section)	34509A00611

5.0 CERTIFICATION OF TEST DATA

This equipment has been tested in accordance with the requirements contained in the appropriate Commission regulation. To the best of my knowledge, these tests were performed using measurement procedures consistent with industry or Commission standards and demonstrate that the equipment complies with the appropriate standards. Each unit manufactured, imported or marketed, as defined in the Commission's regulations, will conform to the sample(s) tested within the variations that can be expected due to quantity production and testing on a statistical basis. I further certify that the necessary measurements were made by Information Transmission Systems Corp., 375 Valley Brook Road, McMurray, Pennsylvania 15317.



Kenneth Foutz
Kenneth Foutz, Vice President, Engineering



Todd Anderson
Todd Anderson, Engineer