2.1033 (c) TECHNICAL REPORT

Subsection
2.1033 (c)(1). APPLICANT: TOSHIBA Corporation

ADDRESS: 1-1, Shibaura 1-Chome, Minato-ku, Tokyo, 105-8001 JAPAN

Subsection
2.1033 (c) (2) FCC ID: CJ6DCE37529A

Subsection
2.1033 (c) (3) Instruction Book:
Operating Instruction (EXHIBIT No.13)

Subsection
2.1033 (c) (4) Types of Emission: 40K0F8W, 40K0F1D, 1M25F9W

Subsection
2.1033 (c) (5) Frequency Range
ANSI/TIA/EIA-95-B Analog System and Band Class 0 CDMA Channel
Transmit Frequency Band : 824.025-848.985 MHz
Receive Frequency Band: 869.025-893.985 MHz
ANSI/TIA/EIA-95-B Band Class 1 CDMA Channel
Transmit Frequency Band : 1850-1910 MHz
Receive Frequency Band: 1930-1990 MHz

Subsection
2.1033 (c) (6) Specific Operating Power Range
Analog System;
Power ATT. 0dB +27.8dBm +/-0.5dB ERP
Power ATT. 4dB +23.8dBm +2.0/-4.0dB ERP
Power ATT. 8dB +19.8dBm +2.0/-4.0dB ERP
Power ATT. 12dB +15.8dBm +2.0/-4.0dB ERP
Power ATT. 16dB +11.8dBm +2.0/-4.0dB ERP
Power ATT. 20dB + 7.8dBm +2.0/-4.0dB ERP
Note; Maximum antenna gain is 1.3 dBd.
Band Class 0 CDMA Channel Mobile Station III;
Operating Range: -50dBm ERP to 25.0dBm ERP (Step range: 1 dB)
Note; Maximum antenna gain is 1.0 dBd.
Band Class 1 CDMA Channel Mobile Station II;
Operating Range: -50dBm EIRP to 24.5dBm EIRP (Step range: 1 dB)
Note; Maximum antenna gain is 0.5 dBi.
Maximum transmit power is monitored by detecting PA output power and controlled by transmit IF signal to maintain the maximum transmit power within the specific level.
The transmit power attenuation and step are determined by calculating characteristics of transmit power versus TX_AGC_ Adjustment Voltage.

Subsection
2.1033 (c) (7) Maximum Power Rating
Analog System Upper Limit: -2.2dBW(0.6W)ERP
Band Class 0 CDMA Channel Mobile Station III: Lower Limit: -7dBW(0.2W)ERP

APPLICANT: TRANSCEIVER TYPE:

TOSHIBA CORPORATION CJ6DCE37529A

		Upper Limit:	0dBw(1.0W)ERP
Band Class 1 CDMA Channel	Mobile Station II:	Lower Limit:	-7dBW(0.2W)EIRP
		Upper Limit:	0dBw(1.0W)EIRP

Subsection

2.1033 (c) (8) DC Voltage and Current into the Final Amplifier Module:

Supply Voltage = 3.7Vdc
Collector Voltage = 3.5Vdc
Collector Current = 0.7 - 0.1Amp.

Subsection

2.1033 (c) (9) Tune-up Procedure:

Tune-up Procedure (EXHIBIT No.8)

Standard Test Conditions:

The following Conditions and Procedures were applied during Testing of this transmitter.

Room Temperature = 23 - 27degrees Celsius
Room Humidity = 30 - 50percent Relative Humidity
Supply Voltage = 3.7V

Prior to Testing, the Unit should be tuned-up according to the Manufacturer's Alignment Procedure.

2.1033 (c) (10) Circuit Descriptions

Means for Frequency Stabilization:

The output frequency of the VCTCXO is frequency locked to the RF signal transmitted from a cellular base station by an AFC circuit. Therefore the frequency stability of an RF signal transmitted from a cellular base station is maintained. The Transmitter Frequencies are determined by a Voltage Controlled Oscillator Phase Locked to a 30kHz Signal for operation in 800MHz band and to a 10KHz Signal for operation in 1.9GHz band derived from this High Stability Oscillator known as the Reference Oscillator

Means for suppression of Spurious Emissions:

Spurious and Harmonic suppression is obtained by proper Shielding Techniques, and the use of (800Mhz Band) Band pass SAW Filters (1900MHz Band)Band pass Dielectric Filters. Under digital mode, in order to keep the transmission level within the linear operation range of the power amplifier, the highest gain of the Transmission Variable Amplifier is limited.
This enable to suppress “conductive Spurious Emissions” under the specified values

Means for Limiting Modulation:

This transmitter is equipped with a device that prevent modulation in excess of 100%. This device, an instantaneous deviation control (IDC) precedes the modulator of the transmitter. It is instantaneous in action for controlling the modulating wave from introduced into the transmitter's frequency modulator. The deviation limit is set by means of an electronic master deviation adjust stage (Exhibit No.6). This allows maximum audio deviation to be set to +/-12kHz. Under digital mode, in order to limit the Modulation Frequency Range, the low pass filter which limits the frequency range is adopted to each of DBP transmitter and ABP transmitter.

Means for Limiting Power:
A Peak Detector at the Output of the Power Amplifier provides a Carrier Power Indicator Signal. This Signal level is Compared with limited power by CPU. A power level is limited setting for level controlled by CPU.

Technical Descriptions:
This Transmitter has been specifically designed for the Domestic Public Cellular Radiotelephone Communications Service.
This transmitter is available as a triple mode phone. Namely, this transmitter is designed to operate under CDMA (Code Division Multiple Access) digital cellular system, AMPS analog cellular system and PCS (CDMA)digital cellular system.
This transmitter is available as a triple mode phone. Namely, this transmitter is designed to operate under CDMA (Code Division Multiple Access) digital cellular system, AMPS analog cellular system and PCS (CDMA)digital cellular system.
CDMA signals are fed to a quadrature phase modulator of 130.38MHz IF signal which is divided by 2 from 260.76MHz signal of a voltage controlled oscillator(T_VCO).
The T_VCO also works as a FM modulator for analog mode and locked to 19.68MHz signal of a VC-TCXO.

The IF signal is amplified and frequency up-converted by a RF local signal into RF signal of 824-849MHz band or 1850-1910MHz band. The RF local signal is generated by a dual band voltage controlled oscillator (Dual_ VCO) and locked to 19.68MHz signal of the VC-TCXO.
The VC-TCXO is also used for a frequency reference of receiving circuit and adjusted to synchronize the received RF signal from base station.
A transmit automatic gain control (AGC) function is performed at the IF amplifier section to adjust specific transmit output power level.
The up-converted signal is switched and fed to a 800MHz band power amplifier power amplifier lineup or to a 1.9GHz band power amplifier lineup. DC power is only supplied to the activated lineup.
The 800MHz band power amplifier lineup consists of an inter stage BPF1(INT-BPF1), a driver 1 (Drv1), an INT_BPF2, a power amplifier (PA), an isolator and a duplexer which are dedicated for 800MHz band.
The 1.9GHz band power amplifier lineup also consists of an INT-BPF1, a Drv1, an INT_BPF2, a PA, an isolator and a duplexer which are dedicated for 1.9GHz band.
INT_BPF2 of 1.9GHz band is split into upper and lower band of 1.9GHz band. The selection the split band is based on the assigned channel.
The output of 800MHz band duplexer and 1.9GHz band duplexer are connected to diplexer to use a dual band antenna.
A peak power detector for both 800MHz and 1.9GHZ band amplifiers provides a carrier power indication signal. The signal level is monitored by a CPU to keep the transmit power not to exceed to the maximum limit.

List of Schematics:
Block Diagram of HANDHELD PORTABLE TRANSCEIVER RF/BB
(EXHIBIT No.2)

Schematic Diagram of HANDHELD PORTABLE TRANSCEIVER RF/BB
(EXHIBIT No.10)

Subsection

2.1033 (c) (11) Equipment Identification:

Equipment's Identification label and its intended Location are as shown in EXHIBIT No.5 (FCC ID Nameplate), and in EXHIBIT No.6(Photograph of inside)

Subsection
2.1033 (c) (12) Photographs:

A complete set of the Photographs showing External and Internal Views of Circuit Details and Construction are provided by from EXHIBIT No.4(External Photos) and No.6(Internal Photos).

Subsection
2.1033 (c) (13). Digital Modulation

Analog speech produced by a microphone is encoded to digital PCM samples using a CODEC. The PCM samples are passed to a Vocoder for QCELP or EVRC encoding, to compress the speech samples. The encoding rate is determined by the Vocoder which formats the speech samples as data packets. A new data packet with data rate information is read by the microprocessor every 20 ms. The maximum information rate becomes 9.6 kbs for Rate Set 1 or 14.4 kbps for rate Set 2. The microprocessor then sends

the data packet to the transmit subsystem, where the information bits are convolutionally encoded, interleaved, modulated by means of 64-ary orthogonal modulation, spread into 1.2288 Mbps I/Q base band signals by means of direct sequence spreading, and passed DAC to covert analog signal.

The process gains for the Rate Set 1 and Rate Set 2 are 128(21dB) and 85.3(19.3dB) respectively.

The I/Q base band signals are filtered and passed to a 130.38 MHz quadrature spreader.

Transmitter IF signal generation at 130.38MHz is performed by combining digitally generated I and Q signals. The tin-and quadrate-phase 130.38MHz local signals are derived from a 260.76MHz phase locked loop.

Subsection
2.1033 (c) (14). The Data Required (EXHIBIT No.11)

(2.1046) RF power output
(2.1057) Modulation characteristics
(2.1049) Occupied bandwidth
(2.1057) Spurious emission at antenna terminals
(2.1058) Field strength of spurious radiation
(2.1059) Frequency stability
(2.1060) Frequency spectrum to be investigated

Subsection
2.1033 (c) (15). External Power Amplifier
Not applied

Subsection
2.1033 (c) (16). AM Broadcast Stereophonic Exciter-generator
Not applied

Subsection
2.1033 (c) (17). Composite System
Not applied

TRANSMITTER FREQUENCY RESPONSE

Subsection 2.987 (a). The Test Set-up for the TRANSMITTER FREQUENCY RESPONSE is as per PAGE 1 of EXHIBIT No.12(Using HP8901B Modulation Analyzer).

With the Audio Signal Generator adjusted to 1,000 Hz, and +/-1.0kHz Deviation, the 0dB Reference Level was determined. With Input Levels held constant and below Limiting at all Frequencies, the Audio SG was varied from 100 to 5,000Hz. The Response in dB, relative to 1,000Hz was measured.

The results are shown in EXHIBIT No.11.

MODULATION LIMITING

Subsection 2.987 (b). The Test Set-up for the MODULATION LIMITING is as per PAGE 1 of EXHIBIT No.12. The Deviation is to be observed by varying the Input Voltage. Test has been performed for three Different Modulation Frequencies.

The results are shown in EXHIBIT No.11.

OCCUPIED BANDWIDTH

Subsection 2.989 (c)(1) The Test Set-up for the OCCUPIED BANDWIDTH is Figure in SPURIOUS EMISSIONS AT ANTENNA TERMINALS, PAGE 1 of EXHIBIT No.12.

Analog mode:

The Audio SG was adjusted to the Frequency of Maximum Response. The Output Level was set to +/-6kHz Deviation.

With Level constant, the Frequency was set to 2,500Hz. Then the Audio Signal level was increased by 16dB.

The measurements ware made by Spectrum Analyzer, and the results are shown in EXIBIT No.11.

In addition, Occupied Bandwidth Data was obtained for the SAT (Supervisory Audio Tone) and ST (Signaling Tone). The results are shown in EXIBIT No.11.

Digital mode:

Modulate the transmitter with OQPSK modulation, using pseudo random date.

List of Photographs:

SPURIOUS EMISSIONS AT ANTENNA TERMINALS

Subsection
2.991
22.917. The Test Set-up for the SPURIOUS EMISSION AT ANTENNA TERMINALS is as per Figure in SPURIOUS EMISSIONS AT ANTENNA TERMINALS, PAGE 2 of EXHIBIT No.12.

The Level of the Carrier and the various Conducted Spurious and Harmonic Frequencies were measured by means of a Calibrated Receiving System used to compare the Output of the Transmitter with than of a Standard Signal Generator at the Spurious Frequency. The Spectrum was scanned from the Lowest Frequency generated in the Equipment to 10GHz.

The results are shown in EXHIBIT No.11.

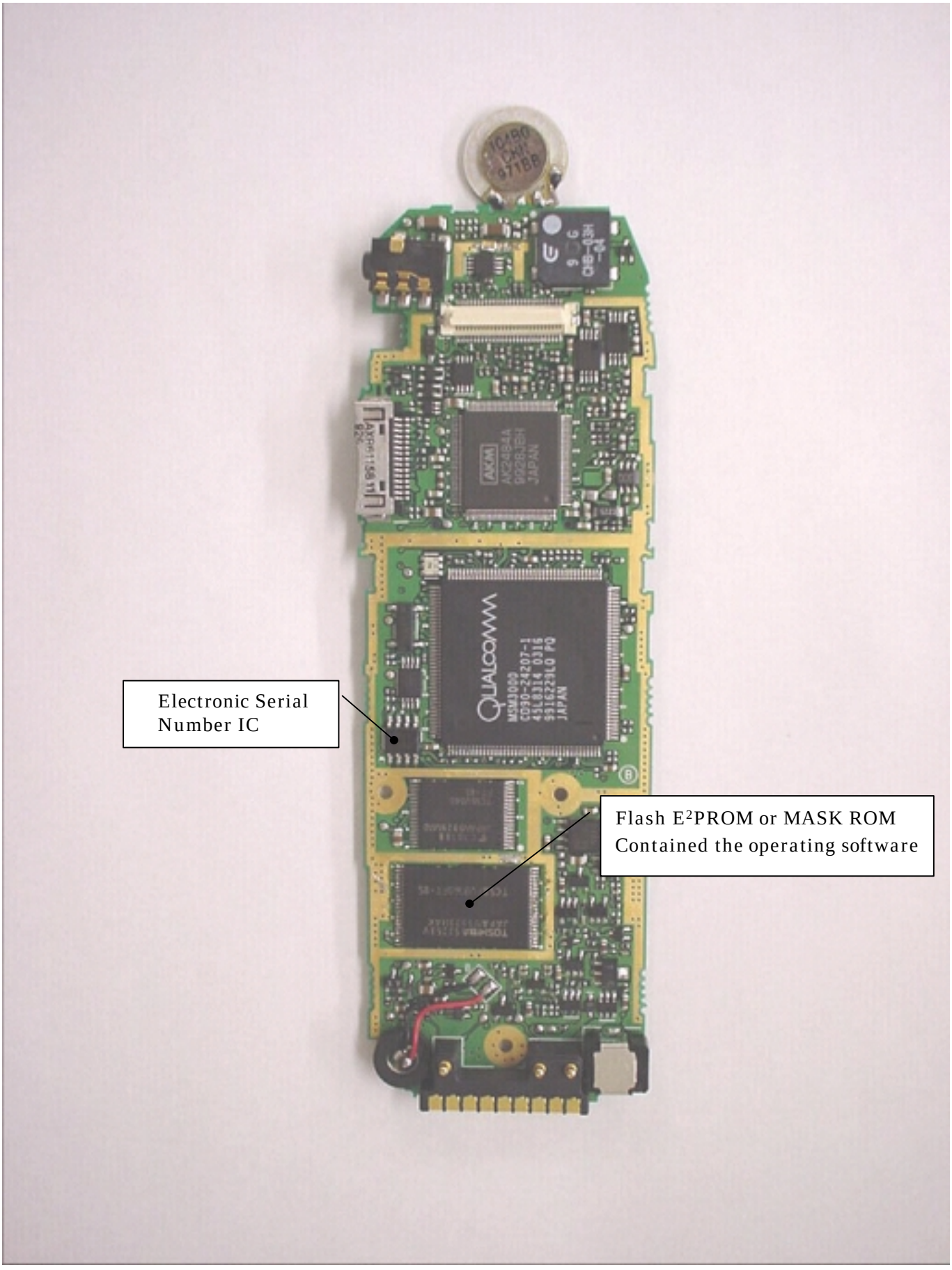
ESN PROTECTION

The ESN data is programmed in the Memory IC (EEPROM) which is used with other data. And the Encoring Technique includes the multiplication by a polynomial. This Memory (EEPROM) is soldered on the PCB as the attached photo shows.

Our operation software's legitimacy is checked by check-sum of whole program. So unauthorized alteration of that unit's operating software render the unit inoperative.

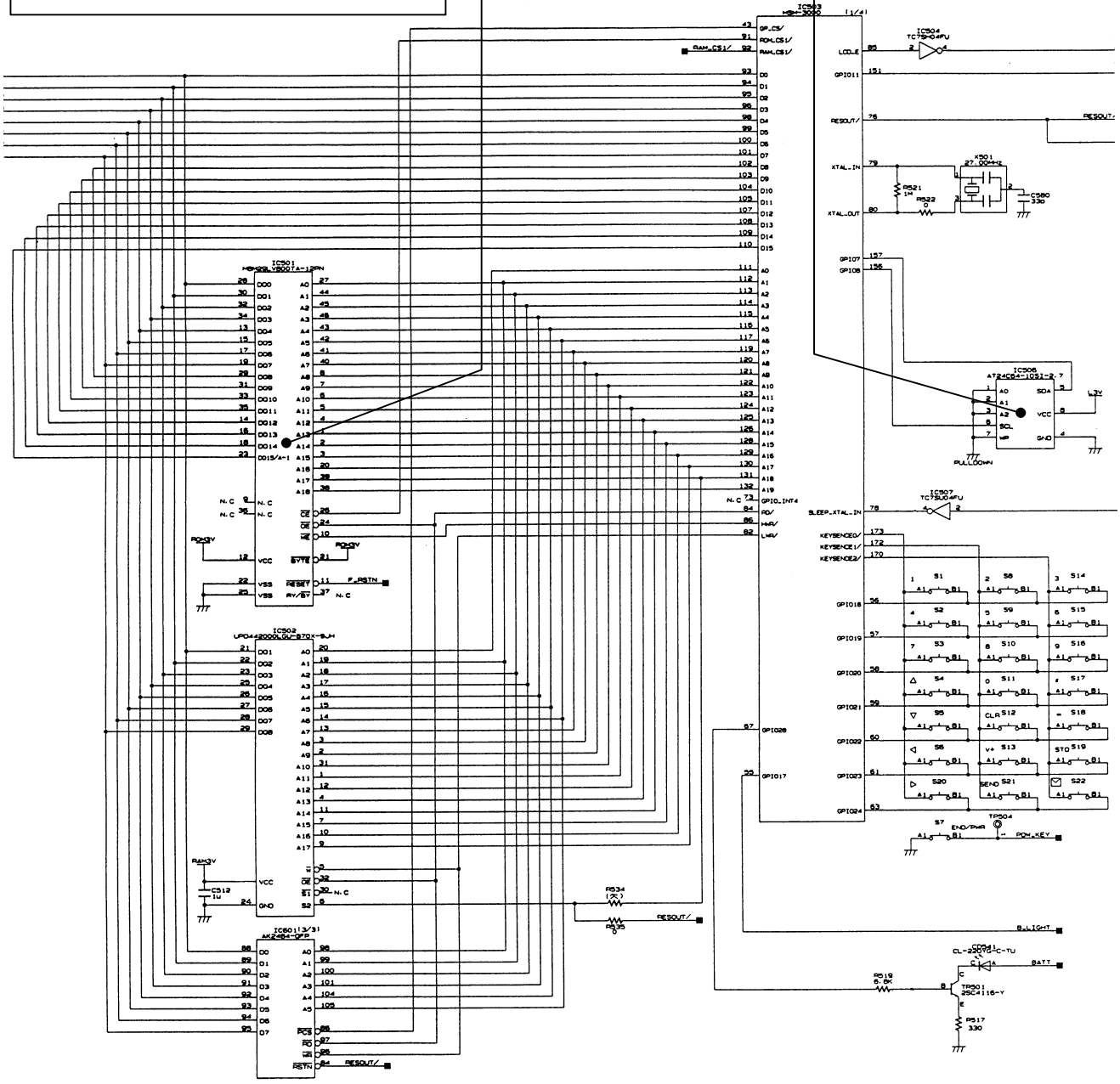
We have attached the other necessary documents as follows:

- Photo showing the location of the ESN IC and the software ROM
- Schematics showing the ESN IC and the software ROM
- ROM (contained the operating software) writer system Diagram


Electronic Serial Number IC
Flash E²PROM or MASK ROM Contained the operating software

Flash EEPROM or Mask ROM Contained the operating for cellular telephone.

Electronic serial number IC



MINATO

MODEL 1930 GANG PROGRAMMER

Massive 16 Mbyte Capacity for Simultaneous Write to 16 Chips

Announcing a New Era in Flexibility

42-pin Socket Adaptor Supports 28- to 42-pin DIP PROMs
Eliminates tiresome socket adaptor replacement.

High-speed Operation Minimizes Write Time

Hardware implementation of address generation, pin array conversion and sum generation functions boosts operation speed. Executes JEDEC standard (x8 bit, 1 Mbit EPROM) CONT processing in about 20 seconds. And because algorithms are executed by a microprocessor and dedicated hardware, the 1930 supports a wide range of PROMs.

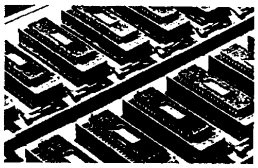
Specifications

Standard 4 Mbyte Capacity Expandable to 16 Mbyte

As PROM capacities continue to rise, the 1930 comes with 4 Mbyte standard, and can be expanded to a full 16 Mbyte: more than enough power to handle PROM cards.

Algorithms Provided for Write to Leading Vendor Devices

including AMD, Fujitsu, Hitachi, Intel, Mitsubishi Electric, National Semiconductor, NEC, Ricoh, Sharp, Texas Instruments, Toshiba, WSI and XICOR.



Standard Support for 13 Data Formats

The RS-232C and parallel interfaces provide data transfer capacity, with support for 13 data formats to match your needs:
Minato (8-bit), Intel hex (8-/16-bit), HP64000ABS, binary, Motorola, ASCII octal, ASCII hex, Tektronix hex (8-bit), Tektronix hex (16-bit), TI SDSMAC, ASCII BHLF, ASCII BNPF, no format.

Two Device Selection Methods

The devices to be written can be selected from a menu, or picked up by the silicon signature. With the menu, all you have to do is select the displayed name from the easy-to-read liquid crystal panel. If silicon signature is used, the device is automatically selected by checking the PROM internal ID code.
Note: It may be impossible to automatically read the ID code from certain PROM varieties.

```
T5716200  cdEB10
VPP=12.50v  25uS

TC578200  cdEA10
VPP=12.50v  50us

uPD_8000  cdEA11
VPP=12.50v  50us
```

Selectable Verify Parameters

Normally the verify V_{CC} voltage is set to 4.75/5.25V, but this can be changed to handle specific user requirements and make possible a new dimension in precision verification.

Write Error Alert with Buzzer and Red LED

If a write error is detected, all 16 red LEDs will light, and the buzzer will sound to alert the operator. The buzzer can be disabled if desired.

Enhanced Reliability Boosts Your Yield

The overall reliability of the programmer has been significantly improved through integration of the circuitry, reduction in the number of required adjustments, enhancement of circuit performance and function, and lower internal temperature through precision design. Write algorithms were developed cooperatively with the PROM manufacturers to provide optimum performance. And the system itself is designed to minimize noise generated by PROM operation, and eliminate inter-socket interference by isolating each socket.

Open Lever Reduces PROM Load/unload Time

Socket unlock can be completed by merely throwing the open levers, each locking eight sockets. With fast unlocking, you can unload and reload faster, too.

Simple Upgrades

We have made it simple to upgrade your system to maintain support for the latest PROM chips. With a flash PROM inside, you can update your system yourself easily.

■ Model 1930 Specifications (main unit)

Devices supported:	64 Kbit and larger EPROM and EEPROM PROM cards
Simultaneous write:	16 chips
Memory capacity:	4 Mbyte standard (32 Mbit) 16 Mbyte maximum (128 Mbit)
Operation modes:	COPY: Data copy from PROM to memory BLANK: PROM blank check PROGRAM: Write data to PROM VERIFY: Compare PROM and memory data CONT: Continuous execution of BLANK—PROGRAM—VERIFY cycle
Data input:	RS-232C and Centronics-compatible parallel. Master ROM copy. LAN (option; external)
Interfaces:	RS-232C and Centronics-compatible parallel. LAN (option; external)
Set programming:	16 patterns
Display:	16-character × 2-row LCD panel
Operating temperature:	5 to 35°C
Power supply:	AC85 to 264V (stepless), 47 to 66Hz
Power consumption:	100VA (peak)
Dimensions:	380W × 150H × 380D (mm)

■ Specifications (SU3000)

Devices supported:	28- to 42-pin DIP EPROMs and EEPROMs
Socket:	42-pin DIP Can also be used for 28-, 32- and 40-pin JEDEC and 40-pin non-JEDEC packages
Power supply:	Supplied from 1930 main unit
Dimensions:	380W × 45H × 260D (mm)

Specifications and external appearances indicated in this catalog are subject to change without notice.
The contents of this catalog are accurate as of June, 1993.

MINATO ELECTRONICS INC.
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Distributed by:

Printed in Japan 93-05-3000FA

MODEL-1891/92　専用

型　番	旧型番	価　格	デバイス形状	1891/92専用ユニット	デバイス
※H02-200	H910-38	¥23,000	32DIP_32DIP	9132A	P28F001BX
※H02-201	H910-51	¥18,000	32DIP_32PLCC	9132A	N28F001BX
※H02-203	H910-50	¥24,000	32DIP_32TSOP	9140A	E28F001BX
H02-400	H910-41	¥28,000	40TSOP	9132A	E28F002, 004
H02-401	H910-40	¥28,000	44SOP	9132A	PA28F200, 400
H02-402	H910-39	¥34,000	56TSOP	9132A	E28F200, 400
H02-403	H910-44	¥31,000	48TSOP	9132A	E28F200, 400
※H02-404	H910-68	¥28,000	44SOP	9132A	PA28F800専用
※H02-405	H910-69	¥33,000	56TSOP	9132A	E28F800専用
※H02-406	H910-70	¥31,000	48TSOP	9132A	E28F800専用
※H02-407	H910-71	¥28,000	40TSOP	9132A	E28F008専用

MODEL-1930　専用

型　番	旧型番	価　格	デバイス形状	ユニット	デバイス
H03-300	H910-8	¥26,000	44SOP	3000(L)	PA28F008SA
H03-301	H910-10	¥27,000	40TSOP	3000(L)	E28F008SA
H03-302	H910-33	¥33,000	56TSOP	3000(L)	E28F016SA
H03-303	H910-37	¥28,000	44SOP	3000(L)	M5M28F016
H03-304	H910-45	¥28,000	56SSOP	3000(L)	DT28F016SA
H03-305	H910-46	¥30,000	48TSOP	3000(L)	MBM29F080/016
※H03-306	H910-56	¥26,000	44SOP	3000(L)	MBM29F200/400/800
※H03-307	H910-57	¥30,000	48TSOP	3000(L)	MBM29F200/400/800
※H03-308	H910-73	¥25,000	40SON	3000専用	MBM29LV004T/B
※H03-309	H910-74	¥22,000	40SON	3000L専用	MBM29LV004T/B
※H03-310	H910-75	¥22,000	40SON	3000(L)	MBM29F17
※H03-311	H910-77	¥28,000	46SON	3000L専用	MBM29LV004/008/080
※H03-312	H910-78	¥24,000	46SON	3000専用	MBM29LV004/008/080
※H03-313※	H910-80※	¥28,000	46SON	3000専用	MBM29LV400/800
※H03-314	H910-81	¥24,000	46SON	3000L専用	MBM29LV400/800
※H03-315	H910-82	¥25,000	42DIP_42DIP	3000(L)	MB8502F016A
H03-400	H910-12	¥27,000	40TSOP	3000(L)	E28F002,004
H03-401	H910-13	¥26,000	44SOP	3000(L)	PA28F200, 400
H03-402	H910-19	¥33,000	56TSOP	3000(L)	E28F200, 400
H03-403	H910-35	¥30,000	48TSOP	3000(L)	E28F200, 400
※H03-404	H910-60	¥26,000	44SOP	3000(L)	PA28F800専用
※H03-405	H910-61	¥33,000	56TSOP	3000(L)	E28F800専用
※H03-406	H910-62	¥30,000	48TSOP	3000(L)	E28F800専用
※H03-407	H910-63	¥27,000	40TSOP	3000(L)	E28F008専用

☆ユニットの（　）は、SU-3000 or 3000L どちらでも可

Socket adapter