

## EXHIBIT 2-1 CFS8DL5800SS1

The 5800SS1 is constructed on a single PCB.

The PCB contains the message encoder chip U2, a loop input, RF transmitter U1 with its output matching components and antenna.

The transmitter is a phase locked loop and PA in one chip (U1) the Frequency Determining Element is Y1 (10.78125Mhz) The PLL produces an output at  $32 \times 10.78125\text{Mhz} = 345\text{Mhz}$ . The transmitter is On-off keyed (AM) by a control signal from the encoder chip (U2) all modulation is done Internally, L3,C9 are U1's PA's external tank circuit, C6,L1,C7, provide harmonic suppression, C14,blocks DC and works with C8,C10, to match the output to the loop antenna.